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CHANGE RECORD

Issue	Date	Sheet	Description of Change	Release
1	SEP. 00	ALL	FIRST ISSUE OF THE DOCUMENT	
2	OCT. 00	Section	Issue for MARSIS IEM TRR and QM/FM SRR	
		§ 1.4.1	Added [AD.12]	
		Table 4.1-1	Editing correction on the first row, last row erasing	
		Table 4.1-2	Editing correction on the sixth row, last row erasing	
		Table 4.2-1	Updating of the last two lines	
		Figure 4.3-3	Updating of the Source Data Field Max length	
		Figure 4.3-4	Updating of the Parameters Field Max length	
		Table 4.3-3	Updating of the FID ad Parameter 3 lengths	
		Figure 4.4-3	Editing correction of the Application Data Min Length	
		Figure 4.4-4	Editing correction of the N Range	
		Table 4.7-1	Table updating	
		Figure 4.7-8	Editing correction of the Packet Type/Subtype numbers	
		Figure 4.7-10	Editing correction of the Packet Type/Subtype numbers	
		§ 5	Paragraph updating according to a new Packetisation Strategy	
3	NOV. 00	Section	Issue for final MARSIS IEM SW configuration	
		§ 1.4	Adding of [AD.13] and [RD.2].	
		§ 2	Paragraph reorganisation, Table 2-1 rewriting, note about Source Part and PUS fields of the TC headers.	
		§ 3	Paragraph reorganisation, adding of Table 3-1 and § 3.2 updating	
		§ 4.1	Adding the explicit description of the test sequence executed to refuse a TC	
		§ 4.2	Updating of Table 4.2-1	
		§ 4.3	Updating of Table 4.3-3, FID = 5 has been added	
		§ 4.6	Updating of Figure 4.6-3, the field Science Data Type has been added with the relative explanatory paragraph. Updating of Auxiliary Data paragraph and Table 4.6-3. Adding of the Dummy scientific Data Structure paragraph.	
		§ 4.7	Updating of the description of TC(206,1) and TC(206,2).	
4	AUG 01	Section	Issue for EM model delivery (SW release 1). MOM-MIN-MAR-0015-ALS dated 27-07-01 (AI#6)	
		§ 2	Updating of Table 2-1 for Flash Memory Updating of Table 2-3 for Slave DSP PT and Flash Memory	
		§ 3	Updating of Table 3-1 for Flash Memories	
		§ 3.1	Updating of Table 3.1-1 for Flash Memories	
		§ 3.3	New paragraph, Table 3.3-1 is Table 4.1-3 of the preceding issue.	
		§ 4.1	Paragraph general updating	
		§ 4.3	Paragraph general updating	
		§ 4.4	Updating of Table 4.4-1 for Flash Memories	

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		§ 4.6	Paragraph general updating	
		§ 4.7	Updating of TC(206,1) and TC(206,2)	
		§ 5	Paragraph general updating	
5	JUN 02	Section	Issue for PFM SW SW-A-1090 rev 3.1	
		§ 3.3	Updating of Table 3.3-1	
		§ 4.1	Updating of Table 4.1-2 & Table 4.1-3	
		§ 4.3	Paragraph general updating	
		§ 4.6	Paragraph general updating	
		§ 4.7	Updating of Fig. 4.7-4 with regard to TC(206,2)	
		§ 6	Added section	
6	JAN. 03	Section	Issue for PFM SW SW-A-1090 rev 4.1	
		§ 1.4	Updating of Applicable and Reference Documents	
		§ 3.3	Updating of Table 3.3-1	
		§ 4.2	Updating of Table 4.2-1	
		§ 4.6.1.2	Updating of Auxiliary Data Tables	
		§ 6	Added section	
		§ 7	Added section	
		§ 8	Previous § 6	

TABLE OF CONTENTS

1. INTRODUCTION

1.1 PURPOSE

This document is the Packet Structure Definition for the for MARSIS Digital Electronics Subsystem (DES).

1.2 SCOPE

This Packet Structure Definition document provides the extension to the Packet Telemetry and Telecommand defined in [AD.2] and [AD.3].

1.3 DEFINITIONS, ACRONYMS AND ABBREVIATIONS

The explanation and definition of terms, acronyms and abbreviations used in this document and not listed below, may be found in [AD.1], [AD.2] and [AD.3].

ADSP 21020	Analogue Device Digital Signal Processor 21020
AIFT	Active Ionospheric Frequency Table
AIS	Active Ionospheric Sounding
APID	Application Process Identification
BIT	Built-In Test
C&C	Command & Control
CSCI	Computer Software Configuration Item
DC/DC	Direct Current to Direct Current converter
DCG	Digital Chirp Generator
DES	Digital Electronic Subsystem
DMS	Data Management System
DOST	Default Operations Sequence Table
DPT	Default Parameters Table
EID	Event Identifier
FID	Failure Identifier
HK	Housekeeping
FM	Flash Memory (Memories)
HW	HardWare
IEM	Interface Engineering Model
IPC	Inter Processor Communication
ISR	Interrupt Service Routine
ISR	Interrupt Service Routine
MLC	Memory Load Interface
OBDH	On-Board Data Handling
OST	Operations Sequence Table
PIS	Passive Ionospheric Sounding

PRI	Pulse Repetition Interval
PT	Parameters Table
QM	Qualified Model
RQ	Software Requirements
RTU	Remote Terminal Unit
S/C	Spacecraft
SCET	S/C Elapsed Time
SD	Sequence Diagram
SDT	Serial Digital Telemetry Interface
SID	Structure Identifier
SPMP	Software Project Management Plan
SRD	Software Requirements Document
SW	SoftWare
TBC	To Be Confirmed
TBD	To Be Defined
TBP	Time Broadcast Pulse
TBW	To Be Written
TC	TeleCommand
TM	TeleMetry
TU	Timing Unit
URD	User Requirements Document

1.4 REFERENCES

1.4.1 Applicable Documents

[AD.1]	"Space/Ground Interface Control Document" ME-ESC-IF-5001 Issue 2.0, 20 December 1999
[AD.2]	"PACKET TELEMETRY STANDARD", PSS-04-106, Issue 1, January 1988.
[AD.3]	"PACKET TELECOMMAND STANDARD", PSS-04-107, Issue 2, April 1992.
[AD.4]	"Instruction for SRD Compilation", IQ-04T–010, Issue 2, January 1998
[AD.5]	"MARSIS DES Software Project Management Plan"; TL16431; Issue 2; June 2000
[AD.6]	"DES HW ARCHITECTURAL DESIGN", TL 15433, Issue 1, March 2000
[AD.7]	Minute Of Meeting of LA-ASS-DT-MN-0004/00 of 7-8/2/00
[AD.8]	Minute Of Meeting of MIN-MAR-0024-ALS of 10/7/00
[AD.9]	Minute Of Meeting of LA-M6-DT-MN-0002/00 of 27/7/00
[AD.10]	"Payload Interface Document Annex A (E-IDS)", MEX-MMT-SP-0007 Issue 2, July 1999.
[AD.11]	"DES/QM SOFTWARE REQUIREMENT DOCUMENT", TL17019, Issue 2 February 2001

[AD.12]	“HW/SW ICD”, TL 17601, Issue 1, March 2001
[AD.13]	Marsis Des Parameters Table, TL 18546, Issue 3, December 2002

1.4.2 Reference Documents

[RD.1]	“INTEROFFICE MEMORANDUM: TM and TC Packet Layout Definition”, 25/7/00
[RD.2]	“DIGITAL SECTION REQUIREMENTS SPECIFICATION”, TNO-MAR-0037-ALS, Issue 2, 19/9/2001.
[RD.3]	“MARSIS ON BOARD PROCESSING ALGORITHMS”, TNO-MAR-0037-ALS, Issue 1, November 2000.
[RD.4]	ADSP-21020 USER’S MANUAL, Analog Devices

2. TC PACKETS DISTRIBUTION AND STRUCTURE

DES shall receive telecommands formatted in telecommand packets from the RTU. Telecommand packets shall be distributed to DES only in STANDBY Mode.
All telecommand source packets shall conform to the structure defined in [AD.3] and shown below for the MARSIS Instrument. Packet fields not specifically described and defined below are listed and entirely defined in [AD.1].

	PACKET HEADER (48 bit)									PACKET DATA FIELD (Variable)		
Field	PACKET ID					PACKET SEQUENCE CONTROL			PACKET LENGTH	DATA FIELD HEADER	APPLIC. DATA	PACKET ERROR CONTROL
Subfield	Version Number	Type	Data Field Header Flag	Application Process ID		Sequen ceFlags	Source Sequence Count (one counter for each Application Process ID)		(octets in Packet Data Field –1)			
				Proc. ID	Pack. Cat.		Source Part (used by DMS)	Sequence Part				
Content	000_b	1	1	$(76,78)_d$	12_d	11_b	........b[I]	$(0,2^{11}-1)_d$	Max $(242-1)_d$			
Wide (bit)	3 b	1 b	1 b	7 b	4 b	2 b	3 b	11b	16 b	32 b		16 b
Wide (oct.)	2 B					2 B			2 B	4 B	Var.ble (Max 236 B)	2 B

Figure 2-1 Telecommand Packet Fields

	PACKET DATA FIELD (Variable)							
Field	DATA FIELD HEADER						APPLICATION DATA	PACKET ERROR CONTROL
Subfield	PUS version	Check. Type	Ack	Pack. Type	Pack. Sub-type	Pad		
Content	Used by DMS ------------b[II]	1	-------b (1)	--------b (2	--------b (3	Used by DMS 0_b		
Wide (bit)	3 b	1 b	4 b	8 b	8 b	8 b		16 b
Wide (oct.)	4 B						Variable (Max 236 B)	2 B

Figure 2-2 Telecommand Packet Data Fields

[I] The TC Source Part field is 'don't care' for DES (it can assume the values $0_d \div 3_d$ according to [AD.1] p. 43).
[II] The TC PUS field is 'don't care' for DES (it can assume the values $0_d \div 4_d$ according to [AD.1] p. 42).
(1) This field can assume the values 0000_b or 0001_b, the two different meanings being described in § 4.1.
(2) Packet Type indicates the type (service) to which the TC Packet relates.
(3) Packet Subtype together with the Packet Type indicates the function of the packet.

TC Process IDs

With reference to [AD.1] the following Process IDs for TCs are assigned:

Pack. Category (dec)	Process ID (dec)	Service (dec)
12	76: FIRMWARE IN C&C BOARD	3, 6, 9, 206, 207
12	77: FIRMWARE IN DSP1 BOARD	6
12	78: FIRMWARE IN DSP2 BOARD	6
12	79: FIRMWARE IN TIMING BOARD	6

Table. 2-1 TC Process IDs

TC Source Sequence Count

A separate source sequence count is maintained for each APID and shall be incremented by 1 whenever the source (APID) releases a packet. The counter wraps around from $2^{14}-1$ to zero and shall start at zero at power-on of the unit.

TC Service Types and Subtypes

DES shall use the TC Packet Types and Subtypes declared mandatory or optional in [AD.1], that are listed in the following table:

Service (dec)	Telecommand (Type/Subtype) (dec)
3	(3,5): Enable Housekeeping Report (3,6): Disable Housekeeping Report
6	(6,2): Load Memory Using Absolute Addresses (6,5): Dump Memory Using Absolute Addresses
9	(9,1): Accept Time Update
206	(206,1): MARSIS Private Telecommand: OST Patch (206,2): MARSIS Private Telecommand: PT Patch
207	(207,1): MARSIS automatic Mode transition Disable

Table 2-2 TC Type/Subtype used by DES

MARSIS TC Packet list

In the following table is reported the TC Packet List applicable to MARSIS DES and it is also specified the Application Process ID. Both Nominal and Redundant TC are specified.

ACRONYM	DESCRIPTION	APID		VERIFIED BY TM
		PID	PCAT	
SIS_HK_EN_N	Nominal Enable Housekeeping Report Packet Generation - TC (3,5)	76	12	SIS_ACC_REP_S SIS_ACC_REP_F
SIS_HK_EN_R	Redundant Enable Housekeeping Report Packet Generation - TC (3,5)	76	12	SIS_ACC_REP_S SIS_ACC_REP_F
SIS_HK_DIS_N	Nominal Disable Housekeeping Report Packet Generation - TC (3,6)	76	12	SIS_ACC_REP_S SIS_ACC_REP_F
SIS_HK_DIS_R	Redundant Disable Housekeeping Report Packet Generation - TC (3,6)	76	12	SIS_ACC_REP_S SIS_ACC_REP_F
SIS_PATCH_N	Nominal Load Memory using Absolute Addresses - TC (6,2)	76÷78,79[III]	12	SIS_ACC_REP_S SIS_ACC_REP_F
SIS_PATCH_R	Redundant Load Memory using Absolute Addresses - TC (6,2)	76÷78,79[1]	12	SIS_ACC_REP_S SIS_ACC_REP_F
SIS_DUMP_TC_N	Nominal Dump Memory using Absolute Addresses - TC (6,5)	76÷78,79[1]	12	SIS_ACC_REP_S SIS_ACC_REP_F
SIS_DUMP_TC_R	Redundant Dump Memory using Absolute Addresses – TC (6,5)	76÷78,79[1]	12	SIS_ACC_REP_S SIS_ACC_REP_F
SIS_TIME_UP_N	Nominal Accept Time Update - TC (9,1)	76	12	SIS_ACC_REP_S SIS_ACC_REP_F
SIS_TIME_UP_R	Redundant Accept Time Update - TC (9,1)	76	12	SIS_ACC_REP_S SIS_ACC_REP_F
SIS_OST_TC_N	Nominal MARSIS Private Telecommand - TC (206,1)	76	12	SIS_ACC_REP_S SIS_ACC_REP_F
SIS_OST_TC_R	Redundant MARSIS Private Telecommand - TC (206,1)	76	12	SIS_ACC_REP_S SIS_ACC_REP_F
SIS_PT_TC_N	Nominal MARSIS Private Telecommand – TC (206,2)	76÷78	12	SIS_ACC_REP_S SIS_ACC_REP_F
SIS_PT_TC_R	Redundant MARSIS Private Telecommand – TC (206,2)	76÷78	12	SIS_ACC_REP_S SIS_ACC_REP_F
SIS_MOD_TR_DIS_TC_N	Nominal MARSIS Automatic Mode Transition Disable Telecommand – TC (207,1)	76	12	SIS_ACC_REP_S SIS_ACC_REP_F
SIS_MOD_TR_DIS_TC_R	Redundant MARSIS Automatic Mode Transition Disable Telecommand - TC (207,1)	76	12	SIS_ACC_REP_S SIS_ACC_REP_F

Table 2–3 Telecommand Packets List

[III] Flash Memory.

3. TM DATA PACKETS ACQUISITION AND STRUCTURE

Standard Telemetry and Science Data from the users are acquired by the DMS-computer via the OBDH-Bus and the RTUs as TM-Blocks containing TM Source Packets.
All telemetry source packets shall conform to the structure defined in [AD.2] and shown below for the MARSIS Instrument. Packet fields not specifically described and defined below are listed and entirely defined in [AD.1].
DES shall provide timing information within each Telemetry packet, with the exception of the first one (the PRI counter value shall be provided instead).

	SOURCE PACKET HEADER (48 bit)								*PACKET DATA FIELD (Variable)*	
Field	PACKET ID					PACKET SEQUENCE CONTROL		PACKET LENGTH	DATA FIELD HEADER	SOURCE DATA
Subfield	Version Number	Type	Data Field Header Flag	Application Process ID		Segment. Flags	Source Sequence Count (one counter for each Application Process ID)	(octets in Packet Data Field –1)		
				Proc. ID	Pack. Cat.					
Content	000_b	0	1	$(76, 80)_d$	$----_d$ (1)	11_b	$(0, 2^{14}-1)_d$	Max $(4106-1)_d$		
Wide (bit)	3 b	1 b	1 b	7 b	4 b	2 b	14 b	16 b	80 b	
Wide (oct.)	2 B					2 B		2 B	10 B	Variable (Max 4096 B)

Figure 3 - 1 Telemetry Source Packet

(1) Pack. Cat: 1 – Acknowledge; 4 – Housekeeping; 7 – Event; 9 – Dump; 12 – Private (Science); this field will be explicited in the following sections.

Field	PACKET DATA FIELD (Variable)							
Field	DATA FIELD HEADER							SOURCE DATA
Subfield	SCET Time	PUS	Check. Flag	Spare	Pack. Type	Pack. Sub-type	Pad	
Content	---b [IV]	---- b [V]		0000b	--------b (1)	--------b (2)	-------b (3)	
Wide (bit)	48 b	3 b	1 b	4 b	8 b	8 b	8 b	
Wide (oct.)	10 B							Variable (Max 4096 B)

Figure 3-2 Telemetry Source Packet Data Field

TM Process Ids

With reference to [AD.1] the following Process IDs for TMs are assigned:

Pack. Category (dec)	Process ID (dec)	Service (dec)
1, 4, 7	76: FIRMWARE IN C&C BOARD	1, 3, 5
9	76: FIRMWARE IN C&C BOARD 77: FIRMWARE IN DSP1 BOARD 78: FIRMWARE IN DSP2 BOARD 79: FIRMWARE IN TIMING BOARD	6
12	76: FIRMWARE IN C&C BOARD 77: SUBSURFACE SOUNDING MODE – TRACKING/DOPPLER & ACQUISITION 78: ACTIVE IONOSPHERIC SOUNDING 79: RAW DATA – CALIBRATION 80: RAW DATA – REACEIVE ONLY	20, 206

Table 3-1 TM Process Ids

TM Source Sequence Count

A separate source sequence count is maintained for each APID and shall be incremented by 1 whenever the source (APID) releases a packet. Therefore the counter corresponds to the order of release of packets by the source and enables the ground to detect missing packets. The counter wraps around from 2^{14} –1 to zero and shall start at zero at power-on of the unit.

[IV] Time of packet creation.
[V] For solicited TM packet (in response to a TC), the same PUS value than the one contained in the TC packet (which is assumed to be always "0") shall be copied in the TM packet. For unsolicited TM packet the PUS value is either 0 (TM destination = Ground only, services 20 and 206) or 2 (TM destination = Ground and DMS, services 3 and 5).
(1) Packet Type indicates the type (service) to which the TM Packet relates;
(2) Packet Subtype together with the Packet Type uniquely identifies the nature of the telemetry contained within the TM Source Packet;
(3) For solicited TM packet (in response to a TC), the same Pad value than the one contained in the TC pack. shall be copied in the TM packet. For unsolicited TM packet the Pad shall be set to zero.

TM Service Types and Subtypes

DES shall use the TM Packet Types and Subtypes listed in the following table:

Service	Telemetry (Type/Subtype)
1	(1,1): Acceptance Report - Success (1,2): Acceptance Report - Failure
3	(3,25): Housekeeping Report
5	(5,1): Event Reporting: Normal/Progress Report (5,2): Event Reporting: Error/Anomaly Report
6	(6,6): Memory Dump
20	(20,3): MARSIS Science Data Transfer
206	(206,3): MARSIS Private Services (spare)

Table 3-2 TM Type/Subtype used by DES

3.1 MARSIS SOLICITED AND UNSOLICITED TM PACKETS

With reference to the table A2.22 of [AD.1], the telemetry's which are on the same line than a telecommand are considered as being a response to this telecommand (*solicited*). Therefore, they shall follow the routing rules for "Solicited TM packets" concerning the TM_destination_ID (PUS version field) and TC_answer_token (Pad field) of the data field header. In addition all telemetry's of service 1 are also considered as a response to the telecommand they acknowledge. Therefore, they shall also follow the routing rules for *"Solicited TM packets"*.

3.1.1 Solicited TM Packet

In table 3.1.1-1 are listed all the telemetry's that shall be considered *"Solicited TM packets".* They shall follow the routing rules for *"Solicited TM packets"* concerning the TM_destination_ID (PUS version field) and TC_answer_token (Pad field) of the data field header.

ACRONYM	DESCRIPTION	APID		VERIFIED TC
		PID	PCAT	
SIS_ACC_REP_S	Telecommand Acceptance Report - Success TM (1,1)	76	1	SIS_HK_EN_N SIS_HK_EN_R SIS_HK_DIS_N SIS_HK_DIS_R SIS_PATCH_N SIS_PATCH_R SIS_DUMP_TC_N SIS_DUMP_TC_R SIS_TIME_UP_N SIS_TIME_UP_R SIS_OST_TC_N SIS_OST_TC_R SIS_PT_TC_N SIS_PT_TC_R SIS_MOD_TR_DIS_TC_N SIS_MOD_TR_DIS_TC_R SIS_MOD_TR _TC_N SIS_MOD_TR_ TC_R
SIS_ACC_REP_F	Telecommand Acceptance Report - Failure TM (1,2)	76	1	SIS_HK_EN_N SIS_HK_EN_R SIS_HK_DIS_N SIS_HK_DIS_R SIS_PATCH_N SIS_PATCH_R SIS_DUMP_TC_N SIS_DUMP_TC_R SIS_TIME_UP_N SIS_TIME_UP_R SIS_OST_TC_N SIS_OST_TC_R SIS_PT_TC_N SIS_PT_TC_R SIS_MOD_TR_DIS_TC_N SIS_MOD_TR_DIS_TC_R SIS_MOD_TR _TC_N SIS_MOD_TR_ TC_R
SIS_DUMP_TM	Memory Dump TM (6,6)	76÷78,79(1)	9	SIS_DUMP_TC_N SIS_DUMP_TC_R

Table 3.1-1 Solicited TM packets

(1) Flash Memories

3.1.2 Unsolicited TM Packet

In table 3.1.2-1 are listed all the telemetry's that shall be considered *"Unsolicited TM packets".* They shall follow the routing rules for *"Unsolicited TM packets"* concerning the TM_destination_ID (PUS version field) and TC_answer_token (Pad field) of the data field header.

ACRONYM	DESCRIPTION	APID	
		PID	PCAT
SIS_HK_TM	Housekeeping Report Packet TM (3,25)	76	4
SIS_PROG_REP	Event Reporting: Normal/Progress Report TM (5,1)	76	7
SIS_ERR_REP	Event reporting: Error/Anomaly Report (Warning) - TM (5,2)	76	7
SIS_SCIENCE_TM	TM (20,3)	77÷80	12
SIS_PRIVATE_TM	TM (206,3)	76	12

Table 3.1-2 Unsolicited TM packets

3.2 TM-BLOCK STRUCTURE

The Source Packet Telemetry Acquisition shall be performed according to the "Packet TM-Block Acquisition Protocol" as shown in Figure 3.2-1 (cf. [AD.10] § 4.3.1).

The telemetry packets shall be collected in TM-Blocks consisting of a defined number of 16 bit words. The first word shall give the number *"n"* of the following 16 bit words (TM-block length). According to [AD.10], the maximum allowed TM-block length is be 6144 words, but the DES maximum TM-block length shall be 5120 words (cf. §5).

An empty TM-block shall consist of only one 16 bit word, indicating the TM-block size information, which shall be set to zero.

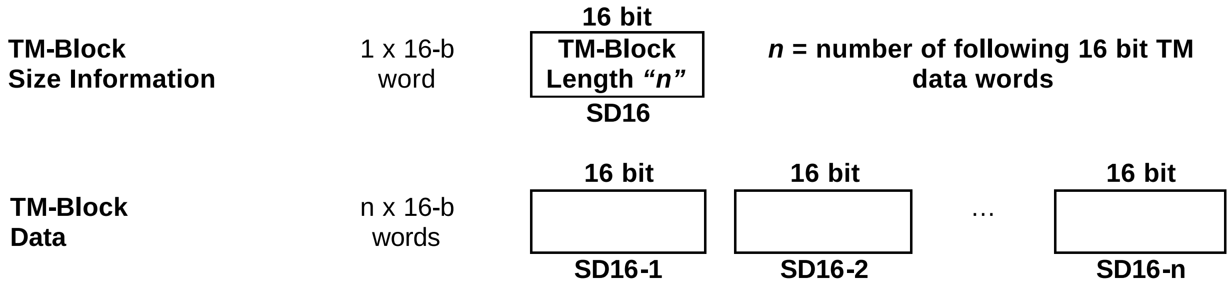


Figure 3.2-1 TM Block Acquisition Protocol

3.3 OPERATION MODE IDENTIFIER

The operation mode identifier are reported in the following table.

OPERATION MODE	ID (dec)
CHECK/INIT	0
STANDBY	1
WARM-UP1	2
WARM-UP2	3
IDLE	4
CALIBR.	5
REC. ONLY.	6
ACT. IONO.	7
SS1	8
SS2	9
SS3	10
SS4	11
SS5	12
data moving from RAM buffer to Flash Memory	13
SPARE	14

Table 3.3-1 Operation Mode IDs

Note that the number 15_d = 1111_b cannot be used. In fact the program RAM is initialised to one and the DES SW shall use this feature to recognise the end of the OST in the error case in which the last OST line is different from the foreseen one (transition to WU-2 mode, cf. [AD.11]).

4. MARSIS TC/TM SERVICES & PACKET DEFINITION

In this section will be defined and detailed those fields in both TM and TC packets that are experiment or MARSIS specific and partially defined (or not defined at all) in [AD.1].

Particular details will be provided in describing both the Source Data and the Application Data fields, respectively for the TM and TC packets.

4.1 SERVICE 1: TELECOMMAND VERIFICATION

This service shall allow the command source to verify identified commands at acceptance by asking the addressed application to generate service type 1 reports in the telemetry stream.

For MARSIS the response required is restricted to:

- Acceptance Success (service sub type 1) or Failure (service sub type 2).

The DES SW shall generate the acceptance Report TM Packet immediately after completion of checks on validity of the TC packet header and data field (within 20 seconds from TC reception).

The response with service 1 upon TC reception is submitted to the value of the Acknowledge (Ack) field of the TC Data Field Header, according to the following scheme.

- TM(1,1) has to be generated *only if* the ACK field of the received TC is 0001_b *and* the TC is received correctly
- TM(1,2) has to be generated *only if* the ACK field of the received TC is 0001_b *and* the TC is not received correctly.
- *If* the ACK field of the received TC is equal to 0000_b *and* the TC is received correctly, none telemetry (TM(1,1)) has to be sent to the S/C.
- *If* the ACK field of the received TC is equal to 0000_b *and* the TC is *not* received correctly, no acknowledge TM (TM(1,2)) has to be sent to the S/C but an ERROR/ANOMALY REPORT TM (TM(5,2)) HAS TO BE GENERATED INSTEAD (cf. service 5 event reporting § 4.3).
- Should the TC be received incomplete and the Ack field be unavailable, the DES SW shall generate an acceptance Report Failure TM(1,2).

Telemetry (1,1): Telecommand Acceptance Report – Success (SIS_ACC_REP_S)

As the TC packet shall be accepted by MARSIS only in STANDBY Support Mode, this Telecommand Verification Telemetry shall then be generated only during this Mode.

	SOURCE PACKET HEADER (48 bit)								*PACKET DATA FIELD (Variable)*	
Field	PACKET ID					PACKET SEQUENCE CONTROL		PACKET LENGTH	DATA FIELD HEADER	SOURCE DATA
Subfield	Version Number	Type	Data Field Header Flag	Application Process ID		Segment. Flags	Source Sequence Count	(octets in Packet Data Field –1)		
				Proc. ID	Pack. Cat.					
Content	000_b	0	1	76_d	1_d	11_b	$(0\ ,2^{14}\text{-}1)_d$	$(14\text{-}1)_d$		
Wide (bit)	3 b	1 b	1 b	7 b	4 b	2 b	14 b	16 b	80 b	
Wide (oct.)	2 B					2 B		2 B	10 B	4 B

Figure 4.1-1 TM(1,1): TC Acceptance Report - Success Packet

	PACKET DATA FIELD (Variable)								
Field	DATA FIELD HEADER							SOURCE DATA	
Subfield	SCET Time	PUS	Check. Flag	Spare	Pack. Type	Pack. Subtype	Pad	TC Packet ID Full copy of the Packet ID of the TC being reported on	TC Sequence Control Full copy of the Packet Sequence Control of the TC being reported on
Content	-----	0_d	0	0000_b	1_d	1_d	0		
Wide (bit)	48 b	3 b	1 b	4 b	8 b	8 b	8 b	16 b	16 b
Wide (oct.)	10 B							4 B	

Figure 4.1-2 TM(1,1): TC Acceptance Report - Success Packet Data Field

Telemetry (1,2): Telecommand Acceptance Report – Failure (SIS_ACC_REP_F)

DES shall not execute any erroneous TC and, when the TC Ack field value is 0001_b, an Acceptance Report Failure TM(1,2) shall be provided to indicate the reason why the TC is erroneous and the command has not been executed. This TM can be generated in every Operation (Support or Operative) Mode.

Standard Failure Codes, uniquely identified by a Failure IDentifier (FID) are used (see Table 4.1-1). The following verification procedure tests are the only performed by the TC validation task in order to accept a TC packet for execution (the Failure ID is also indicated):

- FID = 1 Check the complete TC Packet reception, within 2 seconds from the reception of its first 16-bit word. Note that the Packet Header has fixed length while the Packet Data Field length is specified in the Packet Length field.
- FID = 2 Evaluate the TC Packet CRC and check it with the Packet Error Control field.
- FID = 3 Check the TC Packet APID of Packet Header for both fields PID and PCAT.
- FID = 4 Check the TC Packet type and subtype (i.e. the command code) of the Packet Data Field Header.
- FID = 5 Check the TC Packet feasibility against the current Operative Mode.
- FID = 6 Check the TC Packet Application Data field consistency against its type and subtype.

The preceding tests are executed in the reported order. The verification procedure shall be interrupted, and the TC Packet refused, as soon as only one inconsistency is detected.

Complementary information related to every specific TC FID shall be contained within the Parameters field of the Source Data field. For each FID the foreseen parameters are described in Table 4.1-2.

In case of Incomplete Packet within Timeout (FID=1), if one of the requested fields (Packet ID, Packet Sequence Control, Packet Type, Sub-Type and Length) is unavailable, the corresponding field of TM(1,2) shall be filled by octets FF_H.

	SOURCE PACKET HEADER (48 bit)								PACKET DATA FIELD (Variable)	
Field	PACKET ID					PACKET SEQUENCE CONTROL		PACKET LENGTH	DATA FIELD HEADER	SOURCE DATA
Subfield	Version Number	Type	Data Field Header Flag	Application Process ID		Segment. Flags	Source Sequence Count	(octets in Packet Data Field –1)		
				Proc. ID	Pack. Cat.					
Content	000_b	0	1	76d	1_d	11_b	$(0\ ,2^{14}\text{-}1)_d$	$(17\text{+max }22\text{-}1)_d$		
Wide (bit)	3 b	1 b	1 b	7 b	4 b	2 b	14 b	16 b	80 b	
Wide (oct.)	2 B					2 B		2 B	10B	variable (max 12 B)

Figure 4.1-3: TM(1,2): TC Acceptance Report - Failure Packet

	PACKET DATA FIELD (Variable)										
Field	DATA FIELD HEADER							SOURCE DATA			
Subfield	SCET Time	PUS	Check. Flag	Spare	Pack. Type	Pack. Subtype	Pad	TC Packet ID Full copy of the Packet ID of the TC being reported on	TC Seq. Control Full copy of the Packet Seq. Control of the TC being reported on	FID	Parameters
Content	-----	0	0	0000_b	1_d	2_d	0				
Wide (bit)	48 b	3 b	1 b	4 b	8 b	8 b	8 b	16 b	16 b	16 b	variable (max 48 b)
Wide (oct.)	10 B							variable (max 12B)			

Figure 4.1-4 TM(1,2): TC Acceptance Report - Failure Packet Data Field

FID	Acronym	Meaning
1_d	*TIMEOUT_OCCURR_TC_FAIL*	Incomplete Packet: incomplete reception within timeout interval (2 sec.).
2_d	*INCORRECT_CHECK_TC_FAIL*	Incorrect checksum (CRC).
3_d	*INCORRECT_APP_ID_TC_FAIL*	Incorrect application ID in the TC packet header.
4_d	*INVALID_CMD_CODE_TC_FAIL*	**Invalid command code.**
5_d	*INCORRECT_STATUS_TC_FAIL*	**Command can not be executed at this time (incorrect status of application to allow command execution).**
6_d	*INCONSISTENT_DATA_TC_FAIL*	**Packet data field inconsistent.**

Table 4.1-1 TM(1,2): TC Acceptance Report - Failure Code definition

FID (2 oct)	Parameter 1 (1 oct) PACK. TYPE	Parameter 2 (1 oct) PACK. SUB-TYPE	Parameter 3 (variable)	Parameter 4 (variable)
1_d: Incomplete Packet within timeout.	Pack. Type from the received TC	Pack. Sub-Type from the received TC	Length field of the Pack. Header of the received TC (2 oct)	Number of received octets (2 oct)
2_d: Incorrect checksum (CRC)	Pack. Type from the received TC	Pack. Sub-Type from the received TC	Received Checksum (2 oct)	Computed Checksum (2 oct)
3_d: Incorrect APID	Pack. Type from the received TC	Pack. Sub-Type from the received TC		
4_d: Invalid type/sub-type (command code)	Pack. Type from the received TC	Pack. Sub-Type from the received TC		
5_d: Command can not be executed at this time.	Pack. Type from the received TC	Pack. Sub-Type from the received TC	ID Relevant to the actual Operative Mode(2 oct)	Reason(1) (2 oct)
6_d: Packet Application Data Field inconsistent	Pack. Type from the received TC	Pack. Sub-Type from the received TC	Position (in octs) of the 1st inconsistent param. (2 oct)	Received value of the 1st inconsistent param.(2 oct)

As regard FID=6, different Data Fields has to be checked for different TCs, according to the following table.

(1) - reason = **0x1 - SCET_UNAVAILABLE**, i.e. the TC has been received before the OBT TC which is the first TC the DES has to accept and execute.
- reason = **0x2 - INVALID_OP_MODE**, i.e. the TC has been received in an operation mode different from STANDBY or IDLE; note that only DUMP TCs are accepted in IDLE mode.
- reason = **0x3 - MASTER_PM_PATCH_TCs_BUFFER_FULL**, i.e. the buffer used to store patch TC targeting the master program memory is full.
- reason = **0x4 - MASTER_PM_PATCH_TCs_UNAVAILABLE_FOR_PATCH_EXECUTION**, i.e. a TC requesting to start executing the patch of the master program memory has been received, but no patch TC targeting the master program memory has been previously sent.
- reason = **0x5 - RECEIVED_TCs_BUFFER_FULL**, i.e. the buffer used to store received TC for further validation is full.
- reason = **0x6 – FLASH_MEMORIES_BUSY**, i.e. the requested operation on FLASH memories cannot be executed, due to another operation already in progress on FLASH memories.

TELECOMMAND TYPE,SUBTYPE	CONDITIONS: FIELDS AD VALUES TO BE CHECKED
TC(3,5)	1. PAD = 0 2. SID = 0
TC(3,6)	1. PAD = 0 2. SID = 0
TC(6,2)	1. Mem I D ÷ Proc ID Matching (ref Table 4.4-1) 2. N in the range 1÷29 3. Start Address within the Proper Memory address range (specified by MEM ID) ref Table 4.4-1 4. [Start Address + (Length of Block * Memory word size)] within the Proper Memory address range (specified by MEM ID). 5. The number of recognised correct blocks equals N; last block ends when the application data field ends.
TC(6,5)	1. Memory ID in MARSIS range 2. N in the range 1÷39 3. Start Address within the Proper Memory address range (specified by MEM ID) 4. [Start Address + (Length of Block * Memory word size)] within the Proper Memory address range (specified by MEM ID). 5. The number of recognised correct blocks equals N
TC(9,1)	NONE
TC(206,1)	1. Memory ID = 177 2. N in the range 1÷13 3. Relative Start Address: 0÷1022 <u>even number</u> 4. Length of the block: 2÷38 <u>even number</u> 5. Rel. Start Address – Length of the Block coherency see AD 15 (PT); [Rel. Start Address + Length of Block] < 1024 6. The number of recognised correct blocks equals N
TC(206,2)	1. Memory ID – Process ID matching (cf. tables 4.4-1 and 3-1): MEM ID = 177 ? PROC ID = 76, MEM ID = 180 ? PROC ID = 77, MEM ID = 184 ? PROC ID = 78. 2. N in the range 1÷19 3. Relative Start Address: see AD 15 (PT); 4. Length of the Block: 1÷38 <u>integer number</u> 5. Rel. Start Address – Length of the Block coherency (see annex 1): [Rel. Start Address + Length of Block] < 364 for MEM ID = 177 PT master size see AD 15 [Rel. Start Address + Length of Block] < 4656 for MEM ID = 180 and 184 PT slaves size see AD 15 6. The number of recognised correct blocks equals N; last block ends when the application data field ends. 7. Check if TC of second boot is correct. Address code matching: see AD 15; 8. Check if TC of warm restart is correct. Address code matching: see AD 15;
TC(207,1)	Mode duration > Current Mode Duration

Table 4.1-3 TM(1,2) FID=6: field to be checked VS TC type and subtype

Note that:

- for TC(6,2) and TC(6,5) points 3 and 4 shall be repeated N times and parameters 3 and 4 refer to the start address of the first inconsistent block;
- for TC(206,1) and TC(206,2) points 3, 4 and 5 shall be repeated N times, and parameters 3 and 4 refer to the start address of the first inconsistent block;

4.2 SERVICE 3: HOUSEKEEPING REPORTING

This service controls the generation of HK report packets. Once every 8 seconds, the DES shall sample HK parameters (see Table 4.2-1) and shall allocated them within the parameters' field of a dedicated HK Report Packet (service sub type 25). Immediately after, the packet shall be queued within a TM-block to be sent to the RTU (cf. § 5).

The HK report generation can be enabled and disabled. The requests for enabling (service sub type 5) and disabling (service sub type 6) HK report generation can be received only during the STANDBY mode. By default, at power-on, HK packet generation is enabled.

Telecommand (3,5): Enable Housekeeping Report Packet Generation (SIS_HK_EN)

	PACKET HEADER (48 bit)									*PACKET DATA FIELD (Variable)*		
Field	PACKET ID					PACKET SEQUENCE CONTROL			PACKET LENGTH	DATA FIELD HEADER	APPLIC. DATA	PACKET ERROR CONTROL
Subfield	Version Number	Type	Data Field Header Flag	Application Process ID		SequenceFlags	Source Sequence Count		(octets in Packet Data Field –1)			
				Proc. ID	Pack. Cat.		Source Part	Sequence Part				
Content	000_b	1	1	76_d	12_d	11_b	......b	$(0\ ,2^{11}-1)_d$	$(8-1)_d$			
Wide (bit)	3 b	1 b	1 b	7 b	4 b	2 b	3 b	11b	16 b	32 b	16 b	16 b
Wide (oct.)	2 B					2 B			2 B	4 B	2 B	2 B

Figure 4.2-1 TC(3,5): Enable HK Report Generation Packet

	PACKET DATA FIELD (Variable)								
Field	DATA FIELD HEADER						APPLICATION DATA		PACKET ERROR CONTROL
Subfield	PUS version	Check. Type	Ack	Pack. Type	Pack. Subtype	Pad	PAD	SID	
Content	.......b	1	0001	3_d	5_d	0_b	00000000_b	0(1)	
Wide (bit)	3 b	1 b	4 b	8 b	8 b	8 b	8 b	8 b	16 b
Wide (oct.)	4 B						1 B	1 B	2 B

Figure 4.2-2 TC(3,5): Enable HK Report Generation Packet Data Field

(1) 0 is the only valid SID value for the DES and it indicates that HK parameters shall be sampled every 8 seconds.

Telecommand (3,6): Disable Housekeeping Report Packet Generation (SIS_HK_DIS)

	PACKET HEADER (48 bit)									PACKET DATA FIELD (Variable)		
Field	PACKET ID					PACKET SEQUENCE CONTROL			PACKET LENGTH	DATA FIELD HEADER	APPLIC. DATA	PACKET ERROR CONTROL
Subfield	Version Number	Type	Data Field Header Flag	Application Process ID		SequenceFlags	Source Sequence Count		(octets in Packet Data Field –1)			
				Proc. ID	Pack. Cat.		Source Part	Sequence Part				
Content	000_b	1	1	76_d	12_d	11_b	......b	$(0, 2^{11}-1)_d$	$(8-1)_d$			
Wide (bit)	3 b	1 b	1 b	7 b	4 b	2 b	3 b	11b	16 b	32 b	16 b	16 b
Wide (oct.)	2 B					2 B			2 B	4 B	2 B	2 B

Figure 4.2-3 TC(3,6): Disable HK Report Generation Packet

	PACKET DATA FIELD (Variable)								
Field	DATA FIELD HEADER						APPLICATION DATA		PACKET ERROR CONTROL
Subfield	PUS version	Check. Type	Ack	Pack. Type	Pack. Subtype	Pad	PAD	SID	
Content	.......b	1	0001_b	3_d	6_d	0_b	00000000_b	0(1)	
Wide (bit)	3 b	1 b	4 b	8 b	8 b	8 b	8 b	8 b	16 b
Wide (oct.)	4 B						1 B	1 B	2 B

Figure 4.2-4 TC(3,6): Disable HK Report Generation Packet Data Field

(1) 0 is the only valid SID value for the DES and it indicates that HK parameters shall be sampled every 8 seconds.

Telemetry (3,25): Housekeeping Report Packet (SIS_HK_TM)

	SOURCE PACKET HEADER (48 bit)								*PACKET DATA FIELD*	
Field	PACKET ID					PACKET SEQUENCE CONTROL		PACKET LENGTH	DATA FIELD HEADER	SOURCE DATA
Subfield	Version Number	Type	Data Field Header Flag	Application Process ID		Segment Flags	Source Sequence Count	(octets in Packet Data Field –1)		
				Proc. ID	Pack. Cat.					
Content	000_b	0	1	76_d	4_d	11_b	$(0 , 2^{14}-1)_d$	$(212-1)_d$		
Wide (bit)	3 b	1 b	1 b	7 b	4 b	2 b	14 b	16 b	80 b	
Wide (oct.)	2 B					2 B		2 B	10 B	1.1.0.1.1.1.1 202 B

Figure 4.2-5 TM(3,25): HK Report Packet fields

	PACKET DATA FIELD (Variable)									
Field	DATA FIELD HEADER							SOURCE DATA		
Subfield	SCET Time	PUS	Chck. Flag	Spare	Pack. Type	Pack. Subtype	Pad	PAD	SID	Parameters DES SW Status Word
Content	-----	2_d	0	0000_b	3_d	25_d	0	0	0[VI]	
Wide (bit)	48 b	3 b	1 b	4 b	8 b	8 b	8 b	8 b	8 b	
Wide (oct.)	10 B							1 B	1 B	200 B

Figure 4.2-6 TM(3,25): HK Report Packet Data Field

[VI] 0 is the only valid SID value for the DES and it indicates that HK parameters shall be sampled every 8 seconds.

4.2.1 HK Report Packet Data Field

4.2.1.1 Science Code Parameters

Refer to §6.1 to determine when Science Code is running.

Current Operative Mode ID[VII]	16 bit
Current PRI#	32 bit
Current SCET (if available)	48 bit
Number of accepted TC	16 bit
Number of refused TC	16 bit
Last BIT results	70 bytes
Number of Acceptance Report (TM (1,2)) queued[VIII]	16 bit
Number of Event Report (TM (5,1) and TM (5,2)) queued[2]	16 bit
Number of HK Report (TM (3,25)) queued[2]	16 bit
Number of Dump Report (TM(6,6)) queued[2]	16 bit
Number of Science Report (TM (20,3)) queued[2]	16 bit
Minor Error Status (don't care)	34 bytes
Number of Individual Echoes Octets stored in the corresponding buffer[IX]	32 bit
FLASH Memories status[X]	32 bit
Number of TM-Block queued	16 bit
SW Version	16 bit
ON-Board Computed PRF	32 bit
PT PRF	32 bit
FLASH Memories TEST/ERASE Init_Status[XI]	32 bit
FLASH Memories TEST/ERASE Current_Status/End_status[XII]	32 bit
FLASH Memories TEST/ERASE Init PRI	32 bit
FLASH Memories TEST/ERASE End PRI	32 bit
Number of 16bit words stored in FLASH Chip0	32 bit

[VII] Refer to Table 3.3-1.

[VIII] During operative mode the TM packet are queued in corresponding buffers, waiting to form a TM-block which will be then acquired from DMS. (cf. §5 for the detailed description of the packetisation strategy).

[IX] The Individual Echoes are stored bare, as they are acquired, to be packetised little by little just before each TM block construction in order to properly fill the TM block itself (cf. §5 for the detailed description of the packetisation strategy).

[X] 0x0 = FLASH_IDLE, 0X1 = FLASH_TEST, 0x2 = FLASH_ERASE, 0x3 = FLASH_READ, 0x4 = FLASH_WRITE, 0x5 = FLASH_ERROR, 0x6 = FLASH_FULL

[XI] bit 31-26 = SPARE (zero filled), bit 25-24 = chip, bit 23-16 = sector, bit 15-0 = offset

[XII] bit 31-30 = test result, bit 29-28 = test status, bit 27-26 = SPARE (zero filled), bit 25-24 = chip, bit 23-16 = sector, bit 15-0 = offset. The following code are used.

- TEST STATUS:
  - 0x0 = END_TEST/NO_OPERATION_IN_PROGRESS
  - 0x1 = Erasing
  - 0x2 = Writing
  - 0x3 = Reading

- TEST RESULT:
  - 0x0 = TEST OK
  - 0x1 = TEST KO

Number of 16bit words stored in FLASH Chip1	32 bit
Number of 16bit words stored in FLASH Chip2	32 bit
Number of 16bit words stored in FLASH Chip3	32 bit
Number of FLASH Data bytes stored into Slave1 DSP RAM buffers	32 bit
Number of FLASH Data bytes stored into Slave2 DSP RAM buffers	32 bit
SPARE	10 byte

Table 4.2-1: TM(3,25), HK Report Packet Data Field – Parameters of the Science Code

4.2.1.2 Default Code Parameters

Refer to §6.1 to determine when Default Code is running.

Current Operative Mode ID	16 bit
Current PRI#	32 bit
Current SCET (if available)	48 bit
# of accepted TC	16 bit
# of refused TC	16 bit
Last BIT results	70 bytes
Number of Acceptance Report (TM (1,2)) queued	16 bit
Number of Event Report (TM (5,1) and TM (5,2)) queued	16 bit
Number of HK Report (TM (3,25)) queued	16 bit
Number of Dump Report (TM(6,6)) queued	16 bit
Number of Science Report (TM (20,3)) queued	16 bit
Don't care	34 byte
Number of Individual Echoes Octets stored in the corresponding buffer	32 bit
Number of Data octets stored in Flash Memories (not implemented)	32 bit
Number of TM-Block queued	16 bit
SPARE	62 byte

Table 4.2-2: TM(3,25), HK Report Packet Data Field – Parameters of the Default Code

4.2.1.3 HK Report Packet BIT Result Field

The Last Bit Result Field (70 byte) is the same for both the previous tables and it is detailed in the following one.

Test executed at run- time	Test executed during bootstrap phase	Test_Flags bit placement	Parameter	Size
N/A	N/A	N/A	TEST_FLAGS[XIII]	32 bit
	X	16	CHECKSUM EEPROM BOOT CODE[XIV] (MASTER DSP)	32 bit

[XIII] Bits 17-31 = 0 (don't care); Bits 0-16:1 = error, 0 = no error

[XIV] Bits 16-31 = expected checksum, stored in the memory device under test;
Bits 0-15 = (evalueted checksum + expected checksum) = *0x0 in case of no error*

	X	15	CHECKSUM MASTER PROGRAM CODE IN EEPROM[2] (MASTER DSP)	32 bit
X	X	14	CHECKSUM PROGRAM CODE IN RAM[2] (MASTER DSP)	32 bit
	X	13	ADDRESS FIRST PROGRAM MEMORY BROKEN CELL[XV] (MASTER DSP)	32 bit
	X	12	ADDRESS FIRST DATA MEMORY BROKEN CELL[3] (MASTER DSP)	32 bit
	X	11	CHECKSUM EEPROM BOOT CODE [2](SLAVE1)	32 bit
	X	10	CHECKSUM PROGRAM CODE EEPROM [2](SLAVE1)	32 bit
X	X	9	CHECKSUM PROGRAM CODE IN RAM[2] (SLAVE1)	32 bit
	X	8	ADDRESS FIRST PROGRAM MEMORY BROKEN CELL[3] (SLAVE1)	32 bit
	X	7	ADDRESS FIRST DATA MEMORY BROKEN CELL[3] (SLAVE1)	32 bit
	X	6	ADDRESS OF FIRST DUAL- PORT MEMOTY BROKEN CELL[3] (SLAVE1)	16 bit
	X	5	CHECKSUM EEPROM BOOT CODE [2](SLAVE2)	32 bit
	X	4	CHECKSUM PROGRAM CODE EEPROM[2] (SLAVE2)	32 bit
X	X	3	CHECKSUM PROGRAM CODE IN RAM [2](SLAVE2)	32 bit
	X	2	ADDRESS FIRST PROGRAM MEMORY BROKEN CELL[3] (SLAVE2)	32 bit
	X	1	ADDRESS FIRST DATA MEMORY BROKEN CELL[3] (SLAVE2)	32 bit
	X	0	ADDRESS OF FIRST DUAL- PORT MEMOTY BROKEN CELL [3](SLAVE2)	16 bit
N/A	N/A	N/A	SPARE	16 bit
			TOTAL	70 bytes

1.1.0.1.1.2 Table 4.2-3 TM(3,25) HK Report Packet Data Field – BIT results Parameters

[XV] 0XFFFFFFFF = NO BROKEN CELL FOUND

4.3 SERVICE 5: EVENT REPORTING

The DES shall use the Event Reporting Service to let transitions between Modes observable by the S/C or Ground. In case of no failure detection the sub type 1 (Normal/Progress Report) shall be used, while, whenever any failure or any malfunction will be detected, the sub type 2 (Error/Anomaly Report - Warning) shall be used.

The Event Identifier (EID) field shall allow to distinguish uniquely the event reported via this service within the whole spacecraft system. In the first parameter field, immediately after the EID, the transition code (MODE Transition IDentifier) is reported, which uniquely identifies the mode transition to be signalled. To each EID field, a number of MODE Tr. IDs is strictly related.

The DES SW shall generate an Event Reporting Packet immediately after completion of the Mode Transition. The MODE Tr. ID in first parameter field will indicate the *current* Mode (transition destination) and the *previous* Mode (transition source).

Complementary information related to a specific Operative Mode transition shall be contained within other parameters' fields which shall follow the first one, as detailed in Table 4.3-2, Table 4.3-3 and Table 4.3-4.

from/to (MODE Tr. ID)	CHECK/INIT	STANDBY	WARM-UP1	WARM-UP2	IDLE	CALIBR.	REC. ONLY	ACT. IONO.	SS1	SS2	SS3	SS4	SS5	FLASH TEST
CHECK/INIT	41501	41517			41565									
STANDBY	41502		41534		41566									
WARM-UP1	41503	41519		41551	41567									
WARM-UP2	41504	41520	41536	41552	41568	41584	41600	41616	41632	41648	41664	41680	41696	41712
IDLE														
CALIBR.	41506			41554	41570	41586	41602	41618	41634	41650	41666	41682	41698	41714
REC. ONLY.	41507			41555	41571	41587	41603	41619	41635	41651	41667	41683	41699	41715
ACT. IONO.	41508			41556	41572	41588	41604	41620	41636	41652	41668	41684	41700	41716
SS1	41509			41557	41573	41589	41605	41621	41637	41653	41669	41685	41701	41717
SS2	41510			41558	41574	41590	41606	41622	41638	41654	41670	41686	41702	41718
SS3	41511			41559	41575	41591	41607	41623	41639	41655	41671	41687	41703	41719
SS4	41512			41560	41576	41592	41608	41624	41640	41656	41672	41688	41704	41720
SS5	41513			41561	41577	41593	41609	41625	41641	41657	41673	41689	41705	41721
FLASH TEST	41514			41562	41578(TBC)	41594	41610	41626	41642	41658	41674	41690	41706	41722

OPERATIVE MODE	CODE (dec)
CHECK/INIT	**0**
STANDBY	**1**
WARM-UP1	**2**
WARM-UP2	**3**
IDLE	**4**
CALIBRATION	**5**
RECEIVE ONLY	**6**
ACTIVE IONO. SOUNDING	**7**
SS1	**8**
SS2	**9**
SS3	**10**
SS4	**11**
SS5	**12**
DATA MOVING IN FLASH	**13**

CODE 14: SPARE

EIDs for MARSIS:	
MIN:	41501
MAX:	42000

(dark grey cell) Not allowed transition: no EID shall be associated.

41xxx Allowed transition: 41xxx EID shall be associated

41xxx (light grey cell) Transition caused by a watchdog reset

Assumptions: 41xxx is the EID associated to transition yy->zz
yy is the previous mode code
zz is the current mode code

Constraints: 42000 >= 41xxx >= 41501 (16 bit needed)
15 >= yy, zz, >= 0 (4 bit needed)

Algorithm: 41xxx = 41501 + (yy + 16 * zz)

Table 4.3-1 TM(5;1,2) Event Reporting: DES commanded Operative Modes Transitions, related MODE Tr. IDs' definition

Telemetry (5,1): Normal/Progress Report (SIS_PROG_REP)

	SOURCE PACKET HEADER (48 bit)								PACKET DATA FIELD (Variable)	
Field	PACKET ID					PACKET SEQUENCE CONTROL		PACKET LENGTH	DATA FIELD HEADER	SOURCE DATA
Subfield	Version Number	Type	Data Field Header Flag	Application Process ID		Segment. Flags	Source Sequence Count	(octets in Packet Data Field –1)		
				Proc. ID	Pack. Cat.					
Content	000_b	0	1	76_d	7_d	11_b	$(0 , 2^{14}-1)_d$	$(26-1)_d$		
Wide (bit)	3 b	1 b	1 b	7 b	4 b	2 b	14 b	16 b	80 b	
Wide (oct.)	2 B					2 B		2 B	10 B	16 B

Figure 4.3-1 TM(5,1): Event Reporting, Normal/Progress Report Packet

	PACKET DATA FIELD (Variable)								
Field	DATA FIELD HEADER							SOURCE DATA	
Subfield	SCET Time	PUS	Chck. Flag	Spare	Pack. Type	Pack. Subtype	Pad	EID	Parameters 1÷4
Content	-----	2_b	0	0000_b	5_d	1_d	0	41801_d 41802_d	
Wide (bit)	48 b	3 b	1 b	4 b	8 b	8 b	8 b	16 b	
Wide (oct.)	10 B							2 B	14 B

Figure 4.3-2: TM(5,1): Event Reporting, Normal/Progress Report Packet Data Field

EID	Parameter 1 (2 oct) Mode Tr. ID	**Parameter 2 (4 oct)**	Parameter 3 (6 oct)	Parameter 4 (2 oct)
41801 Mode Tr. IDs indicating a transition from any Operation Mode (except IDLE) to a Support Mode (except IDLE)	41517÷41561	transition PRI#	transition SCET	FF FF
41802 **Mode Tr. IDs indicating a transition from any Operation Mode (except IDLE) to an Operative Mode**	41584÷41705	transition PRI#	**transition SCET**	**OST line #(1)**

Table 4.3-2 TM(5,1): Event Reporting, Normal/Progress Report Packet – Source Data field: parameters' definition

(1) OST line # is the number of the current OST line *AFTER* the transition.

Telemetry (5,2): Error/Anomaly Report – Warning (SIS_ERR_REP)

In the case of the Error/Anomaly report, following the Mode Tr. ID, the Failure code IDentifier (FID) shall specify, for each single EID, the particular detected failure or malfunction. This parameter shall assume the value FF FF_H when the EID uniquely identifies the failure or malfunction.

Note that all the EIDs but the number 41908 involve an Anomaly Transition specified by the MODE Tr. ID (parameter 1). The EID 41908, on the contrary, *doesn't involve any Mode Transition* and refers to an erroneous TC reception. This telemetry shall be generated when an erroneous TC is received with ACK field equal to 0000_b (cf. §4.1).

	SOURCE PACKET HEADER (48 bit)								***PACKET DATA FIELD (Variable)***	
Field	**PACKET ID**					**PACKET SEQUENCE CONTROL**		**PACKET LENGTH**	**DATA FIELD HEADER**	**SOURCE DATA**
Subfield	**Version Number**	**Type**	**Data Field Header Flag**	**Application Process ID**		**Segment. Flags**	**Source Sequence Count**	**(octets in Packet Data Field –1)**		
				Proc. ID	**Pack. Cat.**					
Content	**000_b**	**0**	**1**	**76_d**	**7_d**	**11_b**	**$(0 , 2^{14}-1)_d$**	**Max $(96-1)_d$**		
Wide (bit)	**3 b**	**1 b**	**1 b**	**7 b**	**4 b**	**2 b**	**14 b**	**16 b**	**80 b**	
Wide (oct.)	**2 B**					**2 B**		**2 B**	**10 B**	**Variable (Max 86 B)**

Figure 4.3-3 TM(5,2): Event Reporting, Error/Anomaly Report – Warning Packet

	PACKET DATA FIELD (Variable)								
Field	**DATA FIELD HEADER**							SOURCE DATA	
Subfield	**SCET Time**	**PUS**	**Chck. Flag**	**Spare**	**Pack. Type**	**Pack. Subtype**	**Pad**	**EID**	**Parameters**
Content	-----	**2_b**	**0**	**0000_b**	**5_d**	**2_d**	**0**	**$41901_d \div 41908_d$**	
Wide (bit)	**48 b**	**3 b**	**1 b**	**4 b**	**8 b**	**8 b**	**8 b**	**16 b**	
Wide (oct.)	**10 B**							**2 B**	**Variable (Max 84B)**

Figure 4.3-4 TM(5,2): Event Reporting, Error/Anomaly Report – Warning Packet Data

EID (2 oct)	Parameter 1 (2 oct) MODE Tr.ID	Parameter 2 (2 oct) FID	Parameter 3 (4 oct) PRI	Parameter 4 (6 oct) SCET	Parameter 5 (70 oct)
41901 ANOMALY TRANSITION BIT failed *not in C/I*	41566÷41577	FF FF_H	Transition PRI	Transition SCET	Last BIT result (70 oct)
41902 ANOMALY TRANSITION BIT failed *in C/I*	41517 14566	FF FF_H	Transition PRI	Transition PRI (SCET not yet available)	Last BIT result (70 oct)
41903 ANOMALY TRANSITION scientificTM packet buffer overflow	41566÷41577	FF FF_H	Transition PRI	Transition SCET	
41904 ANOMALY TRANSITION no SCET available	41566	FF FF_H	Transition PRI		
41905 ANOMALY TRANSITION for HW watchdog	41517÷41566	FF FF_H	Transition PRI	Transition SCET	Last BIT results (70 oct)
41906 ANOMALY TRANSITION to IDLE for SW watchdog	41566÷41577 (SW)	Timer_ID (see Table ***)	Transition PRI	Transition SCET	Last BIT result (70 oct)
41907 ANOMALYTRANSITION SCET* or OST line inconsistency	41566 (SCET inc.) 41568÷41577 (OST inc.)	50, 51 see Table 4.3-6	Transition PRI	Transition SCET	see Table 4.3-5 (14 oct)

Table 4.3-3 TM(5,2): Event Reporting, Error/Anomaly Report Packet - Source Data field: EID 41901÷41907, parameters' definition

EID (2 oct)	Parameter 1 TC Pack ID (2 oct)	Parameter 2 TC Pack Seq. Contr. (2 oct)	Parameter 3 FID (2 oct)	Parameter 4 Pack. Type (1 oct)	Parameter 5 Pack. Sub-Type (1 oct)	Parameter 6 (2 oct)	Parameter 7 (2 oct)
41908 erroneous TC ACK = 0000_b	Full copy of the Pack ID of the TC being reporting on	Full copy of the Pack Sequence Control of the TC being reporting on	1_d: Incomplete Packet within timeout.	Pack. Type from the received TC	Pack. Sub-Type from the received TC	Length field of the Pack. Header of the received TC (2 oct)	Number of received octets (2 oct)
41908 erroneous TC ACK = 0000_b	Full copy of the Pack ID of the TC being reporting on	Full copy of the Pack Sequence Control of the TC being reporting on	2_d: Incorrect checksum (CRC)	Pack. Type from the received TC	Pack. Sub-Type from the received TC	Received Checksum (2 oct)	Computed Checksum (2 oct)
41908 erroneous TC ACK = 0000_b	Full copy of the Pack ID of the TC being reporting on	Full copy of the Pack Sequence Control of the TC being reporting on	3_d: Incorrect APID	Pack. Type from the received TC	Pack. Sub-Type from the received TC	FF FF_H	FF FF_H
41908 erroneous TC ACK = 0000_b	Full copy of the Pack ID of the TC being reporting on	Full copy of the Pack Sequence Control of the TC being reporting on	4_d: Invalid type/sub-type (command code)	Pack. Type from the received TC	Pack. Sub-Type from the received TC	FF FF_H	FF FF_H
41908 erroneous TC ACK = 0000_b	Full copy of the Pack ID of the TC being reporting on	Full copy of the Pack Sequence Control of the TC being reporting on	5_d: Command can not be executed at this time.	Pack. Type from the received TC	Pack. Sub-Type from the received TC	ID Relevant to the actual Operative Mode(2 oct)	Reason (2 oct)
41908 erroneous TC ACK = 0000_b	Full copy of the Pack ID of the TC being reporting on	Full copy of the Pack Sequence Control of the TC being reporting on	6_d: Packet Application Data Field inconsistent	Pack. Type from the received TC	Pack. Sub-Type from the received TC	Position (in octs) of the 1^{st} inc. param. (2 oct)	Received value of the 1^{st} inc. param. (2 oct)

Table 4.3-4 TM(5,2): Event Reporting, Error/Anomaly Report Packet – Source Data field: EID 41908, parameters' definition

As for TM(1,2) (cf. Table 4.1-2):

- FID = 1 all parameters: FF FF_H if not available;
- FID = 5 parameter 7: see note (1) to Table 4.1-2;
- FID = 6: see Table 4.1-3 for executed checks.

ID	FID	MEANING
BOOT_BIT_S1_TOUT	0x**03**	Timeout on Slave1 Bootstrap BIT results reception
BOOT_BIT_S2_TOUT	0x04	Timeout on Slave2 Bootstrap BIT results reception
BOOT_BIT_S1_and *S2*_TOUT	0x05	Timeout on both Slave1 and Slave2 Bootstrap BIT results reception
S1_Par_Eval_TOUT	0x06	Timeout on Slave1 phase correction terms evaluation (ACQ or TRK)
S2_Par_Eval_TOUT	0x07	Timeout on Slave2 phase correction terms evaluation (ACQ or TRK)
S1_Patch_TOUT	0x08	Timeout on Slave1 Patch execution
S2_Patch_TOUT	0x09	Timeout on Slave2 Patch execution
S1_Dump_TOUT	0x0a	Timeout on Slave1 Dump execution
S2_Dump_TOUT	0x0b	Timeout on Slave2 Dump execution
S1_BIT_TOUT	0x0c	Timeout on Slave1 run-time BIT results reception
S2_BIT_TOUT	0x0d	Timeout on Slave2 run-time BIT results reception
S1_SA_EC_TOUT	0x0e	Timeout on Slave1 Synthetic Aperture/Echo Collection phases
S2_SA_EC_TOUT	0x0f	Timeout on Slave2 Synthetic Aperture/Echo Collection phases
S1_LED_POST_SA_TOUT	0x10	Timeout on Slave 1 for: - Tracking Post ynthetic Aperture results reception; - Acquisition LED results reception; - AIS final results reception
S2_LED_POST_SA_TOUT	0x011	Timeout on Slave 2 for: - Tracking Post ynthetic Aperture results reception; - Acquisition LED results reception; AIS final results reception
S1_Not_SS_TOUT	0x12	Timeout on Slave 1 for: - HW_Cal/Rec_Only results reception; - AIS Maximum Exponent reception
S2_Not_SS_TOUT	0x13	Timeout on Slave 2 for - HW_Cal/Rec_Only results reception; - AIS Maximum Exponent reception
S1_NPM_TOUT	0x14	Timeout on Slave1 NPM results reception
S1_PIS_TOUT	0x15	Timeout on Slave1 PIS results reception

Table 4.3-5: ID, FID numbers and meaning

FID	Corresponding Event
50	SCET* Inconsistency: SCET* - SCET_CURRENT < W_UP1+W_UP2 duration = 5 + 20 sec. 14 byte = 6 byte SCET* + 6 byte CURRENT_ SCET + 2 byte FF FF_H (transition STBY_IDLE)
51	OST Inconsistency: mode selection field value different from 3_d, 5_d, 12_d (cf. Table 3.3-1). 14 byte = 2 byte 1st inc. OST Line # (from zero) + 12 byte 1st inc OST LINE

Table 4.3-6: FID numbers and corresponding events

4.4 SERVICE 6: MEMORY MANAGEMENT

This service supports scatter bad and dump, as well as block load and dump, of an on-board memory. Scattered loading of selected non-contiguous locations by means of a single TC shall be possible.

Only Absolute address method of addressing the memory is supported by this service: this allows the user to specify a real address start loading or dumping from.

With regard to the DES Dump and Patch functionality:

- Memory patch and dump Telecommands shall be accepted from MARSIS only in STANDBY Mode.
- All DES memory areas (volatile and non volatile) shall be accessible for dumps.
- All DES writable memory areas shall be accessible for patch operations.
- It shall be possible to load/modify the Operations Sequence Table and Parameters Table performing a patch operation on the relevant EEPROM memories. This operation shall be done using TC(6,2) defined in the following).
- The length of the area to be dumped shall not be limited by the size of the maximum TM packet size.
- The DES SW shall generate, as result of the TC(6,5), as many TM(6,6) dump packets as required to cover the entire commanded dump area.
- There shall be no constraints imposed on how to break down the dump area into TM(6,6) dump packets.

The destination memory to be patched/dumped shall be uniquely identified by a Memory ID, as detailed in the following table.

Process ID	Destination	Memory ID	Memory Type	Bank #	Memory size and width	Absolute Start-End Address	Dump Range	Patch Range
76	C&C	176	EEPROM	1	128K x 48bit	0x0 – 0x1FFFF	0x0 – 0x1FFFF	0xB000 – 0x1FFFF
	C&C	177	Program SRAM	1	512K x 48bit	0x20000 – 0x9FFFF	0x20000 – 0x9FFFF	0x20000 – 0x9FFFF
	C&C	178	Data SRAM	0	512K x 32bit	0x0 – 0x7FFFF	0x0 – 0x7FFFF	0x0 – 0x7FFFF
	C&C	191	FPGA Registers (memory mapped)	0	Variable (see annex 1)	0x80000 - 0xABFFF	See Annex1	See Annex1
77	DSP1	179	EEPROM	1	128K x 48bit	0x0 – 0x1FFFF	0x0 – 0x1FFFF	0x2000 – 0x1FFFF
	DSP1	180	Program SRAM	1	512K x 48bit	0x20000 – 0x9FFFF	0x20000 – 0x9FFFF	0x20000 – 0x9FFFF
	DSP1	181	Data SRAM	0	512K x 32bit	0x0 – 0x7FFFF	0x0 – 0x7FFFF	0x0 – 0x7FFFF
	DSP1	182	Dual-port SRAM	0	8K x 16bit	0x80000- 0x81FFFF	0x80000-0x81FFFF	0x80000-0x81FFFF
78	DSP2	183	EEPROM	1	128K x 48bit	0x0 – 0x1FFFF	0x0 – 0x1FFFF	0x2000 – 0x1FFFF
	DSP2	184	Program SRAM	1	512K x 48bit	0x20000 – 0x9FFFF	0x20000 – 0x9FFFF	0x20000 – 0x9FFFF
	DSP2	185	Data SRAM	0	512K x 32bit	0x0 – 0x7FFFF	0x0 – 0x7FFFF	0x0 – 0x7FFFF
	DSP2	186	Dual-port SRAM	0	8K x 16bit	0x80000- 0x81FFFF	0x80000-0x81FFFF	0x80000-0x81FFFF
79	TIMING	187	FLASH (chip 0)	0	2M x 16 bit	0x0 – 0x1FFFFF	0x0 – 0x1FFFFF	N/A
	TIMING	188	FLASH (chip 1)	0	2M x 16 bit	0x0 – 0x1FFFFF	0x0 – 0x1FFFFF	N/A
	TIMING	189	FLASH (chip 2)	1	2M x 16 bit	0x0 – 0x1FFFFF	0x0 – 0x1FFFFF	N/A
	TIMING	190	FLASH (chip 3)	1	2M x 16 bit	0x0 – 0x1FFFFF	0x0 – 0x1FFFFF	N/A

Table 4.4-1 Memory Management, MARSIS Payload Memory ID definition

Depending on the memory width, the memory structure is defined as follows:

For 16 bit memory width

Data word
2 octets

For 32 bit memory width

Most Significant Word	Least Significant Word
2 octets	**2 octets**

For 40 bit memory width

Not Used	Most Sign. Byte	Middle Data Word	Least Significant Word
1 octet	1 octet	2 octets	2 octets

For 48 bit memory width

Most Significant Word	Middle Data Word	Least Significant Word
2 octets	2 octets	2 octets

Figure 4.4-1 Memory Management, Memory structure

According to [AD.1], Memory Management TCs and TMs shall be structured as described in the following.

Telecommand (6,2): Load Memory Using Absolute Addresses (SIS_PATCH)

	PACKET HEADER									*PACKET DATA FIELD (Variable)*		
Field	PACKET ID					PACKET SEQUENCE CONTROL			PACKET LENGTH	DATA FIELD HEADER	APPLIC. DATA	PACKET ERROR CONTROL
Subfield	Version Number	Type	Data Field Header Flag	Application Process ID		Sequence Flags	Source Sequence Count (one counter for each Application Process ID)		(octets in Packet Data Field –1)			
				Proc. ID	Pack. Cat.		Source Part	Sequence Part				
Content	000_b	1	1	$(76 \div 79)_d$	12_d	11_b	$\ldots\ldots_b$	$(0 \div 2^{11}-1)_d$	$((16 \div 242)-1)_d$			
Wide (bit)	3 b	1 b	1 b	7 b	4 b	2 b	3 b	11b	16 b	32 b		16 b
Wide (oct.)	2 B					2 B			2 B	4 B	$(10 \div 236)$ B	2 B

Figure 4.4-1 TC(6,2): Load Memory Using Absolute Addresses Packet

	PACKET DATA FIELD (Variable)											
Field	DATA FIELD HEADER						APPLICATION DATA					PACK. ERR CTRL
Subfield	PUS version	Check. Type	Ack	Pack. Type	Pack. Sub-type	Pad	1.1.0.1.1.2.1	N(1)	Block (Repeated N Times)			
									Start Address(2)	Length of the Block(3)	Data(4)	
Content	$\ldots_b$	1	0001_b	6_d	2_d	0_b	$(176 \div 191)_d$	$(1 \div 29)_d$				
Wide (bit)	3 b	1 b	4 b	8 b	8 b	8 b	8 b	8 b	32 b	16 b		16 b
Wide (oct.)	4 B						1 B	1B	4 B	2 B	2 B $\div$ V.ble in 2 B	2 B

Figure 4.4-2 TC(6,2): Load Memory Using Absolute Addresses Packet Data Field

(1) **N**: number of blocks to be loaded. This field is systematically present, even in case it is equal to 1 and there is only one block.

(2) **Start Address**: defines the address, of the first word to be loaded. The other words will be loaded consecutively from this start address.

(3) **Length of Block**: number of 48, 40, 32, or 16 bit words to be loaded (dependant of the memory width of the memory type). This information allows in particular to define the end of the block to be loaded, and to find the header of the next block to be loaded.

(4) **Data**: data to be loaded within the block from the defined start address.

Telecomand (6,5): Dump Memory Using Absolute Address (SIS_DUMP_TC)

	PACKET HEADER									PACKET DATA FIELD (Variable)		
Field	PACKET ID					PACKET SEQUENCE CONTROL			PACKET LENGTH	DATA FIELD HEADER	APPLIC. DATA	PACKET ERROR CONTROL
Subfield	Version Number	Type	Data Field Header Flag	Application Process ID		Sequence Flags	Source Sequence Count		(octets in Packet Data Field –1)			
				Proc. ID	Pack. Cat.		Source Part	Sequence Part				
Content	000_b	1	1	$(76, 79)_d$	12_d	11_b	$\ldots\ldots_b$	$(0, 2^{11}-1)_d$	$((14, 242)-1)_d$			
Wide (bit)	3 b	1 b	1 b	7 b	4 b	2 b	3 b	11b	16 b	32 b		16 b
Wide (oct.)	2 B					2 B			2 B	4 B	(8, 236) B	2 B

Figure 4.4-3 TC(6,5): Dump Memory Using Absolute Addresses Packet

	PACKET DATA FIELD(Variable)										
Field	DATA FIELD HEADER						APPLICATION DATA				PACK. ERR CTRL
Subfield	PUS version	Check. Type	Ack	Pack. Type	Pack. Subtype	Pad	Memory ID	N(1)	Block (Repeated N Times): Start Address(2)	Block (Repeated N Times): Length of the Block(3)	
Content	$\ldots_b$	1	0001_b	6_d	5_d	0_b	$(176, 191)_d$	$(1, 39)_d$			
Wide (bit)	3 b	1 b	4 b	8 b	8 b	8 b	8 b	8 b	32 b	16 b	16 b
Wide (oct.)	4 B						1 B	1B	4 B	2 B	2 B

Figure 4.4-4 TC(6,5): Dump Memory Using Absolute Addresses Packet Data Field

(1) **N**: number of blocks to be dumped. This field is systematically present, even in case it is equal to 1 and there is only one block;
(2) **Start Address**: defines the address, of the first word to be dumped. The other words will be dumped consecutively from this first address;
(3) **Length of Block**: number of 48, 40, 32, or 16 bit words to be dumped (dependant of the memory width of the memory type). This information allows in particular to define the end of the block to be dumped, and to find the header of the next block to be dumped;

Telemetry (6,6): Memory Dump Using Absolute Address Report (SIS_DUMP_TM)

	SOURCE PACKET HEADER (48 bit)								PACKET DATA FIELD (Variable)	
Field	PACKET ID					PACKET SEQUENCE CONTROL		PACKET LENGTH	DATA FIELD HEADER	SOURCE DATA
Subfield	Version Number	Type	Data Field Header Flag	Application Process ID		Segment. Flags	Source Sequence Count (one counter for each Application Process ID)	(octets in Packet Data Field –1)		
				Proc. ID	Pack. Cat.					
Value	000_b	0	1	$(76, 79)_d$	9_d	11_b	$(0, 2^{14}-1)_d$	Max $(4106-1)_d$		
Wide (bit)	3 b	1 b	1 b	7 b	4 b	2 b	14 b	16 b	80 b	
Wide (oct.)	2 B					2 B		2 B	10 B	Variable (Max 4096 B)

Figure 4.4-5 TM(6,6): Memory Dump Using Absolute Addresses Report Packet

	PACKET DATA FIELD (Variable)											
Field	DATA FIELD HEADER							SOURCE DATA				
Subfield	SCET Time	PUS	Check. Flag	Spare	Pack. Type	Pack. Subtype	Pad	Memory ID	N [1]	Block (Repeated N Times)		
										Start Address [2]	Length of the Block [3]	Data [4]
	-----	000_b	0	0000_b	6_d	6_d	0_b	$(176, 191)_d$	$(1, 511)_d$			
Wide (bit)	48 b	3 b	1 b	4 b	8 b	8 b	8 b	8 b	8 b	32 b	16 b	
Wide (oct.)	10 B							1 B	1 B	4 B	2 B	2 B, V.ble in 2 B

Figure 4.4-6 TM(6,6): Memory Dump Using Absolute Addresses Report Packet Data Field

(1) **N**: number of blocks to be dumped. This field is systematically present, even in case it is equal to 1 and there is only one block;

(2) **Start Address**: defines the address, of the first word to be dumped. The other words will be dumped consecutively from this first address;

(3) **Length of Block**: number of 48, 40, 32, or 16 bit words to be dumped (dependant of the memory width of the memory type). This information allows in particular to define the end of the block to be dumped, and to find the header of the next block to be dumped;

(4) **Data**: data to be loaded within the block from the defined start address;

4.5 SERVICE 9: TIME SYNCHRONISATION

This service handles the spacecraft time distribution on-board and instruments synchronisation.

In order to synchronise MARSIS the DMS shall send to the DES the TC time packet (using TC(9,1)) with the new calculated time. On reception of TC(9,1) the DES shall process the TC time packet and shall write the SCET value in the specific OBT register.

The TC Time Packet shall be distributed to DES only in STANDBY Mode and it shall be the first MLC received by DES after the switch-on and after the conclusion of CHECK/INIT Mode.

Telecommand (9,1): Accept Time Update (SIS_TIME_UP)

	PACKET HEADER									***PACKET DATA FIELD (Variable)***		
Field	**PACKET ID**					**PACKET SEQUENCE CONTROL**			**PACKET LENGTH**	**DATA FIELD HEADER**	**APPLIC. DATA**	**PACKET ERROR CONTROL**
Subfield	**Version Number**	**Type**	**Data Field Header Flag**	**Application Process ID**		**SequenceFlags**	**Source Sequence Count**		**(octets in Packet Data Field –1)**			
				Proc. ID	**Pack. Cat.**		**Source Part**	**Sequence Part**				
Content	**000_b**	**1**	**1**	**76_d**	**12_d**	**11_b**	**$\ldots._b$**	**$(0, 2^{11}-1)_d$**	**$(12-1)_d$**			
Wide (bit)	**3 b**	**1 b**	**1 b**	**7 b**	**4 b**	**2 b**	**3 b**	**11b**	**16 b**	**32 b**		**16 b**
Wide (oct.)	**2 B**					**2 B**			**2 B**	**4 B**	6 B	**2 B**

Figure 4.5-1 TC(9,1): Accept Time Update Packet

	PACKET DATA FIELD (Variable)							
Field	**DATA FIELD HEADER**						**APPLICATION DATA**	**PACKET ERROR CONTROL**
Subfield	**PUS version**	**Chck. Type**	**Ack**	**Pack. Type**	**Pack. Subtype**	**Pad**	**On board Time at next TBP**	
Content	**$\ldots._b$**	**1**	**0001_b**	**9_d**	**1_d**	**0_b**	**On-board time at next Time Broadcast Pulse**	
Wide (bit)	**3 b**	**1 b**	**4 b**	**8 b**	**8 b**	**8 b**		**16 b**
Wide (oct.)	**4 B**						6 B	**2 B**

Figure 4.5-2 TC(9,1): Accept Time Update Packet Data Field

4.6 SERVICE 20: SCIENCE DATA TRANSFER

This service controls the collection of science data via the RTU.

Packet generation for Telemetry (20,3) shall follow the policy defined in §5 (Scientific Data Packetisation Strategy).

Because the definition of the Source Data field is experiment specific, the definition of the Source Data field is the subject of this section.

Telemetry (20.3): science Report on RTU Link (SIS_SCIENCE_TM)

	SOURCE PACKET HEADER (48 bits)								***PACKET DATA FIELD (Variable)***	
Field	**PACKET ID**					**PACKET SEQUENCE CONTROL**		**PACKET LENGTH**	DATA FIELD HEADER	SOURCE DATA
Subfield	**Version Number**	**Type**	**Data Field Header Flag**	**Application Process ID**		**Segment. Flags**	**Source Sequence Count (single counter for each single Application Process ID)**	**(octets in Packet Data Field –1)**		
				Proc. ID	**Pack. Cat.**					
Content	**000_b**	**0**	**1**	**$(77, 80)_d$**	**12_d**	**11_b**	**$(0, 2^{14}-1)_d$**	**Max $(4106\text{-}1)_d$**		
Wide (bit)	**3 b**	**1 b**	**1 b**	**7 b**	**4 b**	**2 b**	**14 b**	**16 b**	**80 b**	
Wide (oct.)	**2 B**					**2 B**		**2 B**	**10 B**	**Variable (Max 4096 B)**

Figure 4.6-1 TM(20,3): Telemetry Science Report on RTU link Packet

	PACKET DATA FIELD (Variable)								
Field	**DATA FIELD HEADER**							**SOURCE DATA**	
Subfield	**SCET Time**	**PUS**	**Chck. Flag**	**Spare**	Pack. Type	**Pack. Subtype**	**Pad**	1.1.0.1.1.2.2 ANCILLARY DATA	1.1.0.1.1.2.3 SCIENTIFIC DATA
Content	**-----**	**0_b**	**0**	**0000_b**	**20_d**	**3_d**	**0_b**		
Wide (bit)	**48 b**	**3 b**	**1 b**	**4 b**	**8 b**	**8 b**	**8 b**	Variable (256 or 28) x 8 b	**Variable**
Wide (oct.)	**10 B**							**Variable (Max 4096 B)**	

Figure 4.6-2: TM(20,3): Telemetry Science Report on RTU link Packet Data Field

	SOURCE DATA									
	ANCILLARY DATA									SCIENTIFIC DATA
	ANCILLARY DATA HEADER								AUXILIARY DATA	
Field	**Scientific Data Packet ID**				**Scientific Data Type**	**Scientific Data Source Seq. Counter**	**Scientific Data Seqm. Flags**	**Spare**		
Subfield	**SCET***	**OST line #**	**OST line**	**Frame ID**						
Wide (bit)	**48 b**	**16 bit**	**96 b**	**16 bit**	**2 b**	**14 b**	**2 b**	**30 b**	**1824 b**	**Variable. Max(4068 or 3840) x 8 b**
Wide (oct.)	**28 B**								**228 B**	**Max (4068 B, 3840 B with AUX. DATA)**

Figure 4.6-3 TM(20,3): Telemetry Science Report on RTU link Packet Source Data Field

4.6.1 Ancillary Data

4.6.1.1 Ancillary Data Header

SCIENTIFIC DATA PACKET ID sub-fields

- SCET*. It is the Operative Phase start time. The *first* FRAME of the *first* Operative Mode starts at the *first* PRI start time *after* SCET*.
- OST line #. It is the number of the OST line relevant to Scientific Data contained in the packet. The counter starts from zero.
- OST Line. It is the whole record of the OST line relevant to Scientific Data contained in the packet. The OST line contains the Operative Mode and the complete instrument settings concerning the packet Scientific Data.
- Frame ID. A single TM(20,3) packet shall not contain Scientific Data acquired in two or more different Frames. The Frame Identifier is the number of the Frame in which the Scientific Data contained in the packed have been acquired. The counter starts from zero and it is reset for each new OST line.

SCIENTIFIC DATA TYPE sub-field

Four type of Scientific Data are foreseen but a single TM(20,3) packet shall not contain data of two or more different types. The Scientific Data Type sub-field distinguishes the different ones according to the codes defined in the following table.

Code	Meaning
01_b	AIS, Calibration or Receive Only Data.
00_b	Individual Echoes data from operative modes SS1-SS5
10_b	Acquisition Data from operative modes SS1-SS5
11_b	Tracking Data from operative modes SS1-SS5

Table 4.6-1 Science Data Type sub-field codes' definition

Note.

- Data Type 01 shall appear in TM(20,3) packets characterised by Process ID equals to 78_d, 79_d or 80_d, while Data Types 00, 01 and 11 shall appear only with Process ID equals to 77_d (cf. Table 3-1). As a consequence, Data Type 01 shall appear in TM(20,3) packets with three *different* Source Sequence Counters, while Data Types 00, 01 and 11 shall appear in packets with the *same* Source Sequence Counter
- Only Data Type 00 and 11 shall be acquired during the *same* Frame. As a consequence, TM(20,3) packets with the same values for the Frame ID and PRI # sub-fields but different Data Type shall appear only if the two different types are 00 and 11.

SCIENTIFIC DATA SOURCE SEQUENCE COUNTER sub-field

Scientific Data acquired during a single Frame can be contained in a single TM(20,3) packet TM or spread over several ones. The Source Sequence Counter specifies the order of the packets in which the Scientific Data acquired in a single Frame are subdivided; in a self standing packet, the counter shall assume the only value zero. In case of Scientific Data Types 00 and 11 acquired in the same frame, two different counters shall be considered. The counters starts form zero and they are reset for each new Frame ID value.

SCIENTIFIC DATA SEGMENTATION FLAGS sub-field

In case of data segmentation, this field implements packet grouping as defined in the following table.

Code	Meaning
01_b	First source packet of a group
00_b	Continuation source packet of a group
10_b	Last source packet of a group
11_b	A self standing source packet not belonging to a group

Table 4.6-2 Data Segmentation Flags field definition

Note that packet grouping applies to packets relevant to a single Frame. In case of Scientific Data Types 00 and 11 acquired in the same frame, two different grouping shall be considered.

4.6.1.2 Auxiliary Data field

In this field there are orbital data and parameters concerning the Scientific Processed Data reported in the TM(20.3) packet. Part of these characterises the instrument setting during raw data acquisition (for both the Acquisition and the Tracking phases). Others, used during the data processing, are useful intermediate results that describe the processing flow.

In case of data segmentation, the Auxiliary Data field shall be present only within the *first* TM(20,3) packet of the corresponding Frame (note that the Ancillary Data Header shall *always* be present within each Science Data Packet). When Scientific Data Types 00 and

11 are acquired in the same frame, two different grouping shall be considered and the auxiliary data field shall be present in the first packet of both groups.

The single sets of Auxiliary Data depend on the Process ID and the Scientific data Type field values. The five different sets are described in the following table where the numerical formats used to represent the numbers are also reported. The initials '<u>Int</u>' and '<u>Uint</u>' stand for binary 32-bit Integer and Unsigned Integer respectively, while '<u>SPfloat</u>' for binary 32-bit Single-Precision Floating-Point format, standard IEEE754/854. In this standard a number n has the following binary format:

bit number	31	30 … 23	///	22	… …. …	0
symbol	s	e_7 … e_0	1.	f_{22}	… … …	f_0

Hidden Bit Binary Point

Figure 4.6-3: IEEE 32-Bit Single-Precision Floating-Point Format.

and $n = (-1)^s*(1.f_{22-0})*2^{e-127}$, where $1 < 1.f_{22-0} < 2$ is a binary number and $0 < e < 255$ is a binary integer number.

The meaning and the default value (if any) of the parameters appearing in the following tables are described in [AD. 11] §2.9 and §3.1.8. 'SCET_FRAME' is the SCET of the Frame beginning, i.e. the left time extreme of the first PRI of the Frame; 'SCET_PAR' is the SCET corresponding to the time of calculation of the orbital parameters.

When for a particular Operative Mode, a parameter is not foreseen (e.g. OP_F2 parameters in a single frequency mode), the corresponding space shall be zero filled.

♦ SS1 Tracking and Individual Echoes

First PRI of the Frame – Uint	32 bit
SCET_FRAME – Uint	48 bit
SCET_PERICENTER – Uint	48 bit
SCET_PAR – Uint	48 bit
H(SCET_PAR) – Spfloat	32 bit
VT(SCET_PAR) – Spfloat	32 bit
VR(SCET_PAR) – Spfloat	32 bit
N_o – Uint	32 bit
ΔS_MIN – Spfloat	32 bit
NB_MIN – Uint	16 bit
M_OCOG_F1 – Spfloat	32 bit
M_OCOG_F2 – Spfloat	32 bit
Index_OCOG_F1 – Uint (1...512)	16 bit
Index_OCOG_F2 – Uint (1...512)	16 bit
TRK_Threshold_F1 – Spfloat	32 bit
TRK_Threshold_F2 – Spfloat	32 bit
ini_ind_TRK_Threshold_F1 – Uint (1...512)	16 bit
ini_ind_TRK_Threshold_F2 – Uint (1...512)	16 bit
last_ind_TRK_Threshold_F1 – Uint (1...512)	16 bit
last_ind_TRK_Threshold_F2 – Uint (1...512)	16 bit
ini_ind_FSRM_F1 – Uint (1...512)	16 bit
ini_ind_FSRM_F2 – Uint (1...512)	16 bit
last_ind_FSRM_F1 – Uint (1...512)	16 bit
last_ind_FSRM_F2 – Uint (1...512)	16 bit
Spare (0x0)	96 bit
ΔS(SCET_PAR) – Spfloat	32 bit
NB(SCET_PAR) – Uint	16 bit
NA_1(SCET_PAR) – Uint	16 bit
NA_2(SCET_PAR) – Uint	16 bit
a2_ini_cm_F1 – Spfloat [I]	32 bit
a2_ini_cm _F2 – Spfloat [I]	32 bit
a2_opt_F1 – Spfloat [I]	32 bit
a2_opt_F2 – Spfloat [I]	32 bit
Ref_CA_opt_F1 – Spfloat [I]	32 bit
Ref_CA_opt_F1 – Spfloat [I]	32 bit
δt_F1 – Uint (0 in case of FSRM failure, else 1...512) [II]	16 bit
δt_F2 – Uint (0 in case of FSRM failure, else 1...512) [II]	16 bit
Sf_F1 – Spfloat [II]	32 bit
Sf_F2 – Spfloat [II]	32 bit

[I] (0x0) if the Contrast Method is not selected.
[II] (0x0) if the FSR Method is not selected

I_c_F1 – Uint (-1 in case of threshold comparison failure, else 1...512)[II]	16 bit
I_c_F2 – Uint (-1 in case of threshold comparison failure, else 1...512)[II]	16 bit
AGC_SA_for_Next_Frame_F1 – Spfloat (db)	32 bit
AGC_SA_for_Next_Frame _F2 – Spfloat (db)	32 bit
AGC_SA_Levels_Current_Frame_F1 (HW register, binary)[III]	8 bit
AGC_SA_Levels_Current_Frame _F2 (HW register, binary)[III]	8 bit
RX_Trig_SA _for_Next_Frame_F1 – Uint (µs)	16 bit
RX_Trig_SA _for_Next_Frame_F2 – Uint (µs)	16 bit
RX_Trig_SA_Current_Frame_F1 – Uint (HW register)[IV]	16 bit
RX_Trig_SA_Current_Frame _F2 – Uint (HW register)[IV]	16 bit
ini_ind_OCOG (1...512) – Uint	16 bit
last_ind_OCOG (1...512) – Uint	16 bit
OCOG_F1 – Spfloat	32 bit
OCOG_F2 – Spfloat	32 bit
A_F1 – Spfloat	32 bit
A_F2 – Spfloat	32 bit
C_LoL_F1 – Int	16 bit
C_LoL_F2 – Int	16 bit
(0x0)	16 bit
(0x0)	16 bit
(0x0)	16 bit
Maximum RE output data exp [m = 0; OP_F1; Dipole] – Uint	8 bit
Maximum IM output data exp [m = 0; OP_F1; Dipole] – Uint	8 bit
Maximum RE output data exp [m = 0; OP_F2; Dipole] – Uint	8 bit
Maximum IM output data exp [m = 0; OP_F2; Dipole] – Uint	8 bit
Maximum RE output data exp [m = 0; OP_F1; Monopole] – Uint	8 bit
Maximum IM output data exp [m = 0; OP_F1; Monopole] – Uint	8 bit
Maximum RE output data exp [m = 0; OP_F2; Monopole] – Uint	8 bit
Maximum IM output data exp [m = 0; OP_F2; Monopole] – Uint	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
AGC_PIS_PT_Value_B1 – Spfloat (db)	32 bit
AGC_PIS_PT_Value_B2 – Spfloat (db)	32 bit

[III] XXMMMDDD; XX = don't care bits, MMM = Monopole Channel bits, DDD = Dipole Channel bits.
[IV] number of (1000/2.8)ns quanta.

AGC_PIS_Levels_B1 – (HW register, binary)[III]	8 bit
AGC_PIS_Levels_B2 – (HW register, binary)[III]	8 bit
K_PIM – Uint	8 bit
PIS Maximum output data exp [B1]	8 bit
PIS Maximum output data exp [B2]	8 bit
Processing_PRF – Spfloat	32 bit
Total	**215 bytes**
Spare	**13 bytes**

Table 4.6-4 Auxiliary Data for SS1 TRK and Individual Echoes (Process ID 77, Science Data Type 11 and 00)

♦ SS2 TRACKING AND INDIVIDUAL ECHOES

First PRI of the Frame – Uint	32 bit
SCET_FRAME – Uint	48 bit
SCET_PERICENTER – Uint	48 bit
SCET_PAR – Uint	48 bit
H(SCET_PAR) – Spfloat	32 bit
VT(SCET_PAR) – Spfloat	32 bit
VR(SCET_PAR) – Spfloat	32 bit
N_o – Uint	32 bit
ΔS_MIN – Spfloat	32 bit
NB_MIN – Uint	16 bit
M_OCOG_F1 – Spfloat	32 bit
M_OCOG_F2 – Spfloat	32 bit
Index_OCOG_F1 – Uint (1...512)	16 bit
Index_OCOG_F2 – Uint (1...512)	16 bit
TRK_Threshold_F1 – Spfloat	32 bit
TRK_Threshold_F2 – Spfloat	32 bit
ini_ind_TRK_Threshold_F1 – Uint (1...512)	16 bit
ini_ind_TRK_Threshold_F2 – Uint (1...512)	16 bit
last_ind_TRK_Threshold_F1 – Uint (1...512)	16 bit
last_ind_TRK_Threshold_F2 – Uint (1...512)	16 bit
ini_ind_FSRM_F1 – Uint (1...512)	16 bit
ini_ind_FSRM_F2 – Uint (1...512)	16 bit
last_ind_FSRM_F1 – Uint (1...512)	16 bit
last_ind_FSRM_F2 – Uint (1...512)	16 bit
Spare (0x0)	96 bit
ΔS(SCET_PAR) – Spfloat	32 bit
NB(SCET_PAR) – Uint	16 bit
NA_1(SCET_PAR) – Uint	16 bit
NA_2(SCET_PAR) – Uint	16 bit
a2_ini_cm_F1 – Spfloat [V]	32 bit
a2_ini_cm _F2 – Spfloat [V]	32 bit
a2_opt_F1 – Spfloat [V]	32 bit
a2_opt_F2 – Spfloat [V]	32 bit
Ref_CA_opt_F1 – Spfloat [V]	32 bit
Ref_CA_opt_F1 – Spfloat [V]	32 bit
δt_F1 – Uint (0 in case of FSRM failure, else 1...512) [V]	16 bit
δt_F2 – Uint (0 in case of FSRM failure, else 1...512) [V]	16 bit
Sf_F1 – Spfloat [V]	32 bit
Sf_F2 – Spfloat [V]	32 bit

[V] cf. note to the same parameter in SS1.

I_c_F1 – Uint (-1 in case of threshold comparison failure, else 1...512) [V]	16 bit
I_c_F2 – Uint (-1 in case of threshold comparison failure, else 1...512) [V]	16 bit
AGC_SA_for_Next_Frame_F1 – Spfloat (db)	32 bit
AGC_SA_for_Next_Frame _F2 – Spfloat (db)	32 bit
AGC_SA_Levels_Current_Frame_F1 (HW register, binary) [V]	8 bit
AGC_SA_Levels_Current_Frame _F2 (HW register, binary) [V]	8 bit
RX_Trig_SA _for_Next_Frame_F1 – Uint (µs)	16 bit
RX_Trig_SA _for_Next_Frame_F2 – Uint (µs)	16 bit
RX_Trig_SA_progr_F1 – Uint (HW register) [V]	16 bit
RX_Trig_SA_progr_F2 – Uint (HW register) [V]	16 bit
ini_ind_OCOG (1...512) – Uint	16 bit
last_ind_OCOG (1...512) – Uint	16 bit
OCOG_F1 – Spfloat	32 bit
OCOG_F2 – Spfloat	32 bit
A_F1 – Spfloat	32 bit
A_F2 – Spfloat	32 bit
C_LoL_F1 – Int	16 bit
C_LoL_F2 – Int	16 bit
SS2_DCEX_1 – Uint	16 bit
SS2_DCEX_2 – Uint	16 bit
SS2_DCEX_3 – Uint	16 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
AGC_PIS_PT_Value_B1 – Spfloat (db)	32 bit
AGC_PIS_PT_Value_B2 – Spfloat (db)	32 bit
AGC_PIS_Levels_B1 – (HW register, binary) [V]	8 bit
AGC_PIS_Levels_B2 – (HW register, binary) [V]	8 bit
K_PIM – Uint	8 bit
PIS Maximum output data exp [B1]	8 bit

PIS Maximum output data exp [B2]	8 bit
Processing_PRF – Spfloat	32 bit
Total	**215 bytes**
Spare	**13 bytes**

Table 4.6-5 Auxiliary Data for SS2 TRK and Individual Echoes (Process ID 77, Science Data Type 11 and 00)

♦ **SS3 Tracking and Individual Echoes**

First PRI of the Frame – Uint	32 bit
SCET_FRAME – Uint	48 bit
SCET_PERICENTER – Uint	48 bit
SCET_PAR – Uint	48 bit
H(SCET_PAR) – Spfloat	32 bit
VT(SCET_PAR) – Spfloat	32 bit
VR(SCET_PAR) – Spfloat	32 bit
N_o – Uint	32 bit
ΔS_MIN – Spfloat	32 bit
NB_MIN – Uint	16 bit
M_OCOG_F1 – Spfloat	32 bit
M_OCOG_F2 – Spfloat	32 bit
Index_OCOG_F1 – Uint (1...512)	16 bit
Index_OCOG_F2 – Uint (1...512)	16 bit
TRK_Threshold_F1 – Spfloat	32 bit
TRK_Threshold_F2 – Spfloat	32 bit
ini_ind_TRK_Threshold_F1 – Uint (1...512)	16 bit
ini_ind_TRK_Threshold_F2 – Uint (1...512)	16 bit
last_ind_TRK_Threshold_F1 – Uint (1...512)	16 bit
last_ind_TRK_Threshold_F2 – Uint (1...512)	16 bit
ini_ind_FSRM_F1 – Uint (1...512)	16 bit
ini_ind_FSRM_F2 – Uint (1...512)	16 bit
last_ind_FSRM_F1 – Uint (1...512)	16 bit
last_ind_FSRM_F2 – Uint (1...512)	16 bit
Spare (0x0)	96 bit
ΔS(SCET_PAR) – Spfloat	32 bit
NB(SCET_PAR) – Uint	16 bit
NA_1(SCET_PAR) – Uint	16 bit
NA_2(SCET_PAR) – Uint	16 bit
a2_ini_cm_F1 – Spfloat [VI]	32 bit
a2_ini_cm _F2 – Spfloat [VI]	32 bit
a2_opt_F1 – Spfloat [VI]	32 bit
a2_opt_F2 – Spfloat [VI]	32 bit
Ref_CA_opt_F1 – Spfloat [VI]	32 bit
Ref_CA_opt_F1 – Spfloat [VI]	32 bit
δt_F1 – Uint (0 in case of FSRM failure, else 1...512) [VI]	16 bit
δt_F2 – Uint (0 in case of FSRM failure, else 1...512) [VI]	16 bit
Sf_F1 – Spfloat [VI]	32 bit
Sf_F2 – Spfloat [VI]	32 bit

[VI] cf. note to the same parameter in SS1.

I_c_F1 – Uint (-1 in case of threshold comparison failure, else 1...512)[VI]	16 bit
I_c_F2 – Uint (-1 in case of threshold comparison failure, else 1...512)[VI]	16 bit
AGC_SA_for_Next_Frame_F1 – Spfloat (db)	32 bit
AGC_SA_for_Next_Frame _F2 – Spfloat (db)	32 bit
AGC_SA_Levels_Current_Frame_F1 (HW register, binary)[VI]	8 bit
AGC_SA_Levels_Current_Frame _F2 (HW register, binary)[VI]	8 bit
RX_Trig_SA _for_Next_Frame_F1 – Uint (μs)	16 bit
RX_Trig_SA _for_Next_Frame_F2 – Uint (μs)	16 bit
RX_Trig_SA_progr_F1 –Uint (HW register)[VI]	16 bit
RX_Trig_SA_progr_F2 –Uint (HW register)[VI]	16 bit
ini_ind_OCOG (1...512) – Uint	16 bit
last_ind_OCOG (1...512) – Uint	16 bit
OCOG_F1 – Spfloat	32 bit
OCOG_F2 – Spfloat	32 bit
A_F1 – Spfloat	32 bit
A_F2 – Spfloat	32 bit
C_LoL_F1 – Int	16 bit
C_LoL_F2 – Int	16 bit
(0x0)	16 bit
(0x0)	16 bit
(0x0)	16 bit
Maximum RE output data exp [m = -1; OP_F1; Dipole] – Uint	8 bit
Maximum IM output data exp [m = -1; OP_F1; Dipole] – Uint	8 bit
Maximum RE output data exp [m = 0; OP_F1; Dipole] – Uint	8 bit
Maximum IM output data exp [m = 0; OP_F1; Dipole] – Uint	8 bit
Maximum RE output data exp [m = 1; OP_F1; Dipole] – Uint	8 bit
Maximum IM output data exp [m = 1; OP_F1; Dipole] – Uint	8 bit
Maximum RE output data exp [m = -1; OP_F2; Dipole] – Uint	8 bit
Maximum IM output data exp [m = -1; OP_F2; Dipole] – Uint	8 bit
Maximum RE output data exp [m = 0; OP_F2; Dipole] – Uint	8 bit
Maximum IM output data exp [m = 0; OP_F2; Dipole] – Uint	8 bit
Maximum RE output data exp [m = 1; OP_F2; Dipole] – Uint	8 bit
Maximum IM output data exp [m = 1; OP_F2; Dipole] – Uint	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
AGC_PIS_PT_Value_B1 – Spfloat (db)	32 bit
AGC_PIS_PT_Value_B2 – Spfloat (db)	32 bit
AGC_PIS_Levels_B1 – (HW register, binary)[VI]	8 bit
AGC_PIS_Levels_B2 – (HW register, binary)[VI]	8 bit
K_PIM – Uint	8 bit

PIS Maximum output data exp [B1]	8 bit
PIS Maximum output data exp [B2]	8 bit
Processing_PRF – Spfloat	32 bit
Total	**215 bytes**
Spare	**13 bytes**

Table 4.6-6 Auxiliary Data for SS3 TRK and Individual Echoes (Process ID 77, Science Data Type 11 and 00)

- **SS4 Tracking and Individual Echoes**

First PRI of the Frame – Uint	32 bit
SCET_FRAME – Uint	48 bit
SCET_PERICENTER – Uint	48 bit
SCET_PAR – Uint	48 bit
H(SCET_PAR) – Spfloat	32 bit
VT(SCET_PAR) – Spfloat	32 bit
VR(SCET_PAR) – Spfloat	32 bit
N_0 – Uint	32 bit
ΔS_MIN – Spfloat	32 bit
NB_MIN – Uint	16 bit
M_OCOG_F1 – Spfloat	32 bit
(0x0)	32 bit
Index_OCOG_F1 – Uint (1...512)	16 bit
(0x0)	16 bit
TRK_Threshold_F1 – Spfloat	32 bit
(0x0)	32 bit
ini_ind_TRK_Threshold_F1 – Uint (1...512)	16 bit
(0x0)	16 bit
last_ind_TRK_Threshold_F1 – Uint (1...512)	16 bit
(0x0)	16 bit
ini_ind_FSRM_F1 – Uint (1...512)	16 bit
(0x0)	16 bit
last_ind_FSRM_F1 – Uint (1...512)	16 bit
(0x0)	16 bit
Spare (0x0)	96 bit
ΔS(SCET_PAR) – Spfloat	32 bit
NB(SCET_PAR) – Uint	16 bit
NA_1(SCET_PAR) – Uint	16 bit
NA DSP2 = NA_1	16 bit
a2_ini_cm_F1 – Spfloat [VII]	32 bit
(0x0)	32 bit
a2_opt_F1 – Spfloat [VIII]	32 bit
(0x0)	32 bit
Ref_CA_opt_F1 – Spfloat [VIII]	32 bit
(0x0)	32 bit
δt_F1 – Uint (0 in case of FSRM failure, else 1...512) [VIII]	16 bit
(0x0)	16 bit
Sf_F1 – Spfloat [VIII]	32 bit
(0x0)	32 bit

[VII] cf. note to the same parameter in SS1.

I_c_F1 – Uint (-1 in case of threshold comparison failure, else 1...512)[VIII]	16 bit
(0x0)	16 bit
AGC_SA_for_Next_Frame_F1 – Spfloat (db)	32 bit
(0x0)	32 bit
AGC_SA_Levels_Current_Frame_F1 (HW register, binary)[VIII]	8 bit
(0x0)	8 bit
RX_Trig_SA _for_Next_Frame_F1 – Uint (µs)	16 bit
(0x0)	16 bit
RX_Trig_SA_progr_F1 – Uint (HW register) [VIII]	16 bit
(0x0)	16 bit
ini_ind_OCOG (1...512) – Uint	16 bit
last_ind_OCOG (1...512) – Uint	16 bit
OCOG_F1 – Spfloat	32 bit
(0x0)	32 bit
A_F1 – Spfloat	32 bit
(0x0)	32 bit
C_LoL_F1 – Int	16 bit
(0x0)	16 bit
(0x0)	16 bit
(0x0)	16 bit
(0x0)	16 bit
Maximum RE output data exp [m = -2; OP_F1; Dipole] – Uint	8 bit
Maximum IM output data exp [m = -2; OP_F1; Dipole] – Uint	8 bit
Maximum RE output data exp [m = -1; OP_F1; Dipole] – Uint	8 bit
Maximum IM output data exp [m = -1; OP_F1; Dipole] – Uint	8 bit
Maximum RE output data exp [m = 0; OP_F1; Dipole] – Uint	8 bit
Maximum IM output data exp [m = 0; OP_F1; Dipole] – Uint	8 bit
Maximum RE output data exp [m = 1; OP_F1; Dipole] – Uint	8 bit
Maximum IM output data exp [m = 1; OP_F1; Dipole] – Uint	8 bit
Maximum RE output data exp [m = 2; OP_F1; Dipole] – Uint	8 bit
Maximum IM output data exp [m = 2; OP_F1; Dipole] – Uint	8 bit
Maximum RE output data exp [m = -2; OP_F1; Monopole] – Uint	8 bit
Maximum IM output data exp [m = -2; OP_F1; Monopole] – Uint	8 bit
Maximum RE output data exp [m = -1; OP_F1; Monopole] – Uint	8 bit
Maximum IM output data exp [m = -1; OP_F1; Monopole] – Uint	8 bit
Maximum RE output data exp [m = 0; OP_F1; Monopole] – Uint	8 bit
Maximum IM output data exp [m = 0; OP_F1; Monopole] – Uint	8 bit
Maximum RE output data exp [m = 1; OP_F1; Monopole] – Uint	8 bit
Maximum IM output data exp [m = 1; OP_F1; Monopole] – Uint	8 bit
Maximum RE output data exp [m = 2; OP_F1; Monopole] – Uint	8 bit
Maximum IM output data exp [m = 2; OP_F1; Monopole] – Uint	8 bit
AGC_PIS_PT_Value_B1 – Spfloat (db)	32 bit
AGC_PIS_PT_Value_B2 – Spfloat (db)	32 bit
AGC_PIS_Levels_B1 – (HW register, binary)[VIII]	8 bit

AGC_PIS_Levels_B2 – (HW register, binary)[VIII]	8 bit
K_PIM – Uint	8 bit
PIS Maximum output data exp [B1]	8 bit
PIS Maximum output data exp [B2]	8 bit
Processing_PRF – Spfloat	32 bit
Total	**215 bytes**
Spare	**13 bytes**

Table 4.6-7 Auxiliary Data for SS4 TRK and Individual Echoes
(Process ID 77, Science Data Type 11 and 00)

♦ SS5 Tracking and Individual Echoes

First PRI of the Frame – Uint	32 bit
SCET_FRAME – Uint	48 bit
SCET_PERICENTER – Uint	48 bit
SCET_PAR – Uint	48 bit
H(SCET_PAR) – Spfloat	32 bit
VT(SCET_PAR) – Spfloat	32 bit
VR(SCET_PAR) – Spfloat	32 bit
N_o – Uint	32 bit
ΔS_MIN – Spfloat	32 bit
NB_MIN – Uint	16 bit
M_OCOG_F1 – Spfloat	32 bit
(0x0)	32 bit
Index_OCOG_F1 – Uint (1...512)	16 bit
(0x0)	16 bit
TRK_Threshold_F1 – Spfloat	32 bit
(0x0)	32 bit
ini_ind_TRK_Threshold_F1 – Uint (1...512)	16 bit
(0x0)	16 bit
last_ind_TRK_Threshold_F1 – Uint (1...512)	16 bit
(0x0)	16 bit
ini_ind_FSRM_F1 – Uint (1...512)	16 bit
(0x0)	16 bit
last_ind_FSRM_F1 – Uint (1...512)	16 bit
(0x0)	16 bit
Spare (0x0)	96 bit
ΔS(SCET_PAR) – Spfloat	32 bit
NB(SCET_PAR) – Uint	16 bit
NA_1(SCET_PAR) – Uint	16 bit
NA DSP2 = NA_1	16 bit
a2_ini_cm_F1 – Spfloat [VIII]	32 bit
(0x0)	32 bit
a2_opt_F1 – Spfloat [VIII]	32 bit
(0x0)	32 bit
Ref_CA_opt_F1 – Spfloat	32 bit
(0x0)	32 bit
δt_F1 – Uint (0 in case of FSRM failure, else 1...512) [VIII]	16 bit
(0x0)	16 bit
Sf_F1 – Spfloat [VIII]	32 bit
(0x0)	32 bit
I_c_F1 – Uint (-1 in case of threshold comparison failure, else 1...512) [VIII]	16 bit

[VIII] cf. note to the same parameter in SS1.

(0x0)	16 bit
AGC_SA_for_Next_Frame_F1 – Spfloat (db)	32 bit
(0x0)	32 bit
AGC_SA_Levels_Current_Frame_F1 (HW register, binary)[VIII]	8 bit
(0x0)	8 bit
RX_Trig_SA _for_Next_Frame_F1 – Uint (µs)	16 bit
(0x0)	16 bit
RX_Trig_SA_progr_F1 – Uint (HW register)[VIII]	16 bit
(0x0)	16 bit
ini_ind_OCOG (1...512) – Uint	16 bit
last_ind_OCOG (1...512) – Uint	16 bit
OCOG_F1 – Spfloat	32 bit
(0x0)	32 bit
A_F1 –Spfloat	32 bit
(0x0)	32 bit
C_LoL_F1 – Int	16 bit
(0x0)	16 bit
(0x0)	16 bit
(0x0)	16 bit
(0x0)	16 bit
Maximum RE output data exp [m = -1; OP_F1; Dipole] – Uint	8 bit
Maximum IM output data exp [m = -1; OP_F1; Dipole] – Uint	8 bit
Maximum RE output data exp [m = 0; OP_F1; Dipole] – Uint	8 bit
Maximum IM output data exp [m = 0; OP_F1; Dipole] – Uint	8 bit
Maximum RE output data exp [m = 1; OP_F1; Dipole] – Uint	8 bit
Maximum IM output data exp [m = 1; OP_F1; Dipole] – Uint	8 bit
Maximum RE output data exp [m = -1; OP_F1; Monopole] – Uint	8 bit
Maximum IM output data exp [m = -1; OP_F1; Monopole] – Uint	8 bit
Maximum RE output data exp [m = 0; OP_F1; Monopole] – Uint	8 bit
Maximum IM output data exp [m = 0; OP_F1; Monopole] – Uint	8 bit
Maximum RE output data exp [m = 1; OP_F1; Monopole] – Uint	8 bit
Maximum IM output data exp [m = 1; OP_F1; Monopole] – Uint	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
(0x0)	8 bit
AGC_PIS_PT_Value_B1 – Spfloat (db)	32 bit
AGC_PIS_PT_Value_B2 – Spfloat (db)	32 bit
AGC_PIS_Levels_B1 – (HW register, binary)[VIII]	8 bit
AGC_PIS_Levels_B2 – (HW register, binary)[VIII]	8 bit
K_PIM – Uint	8 bit

PIS Maximum output data exp [B1]	8 bit
PIS Maximum output data exp [B2]	8 bit
Processing_PRF – Spfloat	32 bit
Total	**215 bytes**
Spare	**13 bytes**

Table 4.6-8 Auxiliary Data for SS5 TRK and Individual Echoes (Process ID 77, Science Data Type 11 and 00)

♦ Auxiliary Data for Active Ionospheric Sounding

First PRI of the Frame – Uint	32 bit
SCET_FRAME – Uint	48 bit
SCET_PERICENTER – Uint	48 bit
SCET_PAR – Uint	48 bit
H(SCET_PAR) – Spfloat	32 bit
VT(SCET_PAR) – Spfloat	32 bit
VR(SCET_PAR) – Spfloat	32 bit
N_o – Uint	32 bit
ΔS_MIN – Spfloat	32 bit
NB_MIN – Uint	16 bit
ah0 – Spfloat	32 bit
ah2 – Spfloat	32 bit
ah4 – Spfloat	32 bit
ah6 – Spfloat	32 bit
ar1 – Spfloat	32 bit
ar3 – Spfloat	32 bit
ar5 – Spfloat	32 bit
ar7 – Spfloat	32 bit
at0 – Spfloat	32 bit
at2 – Spfloat	32 bit
at4 – Spfloat	32 bit
at6 – Spfloat	32 bit
ΔS(SCET_PAR) – Spfloat	32 bit
NB (160 dec) – Uint	16 bit
AGC_AIS (last PRI of current frame) – Spfloat (db)	32 bit
AGC_AIS_Level (last PRI of current frame) – (HW register, binary)[IX]	8 bit
RX_Trig_AIS – Uint (μs)	16 bit
RX_Trig_AIS_progr – Uint (HW register)[X]	16 bit
AIS Maximum output data exp – Uint	8 bit
ah1 – Spfloat	32 bit
ah3 – Spfloat	32 bit
ah5 – Spfloat	32 bit
ah7 – Spfloat	32 bit
ar0 – Spfloat	32 bit
ar2 – Spfloat	32 bit
ar4 – Spfloat	32 bit
ar6 – Spfloat	32 bit
at1 – Spfloat	32 bit

[IX] XXMMMDDD; XX = don't care bits, MMM = Monopole Channel bits, DDD = Dipole Channel bits
[X] number of (1000/2.8)ns quanta

at3 – Spfloat	32 bit
at5 – Spfloat	32 bit
at7 – Spfloat	32 bit
Total	**156 bytes**
Spare	**72 bytes**

Table 4.6-9: Auxiliary Data for Active Ionospheric Sounding (Process ID 78, Science Data Type 01)

♦ Auxiliary Data for Calibration

First PRI of the Frame – Uint	32 bit
SCET_FRAME – Uint	48 bit
SCET_PERICENTER – Uint	48 bit
SCET_PAR – Uint	48 bit
H(SCET_PAR) – Spfloat	32 bit
VT(SCET_PAR) – Spfloat	32 bit
VR(SCET_PAR) – Spfloat	32 bit
N_o – Uint	32 bit
ΔS_MIN – Spfloat	32 bit
NB_MIN – Uint	16 bit
ah0 – Spfloat	32 bit
ah2 – Spfloat	32 bit
ah4 – Spfloat	32 bit
ah6 – Spfloat	32 bit
ar1 – Spfloat	32 bit
ar3 – Spfloat	32 bit
ar5 – Spfloat	32 bit
ar7 – Spfloat	32 bit
at0 – Spfloat	32 bit
at2 – Spfloat	32 bit
at4 – Spfloat	32 bit
at6 – Spfloat	32 bit
ΔS(SCET_PAR) – Spfloat	32 bit
NB (160 dec) – Uint	16 bit
AGC_CAL_PT_Value – Spfloat (db)	32 bit
AGC_CAL_Level – (HW register, binary)[XI]	8 bit
RX_Trig_CAL_comp – Uint (µs)	16 bit
RX_Trig_CAL_progr – Uint (HW register)[XII]	16 bit
SPARE (0x0)	8 bit
ah1 – Spfloat	32 bit
ah3 – Spfloat	32 bit
ah5 – Spfloat	32 bit
ah7 – Spfloat	32 bit
ar0 – Spfloat	32 bit
ar2 – Spfloat	32 bit
ar4 – Spfloat	32 bit
ar6 – Spfloat	32 bit
at1 – Spfloat	32 bit
at3 – Spfloat	32 bit

[XI] XXMMMDDD; XX = don't care bits, MMM = Monopole Channel bits, DDD = Dipole Channel bits
[XII] number of (1000/2.8)ns quanta

at5 – Spfloat	32 bit
at7 – Spfloat	32 bit
Total	**155 bytes**
Spare	**73 bytes**

Table 4.6-10: Auxiliary Data for Calibration (Process ID 79, Science data Type 01)

♦ Auxiliary Data for Receive Only

First PRI of the Frame – Uint	32 bit
SCET_FRAME – Uint	48 bit
SCET_PERICENTER – Uint	48 bit
SCET_PAR – Uint	48 bit
H(SCET_PAR) – Spfloat	32 bit
VT(SCET_PAR) – Spfloat	32 bit
VR(SCET_PAR) – Spfloat	32 bit
N_0 – Uint	32 bit
NB_MIN – Uint	16 bit
NB_MIN – Uint	32 bit
ah0 – Spfloat	32 bit
ah2 – Spfloat	32 bit
ah4 – Spfloat	32 bit
ah6 – Spfloat	32 bit
ar1 – Spfloat	32 bit
ar3 – Spfloat	32 bit
ar5 – Spfloat	32 bit
ar7 – Spfloat	32 bit
at0 – Spfloat	32 bit
at2 – Spfloat	32 bit
at4 – Spfloat	32 bit
at6 – Spfloat	32 bit
ΔS(SCET_PAR) – Spfloat	32 bit
NB(160 dec) – Uint	16 bit
AGC_RO_PT_Value – Spfloat (db)	32 bit
AGC_RO_Level – (HW register, binary) [XIII]	8 bit
RX_Trig_RO_comp – Uint (µs)	16 bit
RX_Trig_RO_progr – Uint (HW register) [XIV]	16 bit
SPARE (0x0)	8 bit
ah1 – Spfloat	32 bit
ah3 – Spfloat	32 bit
ah5 – Spfloat	32 bit
ah7 – Spfloat	32 bit
ar0 – Spfloat	32 bit
ar2 – Spfloat	32 bit
ar4 – Spfloat	32 bit
ar6 – Spfloat	32 bit
at1 – Spfloat	32 bit
at3 – Spfloat	32 bit

[XIII] XXMMMDDD; XX = don't care bits, MMM = Monopole Channel bits, DDD = Dipole Channel bits
[XIV] number of (1000/2.8)ns quanta

at5 – Spfloat	32 bit
at7 – Spfloat	32 bit
Total	**155 bytes**
Spare	**73 bytes**

Table 4.6-11: Auxiliary Data for Receive Only (Process ID 80, Science data Type 01)

♦ **Auxiliary Data for Acquisition Phase**

First PRI of the Frame – Uint	32 bit
SCET_FRAME – Uint	48 bit
SCET_PERICENTER – Uint	48 bit
SCET_PAR – Uint	48 bit
H(SCET_PAR) – Spfloat	32 bit
VT(SCET_PAR) – Spfloat	32 bit
VR(SCET_PAR) – Spfloat	32 bit
N_o – Uint	32 bit
∆S_MIN – Spfloat	32 bit
NB_MIN – Uint	16 bit
ah0 – Spfloat	32 bit
ah2 – Spfloat	32 bit
ah4 – Spfloat	32 bit
ah6 – Spfloat	32 bit
ar1 – Spfloat	32 bit
ar3 – Spfloat	32 bit
ar5 – Spfloat	32 bit
ar7 – Spfloat	32 bit
at0 – Spfloat	32 bit
at2 – Spfloat	32 bit
at4 – Spfloat	32 bit
at6 – Spfloat	32 bit
∆S(SCET_PAR) – Spfloat	32 bit
NB – Uint	16 bit
AGC_PIS_ PT_Value_B1 – Spfloat (db)	32 bit
AGC_PIS_ PT_Value_B2 – Spfloat (db)	32 bit
AGC_PIS_Levels_ B1 – (HW register, binary)	8 bit[1]
AGC_PIS_Levels_B2 – (HW register, binary)	8 bit[1]
K_PIM – Uint	8 bit
PIS Maximum output data exp [B1]	8 bit
PIS Maximum output data exp [B2]	8 bit
AGC_NPM_PT_Value – Spfloat	32 bit
AGC_NPM_Levels – (HW register, binary)	8 bit[1]
NPM_Int_F1 – Spfloat	32 bit
NPM_Int_F2 – Spfloat[XV]	32 bit
X_F1|X_F2 (allowed values: 1, 2, 3, 4 for both X_F1 and X_F2) - binary[XVI]	8 bit
AGC_COLL_X_F1 – Spfloat	32 bit
AGC_COLL_X_F2 – Spfloat[XV]	32 bit
AGC_COLL_X_Levels_F1 – (HW register, binary)[XVII]	8 bit

[XV] (0x0) in case of single frequency mode (i.e. SS4, SS5)
[XVI] MMMMNNNN; M-bits represent X_F1, N-bits represet X_F2

AGC_COLL_X_Levels_F2 – (HW register, binary)[XV, XVII]	8 bit
RX_Trig_ACQ_comp – Uint (µs)	16 bit
RX_Trig_ACQ_progr – Uint (HW register)[XVIII]	16 bit
AGC_SA_for_TRK_Frame_F1 (0 in case of LED failure) – Spfloat	32 bit
AGC_SA_for_TRK_Frame_F2 (0 in case of LED failure) – Spfloat[XV]	32 bit
RX_Trig_SA_for_TRK_Frame_F1 (0 in case of LED failure) – Uint (µs)	16 bit
RX_Trig_SA_ for_TRK_Frame_F2 (0 in case of LED failure) – Uint (µs)[XV]	16 bit
Det_Thresh_F1 – Spfloat	32 bit
Det_Thresh_F2 – Spfloat [XV]	32 bit
K_Det_Thres_F1 – Spfloat	32 bit
K_Det_Thres_F2 – Spfloat [XV]	32 bit
K_Det_Thres_min_F1 – Spfloat	32 bit
K_Det_Thres_ min_F2 – Spfloat [XV]	32 bit
F_ACQ_F1 Re – Spfloat	32 bit
F_ACQ_F1 Im – Spfloat	32 bit
F_ACQ_F2 Re – Spfloat [XV]	32 bit
F_ACQ_F2 Im – Spfloat [XV]	32 bit
N_D (0 in case of LED failure) – Uint	16 bit
K_AGC (0 in case of LED failure) - Spfloat	32 bit
Aref (0 in case of LED failure) - Spfloat	32 bit
Ref_Fun_Flag_F1 (0 = default, 1 = corrected) - Uint	8 bit
Ref_Fun_Flag_F2 (0 = default, 1 = corrected) – Uint [XV]	8 bit
i_le_F1 (-1 in case of LED failure, esle 1...1024) – int	16 bit
i_le_F2 (-1 in case of LED failure, else 1...1024) – int [XV]	16 bit
T_le_F1 (-Tc in case of LED failure) – Spfloat	32 bit
T_le_F2 (-Tc in case of LED failure) – Spfloat [XV]	32 bit
Maximum RE output data exponent [OP_F1] – Uint	8 bit
Maximum IM output data exponent [OP_F1] – Uint	8 bit
Maximum RE output data exponent [OP_F2] – Uint [XV]	8 bit
Maximum IM output data exponent [OP_F2] – Uint [XV]	8 bit
NS_LED - Uint	16 bit
Processing_PRF – Spfloat	32 bit
Total	225 bytes
Spare	3 bytes

Table 4.6-12 Auxiliary Data for Acquisition Phase
(Process ID 77, Science Data Type 10)

[XVII] XXMMMDDD; XX = don't care bits, MMM = Monopole Channel bits, DDD = Dipole Channel bits
[XVIII] number of (1000/2.8)ns quanta

4.6.2 Scientific Data field

The structure of the Scientific Data field, related to the particular Operative Mode relevant to the data, is described in the following table. The operative modes and sub-modes are reported with the corresponding Mode Selection code, Process ID and Scientific Data Type. In the table bit/sa stands for bit per sample; refer to notes to further information.

SCIENTIFIC DATA IDs				DATA RATE[3]		ORDER WITHIN PACKET(S)[1]												
Operative Mode	Mode Sel[4].	Proc. ID & Data Type[5]		byte per Frame	TM-Pack. number[1]	Dipole-F1 (byte)[2]			Dipole-F2 (byte)[2]			Monopole-F1 (byte)[2]			Monopole-F2 (byte)[2]			PIS F1 & F2 (byte)
Calibration	0101_b	79_d	01_b	313600	78	156800 (8 bit/sa C2)			0			156800 (8 bit/sa C2)			0			0
Rec. Only	0110_b	80_d	01_b	313600	78	156800 (8 bit/sa C2)			0			156800 (8 bit/sa C2)			0			0
AIS	0111_b	78_d	01_b	25600	7	25600 (16-bit/sa RE)						0						0
SS1-ACQ	1000_b	77_d	10_b	4608	2	1024 (8 bit/sa RE)	1024 (8 bit/sa IM)	X 1	1024 (8 bit/sa RE)	1024 (8 bit/sa IM)	X 1	0			0			512 (16 bit/sa RE)
SS1-TRK	1000_b	77_d	11_b	4608	2	512 (8 bit/sa RE)	512 (8 bit/sa IM)	X 1	512 (8 bit/sa RE)	512 (8 bit/sa IM)	X 1	512 (8 bit/sa RE)	512 (8 bit/sa IM)	X 1	512 (8 bit/sa RE)	512 (8 bit/sa IM)	X 1	512 (16 bit/sa RE)
SS1-In.Ec.	1000_b	77_d	00_b	501760 (max)	variable	980*128 (max) (8 bit/sa C2)			980*128 (max) (8 bit/sa C2)			980*128 (max) (8 bit/sa C2)			980*128 (max) (8 bit/sa C2)			0
SS2-ACQ	1001_b	77_d	10_b	4608	2	1024 (8 bit/sa RE)	1024 (8 bit/sa IM)	X 1	1024 (8 bit/sa RE)	1024 (8 bit/sa IM)	X 1	0			0			512 (16 bit/sa RE)
SS2-TRK	1001_b	77_d	11_b	2560	1	1024 (32 bit/sa RE)			1024 (32 bit/sa RE)			0			0			512 (16 bit/sa RE)
SS2-In.Ec.	1001_b	77_d	00_b	501760 (max)	variable	980*256 (max) (8 bit/sa C2)			980*256 (max) (8 bit/sa C2)			0			0			0
SS3-ACQ	1010_b	77_d	10_b	4608	2	1024 (8 bit/sa RE)	1024 (8 bit/sa IM)	X 1	1024 (8 bit/sa RE)	1024 (8 bit/sa IM)	X 1	0			0			512 (16 bit/sa RE)

SS3-TRK	1010_b	77_d	11_b	6656	2	512 (8 bit/sa RE)	512 (8 bit/sa IM)	X 3	512 (8 bit/sa RE)	512 (8 bit/sa IM)	X 3	0			0	512 (16 bit/sa RE)
SS3-In.Ec.	1010_b	77_d	00_b	501760 (max)	variable	980*256 (max) (8 bit/sa C2)			980*256 (max) (8 bit/sa C2)			0			0	0
SCIENTIFIC DATA IDs				DATA RATE [3]		ORDER WITHIN PACKET(S) [1.]										
Operative Mode	Mode Sel[4].	Proc. ID & Data Type[5]		byte per Frame	TM-Pack. number[1.]	Dipole-F1 (byte)[2]			Dipole-F2 (byte)[2]			Monopole-F1 (byte)[2]			Monopole-F2 (byte)[2]	PIS (byte)
SS4-ACQ	1011_b	77_d	10_b	2560	1	1024 (8 bit/sa RE)	1024 (8 bit/sa IM)	X 1	0			0			0	512 (16 bit/sa RE)
SS4-TRK	1011_b	77_d	11_b	10752	3	512 (8 bit/sa RE)	512 (8 bit/sa IM)	X 5	0			512 (8 bit/sa RE)	512 (8 bit/sa IM)	X 5	0	512 (16 bit/sa RE)
SS4-In.Ec.	1011_b	77_d	00_b	501760 (max)	variable	980*256 (max) (8 bit/sa C2)			0			980*256 (max) (8 bit/sa C2)			0	0
SS5-ACQ	1100_b	77_d	10_b	2560	1	1024 (8 bit/sa RE)	1024 (8 bit/sa IM)	X 1	0			0			0	512 (16 bit/sa RE)
SS5-TRK	1100_b	77_d	11_b	6656	2	512 (8 bit/sa RE)	512 (8 bit/sa IM)	X 3	0			512 (8 bit/sa RE)	512 (8 bit/sa IM)	X 3	0	512 (16 bit/sa RE)
SS5-In.Ec.	1100_b	77_d	00_b	501760 (max)	variable	980*64*4 (max) (8 bit/sa C2)			0			980*64*4 (max) (8 bit/sa C2)			0	0

Table 4.6-8: TM(20,3) Scientific Data field fine structure.

<u>Notes</u>.

1. When the amount of data produced in a single Frame has to be split in more than one packet, the data stream is interrupted abruptly anywhere it is necessary and remaining data are reported in the following. All the packets but last are completely are 4112 byte long. The figure below clarifies this procedure in the case SS1-TRK.

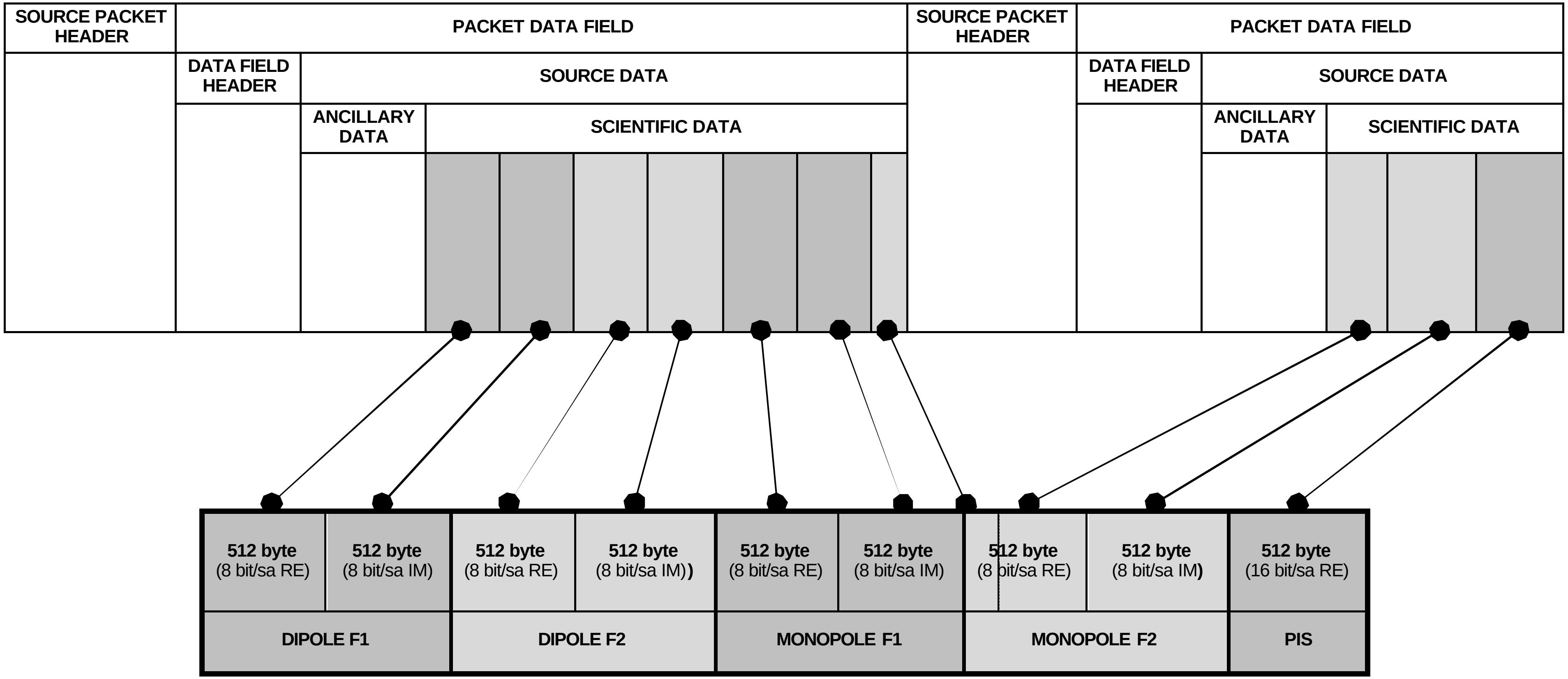


Figure 4.6-5: Scientific Data Stream Split in two or more TM(20,3) packets.

2. the string "X n" (where n = 1,3,5) in the boxes below refers to the number of doppler filters foreseen in the Operative Mode (cf. [AD.11] § 3.1.8.2.3). With three doppler filters (indexes m = -1,0,1), the data order in the packet(s) shall be:

- m = -1: 512 byte real part, 512 byte imaginary part;

- m = 0: 512 byte real part, 512 byte imaginary part;
- m = 1: 512 byte real part, 512 byte imaginary part.

Likewise, with five doppler filters (indexes m = -2,-1,0,1,2), the data order in the packet(s) shall be:

- m = -2: 512 byte real part, 512 byte imaginary part;
- m = -1: 512 byte real part, 512 byte imaginary part;
- m = 0: 512 byte real part, 512 byte imaginary part;
- m = 1: 512 byte real part, 512 byte imaginary part;
- m = 2: 512 byte real part, 512 byte imaginary part.

3. The data rate refers to the bare scientific data only, the packets' headers have to be added to obtain the real TM(20,3) data rate.
4. Cf. Table 3.3-1
5. Cf. Table 3-1 and Table 4.6-1.

4.7 SERVICE 206-207: PRIVATE SERVICES

Services included in the range from 206 to 210 are specifically dedicated to MARSIS DES. In particular the DES shall use the following TM and TC, belonging to services 206 and 207 listed here below:

- Telecommand (206,1) Operation Sequence Table Loading (SIS_OST_TC).
- Telecommand (206,2) Parameter Table Loading (SIS_PT_TC).
- Telemetry (206,3) Private TM (Spare) (SIS_PRIVATE_TM).
- Telecommand (207,1) Automatic Mode Transition Disable (SIS_MOD_TR_DIS_TC).

Telecommand (206,1): Operation Sequence Table Loading (SIS_OST_TC)

TC(206,1) shall be used to load the OST into the RAM memory; it shall be accepted by MARSIS only in STANDBY Support Mode The structure of the OST and the meaning of the fields' codes in its lines are described in the Annex 1.
The Application Data field shall be the same of TC(6,2) with the exception of the Start Address, that shall be a relative address, that is an offset address with respect to the start address reserved in RAM memory for the OST (base address).

	PACKET HEADER									*PACKET DATA FIELD (Variable)*		
Field	PACKET ID					PACKET SEQUENCE CONTROL			PACKET LENGTH	DATA FIELD HEADER	APPLIC. DATA	PACKET ERROR CONTROL
Subfield	Version Number	Type	Data Field Header Flag	Application Process ID		Sequen ceFlags	Source Sequence Count		(octets in Packet Data Field –1)			
				Proc. ID	Pack. Cat.		Source Part	Sequence Part				
Content	000_b	1	1	76_d	12_d	11_b	…. b	$(0 , 2^{11}-1)_d$	$((26 , 242)-1)_d$			
Wide (bit)	3 b	1 b	1 b	7 b	4 b	2 b	3 b	11b	16 b	32 b		16 b
Wide (oct.)	2 B					2 B			2 B	4 B	(20÷236) B	2 B

Figure 4.7-1 TC(206,1): Operations Sequence Table Loading Packet

	PACKET DATA FIELD (Variable)											
Field	**DATA FIELD HEADER**						**APPLICATION DATA**					**PACK. ERR CTRL**
Subfield	**PUS version**	**Chck. Type**	**Ack**	**Pack. Type**	**Pack. Sub-Type**	**Pad**	Memory ID	**N**	Block (Repeated N Times) Start Address	Length of the Block	**Data**	
Content	**…. b**	**1**	**0001_b**	**206_d**	**1_d**	**0_b**	**177_d**	**$(1 ¸ 13)_d$**				
Wide (bit)	**3 b**	**1 b**	**4 b**	**8 b**	**8 b**	**8 b**	**8 b**	**8 b**	**32 b**	**16 b**		**16 b**
Wide (oct.)	**4 B**						**1 B**	**1B**	**4 B**	**2 B**	12 B ÷V.ble in1 2 B	**2 B**

Figure 4.7-2: TC(206,1): Operations Sequence Table Loading Packet Data Field

Due to the relative address policy, since two RAM rows are necessary to store one OST line, to load k≤19 <u>consecutive</u> 96-bit OST lines, starting from the line n = 0,1,2,…,511 <u>included</u> (because the OST is composed of 512 lines maximum, <u>it has to be 2n+2k < 1024</u> - see also Table 4.1-3),the following conventions have to be used:

- start address = 2n,
- length of the block = 2k,
- data structure (two RAM rows for each one OST line):

RAM bit #	**47 ¸ 32**	31÷16	**15 ¸ 0**
	OST bit # 0 ¸ 15	**OST bit # 16 ¸ 31**	**OST bit # 32 ¸ 47**
	OST bit # 48 ¸ 63	**OST bit # 64 ¸ 79**	**OST bit # 80 ¸ 95**

Figure 4.7-3: OST line structure in RAM memory

Telecommand (206,2): Parameter Table Loading (SIS_PT_TC)

TC(206,2) shall be used to load PT values into the RAM memory; it shall be accepted by MARSIS only in STANDBY Support Mode. The structure of the PT is described in the Annex 1.

The Application Data field shall be the same of TC(6,2) with the exception of the Start Address, that shall be a <u>relative address</u>, that is an offset address with respect to the start address reserved in RAM memory for the PT (base address).

	PACKET HEADER									PACKET DATA FIEL (variable)		
Field	PACKET ID					PACKET SEQUENCE CONTROL			PACKET LENGTH	DATA FIELD HEADER	APPLIC. DATA	PACKET ERROR CONTROL
Subfield	Version Number	Type	Data Field Header Flag	Application Process ID		SequenceFlags	Source Sequence Count		(octets in Packet Data Field –1)			
				Proc. ID	Pack. Cat.		Source Part	Sequence Part				
Content	000_b	1	1	76_d , 78_d	12_d	11_b	…. b	$(0 , 2^{11}-1)_d$	$((16 , 242)-1)_d$			
Wide (bit)	3 b	1 b	1 b	7 b	4 b	2 b	3 b	11b	16 b	32 b		16 b
Wide (oct.)	2 B					2 B			2 B	4 B	236 B	2 B

Figure 4.7-4 TC(206,2): Parameters Table Loading Packet

	PACKET DATA FIELD (Variable)											
Field	DATA FIELD HEADER						APPLICATION DATA					PACK. ERR CTRL
Subfield	PUS version	Chck. Type	Ack	Pack. Type	Pack. Sub-type	Pad	Memory ID	N	Block (Repeated N Times)			
									Start Address	Length of the Block	Data (parameters)	
Content	…. b	1	000-b	206_d	2_d	0_b	177_d 180_d 184_d	$(1 , 19)_d$				
Wide (bit)	3 b	1 b	4 b	8 b	8 b	8 b	8 b	8 b	32 b	16 b		16 b
Wide (oct.)	4 B						1 B	1B	4 B	2 B	6 B + V.ble in 6 B	2 B

Figure 4.7-5 TC(206,2): Parameters Table Loading Packet Data Field

One RAM row is necessary to store each single PT parameter. Refer to Annex 1 for the detailed bit structure and start address of each parameter.

Due to the relative address policy, since each single PT parameter is stored in one RAM row, to load k = 38 consecutive 48-bit parameters, starting from the address number n included, the following conventions have to be used:

- start address = n,
- length of the block = k,
- due to PT dimensions, it has to be (see Annex 1 and cf. Table 4.1-3):
  - n + k < 364 if Mem ID = 177,
  - n + k < 4656 if Mem ID = 180 and 184.

Telemetry (206,3): (SIS_PRIVATE _TM): SPARE

	SOURCE PACKET HEADER (48 bit)								PACKET DATA FIELD (Variable)	
Field	PACKET ID					PACKET SEQUENCE CONTROL		PACKET LENGTH	DATA FIELD HEADER	SOURCE DATA
Subfield	Version Number	Type	Data Field Header Flag	Application Process ID		Segment. Flags	Source Sequence Count	(octets in Packet Data Field –1)		
				Proc. ID	Pack. Cat.					
Content	000_b	0	1	76_d	12_d	11_b	$(0, 2^{14}-1)_d$	Max $(4106\text{-}1)_d$		
Wide (bit)	3 b	1 b	1 b	7 b	4 b	2 b	14 b	16 b	80 b	
Wide (oct.)	2 B					2 B		2 B	10 B	Variable (Max 4096 B)

Figure 4.7-8 TM(206,3): SPARE Private TM Packet

	PACKET DATA FIELD (Variable)							
Field	DATA FIELD HEADER							SOURCE DATA
Subfield	SCET Time	PUS	Chck. Flag	Spare	Pack. Type	Pack. Sub-type	Pad	
Content	-----	0_b	0	0000_b	20_d	3_d	0_b	TBD
Wide (bit)	48 b	3 b	1 b	4 b	8 b	8 b	8 b	
Wide (oct.)	10 B							Variable (Max 4096 B)

Figure 4.7-9 TM(206,3): SPARE Private TM Packet Data Field

Telecommand (207,1): Nominal Mode Transition Disable (SIS_MOD_TR_DIS_TC)

This TC shall be used to change the nominal duration of STANDBY Support Mode, i.e. to disable the nominal Mode Transition from STANDBY to WARM-UP1 Support Mode. The DES shall accept this TC only in STANDBY Support Mode.

By default STANDBY Mode duration is fixed to 240 seconds, within the Application Data field of this TC shall be indicated, expressed in 32-bit Unsigned Integer, the new STANDBY Mode duration in seconds from C/I-STANDBY transition time. The Mode Transition shall occur automatically at the end of STANDBY Mode, according to the new Mode duration.

	PACKET HEADER									PACKET DATA FIELD (Variable)		
Field	PACKET ID					PACKET SEQUENCE CONTROL			PACKET LENGTH	DATA FIELD HEADER	APPLIC. DATA	PACKET ERROR CONTROL
Subfield	Version Number	Type	Data Field Header Flag	Application Process ID		SequenceFlags	Source Sequence Count		(octets in Packet Data Field –1)			
				Proc. ID	Pack. Cat.		Source Part	Sequence Part				
Content	000_b	1	1	76_d	12_d	11_b	.... b	$(0, 2^{11}-1)_d$	$(10-1)_d$			
Wide (bit)	3 b	1 b	1 b	7 b	4 b	2 b	3 b	11b	16 b	32 b	32 b	16 b
Wide (oct.)	2 B					2 B			2 B	4 B	4 B	2 B

Figure 4.7-10: TC(207,1): Automatic Mode Transition Disable Packet

	PACKET DATA FIELD (Variable)							
Field	DATA FIELD HEADER						APPLICATION DATA	PACKET ERROR CONTROL
Subfield	PUS version	Chck. Type	Ack	Pack. Type	Pack. Subtype	Pad	Mode Duration	
Content	.... b	1	$0001-_b$	207_d	1_d	0_b	32 b	
Wide (bit)	3 b	1 b	4 b	8 b	8 b	8 b		16 b
Wide (oct.)	4 B						4 B	2 B

Figure 4.7-11: TC(207,1): Automatic Mode Transition Disable Packet Data Field

5. TM-BLOCK BUILDING-UP STRATEGY

The DMS shall sequentially poll each Packet Terminal and after a positive poll (TM packets available) a complete TM-Block shall be acquired before the next packet terminal is polled. As a consequence, in order to minimise the number of the negative polls (TM packets not available), whenever it is possible, a single TM-Block shall be formed using the currently available data. Anyhow, given that after a positive poll only one complete TM-block shall be acquired by the DMS, the maximisation of the TM-block shall be adopted.

The TM-Block building-up strategy shall be based on the following preliminary remarks.

- The DMS shall sequentially poll each Packet Terminal and in case of packets available, it shall acquire one complete TM-Block before changing to the next terminal, at least one second after.
- During positive polling the OBDH bus shall execute 16384 interrogations per second, among these, 62.5% is the minimum ensured for the TM-Block acquisition ([AD.10] IFDC-001).
- The Data Rate during the interrogations for the TM-Block acquisition is 131.072 kbps ([AD.10] IFDM-040).
- Given the two preceding points, in one second (minimum interrogation period) the OBDH bus ensures the acquisition of 131.072*0.625 kb = 81.920 kb = 5120 16 bit word, this will then be the DES maximum TM-Block length.
- The TM Packet terminal has to ensure towards the OBDH bus the memorisation of 16 seconds of produced TM data.
- Different categories of data shall not be included in the same packet.

Given the preceding constraints, to easy the TM-Block building-up and to optimise the data acquisition, the following static memory buffers shall be allocated in the Data Memory of the Master DSP (Mem. ID = 177).

0. A *Polling Buffer* composed of 16 memory slots of 5120 16-bit words to memorise 16 TM-Blocks (one per slot) towards the OBDH bus for a maximum of 16 seconds The DMS polling shall be always addressed to the first non empty slot of this buffer.
1. An *Event Report Buffer* TBD 16-bit words deep, where the corresponding data are queued structured in packets.
2. An *Acceptance Report Buffer* TBD 16-bit words deep, where the corresponding data are queued structured in packets.
3. A *Housekeeping Buffer* TBD 16-bit words deep where the corresponding data are queued structured in packets.

4. A *Science Buffer* TBD 16-bit words deep where the processed scientific data queued structured in packets. In all the Operative Mode (SS1-SS5, Calibration, and Receive Only), the Science Data, apart from Individual Echoes, are allocated within the Data Field of the proper TM packet(s) during the same Frame of acquisition (TBC). The packed just built are then immediately queued in the Science Buffer.
5. An *Individual Echoes Buffer* TBD 16-bit words deep where the individual echoes, (relative to one SS1–SS2 Operative Mode Frame), are queued bare as they are acquired, without any packet structure.
6. A *Dump Buffer* TBD 16-bit words deep where the corresponding data are queued structured in packets.

The status of the preceding buffers is monitored by means of the HK-Packet (cf. Table 4.2-1). When one of the preceding buffers 1¸6, is full the DES shall execute automatically a transition to IDLE regardless the current Operation Modes (TBC) (cf. Table 4.3-3 EID 41903).

Given this memory allocation, TM-Blocks shall be built according to the following strategy. A dedicated SW task shall awake periodically one time every k second and shall poll all TM buffers always in the strict order 1¸6 (in stand-by mode the value of k is determined by the parameter 137 of the Master Parameter Table, in every other mode, k = 1). In case of positive poll from a particular TM buffer, the task shall try to copy all its queued packed inside the first empty slot in the polling buffer (buffer number 0), trying to fill it. The task shall run to the next TM buffer when all the packets of the actually polled one shall be copied. When the single interested slot is filled up, i.e. a complete packet cannot be added, or when all the buffers 1¸6 are empty, the tasks shall rest to awake again in the next one second period. Note that, in this way, for each second, at most one TM-Block shall be built. Every time the TM-Block SW task awakes, if there isn't any empty slot, i.e. there are 16 TM-Blocks ready to be acquired by the DMS in the polling buffer, the tasks rests immediately.

Since all packets are copied rigidly inside the slot (they cannot be broken up), it shall happen that the actual TM-Blocks memorised in polling buffer slots shall be shorter than 5120 16-bit words. This eventuality shall be less probable when Individual Echoes (buffer number 5) shall be present. These data shall be queued bare and shall be packetised during the TM-Block building, in this way, TM packets of variable length can be built in order to fill up completely the TM-Block (5120 16-bit words).

Note that since Individual Echoes packet length shall be in the range TBD-4112 byte, there shall be always possibility of TM-Blocks shorter than the maximum allowed.

As a consequence of the preceding policy, both number and dimension of the packets included in a TM-block, and the dimension of TM-Block itself, are variable, depending on the actual Operation Mode, frame duration and DMS polling frequency. In any case, the first word of a TM-block shall always indicate the length (in words) of the whole TM-block, as detailed in § 3.2.

6. STAND BY MODE NOMINAL OPERATIONS

6.1 DOUBLE BOOT APPROACH

At the power on, the code in the Master DPS EEPROM Protected Area (Memory Management & Data Handling Code, i.e. MASTER default code), the PT and the OST ones, and the whole EEPROM contents of the two Slaves DSP are copied in the corresponding Program RAM Memories (Check-Init). The Codes just copied are executed, running DES in the Stand-By mode, where it remains *until* power-Off, unless it receives a dedicated TC(206,2). In this case the code memorised in the Master DSP EEPROM Patchable Area (Copy of Memory Management and Data Handling Code together with Science one, i.e. MASTER patchable code) is copied in its Program RAM Memory *overwriting* entirely the default one. In the meanwhile, the two slave DSPs run in the processor internal idle. Once the MASTER patchable code is copied in RAM (second boot, i.e. science code loading operations), the DES shall remain in Stand-By for 60 sec, then the automatic transition to WA_UP1 mode shall occur.

6.1.1 Operations' Limitation Before Second Boot

Before second boot, TC(6,5) with MEM ID 187, 188, 189, 190 (FLASH MEMORY dump) are refused. Flash Memory dump shall have to be executed *after* the second boot.

6.1.2 Master Patchable Code Starting-Up Tc(206,2)

The second boot shall be executed when, after the first one and during the Stand-By Mode, the DES shall receive the following dedicated TC(206,2) - PT patch TC for Master Patchable Code Starting-Up:

"1C CC D8 00 00 13 11 CE 02 00 B1 01 00 00 00 26 00 01 FF F2 C0 DE 2F FF 74 99."

Note that its *first and only block* has an application data field with the following structure:

- Mem. ID = 0xB1 = 177 d,
- Blocks' No = 0x01 = 1d,
- Start Address = 0x00000026 = 38d,
- Blocks' Length = 0x0001 = 1d,
- data field (parameter) = 48 bit code FF F2 C0 DE 2F FF.

The PT patch is actually dummy, it is not really executed.

6.1.3 Double Boot Operations' Caracteristics

Worth noting characteristics of the **double boot operation** are the following.

I. The second boot shall be executed immediately after the TC(206,2) of Master Patchable Code Starting-Up shall be accepted *and* no TM blocks remain in the DES buffer to be acquired by DMS. The PT patch corresponding to this TC *shall not* be executed.

II. The second boot shall require 20 sec to be executed completely. That is to say that if there are *not* dump TM(6,6) queued in TM blocks, the DES shall be ready to receive, validate and execute TCs 20 sec after the OBDH bus interrogations containing the TC(206,2) of Master Patchable Code Starting-Up.

III. If DES doesn't receive any TC(207,1) (Automatic Mode Transition Disable) after the double boot execution, it shall run in WA_UP1 Mode 80 sec after the OBDH bus interrogations containing the TC(206,2) of Master Patchable Code Starting-Up.

IV. All the TCs queued in the 64 slot buffer (cf. §6.2) after the TC(206,2) of Master Patchable Code Starting-Up, shall be lost because this buffer shall be cleared during the double boot execution. No TM(1,2) nor TM(5,2) shall be generated regarding the TCs present (if any).

V. The DES shall execute a new "double boot", i.e. the Master DSP EEPROM Patchable Area shall be copied in the MASTER Program RAM whenever, during Stand-By Mode, a correct TC(206,2) of Master Patchable Code Starting-Up is received and validated.

VI. If any error occurs in the TC(206,2) of Master Patchable Code Starting-Up, the TC is refused and the second boot doesn't occur.

VII. From the TCs' reception, validation and execution point of view, the DES Stand-By states before and after the double boot execution are exactly the same, a part from TC(207,2) (in the state before, this TC has no consequences, even if it is accepted) and TC(6,5) with MEM ID 187, 188, 189, 190 (FLASH MEMORY dump, cf. §6.1.1)

VIII. The OST and PT Program RAM areas written at the first boot are not interested by the second boot Program RAM code overwriting. As a consequence, every patch of these areas, whenever it is executed, is maintained after the second boot.

6.2 TCs VALIDATION AND EXECUTION

The DES has an internal buffer where up to 64 TCs can be stored as soon as they are received, waiting to be validated and executed one at a time. A single TC slot is cleared out once the relevant TC execution is completed.

6.2.1 TCs Of Fast Execution

The following MARSIS DES TCs require less then 10 msec to be validated and executed:

- TC(3,5),
- TC(3,6),
- TC(9,1),
- TC(206,1),
- TC(206,2),
- TC(207,1).

6.2.2 TCs Of Slow Execution

The following MARSIS DES TCs have not a negligible validation and execution time:

- TC(6,2) with MEM IDs 176, 179, 183 (EEPROM Memories Patch) requires up to 1 sec to be validated and executed,
- TC(6,2) with MEM IDs 177, 178, 180, 181, 184,185 (RAM Memories Patch) requires up to 200 ms to be validated and executed,
- TC(6,5) (Memories Dump) has an execution time depending on the memory size to be dumped. In the dump process, the DMS TM acquisition is the bottleneck, then, every OBDH bus 16384 interrogations per second cycle[1], up to (16384*.625)/2 = 5120 16 bit words can be acquired per second cycle. As a consequence, if p is the DMS polling frequency assigned to MARSIS, 5k 16-bit words can be dumped every 1/p sec, assuming no other TMs present.

6.2.3 TCs Reception Management During Tcs Execution

During the execution of TC(6,2) with MEM IDs 176, 179 and 183 the DES shall not be able to manage any new TC's reception, i.e. it shall not be able to queue any new TC in the 64 slot buffer of §6.2. As a consequence, if during the TC(6,2) execution an OBDH interrogation containing a TC slot occur, the contained TCs shall be lost and no TM(1,2), nor TM(5,2) shall be generated. On the contrary, during the execution of all the other TCs, the DES shall be able to queue TCs and if the 64 slot buffer is full, TM(1,2) or TM(5,2) shall be generated (FID = 5, reason = 0x5 - RECEIVED_TCs_BUFFER_FULL, i.e. the buffer used to store received TC for further validation is full).

6.2.4 Constraint On Tcs' Distribution

Due to the states described in §6.2.1 and §6.2.2, the DMS TCs' distribution shall have to be compliant with the following conditions in order to assure the reception of all the TCs.

I. In each OBDH TC slot shall have to be present TCs listed in §6.2.1 <u>*or*</u> TCs(6,2) with MEM IDs 176, 179 and 183 (EEPROM Memories Patch) <u>*or*</u> TC(6,2) with MEM IDs 177, 178, 180, 181, 184,185 (RAM Memories Patch) <u>*or*</u> TC(6,5) (Memories Dump).

II. Each OBDH TC slot can contain up to 64 TCs of the set in §6.2.1. No constraints are set on structure and timing of the following TC slots.

III. Each OBDH TC slot can contain up to 64 TC(6,5). Being m the dimension in k 16-bit word of the entire memory area to be dumped by these TCs, the following TC slot shall have to occur at least (m/5)*(1/p) sec *later* (cf. §6.2.2). No constraints are set on the composition of these next TC slot.

IV. Each OBDH TC slot can contain *only one* TC(6,2) with MEM IDs 176, 179 and 183, which shall have to be the *only one* TC present. No constraints are set on the composition of the next TC slots.

[1] cf. PID A, MEX-MMT-SP-0007 Rev 2, annex A, §4 Command Distribution and Data Acquisition Protocols, IFDC-001, IFDC-202 and IFDC-210.

V. Each OBDH TC slot can contain up to 5 TC(6,2) with MEM IDs MEM IDs 177, 178, 180, 181, 184 and 185. No constraints are set on the composition of the next TC slots.

6.3 DOUBLE BOOT OPERATIONS

As a consequence of the statements in §0 and in §6.2.4, the events' sequence of a typical science observation that necessarily involves a **double boot operation**, shall have to be as structured follow.

I. Power on.

II. Autonomous first boot (Check-Init Mode).

III. Autonomous Mode Transition from Check-Init to Stand-By after 6 sec *(TBC)* after power on.

IV. Send the TC(9,1).

V. 8 sec wait to receive the SYNC signal and to let the DES timing synchronisation.

VI. Send TCs(206,1) and TCs(206,2) necessary to define the OSTs (i.e. scientific observations details) and to set the concerning PT parameters' values. If p is the DMS polling frequency, this step shall require 1/p sec *for each* OBDH TC slot used. Each TC slot can contain up to 64 TCs(206,1) and TCs(206,2).

VII. Send up to 64 TCs(6,5) in a *single* OBDH TC slot to let the memory dump of areas of particular interest (if any).

VIII. (m/5)*(1/p) sec wait to let dump TM(6,6) acquisition by DMS. Here m is the dimension in k 16-bit word of the entire memory area concerning the TCs of point VII and p is the DMS polling frequency.

IX. Repeat point VII and VIII *if* the number of TCs(6,5) to be sent is greater than 64.

X. Send the Master Patchable Code Starting-Up TC(206,2) (cf. §0).

XI. 8 sec wait necessary to validate the preceding TC(206,2), and to let the corresponding Acceptance Report TM(1,1) to be generated by the DES and acquired by the DMS.

XII. 12 sec wait to execute the second boot (i.e. Master Patchable code loading operations).

XIII. 60 sec wait in Stand-By (unless TC(207,2) shall be is sent after the second boot).

XIV. Autonomous Mode Transition from Stand-By to WA-UP1

The following table summarises the schedule of the preceding step.

STEP	STARTING TIME (sec)
I & II & III	t0
IV & V	t1 = t0 + 6 (tbc)
VI	t2 = t1 + 8
VII & VIII & IX	t3 = t2 + n/p (n = number of TC slot used in VI)
X & XI	t4 = t3 + k*(m/5)*(1/p) (k = number of iterations of VII & VIII)
XII	t5 = t4 + 8
XIII	t6 = t5 + 12
XIV	t7 = t6 + 60

Table 6.3-1: schedule of the typical operations' scenario

6.4 EEPROM PATCH OPERATIONS

During Stand-By mode, running in the MASTER Program RAM the Default Code and the only code of the slave DSPs, patches can be executed on the patchable EEPROM area of each DSP via TC(6,2) Since the first segment of each EEPROM memory is protected, the allowed values for the tern [Process ID, Memory ID, Start Address] are listed in the following table:

	Process ID.	Memory ID.	allowed Start Addresses (interval)
MASTER DSP	76	176	[0xB000, 0x1FFFF]
SLAVE1 DSP	77	179	[0x2000, 0x1FFFF]
SLAVE2 DSP	78	183	[0x2000, 0x1FFFF]

Table 1.4-1: patch TC(6,2) field values matching

If the field values don't match the scheme reported, the TC(6,2) is refused.

As a consequence of the statements in §6.2.4, IV, the events' sequence of a typical EEPROM memory patch scenario shall have to be structured as follow.

I. Power on.

II. Autonomous first boot (Check-Init Mode).

III. Autonomous Mode Transition from Check-Init to Stand-By after 6 sec *(TBC)* after power on.

IV. Send the TC(9,1).

V. 8 sec wait to receive the SYNC signal and to let the DES timing synchronisation.

VI. Send a *single* TC(6,2) with MEM IDs 176, 179 and 183 within the next OBDH interrogations TC slot.

VII. Repeat step VI until all scheduled patch TCs have been sent.

VIII. Power off.

Note that, given the DMS polling strategy, the point VI guarantees the following:

STRICT CONSTRAINT: EEPROM patch TCs must be sent to MARSIS DES up to a *maximum* of a *single* TC per second.

This scheme is necessary otherwise some TC could be lost. In fact, the DES validates *and* executes immediately after each single TC, one per time, before taking into consideration the following one. Normally, the next incoming TCs, before validation, are queued in a 64 slot buffer in the Master DSP Data RAM, but the execution of an EEPROM patch TC(6,2) has to be executed with disabled interrupts. As a consequence, during this execution time, the next incoming TC cannot even be completely acquired and memorised in the this buffer, because the Master DSP is not able to read the interface register where the DMS writes the TC word per word. At the interrupts' enabling, one ore more TC could be lost completely or in part (note that the DES refuses every incomplete TC). The one per seconds maximum TC flux, is then necessary to guarantee the complete execution of an EEPROM patch TC(6,2) before the next is sent to the DES.

6.5 RAM PATCH OPERATIONS AND WARM RESTART APPROACH

During stand-by mode, running in the MASTER RAM the default code or the patchable one (i.e. executed the second boot or not, cf. §6.1), it is possible to patch the Program and Data RAM of MASTER and Slaves DSPs.

6.5.1 Ram Patch Execution

The patch operations shall be executed by means of the dedicated TC(6,2) characterised by (cf. Table 4.4-1):

- Process ID 76, Memory IDs 177 and 178 (Master, Program and Data RAM),
- Process ID 77, Memory IDs 180 and 181 (Slave1, Program and Data RAM),
- Process ID 78, Memory IDs 184 and 185 (Slave2, Program and Data RAM).

6.5.2 Constraint On Ram Patch Tcs' Distribution

The DES is able to manage up to 5 RAM patch TC(6,2) per second (cf. §6.2.4).

6.5.3 TCs Acceptance Report

For Memory IDs 178, 180, 181, 184 and 185, TM(1,1) or TM(1,2) or TM(5,2) generation reflects validation and direct execution result of the corresponding TC. For Memory IDs 177 report TMs only reflect the result of TC validation and *queuing* in a dedicated Master Program RAM BUFFER, in fact Master Program RAM patches are *not* executed immediately after TC validation. The previous RAM BUFFER is 2.4 Mbyte deep if the the MASTER default code is running, or 2.388 Mbyte if the patchable one is (cf. §6.1).

6.5.4 New Code Execution: Warm Restart

Being the relevant data queued in the dedicated buffer (cf. previous section), the Master Program RAM patches shall be really executed immediately after the receiving and validation of the following dedicated TC(206,2) – PT patch TC for Warm Restart:

"1C CC D8 00 00 13 11 CE 02 00 B1 01 00 00 00 39 00 01 FF FF DE AD FF FF 74 99"

Note that its *first and only block* has an application data field with the following structure:

- Mem. ID = 0xB1 = 177 d,
- Blocks' No = 0x01 = 1d,
- Start Address = 0x00000039 = 57d,
- Blocks' Length = 0x0001 = 1d,
- data field (parameter) = 48 bit code FF FF DE AD FF FF.

The PT patch is actually dummy, it is not really executed. If any of the TCs listed in §6.5.1 is not received before the previous TC, it shall be refused.

The actual code overwriting in the Master RAM shall be carried out by the Master EEPROM code. At the end of data copying, the new RAM program shall be *autonomously* executed starting from the first Master Program RAM address (Warm Restart). The warm restart TC(206,2) is the following:

6.5.5 Ram Patch Warning

The Data and Program RAM, in the Master DSP as in the Slave ones, are strictly related. As a consequence, it is highly probable that if the only Program or the Data memory is pached, without upgrading the other accordingly, the SW shall go in an instable state and the HW watchdog shall be released.

6.5.6 Ram Patch Events' Sequence

As a consequence of the statements in previous sections the events' sequence of a typical RAM memories patch scenario shall have to be structured as follows.

I. Power on.

II. Autonomous first boot (Check-Init Mode).

III. Autonomous Mode Transition from Check-Init to Stand-By after 6 sec *(TBC)* after power on.

IV. Send the TC(9,1).

V. 8 sec wait to receive the SYNC signal and to let the DES timing synchronisation.

VI. Send the PT patch TC(206,2) for second boot execution *and* TC(207,1) for delay of autonomous transition to WA-UP2 (the second boot is actally optional).

VII. Send a up to 5 TC(6,2) with MEM IDs 177, 178, 180, 181, 184 and 185 per second.

VIII. Repeat step VII until all scheduled patch TCs have been sent.

IX. Send the PT patch TC(206,2) for warm restart.

X. Execute all operations requested by the new code just pached.

XI. Power off.

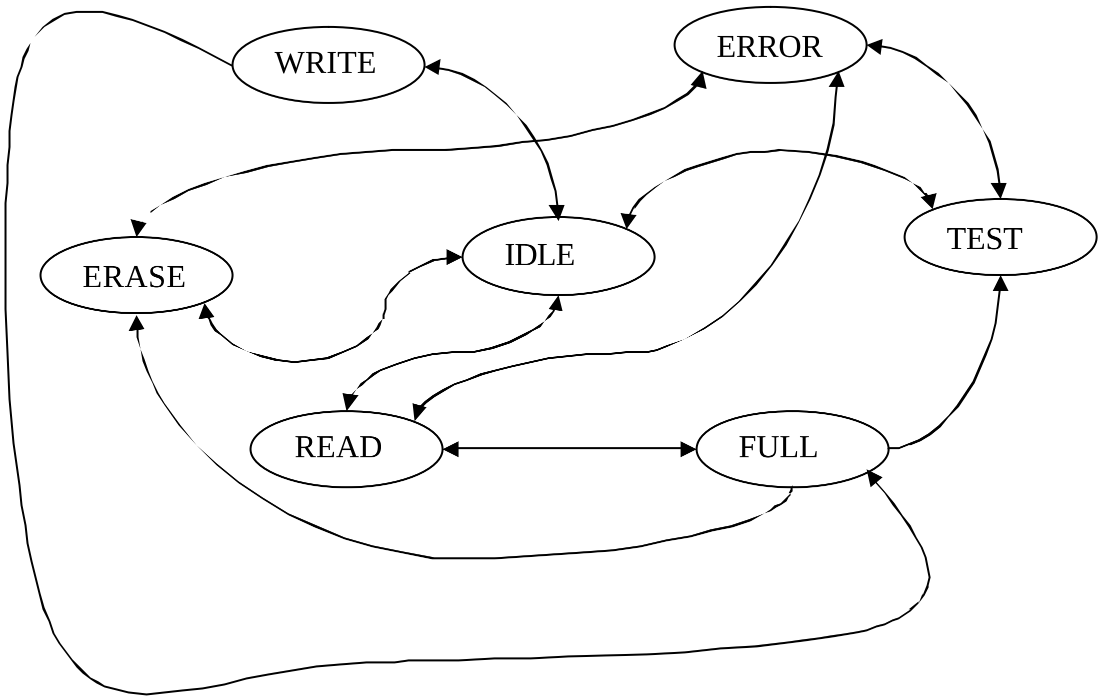
7. MARSIS FLASH MEMORY APPROACH

7.1 FM STATES

FM shall have 7 states:
- idle,
- error
- test,
- erase,
- write,
- read,
- full.

7.1.1 FM Allowed State Transition

The only allowed state transitions are described in the following diagram.



7.1.2 FM Check at Power-On

At power-on the FM filling state shall be evaluated skimming the memories looking for consecutive data amount fields in the packet data header (cf. §7.7.5), until an empty address m (chip, sector and offset) is reached (empty stand for pattern “FFFF”). Given the structure of the packet data header, the first FM empty address has to be the number m-20 (16-bit-word for each address). If the whole intervall [m-20,m] shall results empty, FM shall enter the IDLE state being m the first address for the next data storage, otherwise it shall enter the ERROR state. If the first FM empty address m-20 shall result greater than the whole FM dept (16 Mbyte), the FM shall enter the FULL state.

7.2 FM IDLE STATE

In idle state FM are ready to be written (write state), dumped (read state), erased (erase state) and tested (test state).

7.3 FM ERROR STATE

FM can enter the error state from test and erase ones, or during the memory check at power on. In the error state FM can be read, tested and erased, but cannot be written.

7.4 FM TEST STATE

It will be possible to test the HW integrity of the 4 Flash Memories banks during Stand-By Mode. At the receiving of a dedicated TC(206,2), all memory banks, address by address singularly, shall be completely erased, dummy written, reread and erased again. The testing start-end address shall be specified in PT. If a single address cannot be read within timeout, FM shall enter the error state. The test results shall be reported in the HK TM(3,25) (cf. §1.11).

7.4.1 TC Handling During Test State

During test, FM cannot be erased, dumped, nor a new test session can be ordered. As a consequence, the TC which induce FM erasing, dumping and testing shall be refused (cf. §1.10).

7.5 FM Erase State

Before writing, Flash Memories have to be erased. Because of this constraint, at the receiving, during Stand-By Mode, of a dedicated TC(206,2), all memory banks, address by address singularly, shall be completely erased, i.e. one filled. The erasing start-end address shall be specified in PT. If a single address cannot be erased within timeout, FM shall enter the error state. The test results shall be reported in the HK TM(3,25) (cf. §1.10).

7.5.1 TC Handling During Erase State

During erase, FM cannot be dumped, tested, nor a new erase session can be ordered. As a consequence, the TC which induce FM dumping, testing and erasing shall be refused (cf. §1.10).

7.6 FM WRITE STATE

7.6.1 FM Data Type

In Flash Memories shall be stored the following data type:
- raw tracking data,
- raw acquisition *and* tracking data,
- uncompressed tracking telemetry,
- uncompressed acquisition *and* tracking telemetry.

7.6.2 FM Data Storage Driving

The data storage in Flash Memories shall be requested in each OST line singularly. Bit No 80÷95 shall state the number n_FM of *consecutive* frames of the OST line itself that has to be stored, while bits No 76÷79 shall determine the data type, according to the following codes.

A. 0000: no data storage**.**

B. 0001: no data storage**. Raw input data of the *first tracking frame* after k_ie frames shall be download in TM(20,3), being k_ie memorised in PT (Tracking Individual Echoes).**

C. 0010: no data storage**. Raw input data of the *first* acquisition frame after k_ie frames shall be download in TM(20,3), being k_ie memorised in PT (Acquisition Individual Echoes).**

D. 0011: raw tracking data storage**. Raw input data of the *first n_FM tracking frames* after k_FM frames, being k_FM memorised in PT (acquisition frames shall be skipped in the n_FM computation, but *not* in the k_FM one).**

E. 0100: raw tracking *and* acquisition data storage**. Raw input data of the *first n_FM frames* (tracking and acquisition) after k_FM frames, being k_FM memorised in PT.**

F. 0101: uncompressed tracking telemetry storage**. Entire 32-bit telemetry of the *first n_FM tracking frames* after k_FM frames, being k_FM memorised in PT (acquisition frames shall be skipped in the n_FM computation, but *not* in the k_FM one).**

G. 0110: uncompressed tracking *and* acquisition telemetry storage**. Entire 32-bit telemetry of the *first n_FM frames* (tracking and acquisition) after k_FM frames, being k_FM memorised in PT.**

H. 0111÷1111: no data storage**.**

The computation of the number n_FM is reset at every new OST line, then if the number n_FM is not reached before the present OST line operations, the remaining frame shall *not* be acquired during the following one operation. Note that in case of preset tracking operations, cases D and E, and cases F and G are exactly alike. In case D÷G, if n_FM = 0, no data shall be storaged.

7.6.3 Flash Memories Writing Strategy

Regardless the selected Operative Mode, the input data-rate is always higher than the Flash Memories write throughput; that is to say, it is not possible to store directly data into the Flash Memories as soon as they are acquired. Because of this drawback, data shall therefore be stored temporary into the Program and Data RAM of the slave DSPs, before being written into Flash Memories.
Presently, 370176 (TBC) words of Program RAM and 431870 (TBC) words of Data RAM are available on each slave DSP for storing raw data; each DSP shall then be able to store up to (370176 * 4) + (431870 * 4) = 3208184 bytes, that shall be organized in a single circular buffer.
Data concerning one or more OST lines, once memorized in the slave DSPs RAM buffer, shall be copied into the Flash Memories during a specific Operative Mode (ID 13), in which no science task shall run. In addition, data copying shall also be executed during all mute PRIs that are not part of a Subsurface Sounding frame.

7.6.4 FM Data Storage Inhibition

For each single OST line, at every frame, dispositions concerning points D÷G of §1.7.2 shall be ignored, i.e. they shall *not* be executed, if one of the following conditions shall occur.

- Data moving from RAM buffer (described in §7.7.3) to FM has started but not completed.
- In the RAM buffer there is not enough empty space to memorise the whole data amount for the present frame.
- The FM are in the full state.
- One of the previous case has occured for a preceding frame of the *current* OST line.

7.6.5 FM Data Header

Each group of science data relevant to a single frame, shall be preceded by a header specifying the related operation parameters, according to the following scheme:

PARAMETER	SIZE	code specification
SCET*	48 bit	NA
OST LINE NUMBER	16 bit uint	NA
OST LINE	96 bit	NA
FRAME ID	16 bit uint	NA
1st PRI OF THE FRAME	32 bit uint	NA
SCET FRAME	48 bit	NA
SCET PERICENTER	48 bit	NA
NA	16 bit uint	NA
BAND	2 bit	00: band 1
		01: band 2
		10: band 3
		11: band 4
CHANNEL(S)	2 bit	00: dipole
		01: dipole & monopole (in the order)
		10: monopole
SCIENCE DATA TYPE	2 bit	00: acquisition raw
		01: uncompress acquisition telemetry
		10: tracking raw
		11: uncompress tracking telemetry
SCIENCE DATA AMOUNT (number of 16 bit word)	26 bit	NA

Table 7.6-1: Falsh Memories Packed Header

7.6.6 FM Data Mapping

In the dedicated RAM memory buffer of each slave DSP, there will be a continuous stream of data referring to the same OST line (H = header, D = data):

H1	D1	H2	D2	H3	D3			Hn	Dn

This stream of data shall be copied in the Flash Memories, the whole one contained in slave DSP1 before the whole one in slave DSP2. In order to reduce the data copying time, the four Flash chips shall be written simultaneously. As a consequence, if the k-th 16 bit word of the stream is copied in the chip number c (c = 0,1,2,3), the word k+1-th is copied in the chip number mod(c+1,4), the word k+2-th in the chip number mod(c+2,4), and so on.

7.7 FM READ STATE

During stand-by mode only, FM can be read, i.e. dumped by means of dump TC(6,5) and TM(6,6).

7.8 FM FULL STATE

When not enough free space is left to storage one more frame, FM enter in full state and the transition to write state is inhibited.

7.9 TC REFUSING DURING FM OPERATIONS

During test and erase states TC(206,2) and TC(6,5) concerning FM further operations shall be refused (cf. §1.5.1 and §1.6.1). As a consequence, TM(1,2) or TM(5,2) shall be generated with FID = 5 and reason = 0x6, i.e. command cannot be executed at this time because the requested operation on FM cannot run, due to another operation already in progress in FM themselves. Note that TC(206,2) and TC(6,5) concerning FM operations don't interrupt FM reading because they are not executed until the carrying out of the TC(6,5) is completed, i.e. until the requested dump TM(6,6) have been transmitted.

7.10 HK REPORT PACKET DATA FIELD PARAMETERS

Every 8 second HK TM(3,25) describes the actual FM status, reporting the actual values of proper FM status parameters (cf. Table 4.2-1).

8 ANNEX1: MEMORY MAPPED REGISTERS

PRI COUNTER
ADDRESS: 0x00088000
WIDTH: 19 BIT
CONTENTS: NUMBER OF PRI SINCE POWER-ON
ACCESS: READ-ONLY

OBT REGISTER LSW
ADDRESS: 0x00086000
WIDTH: 32 bit
CONTENTS: lower 32 bits of the On-Board Time to be loaded by the TSY pulse
ACCESS: WRITE-ONLY

OBT REGISTER MSW
ADDRESS: 0x00088000
WIDTH: 16 bits
CONTENTS: Most significant Word of the On Board Time to be loaded with the TSY pulse
ACCESS: WRITE-ONLY

OBT FREEZE REGISTER LSW
ADDRESS: 0x00080000
WIDTH: 32bit
CONTENTS: least significant bits of the counted On-Board Time
ACCESS: READ-ONLY

OBT FREEZE REGISTER MSW
ADDRESS: 0x00082000
WIDTH: 16 bits
CONTENTS: most significant bits of the counted OBT
ACCESS: READ-ONLY

MLC REGISTER
ADDRESS: 00084000
WIDTH: 16 bits
CONTENTS: next telecommand word
ACCESS: READ-ONLY

TM REGISTER
ADDRESS: 00084000
WIDTH: 16 bits
CONTENTS: atomic telemetry word to be sent to the S/C
ACCESS: WRITE-ONLY

INTERRUPT FLAG REGISTER
ADDRESS: 0x00094000 to read
0x00092000 to clear (zero)
WIDTH: 6 bits
CONTENTS: see table
ACCESS: READ/WRITE

Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1: DSP1 interrupt occurred	1: DSP2 interrupt occurred	1: PRF interrupt occurred	1: TIMING request occurred	Not used	1: watchdog not expired
0: no DSP1 interrupt	0: no DSP2 interrupt	0: no PRF interrupt	0: no TIMING request	Not used	0: watchdog has expired

INTERRUPT MASK REGISTER
ADDRESS: 0x0008E000
WIDTH: 5 bits
CONTENTS: see table
ACCESS: WRITE-ONLY

Bit5	Bit4	Bit3	Bit2	Bit1
1: DSP2 interrupt masked	1: DSP1 interrupt masked	1: PRF interrupt masked	1: TIMING request masked	Not used
0: DSP2 interrupt unmasked	0: no DSP1 interrupt unmasked	0: PRF interrupt unmasked	0: TIMING request unmasked	Not used

DCG BUFFER REGISTERS
ADDRESS: 0x00090000
ACCESS: WRITE-ONLY

Register 1

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
START FREQUENCY MSB								X	X	X	X	X	**0**	**0**	**0**
DATA								SPARE					**ADDRESS**		

Register 2

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
START FREQUENCY LSB								X	X	X	X	X	**0**	**0**	**1**
DATA								SPARE					**ADDRESS**		

Register 3

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
STEP FREQUENCY MSB								X	X	X	X	X	**0**	**1**	**0**
DATA								SPARE					**ADDRESS**		

Register 4

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
STEP FREQUENCY LSB								X	X	X	X	X	**0**	**1**	**1**
DATA								SPARE					**ADDRESS**		

Register 5

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
STEP NUMBER												X	**1**	**0**	**0**
DATA												X	**ADDRESS**		

Register 6

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
STEP DURATION								X	X	X	X	X	**1**	**0**	**1**
DATA								SPARE					**ADDRESS**		

Writing “0x7” at this address (90000) forces the transmission of the 6 registers contents to the DCG.

WATCHDOG COUNTER
ADDRESS: 0x00082000
WIDTH: 13bits
CONTENTS: value of time loaded in a counter
ACCESS: WRITE-ONLY

OUTPUT REGISTER
ADDRESS: 0x0008C000
WIDTH: 5 bits
CONTENTS: see table
ACCESS: WRITE-ONLY

Bit4	Bit3	Bit2	Bit1	Bit0
TBD	TBD	0: RX switched OFF	0: TX switched OFF	0: DES in Tracking
TBD	TBD	1: TX switched ON	1: TX switched ON	1: DES in Acquisition

SYSTEM RESET COMMAND

ADDRESS: 0x00080000
WIDTH: 1
CONTENTS: it is not a register; when writing at that address whichever value, a reset pulse is issued to the DSP1/DSP2/TIMING boards.
ACCESS: WRITE-ONLY

Effects of reset pulse on the system:
- DSP1 and DSP2 CPUs are reset
- TIMING FPGA is put in the reset state, just like a power-on
- NOTE: MASTER (C&C) CPU is not reset, neither its FPGA, nor DCG.

Explicitly NOT reset by this command:
- DC/DC converters ON commands are NOT reset
- Watchdog flag is NOT reset
- PRF counter

In order to force a (self-)reset on the MASTER, use the watchdog, by writing a number close to FFFF. But: the watchdog will restart with its flag at 1.

REGISTERS ON TIMING BOARD

MODE_R REGISTER
ADDRESS: 0xAA000
CONTENTS: see table
ACCESS: READ/WRITE

Code	PRI	meaning
00h	MUTE	No operation in this PRI, except AIS
10h	SS1-SA	SubSurface mode 1, synthetic aperture
11h	SS2_3-SA	SubSurface mode 2 or 3, synthetic aperture
12h	SS4-SA	SubSurface mode 4, synthetic aperture
13h	SS5-SA	SubSurface mode 5, synthetic aperture
14h	ACQ-1	Acquisition phase, echo to DSP1
15h	ACQ-2	Acquisition phase, echo to DSP2
16h	NPM-1	Noise Passive Measurement, DSP1
17h	NPM-2	Noise Passive Measurement, DSP2
18h	PIG-D-1	Passive Ionosphere Gate, dipole, DSP1
19h	PIG-D-2	Passive Ionosphere Gate, dipole, DSP2
1Ah	PIG-M-1	Passive Ionosphere Gate, monopole, DSP1
1Bh	PIG-M-2	Passive Ionosphere Gate, monopole, DSP2
3Ch	AIS-1	Active Ionosphere Sounding, DSP1
3Dh	AIS-2	Active Ionosphere Sounding, DSP2
1Eh	HWCAL	Calibration
1Fh	REC	Receive only
20h	MUTE AIS	No operation, in AIS

RX_DIST1_R REGISTER
ADDRESS: 0xAA001
CONTENTS: see table
ACCESS: READ/WRITE

register	format															
	B 15															**B 0**
RX_DIST1_R	Number of 2.8MHz intervals form the chirp pulse to the first frequency LO DCG trigger															

RX_DIST2_R REGISTER
ADDRESS: 0xAA002
CONTENTS: see table
ACCESS: READ/WRITE

register	format															
	B 15															**B0**
RX_DIST2_R	Number of 2.8MHz intervals from the chirp pulse to the first frequency LO DCG trigger															

TX_settings_f1 REGISTER
ADDRESS: 0xAA003
CONTENTS: see table
ACCESS: READ/WRITE

register	format															
	B 15															**B 0**
TX_settings_f1										IOPWRCTL_f1				XMIT_SEL_f1		

IOPWRCTL			
MSB			*LSB*
IOPWRCTL4	IOPWRCTL3	IOPWRCTL2	IOPWRCTL1

XMIT_SEL		
MSB		*LSB*
XMIT_SEL3	XMIT_SEL2	XMIT_SEL1

TX_settings_f2 REGISTER
ADDRESS: 0xAA004
CONTENTS: see table
ACCESS: READ/WRITE

register	**format**															
	B 15															**B 0**
TX_settings_f2										IOPWRCTL_f2				XMIT_SEL_f2		

IOPWRCTL			
MSB			*LSB*
IOPWRCTL4	IOPWRCTL3	IOPWRCTL2	IOPWRCTL1

XMIT_SEL		
MSB		*LSB*
XMIT_SEL3	XMIT_SEL2	XMIT_SEL1

RX_settings_f1 REGISTER
ADDRESS: 0xAA005
CONTENTS: see table
ACCESS: READ/WRITE

register	format															
	B 15															B 0
RX_settings_f1			RXSWPOS_f1		ATTSEL_f1						FILTSEL_f1					

RXSWPOS	
MSB	*LSB*
RXSWPOS2	RXSWPOS1

ATT_SEL					
MSB					*LSB*
ATT2_SEL3	ATT2_SEL2	ATT2_SEL1	ATT1_SEL3	ATT1_SEL2	ATT1_SEL1

FILT_SEL					
MSB					*LSB*
FILT2_SEL3	FILT2_SEL2	FILT2_SEL1	FILT1_SEL3	FILT1_SEL2	FILT1_SEL1

RX_settings_f2 REGISTER
ADDRESS: 0xAA006
CONTENTS: see table
ACCESS: READ/WRITE

Register	format															
	B 15															B 0
RX_settings_f2			RXSWPOS_f2		**ATTSEL_f2**						FILTSEL_f2					

RXSWPOS	
MSB	*LSB*
RXSWPOS2	RXSWPOS1

ATT_SEL					
MSB					*LSB*
ATT2_SEL3	ATT2_SEL2	ATT2_SEL1	ATT1_SEL3	ATT1_SEL2	ATT1_SEL1

FILT_SEL					
MSB					*LSB*
FILT2_SEL3	FILT2_SEL2	FILT2_SEL1	FILT1_SEL3	FILT1_SEL2	FILT1_SEL1

See RX_settings_f2 register for bit meaning.

MAX_ATT REGISTER
ADDRESS: 0xAA007
CONTENTS: see table
ACCESS: READ/WRITE

register	**format**															
	B 15															**B 0**
MAX_ATT			RXSWPOS_maxatt		**ATTSEL_maxatt**						FILTSEL_maxatt					

FLASH_M REGISTER
ADDRESS: 0xAA008
CONTENTS: see table
ACCESS: READ/WRITE

Register	Format															
	B15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**B0**
FLASH_M	**Ready/busy**					**\AD1**	**\AD0**		**A20**	**A19**	**A18**	**A17**	**A16**	**A15**	**A14**	**A13**

AD1	AD0	BANK
0	0	2Mx16 LOW
0	1	2M x 16 midlow
1	0	2M x 16 midhigh
1	1	2Mx16 HIGH