Enable/Disable write to ACC ASW/BSW code and constants
File: C_CRP_OBS_2102.xls
Author: Liviu Stefanov

# Procedure Summary

## Objectives

This Herschel and Planck common OBSM contingency procedure is used to Enable or Disable the write access to the ACC ASW/BSW code and constants (i.e. write access to CPU RAM). The write access via TC(6,2) or TC(8,4,7,1) is enabled/disabled.

Note: The write access to ACC CPU and COCOS registers or EEPROM can be Enabled/Disabled using procedure C_CRP_OBS_2100.

## Summary of Constraints

n/a

## Spacecraft Configuration

**Start of Procedure**

ACC in operational mode
- Write access to ACC CPU RAM Enabled or Disabled

**End of Procedure**

ACC in operational mode
- Write access to ACC CPU RAM Disabled or Enabled

## Reference File(s)

**Input Command Sequences**

**Output Command Sequences**

OCRP210E
OCRP210F

## Referenced Displays

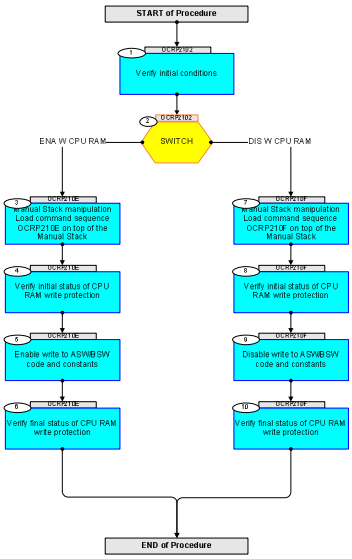
**ANDs** **GRDs** **SLDs**
ZAA09999

## Configuration Control Information

| DATE | FOP ISSUE | VERSION | MODIFICATION DESCRIPTION | AUTHOR | SPR REF |
|---|---|---|---|---|---|
| 30/01/08 | 1 | 1 | Created | lstefanov-hp | |

Enable/Disable write to ACC ASW/BSW code and constants
File: C_CRP_OBS_2102.xls
Author: lstefanov-hp

# Procedure Flowchart Overview



Enable/Disable write to ACC ASW/BSW code and constants
File: C_CRP_OBS_2102.xls
Author: lstefanov-hp

| Step No. | Time | Activity/Remarks | TC/TLM | Display/ Branch | AIT Comment |
|---|---|---|---|---|---|
| | | **Beginning of Procedure** | | | |
| | OCRP2102 | *TC Seq. Name :* OCRP2102 ( ENA/DIS W CPU RAM )<br>Enable/Disable write to ACC ASW/BSW code and constants<br><br>*TimeTag Type:*<br>*Sub Schedule ID:* | | | |
| 1 | | Verify initial conditions | | Next Step:<br>2 | |
| | | Check:<br>- ACC in operational mode<br>- ENA/DIS status of write access to ACC ASW/BSW code and constants (write to CPU RAM) | | | |
| 1.1 | | Check ACC in operational mode | | | |
| 1.2 | | Check write protection status | | | |
| | | **Note:**<br>Note that the parameter CPU RAM write protection status (doughter of **DID_BSW_MEM_ACCESS**) is part of the **default ACC diagnostic packet** (**BSW1**); thus to acquire this parameter the packet **must be enabled**. | | | |
| | | **Note:**<br>Following TM check assumes **write** access to CPU and COCOS registers and EEPROM is **Disabled**. | | | |
| | | Verify Telemetry<br>**CpuRamWriteProt AEGU2050** | **= ENABLED** | AND=ZAA09999 | |
| 2 | | SWITCH<br><br>type: [Switch] | | Next Step:<br>ENA W CPU RAM<br>3<br>DIS W CPU RAM<br>7 | |
| | | End of Sequence | | | |
| | OCRP210E | *TC Seq. Name :* OCRP210E ( ENA W ACC CPU RAM )<br>Enable write to ACC ASW/BSW code and constants<br><br>*TimeTag Type: N*<br>*Sub Schedule ID:* | | | |
| 3 | | Manual Stack manipulation<br>Load command sequence OCRP210E on top of the Manual Stack | | Next Step:<br>4 | |

Enable/Disable write to ACC ASW/BSW code and constants
File: C_CRP_OBS_2102.xls
Author: lstefanov-hp

| Step No. | Time | Activity/Remarks | TC/TLM | Display/ Branch | AIT Comment |
|---|---|---|---|---|---|
| 3.1 | | Sequence data<br><br>FP: N/A<br>TT: N/A | | | |
| | | | | | |
| 4 | | Verify initial status of CPU RAM write protection | | Next Step:<br>5 | |
| | | **Note:**<br>Protection Enabled = Write access Disabled<br>Protection Disabled = Write access Enabled | | | |
| | | **Note:**<br>Note that the parameter CPU RAM write protection status (doughter of **DID_BSW_MEM_ACCESS**) is part of the **default ACC diagnostic packet** (**BSW1**); thus to acquire this parameter the packet **must be enabled**. | | | |
| | | Verify Telemetry<br>**CpuRamWriteProt AEGU2050** | **= ENABLED** | AND=ZAA09999 | |
| | | | | | |
| 5 | | Enable write to ASW/BSW code and constants | | Next Step:<br>6 | |
| | | Uplink TC with **ARM GO** | | | |
| | | Execute Telecommand<br>**EnableCodeWrite**<br><br>*TC Control Flags :*<br>**GBM IL DSE**<br>**--Y -- ---**<br>*Subsch. ID : 20*<br>Det. descr. : Enable write to ASW/BSW code and constants | **AC804070** | **TC** | |
| | | | | | |
| 6 | | Verify final status of CPU RAM write protection | | Next Step:<br>END | |
| | | **Note:**<br>Protection Enabled = Write access Disabled<br>Protection Disabled = Write access Enabled | | | |
| | | **Note:**<br>Note that the parameter CPU RAM write protection status (doughter of **DID_BSW_MEM_ACCESS**) is part of the **default ACC diagnostic packet** (**BSW1**); thus to acquire this parameter the packet **must be enabled**. | | | |
| | | Verify Telemetry<br>**CpuRamWriteProt AEGU2050** | **= DISABLED** | AND=ZAA09999 | |
| | | | | | |
| | | End of Sequence | | | |
| OCRP210F | | *TC Seq. Name :* OCRP210F ( DIS W ACC CPU RAM )<br>Disable write to ACC ASW/BSW code and constants<br><br>*TimeTag Type: N*<br>*Sub Schedule ID:* | | | |

Enable/Disable write to ACC ASW/BSW code and constants
File: C_CRP_OBS_2102.xls
Author: lstefanov-hp

| Step No. | Time | Activity/Remarks | TC/TLM | Display/ Branch | AIT Comment |
|---|---|---|---|---|---|
| 7 | | Manual Stack manipulation<br>Load command sequence OCRP210F on top of the Manual Stack | | Next Step:<br>8 | |
| | | | | | |
| 7.1 | | Sequence data<br><br>FP: N/A<br>TT: N/A | | | |
| | | | | | |
| 8 | | Verify initial status of CPU RAM write protection | | Next Step:<br>9 | |
| | | **Note:**<br>Protection Enabled = Write access Disabled<br>Protection Disabled = Write access Enabled | | | |
| | | **Note:**<br>Note that the parameter CPU RAM write protection status (doughter of **DID_BSW_MEM_ACCESS**) is part of the **default ACC diagnostic packet** (**BSW1**); thus to acquire this parameter the packet **must be enabled**. | | | |
| | | Verify Telemetry<br>**CpuRamWriteProt AEGU2050** | **= DISABLED** | AND=ZAA09999 | |
| | | | | | |
| 9 | | Disable write to ASW/BSW code and constants | | Next Step:<br>10 | |
| | | Uplink TC with **ARM GO** | | | |
| | | Execute Telecommand<br>**DisableCodeWrite**<br><br>*TC Control Flags :*<br>**GBM IL DSE**<br>**--Y -- ---**<br>*Subsch. ID : 20*<br>Det. descr. : Disable write to ASW/BSW code and constants | **AC802070** | **TC** | |
| | | | | | |
| 10 | | Verify final status of CPU RAM write protection | | Next Step:<br>END | |
| | | **Note:**<br>Protection Enabled = Write access Disabled<br>Protection Disabled = Write access Enabled | | | |
| | | **Note:**<br>Note that the parameter CPU RAM write protection status (doughter of **DID_BSW_MEM_ACCESS**) is part of the **default ACC diagnostic packet** (**BSW1**); thus to acquire this parameter the packet **must be enabled**. | | | |
| | | Verify Telemetry<br>**CpuRamWriteProt AEGU2050** | **= ENABLED** | AND=ZAA09999 | |
| | | | | | |
| | | End of Sequence | | | |

Enable/Disable write to ACC ASW/BSW code and constants
File: C_CRP_OBS_2102.xls
Author: lstefanov-hp



| Step No. | Time | Activity/Remarks | TC/TLM | Display/ Branch | AIT Comment |
|---|---|---|---|---|---|
| | | **End of Procedure** | | | |