

Enable/Disable write to CDMU ASW/BSW code and constants
 File: C_CRP_OBS_1102.xls
 Author: Liviu Stefanov



Procedure Summary

Objectives

This Herschel and Planck common OBSM contingency procedure is used to Enable or Disable the write access to the CDMU ASW/BSW code and constants (i.e. write access to CPU RAM). The write access via TC(6,2) or TC(8,4,7,1) is enabled/disabled.

Note: The write access to CDMU CPU and COCOS registers or EEPROM can be Enabled/Disabled using procedure C_CRP_OBS_1100.

Summary of Constraints

n/a

Spacecraft Configuration

Start of Procedure

CDMU in operational mode
 - Write access to CDMU CPU RAM Enabled or Disabled

End of Procedure

CDMU in operational mode
 - Write access to CDMU CPU RAM Disabled or Enabled

Reference File(s)

Input Command Sequences

Output Command Sequences

OCRP110E
 OCRP110F

Referenced Displays

ANDs **GRDs** **SLDs**
 ZAD51999

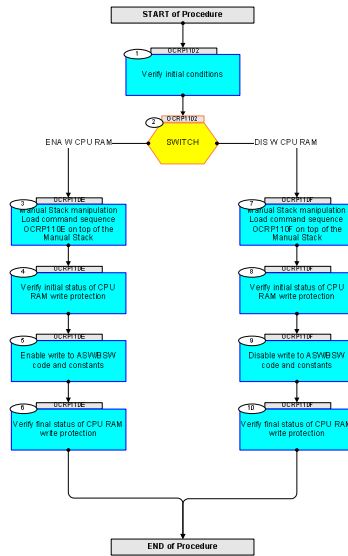
Configuration Control Information

DATE	FOP ISSUE	VERSION	MODIFICATION DESCRIPTION	AUTHOR	SPR REF
30/01/08	1	1	Created	lstefanov-hp	

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Procedure Flowchart Overview



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Step No.	Time	Activity/Remarks	TC/TLM	Display/ Branch	AIT Comment
Beginning of Procedure					
OCR1102		TC Seq. Name :OCR1102 (ENA/DIS W CPU RAM) Enable/Disable write to CDMU ASW/BSW code and constants TimeTag Type: Sub Schedule ID: <input type="checkbox"/>			
1		Verify initial conditions		Next Step: 2	
		Check: - CDMU in operational mode - ENA/DIS status of write access to CDMU ASW/BSW code and constants (write to CPU RAM)			
1.1		Check CDMU in operational mode			
1.2		Check write protection status			
		Note: Note that the parameter CPU RAM write protection status (daughter of DID_BSW_MEM_ACCESS) is part of the default CDMU diagnostic packet (BSW1) ; thus to acquire this parameter the packet must be enabled .			
		Note: Following TM check assumes write access to CPU and COCOS registers and EEPROM is Disabled .			
		Verify Telemetry <div style="display: flex; justify-content: space-between; width: 100%;"> CpuRamWriteProt DELOH160 = ENABLED </div>		AND=ZAD51999	
2		SWITCH type: [Switch]		Next Step: ENA W CPU RAM 3 DIS W CPU RAM 7	
End of Sequence					
OCR110E		TC Seq. Name :OCR110E (ENA W CDMU CPU RAM) Enable write to CDMU ASW/BSW code and constants TimeTag Type: N Sub Schedule ID: <input type="checkbox"/>			
3		Manual Stack manipulation Load command sequence OCR110E on top of the Manual Stack		Next Step: 4	

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Step No.	Time	Activity/Remarks	TC/TLM	Display/ Branch	AIT Comment
End of Procedure					