Document Type: SPECIFICATION

HASI DPU SOFTWARE

USER REQUIREMENTS DOCUMENT

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DOCUMENT CHANGE RECORD

ISSUE	DATE	TOTAL PAGES	PAGES AFFECTED	DESCRIPTION OF MODIFICATIONS
1 Draft	Oct 91	--	ALL	General description
2 Draft	Nov 91	--	ALL	Small changes
3 Draft	May 92	--	--	Changes after EPDR
4 Draft	May 93	--	ALL	First draft version after DELTA EPDR of 1/2 March 1993
5 Draft	June 93	--	--	Added OP MODES definition. Added HW I/F spec. (draft); PPI req. still missing
6 Draft	02/07/93	--	--	Lat Draft Issue before freezing of version 1.0
7 Draft	14/10/93	--	--	Updated after PARIS Meeting of 8-9 Jul 1993.
1	07/10/93		ALL	Updated after Progress Meeting in OG sept. 1994
2	20/09/94			OG Working copy - red line copy of Issue 1
3	Oct 94			OG Working copy - red line copy of Issue 2
4	14/12/94	225	ALL	Updated for memory size optimization and for add RAE requirements; ACC, PPI and PWA req. changes agreed with CO'Is
5	03/01/95	210	ALL	Updated after Meeting held in Padua the 15/12/94; the modifications are agreed with PI.
6	01/06/95	201	SOME	Update after CDR (March 95) and system test.
7	30/09/95		18,34,35, 130,142-147	EEPROM override capability.
			29,50,124,136 ,137	Entry worst_case.
			53,113, 182,184-189	Typewriter errors.
			55,57-59, 125,133, 176,179-181	Software testing.
			60,61,64,65	PROM default values.

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1. INTRODUCTION

1.1 PURPOSE

The purpose of this document is to specify all the users' requirements for the HASI experiment that are capable of being implemented by DPU on board software.
They include experimenters' requirements (scientific source) as well as system requirements (OG source).

This document is produced during the User Requirements definition phase of the software life cycle defined in ESA PSS-05-0 issue 2. It shall be the basis for the production of HASI-DPU Software Requirements Document.

The structure and function breakdown within this document is based on the functions identified for HASI in EID part A and part B documents.

1.2 SCOPE

This document shall be the baseline for all the HASI DPU software activities.

It shall constitute the only reference for the specification of each functionality to be accomplished by HASI-DPU-SW unless expressly specified.

Each applicable user requirement shall be identified by a unique requirement identification label in the form:

URD-<section number>-<requirement number>-<need>

where
<section number> refers to this document numbering
<requirement number> refers to this document numbering
<need> may be omitted for essential requirement
may be "N" or "N.E." for not essential requirement

1.3 DEFINITIONS, ACRONYMS and ABBREVIATIONS

HASI : Huygens Atmospheric Structure Instrument

DPU : Data Processing Unit of HASI experiment

HASI-DPU-SW : Hasi experiment on board sw residing on the DPU master processor

PPI : Pressure Profile Instrument

TEM : Temperature sensors instrument

PWA : Permittivity and Wave Altimeter

ACC : Accelerometers instrument

CDMS/U : Command and Data Management System/Unit

BCP : Broadcast pulse

OG : Officine Galileo

ESA : European Space Agency

EID : Experiment interface document

URD : (Software) User Requirement Document

PRL : Probe Relay Link

AIV : Assembly and Integration Verification

H/C : Health Check

HK : Housekeeping

SW : Software

HW : Hardware

TM : Telemetry

TC : Telecommand

ML : Memory load

DDBL : Descent Data Broadcast List

MCA : Magnetic Coil Actuator

PIFS : Probe Interface Simulator

ADC : Analog to Digital Converter

EPDH : OG elec. modules only (CPU, A/D, CDMS, DC/DC Conv. and MB)

SB : Status Block Message

C/O : Checkout

CRC : Cyclic Redundance Check

FMI : Finnish Meteorological Institute

RAE : Radar Altimeter Extension

1.4 REFERENCES

1.4.1 APPLICABLE DOCUMENTS

AD-1 "ESA Software Engineering Standards issue 2" ESA-PSS-05-0 issue 2

AD-2 "HASI Software Project Plan issue 1" HASI-PL-OG-004

AD-3 "Huygens EID part A issue 1 rev 3" EID-A

AD-4 "HASI EID part B Issue 1 rev 1" EID-B

AD-5 "PWA Specification issue 2" HASI-SP-LPCE-001

AD-6 "TEM Specification issue 2" HASI-SP-UFT-001

AD-7 "PPI Specification issue 3" HASI-SP-FMI-001

AD-8 "ACC Specification issue 2" HASI-SP-UKC-001

AD-9 MoM HASI-EPDR 3-5 sept 91 OG

AD-10 MoM HASI-PWA 25/26 sept 91 Gratz

AD-11 "DBS Specification issue 2" HASI-SP-SSD-001

AD-12 MoM HASI Design Report 2/3 Dec 91 OG

AD-13 Mom HASI delta EPDR 2/3 Mar 93 OG

AD-14 Mom HASI delta EPDR splinter meetings 4 Mar 93

AD-15 Mom HASI progress meeting (splint) 5/6 May 93

AD-16 ECR-07: Radar Altimeter

1.4.2 REFERENCED DOCUMENTS

RD-1 "Huygens system specification issue 02" HUY.AS/c.100.SY.0043

RD-2 "Huygens PDR system design report issue 01" HUY.AS/c.100.RE.00106

1.5 OVERVIEW

The HASI experiment will lay on experiment platform of the Huygens Titan Probe that is in turn part of the Cassini orbiter (see FIG. 1/2). The Probe consists of a descent module enclosed by a decelerator and an aft cover (see FIG. 3).

The Cassini spacecraft will be launched from Cape Canaveral air Force Station in October 1997; arrival at Saturn will occur in November 2004.

Before Titan encountering, the Probe will be spun up and separated form the Orbiter; Then the Probe will approach and enter the Titan atmosphere. During the Entry in the Titan atmosphere, HASI will achieve its primary scientific objective of the Cassini mission for the study of the Titan atmosphere by means of the acceleration profile yield by ACC sensor data.

After the entry in the Titan atmosphere, at an altitude of approximately 170 Km and a speed of about Mach 1.5, a mortar deploys a drogue parachute that pulls off the aft cover and inflates the main parachute; after a short period the decelerator is separated and falls away. The Descent then continues under the main parachute.

After 15 minutes the main parachute is released and the Probe is stabilized by a small drogue chute as it falls to the surface. Descent profile is shown in fig. 5/6.

During this descent, by several sensors, ranging from accelerometers and temperature sensors to pressure and electric field sensors, it shall collect and relay back to the Probe CDMS information about the vertical structure of the atmosphere as the Huygens Probe descends. (See FIG. 4)

The HASI operations shall be driven by mission information periodically provided by the Probe CDMS and shall be in accordance a predefined mission programme. It shall operate depending on mission altitude and time as well as on occurring of predefined events.

HASI experiment will return to Probe CDMS telemetry scientific and housekeeping data according to the single experimenters' requirements and to the available Probe Relay Link bit rate.

During CRUISE or GROUND operations HASI activities shall be driven by the Probe CDMS by means of a set of predefined commands able to carry out periodic health check functionality (e.g. sw uploading, device health-checks, calibrations or more complex test session).

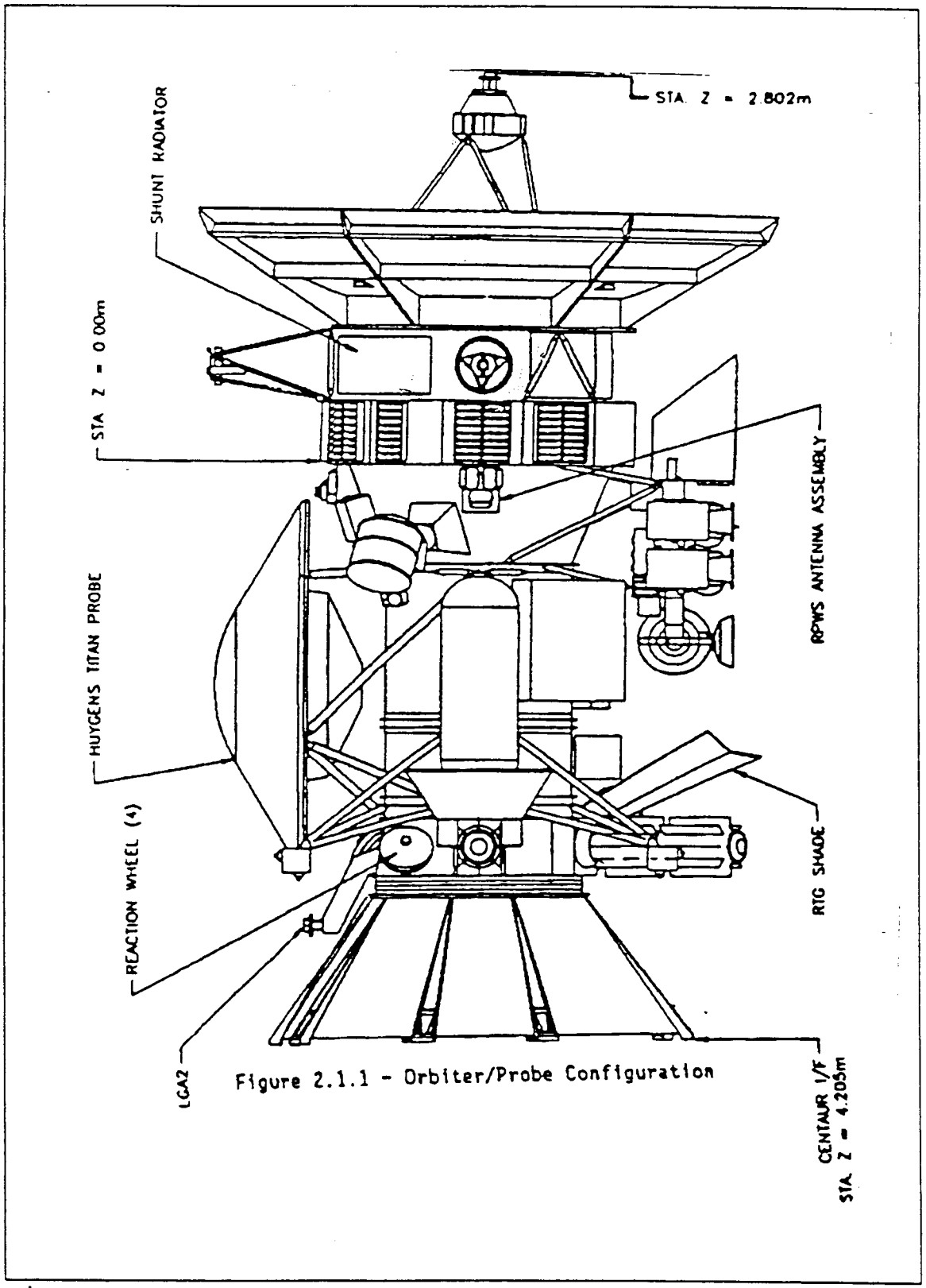


Figure 2.1.1 - Orbiter/Probe Configuration

Figura 1 : CASSINI ORBITER

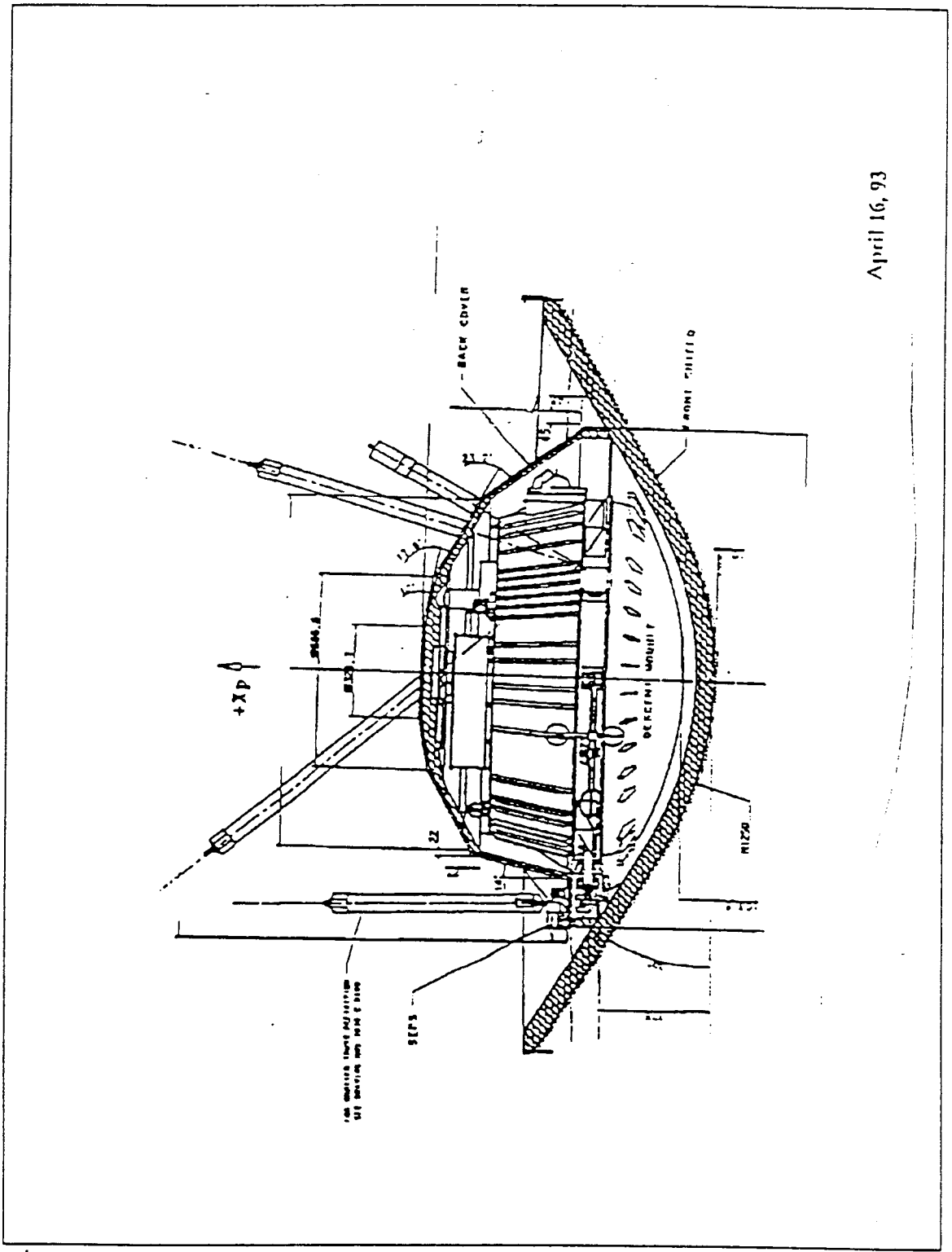


Figura 2 : HUYGENS TITAN PROBE

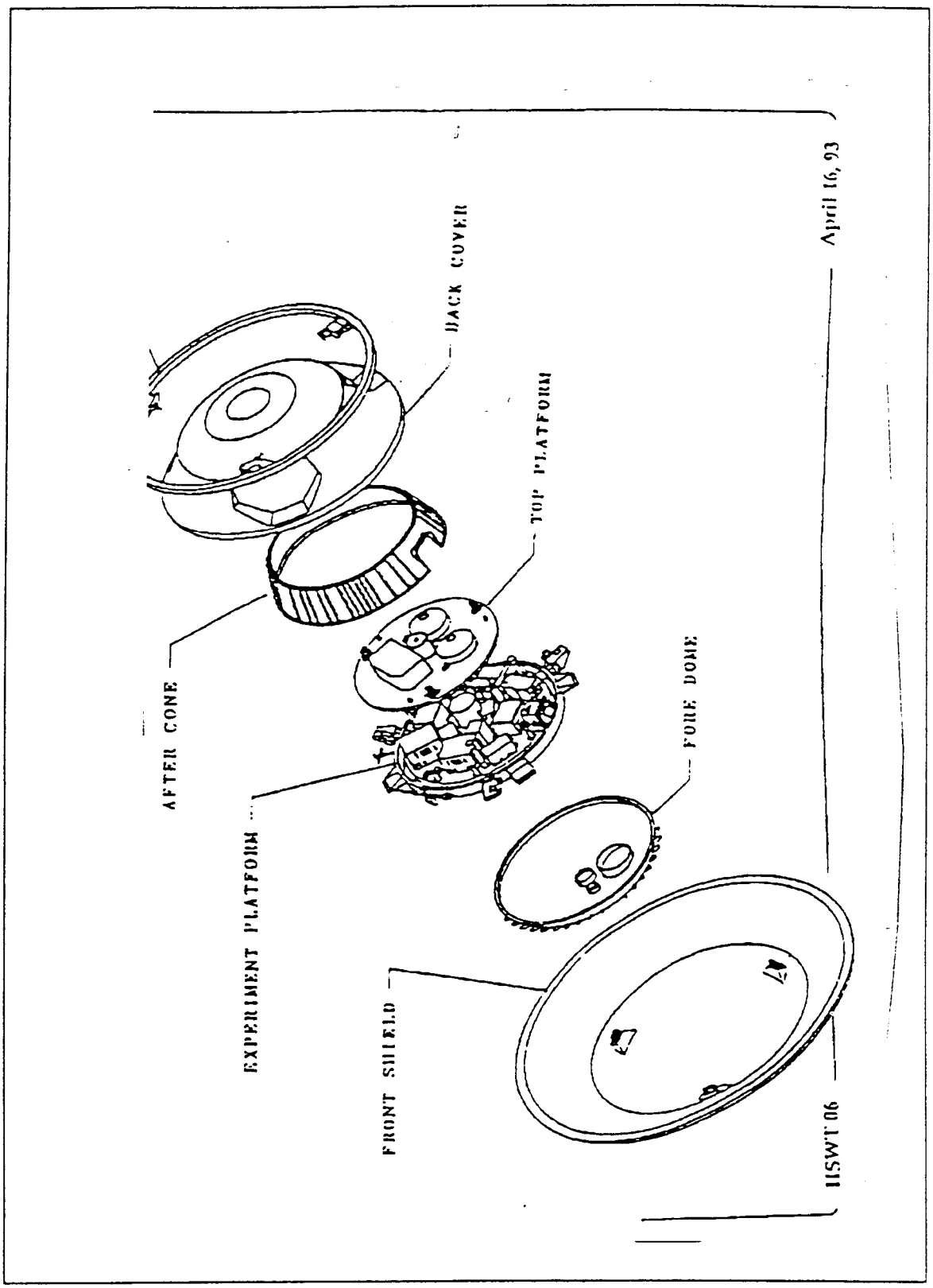


Figura 3 : PROBE SYSTEM CONFIGURATION

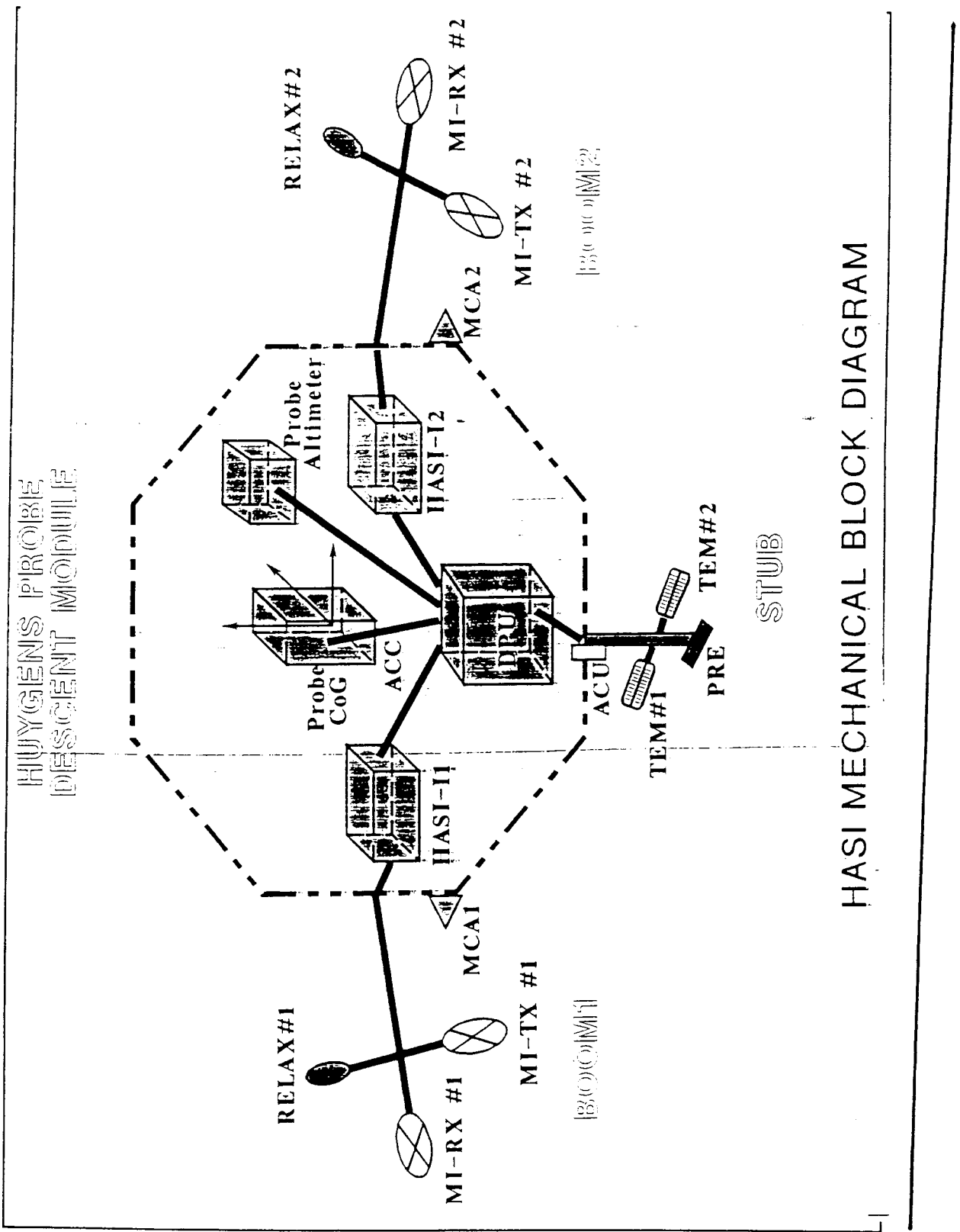


Figura 4 : HASI CONFIGURATION

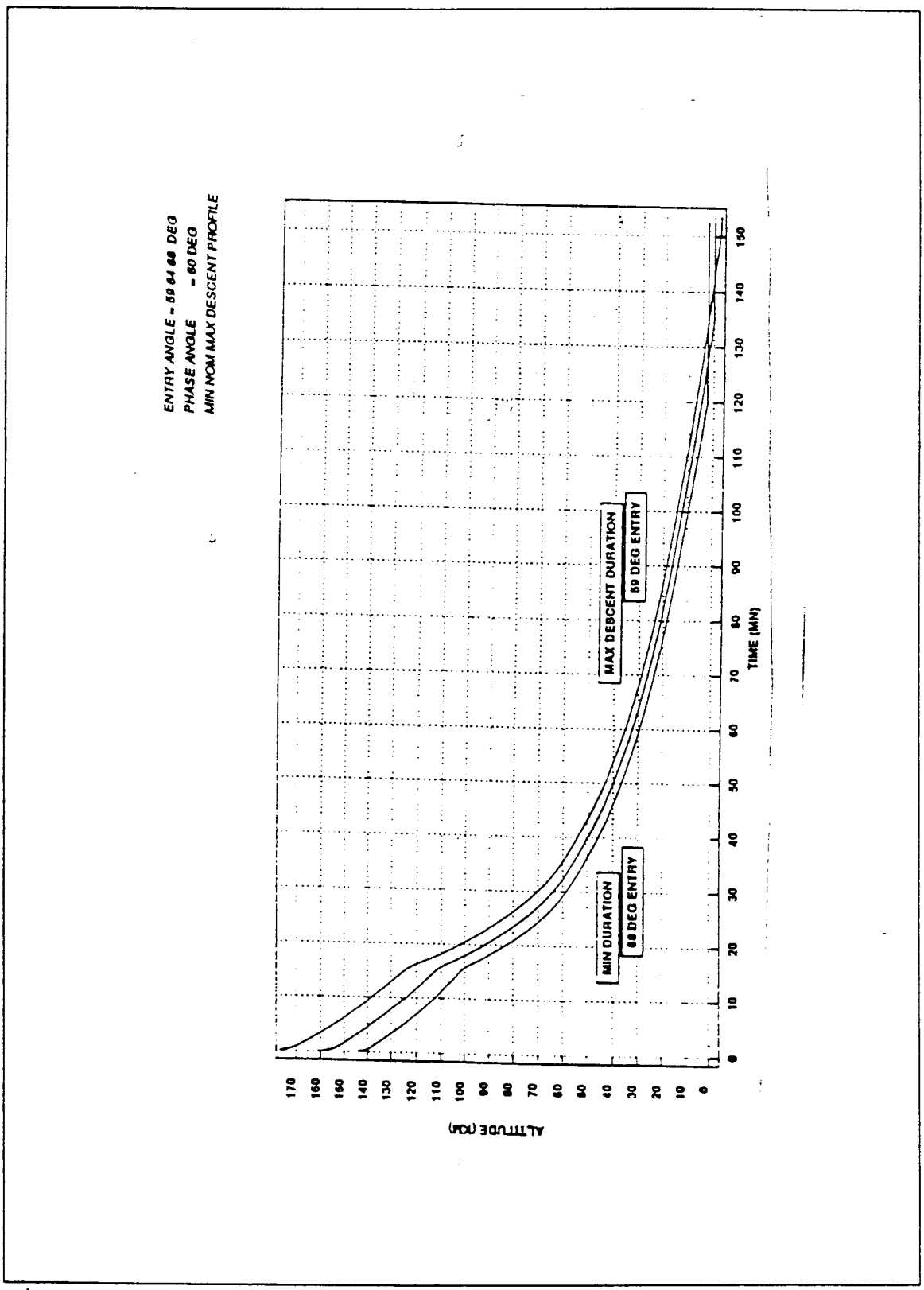


Figura 5 : DESCENT PROFILE

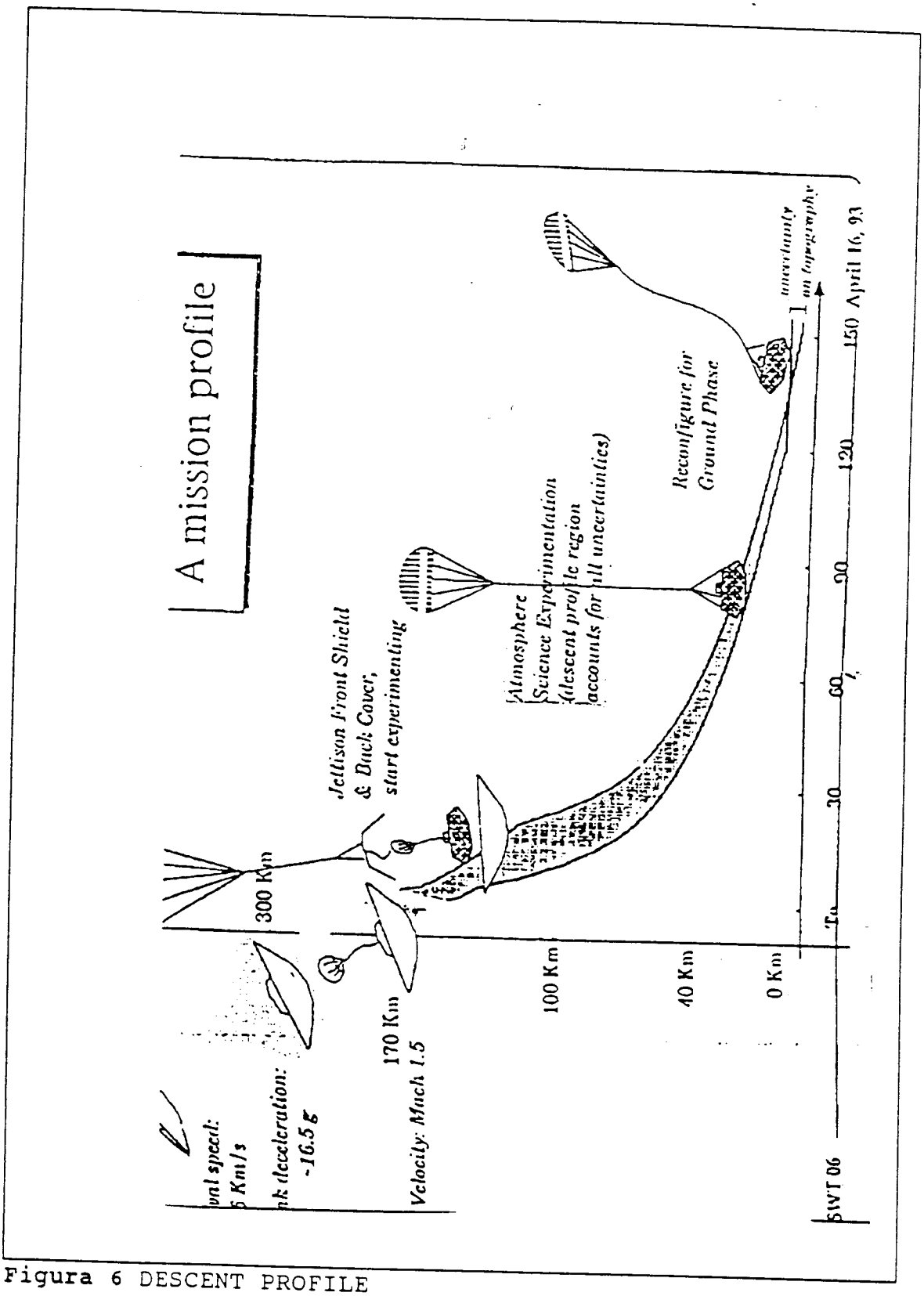


Figura 6 DESCENT PROFILE

2. GENERAL DESCRIPTION

2.1 PRODUCT PERSPECTIVE

GENERAL DESCRIPTION

The HASI program flight software is executed by one microprocessor that is part of the DPU.
It is linked to the CDMS and collects science data measurements from the connected sensors by means of an ADC converter plus a dedicated interface for pressure data.

A Digital Signal Processor (DSP) performs and controls the measurements and the experiments of the PWA. The DSP is linked to the main processor via a parallel interface; its flight software is considered embedded in the component itself.

The collected science data are transferred to CDMS via ESA Standard Telemetry packets.

START UP

After reset (caused by power-on or by unwanted events like SEU) the microprocessor begins its start-up activities that consist of health checks, initialization and warm-up of devices, EEPROM lookup for code or parameters updates which, after an integrity check, shall be loaded in the processor RAM.
To avoid HASI deadlock due to the code parameters loaded into the EEPROM, HASI has the capability to override the EEPROM content itself.
For instance using a combination of DDBL info (SPIN rate value equal to maximum and phase = CHECKOUT), the HASI-DPU-SW skips the EEPROM loading and then, via TC, the EEPROM will be overridden.

The results of these start-up activities shall be reported to CDMS through dedicated TM packets and summarized in the STATUS WORD register.

After successful startup the HASI-DPU-SW shall check the occurring of DDBL packets upon the Memory Load interface.

Back-up modes shall be foreseen in order to recovery from start-up failures and DDBL absence.

HASI OPERATIONS

The HASI-DPU-SW decides which CDMU channel to use by means of reading the CDMS PROCESSOR VALID line and assessing the correctness of received DDBL packets.

As soon as good DDBL packets are received, the concerning MISSION phase (or operative mode) is entered.

The HASI-DPU-SW shall recognize the operative modes by means of the DDBL information and perform its mission profile according to the broadcasted mission time.

Two operative modes phases shall be recognized by the HASI-DPU-SW: CHECKOUT (i.e. simulated descent) and TITAN DESCENT.

TELECOMMAND OPERATIONS

During the CHECKOUT phases (e.g. simulated descent) HASI may receive telecommands coming from ground via CDMS together with the DDBL messages.

When a Telecommand is received the CHECKOUT FUNCTION is suspended for the time necessary to carry out the pertained Telecommand and report results by means of dedicated Telemetry packets. Upon completion HASI shall restart the suspended function according to the most recent DDBL and shall be ready to execute a new telecommand.

As exception to above written, few special Telecommands are performed in a fraction of time and don't cause CHECKOUT function to be suspended.

Special policies shall be implemented in order to avoid deadlocks of Telecommand operations.

Commandable checkout functions shall comprehend reset of the DPU, health checks, dumping and replacing of DPU memory locations (RAM or EEPROM), dispatching of test commands to the PWA slave processor.

NOTE: The use of Telecommands after LAUNCH shall be restricted to special investigations or recovery actions.

ENTRY/DESCENT OPERATIONS

Starting with reception of valid DDBL and mission flag indicating ENTRY/DESCENT and after Tacc (expressed in DDBL time), HASI-DPU-SW shall perform continuous measurements of the Accelerometers.

The measurements shall be stored till 1.5 min after Tdata instant for later transfer to CDMS as the PROBE-ORBITER data link is not available in this time interval.

One minute after the T0 instant, according to the "protected energize" time window, the HASI-DPU-SW shall attempt to release the booms devices by means of two repetitions of MCA activation bursts.

After TdataH up to recognition of "proximity of impact" time the micro executes a loop during which accelerometers, temperature, pressure and PWA signals are sampled and on-line processed by peculiar algorithms; the modality of each one changes according to the evolution of the mission time and phases.

When the "proximity of impact" event is recognized by the DPU, the internal accelerometers are gated for the purpose of triggering the real impact instant.

After real impact up to the end of the mission (Tloss) the program keeps on collecting surface measurements and transferring them to CDMS.

Health check results are periodically transmitted to CDMS via Telemetry packets and summarized in the STATUS WORD register.

2.2 USER CHARACTERISTICS

HASI SCIENTIFIC OBJECTIVES

The primary scientific objectives of the Cassini mission for the study of Titan are summarized in the ESA/NASA report on the Phase A study as:

1) Determine abundances of atmospheric constituents (including any noble gases); establish isotope ratios for abundant elements; constrain scenarios of formation and evolution of Titan and its atmosphere.

2) Observe vertical and horizontal distributions of trace gases; search for more complex organic molecules; investigate energy sources for atmospheric chemistry; model the photochemistry of the stratosphere; study the formation and composition of aerosol.

3) Measure winds and global temperatures; investigate cloud physics, general circulation and seasonal effects in Titan's atmosphere; search for lightning discharges.

4) Investigate the upper atmosphere, its ionization , and its role as a source of neutral and ionized material for the magnetosphere of Saturn.

The scientific objectives of the Huygens Atmospheric Structure Instrument (HASI) are:

a) Determine the density pressure and temperature conditions corresponding to the higher part of the atmosphere during the entry phase. Of particular interest is the determination of the physical condition in this region where the "detached" haze, observed by Voyager, is formed.

b) Measure the stratospheric density, T, P profile of the stratosphere during the descent phase and identify the composition in these layers in terms of trace constituents which condense in this part of the atmosphere. Interpret any data which may suggest the existence of clouds in the upper troposphere.

c) Measure P,T in the lower troposphere and determine the existence and extent of a convective zone.

d) Determine (in case of survival after impact), the nature of the surface.

e) Determine the atmospheric electric conductivity and investigate ionization processes, wave electric fields and atmospheric lightning. Detect acoustic noise due to turbulence and thunders. Characterize electric properties, conductivity and permittivity of the surface material.

f) Determine the surface large scale and small scale topography, the surface dielectric properties and in particular to be able to remotely distinguish between a liquid or a solid surface before impact. If the surface is liquid information on surface winds may be obtained. All data are measured along the ground track of the descending probe due to horizontal winds during the last 30 Km.

The pressure (PPI), temperature (TEM) sensors and the accelerometers (ACC) address the points (a-d). They will provide the pressure, temperature and density profiles along the path of the Huygens Probe in the Titan atmosphere.

The accelerometers will also measure the shock at the impact and in the case of Probe survival the pressure and temperature sensors will give the surface environmental conditions.

The Permittivity and Wave Altimeter (PWA) will address points e) and f).

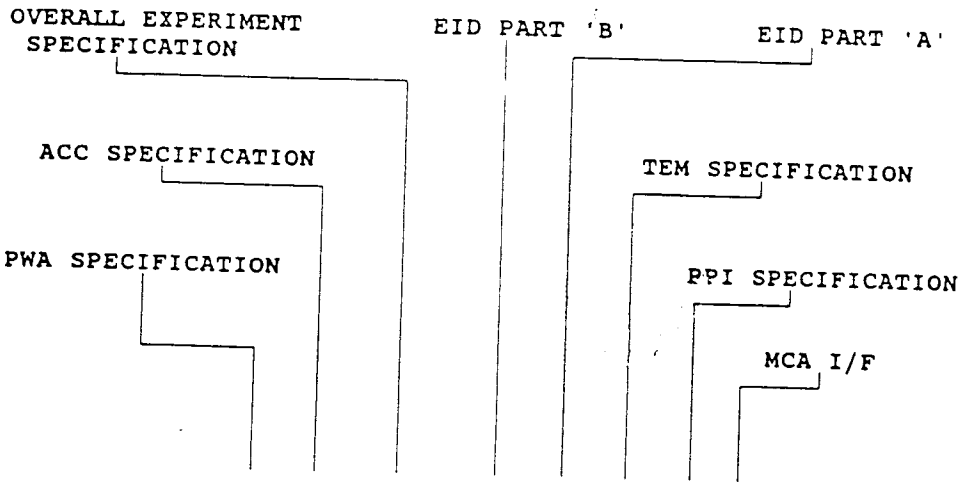
2.3 GENERAL CONSTRAINTS

General constraints affecting the realization of the HASI DPU SW are :

- limited size of memory (32Kb ROM, 64Kb RAM)
- absence of co-processors
- complexity of PROM-EEPROM-RAM program dynamical relocation and self-checking
- complexity of CDMS HW/SW interface
- several sensors HW/SW interfaces
- limited telemetry data rate budget.

2.4 ASSUMPTION AND DEPENDENCIES

SPECIFICATION TREE



HASI DPU SOFTWARE USER REQUIREMENT

2.5 OPERATIONAL ENVIRONMENT

The HASI-DPU-SW shall be a hard constrained real time embedded Software.

Hard deadlines are foreseen for some functions.

It shall reside on PROMs laying on a microprocessor based electronic board of the HASI DPU box located on the Probe experiment platform (see FIG. 3)

The HASI DPU SW shall interact with the external devices by means of dedicated interface (see FIG.4/7/8/9), they are :

- CDMS interface
- PWA interface
- ACC interface
- PPI interface
- TEM interface
- MCA interface

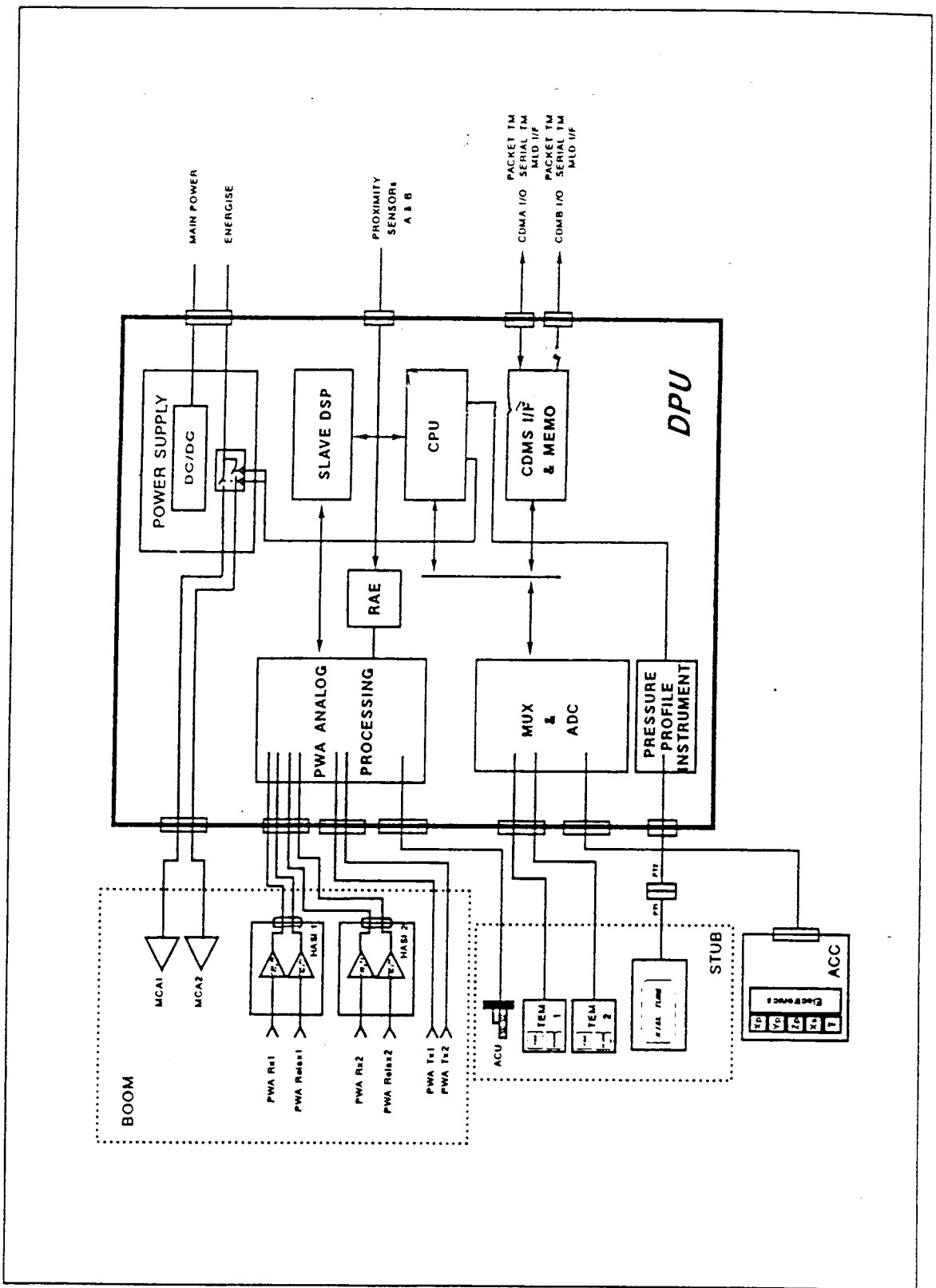


Figura 7 : HASI FUNCTIONAL DIAGRAM

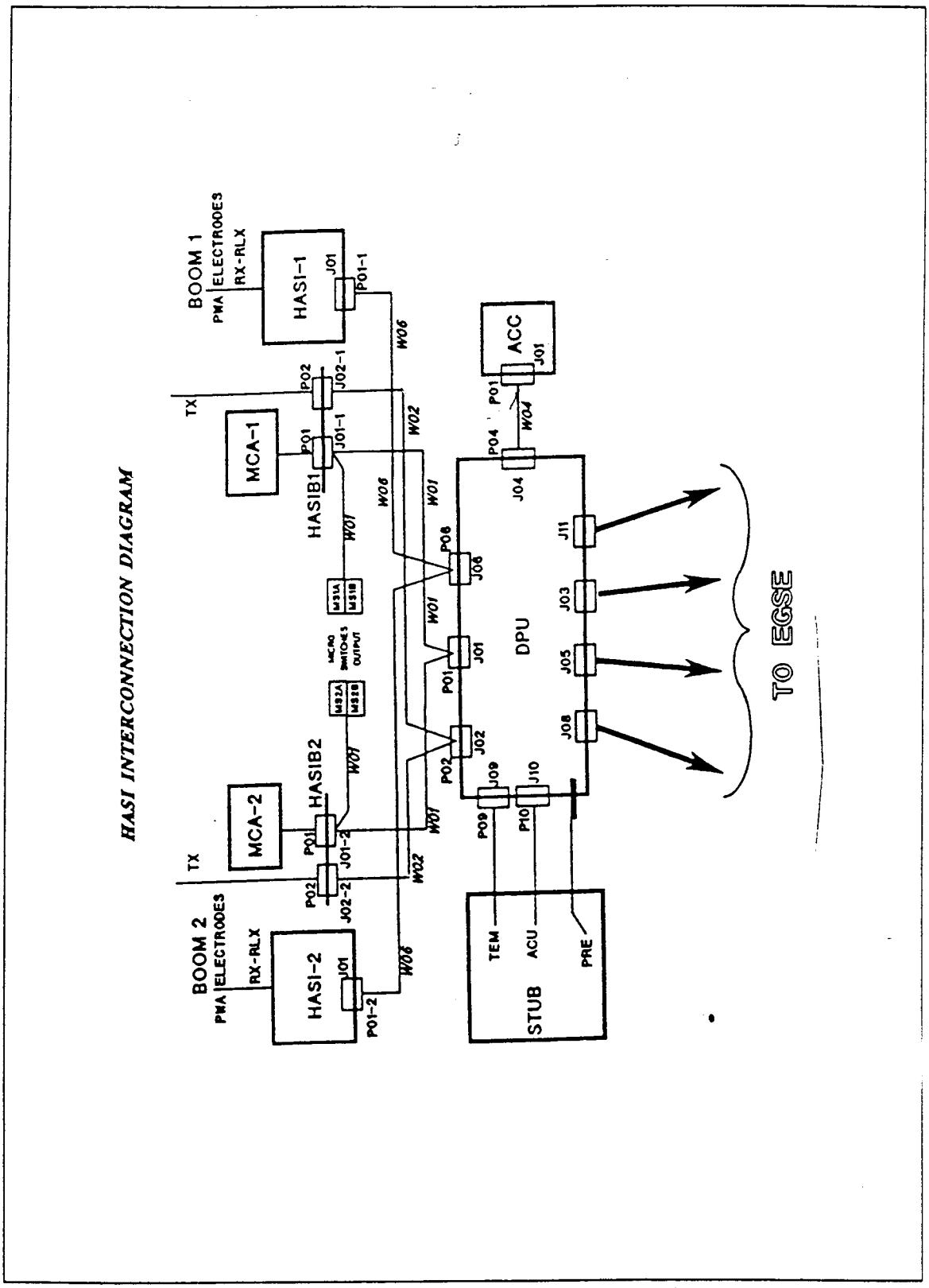


Figura 8 : HASI INTERCONNECTION BLOCK DIAGRAM

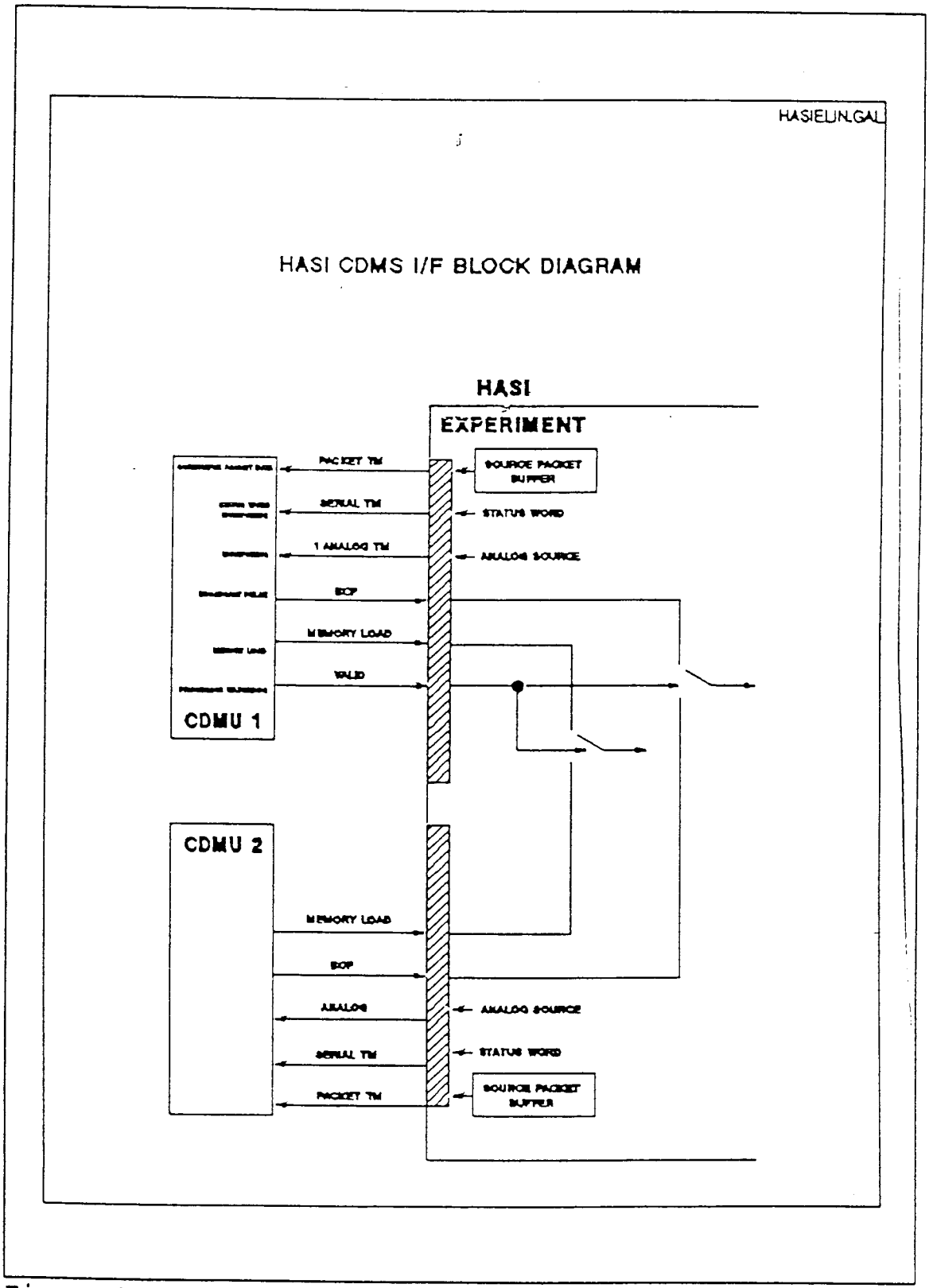


Figura 9 : HASI EXPERIMENT INTERFACE

3. SPECIFIC REQUIREMENTS

3.1 CAPABILITY REQUIREMENTS

3.1.1 MISSION DEFINITION

The HASI mission definition is based upon the Huygens mission that is divided into two major phases.

- PRE-SEPARATION phases (Checkout Operations)
- POST-SEPARATION phases (Titan Mission)

After the HASI AIV is completed and before the Launch, HASI shall be considered in GROUND phase.
The CRUISE phase starts at the Cassini spacecraft earth escape and ends with the Probe Separation from the Orbiter. Its nominal duration is 7 years.
Once approximately each six months during this phase, HASI shall be powered on to execute periodical health-checks and then powered off.
These health-checks activities shall be a subset of already carried out GROUND activities.
During the CHECKOUTS phases, the HASI-DPU-SW on board SW shall be capable to execute a CHECKOUT procedure (nominally a simulated descent) using CDMS DDBL information.
When commanded by the Probe CDMS the HASI-DPU-SW shall be capable to execute a set of special checkout functions.

PRE-SEPARATION phases shall comprise:

- GROUND C/O
- GROUND C/O SUSPENDED
- GROUND C/O DEACTIVATED

- FLIGHT C/O
- FLIGHT C/O SUSPENDED
- FLIGHT C/O DEACTIVATED

After the Probe separation, some minutes (Tentry-5min) before the entry in the Titan atmosphere, HASI shall be powered on and the DDBL information received (the DDBL is broadcasted even before HASI is on). The HASI-DPU-SW then, shall recognize the Titan descent initiation and perform the predefined functions related to each POST-SEPARATION phase.

POST-SEPARATION phase shall comprise the TITAN DESCENT.

UR-3.1.1-1 : The above mission phases shall be recognized by HASI-DPU-SW on the basis of the following DDBL information :

PHASE	DDBL INFO
TITAN DESCENT	phase=0000 0000 binary
GROUND	phase=0000 0011
GROUND SUSPENDED	phase=0000 1100
GROUND DEACTIVATED	phase=0000 1111
FLIGHT	phase=1111 0011
FLIGHT SUSPENDED	phase=1111 1100
FLIGHT DEACTIVATED	phase=1111 1111

UR-3.1.1-2 : GENERAL MISSION TIMELINE

Here follows a definition of mission sequence by events and time.

EVENT TIME	EVENT NAME	EVENT DESCRIPTION
-TBD years	Launch	Start CRUISE phase
-TBD years	----	FLIGHT checkouts
-TBD days	----	Pre-separation checkouts
-22 days	Tsep	Probe separation
0:00	Tp (-18 min to T0)	Probe activation
8:00	**Thasi** (-10 min to T0) (Tentry-5min)	Hasi activation (STARTUP phase)
+11:00	----	(start ENTRY phase)
+11:30	Tacc	Start sampling ACC
+13:00 min (estimated)	Tentry	Entry in the atmosphere
+18:00	DDBL Time reset	
0:00	T0	Mortar firing
+ 0:01	-----	Parachute deployment
+ 0:55	-----	Protected energize on
+ 1:00	---- **Td1** Tdata	(start DESCENT 1st phase) **1st Boom release try** Probe Relay Link activ.
+ 1:55	------	2nd HASI Power on
+ 2:20	**Td2**	**2nd Boom release try**
+ 2:30	**TdataH**	(start DESCENT 2nd phase)
+ 3:25	Teoff	Protected energize off
+ 10:00	Tswitch	Switch packet allocation
+ 32 (*)	Tradar	(start DESCENT 3rd phase)
+ 133 min (estimated based on nominal profile		Last Kilometer (start IMPACT phase)
+119 min	**Tproximity**	**Start IMPACT phase when HASI is in BACKUP mode** (i.e. DDBL absence)
+135 min (estimated)	**Timpact**	**Surface touch down** (start SURFACE phase)
+TBD min	Tloss	Loss of radio link (END OF MISSION)

NOTE: Td2 must be greater than 2nd HASI power on time plus the time necessary to the startup function.

(*) this time corresponds to T_A + 32 min (T_A is the arming time, that appens few seconds before T0).

3.1.2 HASI-DPU-SW OPERATIVE MODES

UR-3.1.2-1 : According to the mission events and phases and DDBL information, the HASI-DPU-SW shall address the following observable modes and states depicted here after :

MODE	SUBMODE	STATE
STARTUP	n.a.	n.a.
TITAN DESCENT	NOMINAL/BACKUP	ENTRY/DESCENT1/DESCENT2/DESCENT3/IMPACT/SURFACE
CHECKOUT	NOMINAL/BACKUP	ENTRY/DESCENT1/DESCENT2/DESCENT3/IMPACT/SURFACE
TELECOMMAND EXECUTION	NOMINAL/BACKUP	ENTRY/DESCENT1/DESCENT2/DESCENT3/IMPACT/SURFACE

UR-3.1.2-2 : The following events shall cause the HASI-DPU-SW to change mode :

- Power-on/reset
- Only at STARTUP the DDBL phases information or DDBL reception error
- Executable Telecommands
- Reset Telecommand

The following events shall cause the HASI-DPU-SW to change state inside an operational mode :

- Mission time evolution (T0, Tdata, TdataH, Tradar)
- Altimeter information
- Impact detection

The mode changes are specified in the following table and in FIG 10.

The following events shall cause the HASI-DPU-SW to change submode inside an operational mode:

- DDBL reception errors
- BCP timeout (refers to 3.1.8-2)

The state changes are detailed inside each operative mode specification.

\ dest. source\	STARTUP	TITAN DESCENT	CHECKOUT	TELECOMMAND EXECUTION
STARTUP	- Power on reset	- STARTUP DDBL test = TITAN DESCENT	- STARTUP DDBL test = CHECKOUT	//
TITAN DESCENT	- Power on reset	//	//	//
CHECKOUT	- Power on reset - reset TC	//	//	-Executable Telecommand
TELECOMMAND EXECUTION	- Power on reset - reset TC	//	- end of telecommand execution	//

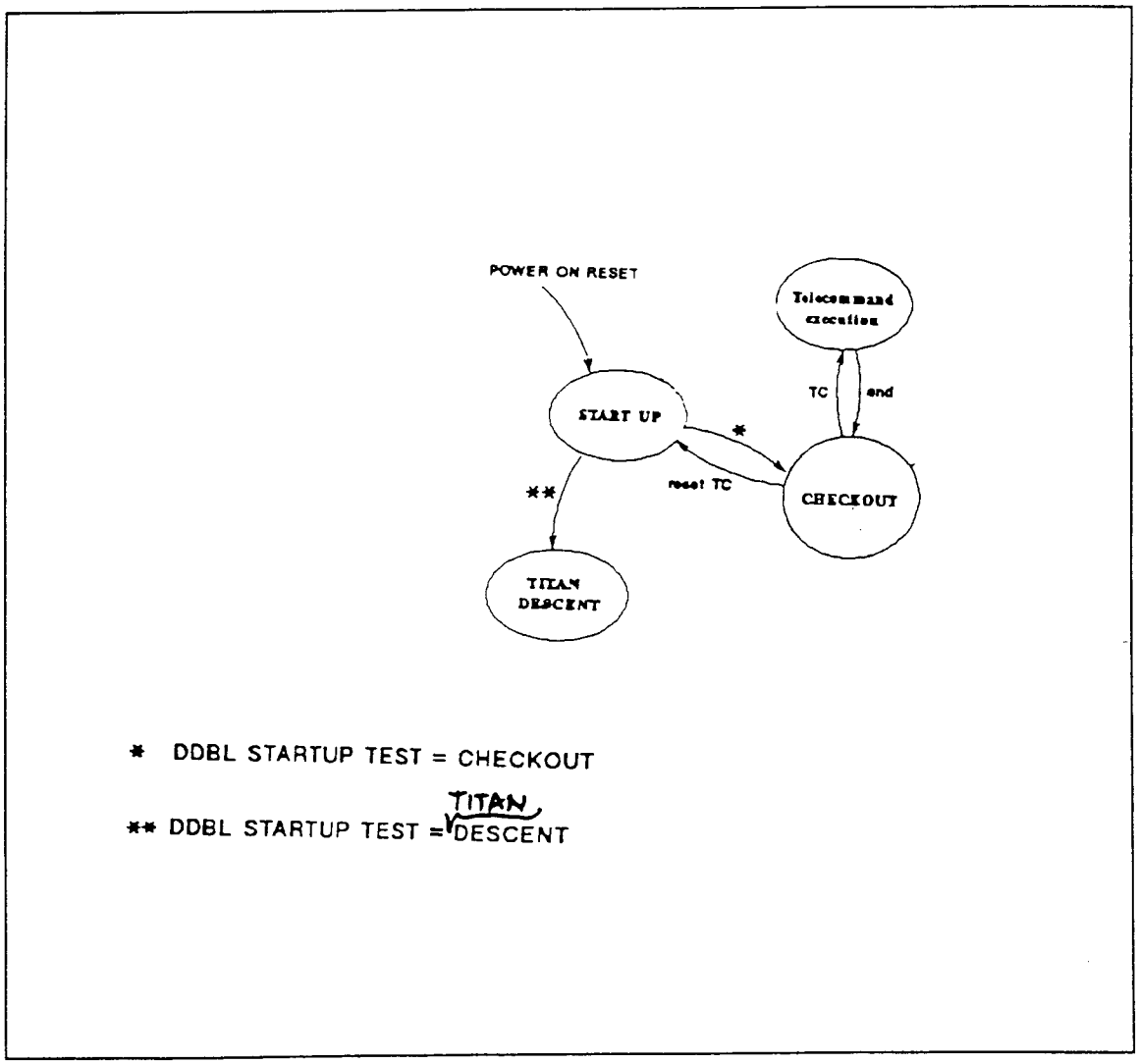


Figura 10 DPU OPERATIVE MODES

UR-3.1.2-3 : STARTUP MODE ENTRY

As soon as the Power on reset or RESET telecommand is performed, the HASI-DPU-SW shall enter the STARTUP MODE and execute as specified in chapter 3.1.3.

UR-3.1.2-4 : TITAN DESCENT MODE ENTRY

UR-3.1.2-4.1 : After the STARTUP DDBL TEST of UR-3.1.3-2.1 results DESCENT mode the HASI-DPU-SW shall enter the TITAN DESCENT MODE and execute its mission program specified in chapter 3.1.4 driven by the DDBL information.

UR-3.1.2-4.2 : In case of no correct reception of the DDBL, from both channels, within **PAR1** (default PROM value = 3) **minutes** since power on reset HASI-DPU-SW shall consider to be in TITAN DESCENT MODE/BACKUP STATE and execute its mission program specified in chapter 3.1.4 driven by the internal MISSION time.
(see STARTUP DDBL TEST UR-3.1.3-2.1)

UR-3.1.2.4-3 : As soon as the TITAN DESCENT MODE is initiated, no other mode shall be taken in account by HASI-DPU-SW. (i.e. only power off-on shall restart the HASI-DPU-SW).

UR-3.1.2-5 : CHECKOUT (GROUND or FLIGHT) MODE ENTRY

After the STARTUP DDBL TEST of chapter 3.1.3 results CHECKOUT mode the HASI-DPU-SW shall start executing the CHECKOUT PROCEDURE as specified in chapter 3.1.5

UR-3.1.2-6 : DELETED.

UR-3.1.2-7 : TELECOMMANDS EXECUTION MODE
(special checkout functions)

Telecommands use after the HASI AIV shall be foreseen only for contingency situation, while intensive use could be made during or before the AIV phase.

Telecommands shall be foreseen to be of two main classes according to their impact on the CHECKOUT PROCEDURES :

- EXECUTABLE TELECOMMANDS that conflict for mission resources and require a HASI-DPU-SW operative mode change

- SETUP COMMANDS that do not require HASI-DPU-SW operative mode change

The detail of each Telecommand is specified in chapter 3.1.7.

UR-3.1.2-7.1 : EXECUTABLE TELECOMMANDS

When the HASI DPU receives an EXECUTABLE TELECOMMAND, the present checkout procedure is suspended for the duration of the performing Telecommand.

The HASI internal status together with the results of the CHECKOUT FUNCTION are sent back by means of dedicated TM packets according to chapter 3.1.10.

At the end of the telecommand execution the HASI-DPU-SW shall restart the suspended checkout function and shall be ready to execute a new TC.

UR-3.1.2-7.2 : SETUP TELECOMMANDS

When HASI receives a SETUP TELECOMMAND, the pertained function is performed in a fraction of time (e.g. PWA test) without observable interruption of the running CHECKOUT procedure (i.e. NO HASI-DPU-SW MODE CHANGE)

UR-3.1.2-8 : The operative mode and status of the HASI-DPU-SW shall be uniquely identified by a bit pattern in the STATUS WORD (according to 3.2.2.1).

3.1.3 STARTUP MODE

UR-3.1.3-1 : At soon as the CPU reset is performed the following activities shall be carried out :

- electronic devices WARM-UP of 300 msec is performed
- STATUS WORD bit #15 is set
- LOOK UP of possible reset cause (watch dog,reset TC, self reset due to program failure condition)
- load in RAM the PROM DEFAULT value of each UPLOADABLE item (tasks, functions and parameters)
- EEPROM test sequence
- clearing of all HW interfaces of chapter 3.2 (specially set MUX 2 on GND channel)
- set ACC range switch = FINE (Highest resolution)
- set STATUS WORD bit 14 to 1
- initialize internal HASI-DPU-SW MISSION TIME

UR-3.1.3-1.1 : EEPROM test sequence

UR-3.1.3-1.1.1 : EEPROM loocked:

a- check the DDBL presence in both CDMU lines.

b- check the received DDBLs

c- in case of DDBLs corrupted (wrong CRC) or timeout (No DDBLs for a time greather than 14 sec), the HASI-DPU-SW shall load the EEPROM into RAM as per UR-3.1.3-1.1.2

d- in case of DDBLs info with TITAN/DESCENT flag or (FLIGHT/GROUND) CHECKOUT with SPIN rate $\neq$ 0xFF, the HASI-DPU-SW load the EEPROM into RAM as per UR-3.1.3-1.1.2

e- only in case of three DDBLs that show (FLIGHT/GROUND) CHECKOUT with SPIN rate = 0xFF, the HASI-DPU-SW shall skip the activity of UR-3.1.3-1.1.2.
This case will be reported by means of an EVENT and shall be sent to ground via EVENT DATA packet.

UR-3.1.3-1.1.2 : The EEPROM loading sequence shall be the following:

a- EEPROM switch ON.

b- search "EEPROM formatted" information (i.e. PARAMETER UPDATE BLOCK) and verify the CRC for each block.

c- if the CRC is correct fill the RAM area with image contained in the EEPROM block.

d- send a Startup Report (one for each EEPROM item) even if the CRC is computed.

e- EEPROM switch OFF.

UR-3.1.3-1.1.2.1 : EEPROM formatted blocks shall be designed in order to allow the following SW maintenance operations:

- update/substitute of tables/parameters.

- correction/substitution of HASI-DPU-SW functions except the BOOM release.

UR-3.1.3-1.2 : DELETED

UR-3.1.3-2 : The following HEALTH CHECKS shall be performed

a- ADC1 3.2 Khz + DMA synchronization check

b- DDBL STARTUP TEST of correctness (UR-3.1.3-2.1)

Failures shall be reported by means of an EVENT and shall be sent to ground via EVENT DATA packet.

UR-3.1.3-2.1: The DDBLs coming from both channels shall be examined starting with the channel as determinated by the PROCESSOR VALID signal to determine the HASI-DPU-SW operative mode to be entered according to the following table:

(DDBL channel A, DDBL channel B) --> HASI-DPU-SW MODE

DDBL B / DDBL A	ENTRY/DESCENT flag	CHECKOUT flag	RECEPTION NOK
ENTRY/DESCENT flag	**TITAN DESCENT MODE**	**TITAN DESCENT MODE**	**TITAN DESCENT MODE**
CHECKOUT flag	**TITAN DESCENT MODE**	**CHECKOUT MODE**	**CHECKOUT MODE**
RECEPTION NOK	**TITAN DESCENT MODE**	**CHECKOUT MODE**	**TITAN DESCENT MODE (*)**

(*) : see UR-3.1.2-4.2

UR-3.1.3-3 : DELETED

UR-3.1.3-4 : DELETED

UR-3.1.3-5 : The startup activities defined from UR-3.1.3-1 to 4 shall be performed within 2 CDMS cycle, i.e. 32 sec.

UR-3.1.3-6 : The Housekeeping activities of chapter 3.1.8 shall be started as soon as possible.

3.1.4 TITAN DESCENT MODE

UR-3.1.4-1 : When in TITAN DESCENT MODE the following 6 states (mission phases) shall be recognized and operated by HASI-DPU-SW according to the evolving mission information :

- ENTRY: until Tdata
- DESCENT 1st PHASE: until TdataH
- DESCENT 2nd PHASE: until Tradar
- DESCENT 3rd PHASE: until Tproximity (in case BACKUP)
  until last kilometer (in case NOMINAL)
- IMPACT: Altitude < 1Km or after Tproximity
- SURFACE: after impact detected by ACC.

UR-3.1.4-2 : There shall be two different way of driving the TITAN DESCENT thus leading to two different SUBMODES :

- NOMINAL MODE in which all the activities shall be driven by the DDBL information
- BACKUP MODE in which (because of incorrect DDBL or BCP) all activities shall be driven by DPU internal clock.

UR-3.1.4-3 : ENTRY PHASE

HASI will be powered on shortly **(at Thasi)** before the entry of the Probe into Titan atmosphere.

The HASI ENTRY phase starts after the Startup completion, just before the entry of the Probe into the Titan atmosphere and ends at the nominal instant of PRL activation **(Tdata)**, 1 minute after the activation of the descent devices (mortar firing at **T0** instant). Its nominal duration is 11 minutes.

The HASI DPU SW shall execute its Entry phase mission programme:

- start ACC sampling after Tacc
- routing DDBL info to PWA and collect the PWA packets in accordance with requirements UR-3.1.14-2
- continuous acquire and buffer of time stamped ACC data according to chapter 3.1.11
- housekeeping functions as per chapter 3.1.8.
- create and enqueue time-stamped TM packets with data from above activities
- preliminary transmission of TM packets (according to CDMS polling rate) without discarding from the queue.

UR-3.1.4-4 : DESCENT 1st PHASE
(before TdataH instant)

This subphase starts soon after the nominal PRL activation instant **(Tdata instant)** and ends 90 seconds after (TdataH instant = T0+2.5 min). Its nominal duration is 90 sec.

The HASI-DPU-SW shall execute its DESCENT 1st phase mission programme:

- sampling and time stamp of ACC, TEM, PPI science and HK data according to TM packet allocation scheme of 3.1.10
- perform 1st and the 2nd booms release attempt by means of MCA activation bursts according to chapter 3.1.15
- housekeeping functions as per chapter 3.1.8
- routing DDBL info to PWA and collect the PWA packets in accordance with requirements UR-3.1.14-2
- create and enqueue time-stamped TM packets with data from above activities
- preliminary transmission of TM packets (according to CDMS polling rate) without discarding from the queue.

UR-3.1.4-5 : DESCENT 2nd PHASE
(after TdataH instant until Tradar)

This subphase starts soon after the **TdataH instant** and ends at **(Tradar instant)**. Its nominal duration is 29.5 minutes.

The HASI-DPU-SW shall execute its DESCENT 2nd phase mission programme:

- sampling and time stamp of ACC, TEM, PPI science and HK data
- routing DDBL info to PWA and collect the PWA packets in accordance with requirements UR-3.1.14-2
- housekeeping functions as per chapter 3.1.8
- create and queue time stamped TM packets with data from above activities and from PWA data packets
- restart transmission of TM packets (acquired during ENTRY and DESCENT 1st phase) according to CDMS polling rate with queue-discarding.

UR-3.1.4-6 : DESCENT 3rd PHASE
(after Tradar)

This subphase starts soon after the **Tradar instant** and ends at the recognition of the proximity of the impact. Its nominal duration is 101 minutes.

The HASI-DPU-SW shall execute its DESCENT 3rd phase mission programme:

- sampling and time stamp of ACC, TEM, PPI science and HK data
- routing DDBL info to PWA and collect the PWA packets in accordance with requirements UR-3.1.14-2
- housekeeping functions as per chapter 3.1.8
- create and queue time stamped TM packets with data from above activities and from PWA data packets
- transmission of TM packets according to CDMS polling rate
- synchronization with CDMS and recognition of Proximity of impact

UR-3.1.4-6.1: The determination of Proximity of the impact shall be performed as follows :

if the DDBL is OK the proximity of impact shall occur when the measured or predidected altitude (in DDBL) indicates **the last Km** otherwise

if the DDBL is absent the proximity of impact shall occur when 119 minutes are elapsed since T0. (i.e. the shortest mission profile is considered the worst case)

UR-3.1.4-7 : IMPACT PHASE

This subphase starts at the recognition of the proximity of the impact, ends at the recognition of the impact **(Timpact instant)** by analysis of ACC data. Its nominal duration is 2 minutes.

The HASI-DPU-SW shall execute its IMPACT phase mission programme:

- sampling and time stamp of ACC, TEM, PPI science and HK data
- routing DDBL info to PWA and collect the PWA packets in accordance with requirements UR-3.1.14-2
- housekeeping functions as per chapter 3.1.8
- create time stamped TM packets with data from above activities
- determine Timpact instant by processing on-line of ACC Xservo data
- create time stamped TM packets of ACC impact frames as detailed in chapter 3.1.11
- transmission of TM packets according to CDMS polling rate

N.E. UR-3.1.4-7.1: The ACC requirements at IMPACT (i.e. UR-3.1.11-9) shall reside in EEPROM area and shall be loaded in RAM at START-UP; the default PROM value for the ACC requirements at IMPACT shall performe the ACC activities as in DESCENT 3rd phase (i.e. UR-3.1.11-8) (**NOT ESSENTIAL**)

UR-3.1.4-8 : SURFACE PHASE

This subphase starts soon after the recognition of the impact event **(Timpact instant)** and never ends but keep on until battery power is exhausted or telemetry link is loss **(Tloss instant)**. Its nominal duration is 30 minutes max.

During this phase the software shall perform the same activities of **UR-3.1.4-6** (DESCENT 3rd PHASE) execpt for **UR-3.1.4-6.1**.

NOTE: HASI SURVIVAL AFTER IMPACT IS NOT CERTAIN.

3.1.5 CHECKOUT MODE

UR-3.1.5-1 : After the DDBL STARTUP TEST results checkout the HASI-DPU-SW shall start executing the predefined CHECKOUT PROCEDURE (i.e. the simulated descent) identical to the TITAN DESCENT MODE functions except the MCA activation of chapter 3.1.15 shall never be performed.

UR-3.1.5-2 : DELETED

UR-3.1.5-3 : DELETED

UR-3.1.5-4 : DELETED

UR-3.1.5-5 : During the CHECKOUT MODE HASI-DPU-SW shall be able to accept and execute Telecommands as defined in chapter 3.1.7; after the execution the interrupted CHECKOUT PROCEDURE shall be restarted.

3.1.6 SHUTDOWN MODE: DELETED

3.1.7 TELECOMMANDS MANAGEMENT

UR-3.1.7-1 During the CHECKOUT phases the HASI-DPU-SW shall be able to execute, if correctly received, telecommands outlined here after:

- SOFT RESET
- PWA TEST
- TEST MODE
- DUMP MEMORY
- LOAD HASI MEMORY

UR-3.1.7-2 Each Telecommand shall comply to ESA-PSS-04-107 Telecommand Packet Standard.

The general Telecommands protocol is defined in EID part A document sect. 3.6.3.6-1, while detail of each Telecommand layout is defined in HASI-IDS.

UR-3.1.7-3 Each Telecommand received during a different mission phase from CHECKOUT shall be ignored.

The dedicated error bit # 6 of the STATUS WORD shall be updated according to chapter 3.2.2.1 and left unchanged until the next telecommand is received or the DPU is reset.

UR-3.1.7-4 Each Telecommand incorrectly received (i.e. not in compliance with specifications of UR-3.1.7-2) shall be ignored and the event shall be recorded in the MISSION HISTORY LOG FILE.

The dedicated error bit # 6 of the STATUS WORD shall be updated according to chapter 3.2.2.1 and left unchanged until the next telecommand is received or the DPU is reset.

UR-3.1.7-5 Telecommands sent before the completion of another Telecommand shall be ignored.

The dedicated error bit # 6 of the STATUS WORD shall be updated according to chapter 3.2.2.1 and left unchanged until the next telecommand is received or the DPU is reset.

UR-3.1.7-6 As soon as a telecommand is successfully received:

- the error bit # 6 of the STATUS WORD shall be updated according to chapter 3.2.2.1;
- a TC echo TM packet shall be sent to both channel with highest priority;
- the pertaining functions shall be performed as detailed hereafter according to the command header (function number).

UR-3.1.7-6.1 **SOFT RESET**

- wait at least 18 sec after its reception
- restart the program from bootstrap leaving the watch_dog to reset the DPU.

UR-3.1.7-6.2 **PWA TEST COMMAND**

The PWA Test Command Number received is inserted in the dedicated "socket" (PWA TEST PARAM) of the next STATUS BLOCK to be transmitted to PWA.

SIMULATED DESCENT shall not be affected.

UR-3.1.7-6.3 **TEST MODE**

This command shall be used to health check the Memory Load lines TM lines and Status Word:

the HASI-DPU-SW shall be set/reset the STATUS WORD bit # 5 according to the command argument.

UR-3.1.7-6.4 **DUMP MEMORY**

- The requested consecutive memory location are dumped according to chapter 3.2.5.2 into dedicated TM packets taken from science allocated ones (PWA science).
- The checkout mode (nominally SIMULATED DESCENT) shall not be interrupted until the command is finished.Then the SIMULATED DESCENT shall restart.

UR-3.1.7-6.5 LOAD HASI MEMORY

- The requested EEPROM, RAM locations (physical addresses) are loaded according to chapter 3.2.5.1
- Report of verified loaded locations is reported by means of 1 dedicated TM packet taken from science allocated ones (PWA science).
- The checkout mode (nominally SIMULATED DESCENT) shall not be interrupted.

UR-3.1.7-6.6 DELETED

UR-3.1.7-6.7 DELETED

UR-3.1.7-6.8 DELETED

UR-3.1.7-6.9 For each unknown command an event shall be recorded in the MISSION HISTORY LOG FILE.

3.1.8 HOUSEKEEPING (Periodical functions)

UR-3.1.8-1 : At a multiple of DDBL rate (nominally each 16 sec.) HASI-DPU-SW shall perform the following periodical functions (the HK TM bit allocation is reported in brackets) :

a- measure of DPU box internal temperature (16 bit)

b- health check of the DPU housekeeping voltages (1 bit)

c- updating of the following bit of the STATUS WORD

PWA link status
PPI frequency status
DPU internal temp
ACC internal temp
HASI-DPU-SW status
Protected Power presence

UR-3.1.8-2 : At DDBL rate (nominally each 2 sec.) HASI-DPU-SW shall perform the following periodical functions :

a- health check of BCP pulse rate (1 bit)

b- health check of PPI HC voltages range (2 bit)

c- health check of incoming DDBL (1 bit)

d- if last DDBL is not okay or BCP is not okay or VALID line has been swapped by CDMS then swap selected CDMU

e- if last DDBL was not okay shift DDBL rate HK activities (e.g. 1 BCP time duration) in order to ensure avoiding of self disturbing the ML and BCP line by CDMU swapping

f- if last BCP was not okay shift DDBL rate HK activities (e.g. 1/2 BCP time duration) in order to ensure avoiding of self disturbing the ML and BCP line by CDMU swapping

g- readout of MCA interface: Protected Power Presence, MCA1 status and MCA2 status (3 bit)

h- health check of PWA data link (1 bit)

i- health check of PPI frequency output line (1 bit)

j- ADC-2 correct working (1 bit)

k- XSERVO Range selection (1 bit)

l- PWA status: Science or Test (1 bit)

see also UR-3.1.9-2

UR-3.1.8-3 DELETED

UR-3.1.8-4 16 bit (1 word) shall be allocated for each 2 second HC report and collected in a dedicated TM packet.

UR-3.1.8-5 56 bit (7 bytes) shall be allocated for history log of not periodical event. Each event shall have a unique code number, 24 bit mission time, 8 bit Time Flag and an event data field and shall be collected in dedicated type of HK TM packet.

UR-3.1.8-5.1 Maximum 64 events for each event code number shall be possible.

UR-3.1.8-6 The total collected TM packets dedicated to HK shall not exceed the rate of 0.2 packet/cycle according to BIT RATE ALLOCATION table of chapter 3.1.10.

3.1.9 DESCENT DATA BROADCAST LIST

UR-3.1.9-1 : The HASI functions and mission time shall be always determined by the DDBL provided every 2 seconds by the CDMS through the ML I/F except :

UR-3.1.9-1.1 : Since the DPU HW allow reception of only one ML channel at a time, in case of incorrect reception of DDBL packets (because of the following rejection criteria) the HASI-DPU-SW shall base its functions upon the internal clock and shall record the event in the HK history LOG event FILE that shall be telemetred to Ground.

UR-3.1.9-1.2 : DDBL rejection criteria :

1) Reception timeout of 1 BCP duration.
2) Invalid Packet Format or invalid CRC.

NOTE : see UR-3.1.8-2

UR-3.1.9-2 : The DDBL layout (standard ESA TC packet) is defined in EID part A sect. 3.6 .
Its content are :

1) Time elapsed in two segments separated by a reset at T0 :
   - from CMDS turn-on to T0
   - from T0 to the end of mission
2) Altitude of the Probe
3) Spin rate of the Probe
4) Mission phases :
   - Entry-Descent
   - Ground checkout /active/suspended/deactivated
   - Flight checkout /active/suspended/deactivated

UR-3.1.9-3 : When the MISSION PHASE flags show the pattern for GROUND CHECKOUT (0000 0011) or FLIGHT CHECKOUT (1111 0011), the HASI-DPU-SW shall initiate the SIMULATED DESCENT, described in chapter 3.1.12, according to the MISSION TIME contained in the DDBL.
NOTE : during CHECKOUT modes DDBL parameters can take any value in order to allow to skip different time part of the mission to be simulated.

UR-3.1.9-4 : When the MISSION PHASE flags show the pattern for GROUND CHECKOUT SUSPENDED (0000 1100) or FLIGHT CHECKOUT SUSPENDED (1111 1100), the HASI-DPU-SW shall continue the SIMULATED DESCENT (with frozen time) until a TELECOMMAND or a new MISSION PHASE flag set.

UR-3.1.9-5 : When the MISSION PHASE flags show the pattern for GROUND CHECKOUT DEACTIVATE (0000 1111) or FLIGHT CHECKOUT DEACTIVATE (1111), the HASI-DPU-SW close and Tx all the HK EVENT LOG packets.

DDBL MISSION PHASES DEFINITION

MISSION PHASE	PATTERN (binary)
ENTRY/DESCENT - TITAN	0000 0000
GROUND CHECKOUT	0000 0011
GROUND CHECKOUT SUSPENDED	0000 1100
GROUND CHECKOUT DEACTIVATED	0000 1111
FLIGHT CHECKOUT	1111 0011
FLIGHT CHECKOUT SUSPENDED	1111 1100
FLIGHT CHECKOUT DEACTIVATED	1111 1111

3.1.10 TELEMETRY DATA MANAGEMENT

UR-3.1.10-1 : The HASI-DPU-SW shall communicate data to ground by means of Telemetry packet through the CMDS I/F depicted in chapter 3.2.2.2.

UR-3.1.10-2 : The used Telemetry packets shall comply to ESA-PSS-04-106 Telemetry Packet Standard.
The general protocol is defined in EID part A document section 3.6.3.7, while details of TM packets lay-out are defined in the HASI IDS.

UR-3.1.10-3 : There shall be up to 255 possible different TM data packets format: one for each data item to be transmitted as defined in HASI-IDS table "TELEMETRY PACKET DATA FORMAT".

UR-3.1.10-3.1 : Each data item to be transmitted has associated a predefined production rate and a bit allocation for produced item (resolution = 1 byte = 8 bits).

NOTE: The largest multiple of the bit allocation that fits in the 112 byte data field of the TM packet determines the utilization percentage of each TM packet.

UR-3.1.10-3.2 : The sum of all data item of the same source (DPU, ACC, TEM, PPI, PWA) must comply with the CDMS packet/cycle "HASI DATA RATE BUDGET" table shown hereafter.

NOTE: THE ALLOCATED RATE MUST BE CONVERTED IN A EQUIVALENT INTEGER NUMBER OF PACKET RATIO (e.g. 0.1 packet/cycle = 1 packet/160 seconds)

UR-3.1.10-3.3 : The data items contained in each TM packet shall be ordered in production chronological order and nominally result from periodical processing of periodical sampled raw data.

UR-3.1.10-3.4 : Each TM packet shall be time stamped with the processing instant of the first data item contained in the packet.
The accuracy of time is better than 125 msec (worst case).
Special TM packets like HOUSEKEEPING or STARTUP reports shall use event occurring or data creation time.

UR-3.1.10-4 : The TM packets shall be enqueued for transmission to CDMS according to their source with the following priorities (decreasing order) :

GROUP 1 : TC REPORTS / HK / ACC ENTRY / ACC IMPACT
GROUP 2 : TEM / PPI / ACC / PWA

UR-3.1.10-4.1 : All the TM packets shall be a single copy to be transmitted on both channel A and B except for PWA packets that it shall be different for both the two channels.

UR-3.1.10-5 : Telemetry transmission to CDMUs shall always be performed as follow:

1. until TdataH — Transmission is redundant
2. after TdataH — Transmission is nominal
3. in case of TC reception (while in CHECKOUT opmode of the HASI-DPU-SW) Tranmission shall be nominal until DPU reset.

UR-3.1.10-6 : DELETED

pitraenew.wk1 CASSINI HASI data rate budget - minimum allocation

Apr. 1995 - Proximity sensor ON at Ta+32' => Tradar= T0+32'

Timeline	T0-10'	T0-6'	T0+1'	T0+2.5'	T0+10'	T0+32'	T0+85'	T0+133'	T0+135'	T0+165'
	Thasi	Tacc	Tdata	Tdatah		Tradar		Tprox	Timp	Tloss
Altitude		1270,0	160,0		130,0	60,0	18,0	1,0	0,0	
time [min]	-10	-6	+1	+2.5	+10	+32	+85	+133	+135	+165
duration [min]	4,00	7,00	1,50	7,50	22,00	53,0	48,00	2,00	30,00	
worst-case cycles	16	27	6	29	83	199	181	8	113	
ACC [pack/cycle]	0,00	0,00	1,50	1,50	1,50	0,75	0,75	0,00	1,00	
Ch_A&B [pack/cycles]	0,00	0,00	3,00	3,00	3,00	1,50	1,50	0,00	2,00	
Ch_A&B [packets]	0,0	0,0	18,0	87,0	249,0	298,5	271,5	0,0	226,0	
extra packets	0,0	86,0	0,0	0,0	0,0	0,0	0,0	0,0	66,0	
total packets	0,0	172,0	18,0	87,0	249,0	298,5	271,5	0,0	358,0	
PRE [pack/cycle]	0,00	0,00	0,50	0,50	0,50	0,50	0,50	0,50	0,50	
Ch_A&B [pack/cycles]	0,0	0,0	1,0	1,0	1,0	1,0	1,0	1,0	1,0	
Ch_A&B [packets]	0,0	0,0	6,0	29,0	83,0	199,0	181,0	8,0	113,0	
TEM [pack/cycle]	0,00	0,00	0,50	0.50	0.50	0,50	0,50	0.50	0,50	
Ch_A&B [pack/cycles]	0,0	0,0	1,0	1,0	1,0	1,0	1,0	1,0	1,0	
Ch_A&B [packets]	0,0	0,0	6,0	29,0	83,0	199,0	181,0	8,0	113,0	
PWA [pack/cycle]	0,00	0,00	0,00	12,00	12,00	11,50	11,50	14,00	12,00	
RAE [pack/cycle]	0,00	0,00	0,00	0,00	0,00	2,00	2,00	2,00	0,00	
Ch_A&B [pack/cycles]	0,0	0,0	0,0	12,0	12,0	13,5	13,5	16,0	12,0	
CH_A&B [packets]	0,0	0,0	0,0	348,0	996,0	2686,5	2443,5	128,0	1356,0	
Hskp [pack/cyc]	0,20	0,20	0,20	0,20	0,20	0,20	0,20	0,20	0,20	
Ch_A&B [pack/cycles]	0,40	0,40	0,40	0,40	0,40	0,40	0,40	0,40	0,40	
Ch_A&B [packets]	6,4	10,8	2,4	11,6	33,2	79,6	72,4	3,2	45,2	
extra packets	3,0	3,0	3,0	0,0	0,0	0,0	0,0	0,0	0,0	
total packets	12	17	8	12	33	80	72	3	45	
science req. (1)	0,20	0,20	2,70	14,70	14,70	15,45	15,45	17,20	14,20	
Ch_A&B req. (1)	0,40	0,40	5,40	17,40	17,40	17,40	17,40	18,40	16,40	
total req.[pack]	12	189	38	505	1444	3463	3149	147	1985	
progr.req.[pack]	12	201	240	744	2188	5651	5338	5485	7323	
Alloc.[pack/cyc]										
Channel A	0	0	0	14	9	9	9	9	9	
Channel B	0	0	0	14	9	9	9	9	9	
Alloc. [pack]	0	0	0	812	1494	3582	3258	144	2034	
progr.all.[pack]	0	0	0	812	2306	5888	5564	5708	7742	
delta pack [r-a]	-12	-189	-38	307	50	119	109	-3	49	
prog. delta pack	-12	-201	-240	68	50	119	109	-3	46	

(%) 1 cycle every 16 seconds

3.1.11 ACC FUNCTIONAL REQUIREMENTS

UR-3.1.11-1 : The following ACC **RAW DATA** (from RD1 to RD7) shall be the base for the subsequent depicted processing. They shall be selected picking 1 each n from each ADC channel (sampled at nominally 400Hz, see ACC I/F) to obtain the following rates at least:

RD1.	Xservo LOW GAIN	12bit @100Hz	
RD2.	Xservo HIGH GAIN	12bit @100Hz	(n=4)
RD3.	Xpiezo	12bit @50Hz	(n=8)
RD4.	Ypiezo	12bit @50Hz	(n=8)
RD5.	Zpiezo	12bit @50Hz	(n=8)
RD6.	Temp1	12bit @1.5625Hz	(n=256)
RD7.	Temp2	12bit @1.5625Hz	

UR-3.1.11-2 : The following **SCIENCE DATA** shall be produced by means of block integration (sum of n consecutive samples) of N **RAW DATA** :

SCDSE.	best Xservo channel	16 bit	@3.125 Hz	N=32
	channel selection flag	1 bit	@3.125 Hz	
	Total	17 bit	@3.125 Hz	
SCDSD.	best Xservo channel	16 bit	@4.167 Hz	N=24
	channel selection flag	1 bit	@4.167 Hz	
	Total	17 bit	@4.167 Hz	
SCDSR.	best Xservo channel	16 bit	@1.754Hz	N=57
	channel selection flag	1 bit	@1.754Hz	
	Total	17 bit	@1.754Hz	
SCDPX.	Xpiezo value	16 bit	@1.6129Hz	N=31
SCDPY.	Ypiezo value	16 bit	@1.6129Hz	N=31
SCDPZ.	Zpiezo value	16 bit	@1.6129Hz	N=31

UR-3.1.11-3 : The following **HOUSEKEEPING DATA** shall be produced by means of block integration (sum of n consecutive samples) of N **RAW DATA** :

HKD1.	Sum of RD6 (Temp1)	16 bit	@0.097 Hz	N=16
HKD2.	Sum of RD7 (Temp2)	16 bit	@0.097 Hz	N=16

HKD2 shall be started half period (about 5 seconds) after HKD1.

UR-3.1.11-4 : The following **STATISTIC DATA** shall be produced from a different selection of 1 each n from each ADC channel according to the following scheme :

STD2. Is Sum of 128 samples picked 1 every 32 (i.e. 42 @12.5 Hz)

Xs : 24 bit (*) @0.1Hz
Xp : 24 bit (**) @0.1Hz
Yp : 24 bit (**) @0.1Hz
Zp : 24 bit (**) @0.1Hz

(*) 24 = 22 sum + 1 best + 1 spare

(**) 24 = 22 sum + 2 spare

UR-3.1.11-5 : DELETED

UR-3.1.11-6 : The following activities shall be performed since the Tacc=11.30 min DDBL time (during ENTRY phase) up to the Tdata instant for a maximum of 7.30 min = 450 sec :

a- Perform UR-3.1.11-1 + UR-3.1.11-2 + UR-3.1.11-3 + UR-3.1.11-4

b- Create less than 100 TM packets (of 112 data field each corresponding to a total of 11200 bytes) according to the following scheme :

1.	SCDSE : 450sec x 3.125Hz = 1407 samples	= 28	TMpack
2.	SCDPX : 450sec x 1.6129Hz = 726 samples	= 13	TMpack(*)
3.	SCDPY : same as above	= 13	TMpack(*)
4.	SCDPZ : same as above	= 13	TMpack(*)
5.	STD2.Xs : 450sec x 0.1Hz = 45 samples	= 2	TMpack(**)
6.	STD2.Xp : same as above	= 2	TMpack(**)
7.	STD2.Yp : same as above	= 2	TMpack(**)
8.	STD2.Zp : same as above	= 2	TMpack(**)
9.	HKD1 : 450sec x 0.1Hz = 45 samples	= 1	TMpack
10.	HKD2 : 450sec x 0.1Hz = 45 samples	= 1	TMpack
	Total data production	= 77	Tm packets

c- Enqueue the above 77 TM packets for redundant transmission to CDMS.

(*) each piezo packet has 52 samples
(**) each STD2 has 37 samples

UR-3.1.11-7.1 : The following shall be performed during DESCENT 1st phase up to the DESCENT 2nd phase: since Tdata instant till TdataH instant (nominally from T0+1 to T0+2.5 for total 1.5min = 90sec) :

a- Perform UR-3.1.11-1 + UR-3.1.11-2 + UR-3.1.11-3 + UR-3.1.11-4

b- Create TM packets of ACC data (at the rate of 1.5/CDMS cycle corresponding to 10.5 byte/sec = 84 bit/sec) composed of the following items :

1. SCDSD : 17bit x 4.167Hz	= 70.84	bit/sec
2. STD2 : 96bit x 0.1Hz	= 9.6	bit/sec
3. HKD1 : 16bit x 0.1Hz	= 1.6	bit/sec
4. HKD2 : 16bit x 0.1Hz	= 1.6	bit/sec
Total data produced	= 83.64	bit/sec
Total produced packets	= 8	

c- Enqueue the above packets for redundant transmission to CDMS

UR-3.1.11-7.2 : The following shall be performed during DESCENT 2nd phase up to the DESCENT 3rd phase: since TdataH instant till Tradar instant (nominally from T0+2.5 to T0+32 for total 29.5min = 1770sec) :

a- Perform UR-3.1.11-1 + UR-3.1.11-2 + UR-3.1.11-3 + UR-3.1.11-4

b- Create TM packets of ACC data (at the rate of 1.5/CDMS cycle corresponding to 10.5 byte/sec = 84 bit/sec) composed of the following items :

1. SCDSD : 17bit x 4.167Hz = 70.84 bit/sec
2. STD2 : 96bit x 0.1Hz = 9.6 bit/sec
3. HKD1 : 16bit x 0.1Hz = 1.6 bit/sec
4. HKD2 : 16bit x 0.1Hz = 1.6 bit/sec

Total data produced = 83.64 bit/sec

c- Enqueue the above packets for transmission to CDMS

UR-3.1.11-8 : The following shall be performed during DESCENT 3rd phase up to the IMPACT phase: since Tradar instant till Proximity of impact (nominally from T0+32 to T0+133 for total 101min = 6060sec) :

a- Perform UR-3.1.11-1 + UR-3.1.11-2 + UR-3.1.11-3 + UR-3.1.11-4

b- Create TM packets of ACC data (at the rate of 0.75/CDMS cycle corresponding to 5.25 byte/sec = 42 bit/sec) composed of the following items :

1. SCDSR : 17bit x 1.754Hz = 29.82 bit/sec
2. STD2 : 96bit x 0.1Hz = 9.6 bit/sec
3. HKD1 : 16bit x 0.1Hz = 1.6 bit/sec
4. HKD2 : 16bit x 0.1Hz = 1.6 bit/sec

Total data produced = 42.62 bit/sec

c- Enqueue the above packets for transmission to CDMS

UR-3.1.11-9 : The following shall be performed during the IMPACT phase : since Tproximity instant till Timpact instant (nominally from T0+133 to T0+135 for total 2min = 120sec) :

a- Perform UR-3.1.11-1

b- Store the 6 sec trace of the impact [Timpact-0.5sec, Timpact+5.5sec] containing the following **IMPACT TRACE DATA** selected picking 1 each n from each ADC channel (sampled at nominally 400Hz, see ACC I/F) obtaining the following rates :

ID1. Xpiezo 16bit @200Hz n = 2
200Hz x 6sec = 1200 samples = 22 TM

ID2. Ypiezo 16bit @200Hz n = 2
200Hz x 6sec = 1200 samples = 22 TM

ID3. Zpiezo 16bit @200Hz n = 2
200Hz x 6sec = 1200 samples = 22 TM

Total produced packets = 66 TM

ID4. Xservo LOW GAIN 12bit @400Hz n = 1

c- Determine the Timpact instant basing upon XPn filtered threshold crossing with the following quadratic filter:
XPn = A*XPn-2 + B*XPn-1 + C*XP

where XP represents the 400 Hz Xservo LOW GAIN acceleration signal (ID4) and XPn filtered Xservo values.

c.1- The A, D, C, Th shall be uploadable parameters; they shall have the following ranges:
A = -1 to 1
B = -1 to 1
C = -1 to 1
Th > 0
The PROM default values shall be:
A = 0.1
B = 0.2
C = 0.7
Th = 5 Volt

UR-3.1.11-10 : The following shall be performed during the SURFACE phase: since Timpact instant forever:

a- Create a set of **66 TM packets** containing the impact trace from the above stored IMPACT TRACE DATA.

b- Enqueue the above packets for transmission to CDMS with the following priority-layout : ID1+ID2+ID3

c- Perform UR-3.1.11-1 + UR-3.1.11-2 + UR-3.1.11-3 + UR-3.1.11.4

e- Create TM packets of ACC data (at the rate of 1/CDMS cycle corresponding to 7 byte/sec = 56 bit/sec) composed of the following items :

1. SCDSR	: 17bit x 1.754Hz	= 29.82 bit/sec
2. STD2	: 96bit x 0.1Hz	= 9.6 bit/sec
3. HKD1	: 16bit x 0.1Hz	= 1.6 bit/sec
4. HKD2	: 16bit x 0.1Hz	= 1.6 bit/sec
Total data produced		= 42.62 bit/sec

c- Enqueue the above packets for transmission to CDMS

UR-3.1.11-11 : XSERVO RANGE SELECTION :

UR-3.1.11-11.1 : After POWER-ON or RESET the range switch shall be set to FINE.

UR-3.1.11-11.2 : During the Entry phase, raw data item RD1 (Xservo low) shall be examined once each block N of SCDSE in order to select Xservo range in the following way :

IF "**PARthresholdRANGE** (default PROM value =95%) trepassed " THEN set range switch to COARSE

The number of samples examined for the above purpose shall be determined in order to not overload the CPU with this low rate task for no more of 1/1000 of CPU load.

UR-3.1.11-11.3 : Soon after **T0+1min** instant the range switch shall be forced to COARSE.

UR-3.1.11-11.4 : The time of RANGE SELECTION EVENT to COARSE shall be recorded in the event LOG TM packet.

UR-3.1.11-12 : BEST XSERVO CHANNEL SELECTION :

UR-3.1.11-12.1 : After POWER-ON or RESET the selected Xservo channel shall be LOW (RD2).

UR-3.1.11-12.2 : Raw data item RD1 and RD2 shall be periodically examined once each block N for each SCDSE, SCDSD and SCDSR in order to select in the following way best Xservo channel to be used :

```
case Xservo = LOW GAIN

      if ABS(Xservo) < "PARXservoLow (default PROM value
      =7%)"

      select Xservo = HIGH GAIN

case Xservo = HIGH GAIN

      if ABS(Xservo) > "PARXservoHigh (default PROM value
      =90%)"

      select Xservo = LOW GAIN
```

The number of samples examined for the above purpose shall be determined in order to not overload the CPU with this low rate task for no more of 1/1000 of CPU load.

UR-3.1.11-13: The actuation of XSERVO range and the selection of XSERVO best channel shall be synchronized with the start of SCDS* blocks.

3.1.12 TEM MANAGEMENT

TEM sensor layout

HEAD 1 (TEM 1)

(V) PTF1 (voltage) thermistor fine sensor 1
(V) PTC1 (voltage) thermistor coarse sensor 1

HEAD 2 (TEM 2)

(V) PTF2 (voltage) thermistor fine sensor 2
(V) PTC2 (voltage) thermistor coarse sensor 2

COMMON TO BOTH HEADS

(V) REFLOW (voltage) reference for low gain
(V) REFHIGH (voltage) reference for high gain

4 CURRENT GENERATOR: 1 for each sensor
2 GAIN: 1 for each measure

(see I/F layout 3.2.3.6.2 chapter)

UR-3.1.12-1 : The following **SCIENCE DATA** measurement_set shall be performed cyclically every 5 seconds **in the same way during all the states** of the TITAN DESCENT or CHECKOUT modes after Tdata instant (i.e. states DESCENT 1st PHASE, DESCENT 2nd PHASE, DESCENT 3rd PHASE, SURFACE):

0 sec measurement_set of F1 (Fine Sensor #1)

1.25 sec measurement_set of C1 (Coarse Sensor #1)

2.5 sec measurement_set of F2 (Fine Sensor #2)

3.75 sec measurement_set of C2 (Coarse Sensor #2)

the measurement_set is defined in **UR-3.1.12-2.**

UR-3.1.12-1.1 : The following SCIENCE DATA measurement_set shall be performed cyclically every 6 seconds in the following way during the IMPACT state of the TITAN DESCENT or CHECKOUT modes:

0 sec measurement_set of F1 (Fine Sensor #1)

1.25 sec measurement_set of F2 (Fine Sensor #2)

2.5 sec measurement_set of F1 (Fine Sensor #1)

3.75 sec measurement_set of F2 (Fine Sensor #2)

the measurement_set is defined in UR-3.1.12-2.

UR-3.1.12-2 : Measurement_set definition

For each sensor x = F1, C1, F2, C2 a voltage measurement set combined with gain selection and current generator switching on_off shall be performed in the following sequence within 130 msec max:

- O2DVTx = averaged offset (1) of (2(VPTx - VREFy)) obtained according to 3.2.3.8.2.2

- O2VRy = averaged offset (1) of (VREFy + VREFy) obtained according to 3.2.3.8.2.2

- D2VTx = averaged value (2) of (2(VPTx - VREFy)) obtained according to 3.2.3.8.2.1

- 2VRy = averaged value (2) of (VREFy + VREFy) obtained according to 3.2.3.8.2.1

- y = LOW/HIGH gain selection on MUX AD according to threshold crossing criteria of 3.1.12.3

(1) i.e. current generators off
(2) i.e. current generators on

UR-3.1.12-3 : Measurement_set (bit allocation) layout

Each sensor measurement set shall be composed of two 24 bits groups to easy TM packeting functions.

O2DVTx LSB = 7 bit sensor offset voltage (*)

D2VTx = 16 bit sensor voltage (**)

selected gain = 1 bit gain selection flag (0 = L / 1 = H)

Total GROUP T = 24 bit

O2VRx LSB = 7 bit reference offset voltage (*)

2VRx = 16 bit reference voltage (**)

selected gain = 1 bit gain selection flag (0 = L / 1 = H)

Total GROUP R = 24 bit

GROUP T = Thermistor data
GROUP R = Reference voltage data

(*) (resolution = 1 ADU/4)
(**) (resolution = 1 ADU/8)

Each measurement_set shall be contained in a single packet.

UR-3.1.12-3.1 : For each sensor measurement, the HASI-DPU-SW shall produce:

OVFMEAN = 16 bit offset thermistor voltage (resolution 1/8 ADU)

OVRMEAN = 16 bit offset reference voltage (resolution 1/8 ADU)

The two offsets shall be the average (running mean @108 sec) of thermistor (reference) voltage offset i.e. O2DVTx (O2VRy).

UR-3.1.12-4 : Gain selection criteria

For each sensor x the low or high gain channel y is selected at the end of the measurement set using the following algorithm with the preceding measurement set values and the preceding gain selection:

UR-3.1.12-4.1: The rough resistors Ratio RRx (real value) is computed with the formula of 3.2.3.8.1, i.e. :

$$RRx = \frac{D2VTx - O2DVTx}{2VRy - O2VRy} + 1$$

with absolute accuracy of +/- 1K.

UR-3.1.12-4.2: The new gain channel y is selected in the following two cases depending on the current gain selection

case y = HIGH (corresponding to temp range 60k-110k)

if RRx * gradient HIGH (PROM default value = 7.32K) >
threshold HIGH (PROM default value = 105K) y = LOW

case y = LOW (corresponding to temp range 100k-330k)

if RRx * gradient LOW (PROM default value = 27.3K) >
threshold LOW (PROM default value = 105K) y = HIGH

NOTE: this is only the logical gain selection to be computed before the physical gain selection of UR-3.2.3.8.2.1 step 5 is performed.

UR-3.1.12-4.2.1: At power-on reset the y gain shall be set to LOW.

UR-3.1.12-5 The above timings may be changed during the design within +- 0.1 sec and must be performed with a tolerance of 10 msec.
The current generator shall be on 100 msec max.

UR-3.1.12-6 The sequence of 4 measurement (one for each HASI-DPU-SW state) must be stored as EEPROM parameter and each one may be exchanged with any one of the other without restrictions (duplicated allowed like master-mind game) i.e. :
MEAS_SEQ = { MEAS1 + MEAS2 + MEAS3 + MEAS4 }
MEAS* = { OVT% + VT% }
* = { 1 or 2 or 3 or 4}
% = { 1 or 2 or 3 or 4}

UR-3.1.12-6.1 The PROM default value of the sequences of TEMs measurement throught different HASI-DPU-SW states are:

DESCENT 1st phase
DESCENT 2nd phase
DESCENT 3rd phase
SURFACE :

F1, C1, F2, C2

IMPACT :

F1, F2, F1, F2

3.1.13 PPI MANAGEMENT

LAY-OUT DESCRIPTION

Measurements of PPI comprehend :
- 24 frequency channel in the range 1-30 Khz
- 2 housekeeping voltages in the range 0-10 volt

the formers must be sampled by means of timer B (according to chapter 3.2.1.6) and the latters must be sampled by means of ADC 2 (according to chapter 3.2.3.6)

Frequency channels are grouped in
- 6 reference channels
- 18 sensor channels

organized in 3 blocks of 8 each (6 sensors + 2 references)

SESSIONS SEQUENCE

UR-3.1.13-1: The PPI measurement and data production shall begin in the DESCENT 1st PHASE of HASI-DPU-SW.

UR-3.1.13-2: The whole PPI measurement and data production activity shall be defined by a sequence **{SSn}** of NORMAL and HEALTH-CHECK SESSIONS of data production covering the whole TITAN DESCENT nominal mission time duration since **Tdata** (T0 + 1 min) up to **Tloss**.

UR-3.1.13-3: The sequence {SSn} shall be specified repeating NORMAL and HEALTH-CHECK session in such a way that takes no more than 27.5 bit/sec of the whole 28 bit/sec PPI bit rate allocation. The repetition of following 7-session basic cycle : [HC+N+N+N+HC+N+N] satisfies the above condition and should be used.

UR-3.1.13-3.1 The PPI measurement during DESCENT until Tloss shall be divided in three different phases in accordance with the following table:

LOW PRES. PHASE : if the DDBL Time is between Tdata and Tpmed;

MEDIUM PRES. PHASE : if the DDBL Time is between Tpmed and Tphigh;

HIGH PRES. PHASE : if the DDBL Time is between Tphigh and Tloss.

The time transition (i.e. Tpmed and Tphigh) shall be uploadable parameters. Their default PROM values shall be the following:

Tpmed = 1:15:00 after T0

Tphigh = 1:45:00 after T0

UR-3.1.13-3.2 The measurement sequence during the three phases shall be fixed and shall be comply with the following sheme:

LOW PRES. PHASE : G A A A H A A;
MEDIUM PRES. PHASE : G B B B H B B;
HIGH PRES. PHASE : G C C C H C C.

where: G, H are health-check sessions
A, B and C are normal sessions.

UR-3.1.13-3.2.1 The duration of one measurement sequence (5 normal sessions plus 2 Health Check sessions) shall be:

(5 * Tn + 2 * Thc) = 3 min and 48 sec

where: Tn = 43.2 sec is the duration of one normal session;

Thc = 6 sec is the duration of one h/c session.

NORMAL SESSIONS

UR-3.1.13-4: NORMAL sessions shall include up to three different types (from 0 to 2 or from A to C). Each of them defines a sequence **{YSh}** of 36 YSi statistical pressure data to be produced at regular rate of 1 each 1.2 sec (0.8333 Hz). Each session duration time is 43.2 sec.

UR-3.1.13-4.1: The physical channel S(i,j) to be used for each step i of each NORMAL session j shall be mapped by means of an EEPROM updatable table of the form:

S = f(i,j)
j : 1...3
i : 1...36
S : 1...24

The default PROM values are in the ANNEX B.

UR-3.1.13-4.2: Each **YSi** shall be a 24 bit data item composed of AVERAGE (16 bit) and VARIANCE (8 bit) of **5 Yi** data and shall be computed according to UR-3.1.13-4.2-1/2/3.
Yi data are defined more ahead.

UR-3.1.13-4.2-1: The YSi-AVERAGE shall be the arithmetical average of the 5 Yi data scaled on signed 16 bit within the [Yimin = -1 , Yimax = 1] range.

UR-3.1.13-4.2-2: The following actions shall be taken in case of Yi beeing outside above range :

CONDITION	CLASSIFICATION	ACTION
-1 <= Yi <= 1	nominal	normal processing
Yi > 1	failure	send Yi = 1
-2 <= Yi < -1	nominal	Yi+1; normal processing
Yi < -2	failure	send Yi = 0
R1 and R2 are closed values	failure	send Yi = 1

UR-3.1.13-4.2-3: The YSi-VARIANCE shall be computed with the following formula:

$$(\text{Sum of } Yi^{\wedge 2})/5 - Y^{\wedge 2}$$

where: Yi values are the samples calculated in accordance with UR-3.1.13-4.4

Y is the average.

UR-3.1.13-4.2-3.1: The YSi-VARIANCE shall be scaled on 8 bits with resolution LSB 2^{-18}.

UR-3.1.13-4.3: Each **Yi** shall be function of a 3-ple composed of **S, R1, R2** near-in-time raw frequency measurements:

Yi = (S(i)-R1(S))/(R2(S)-R1(S))

where :

S(i) is the sensor measurement of the i-th session step defined by map of UR-3.13-4.1

R1(S) is the measurement of 1st reference channel of the block containing the sensor S

R2(S) is the measurement of 2nd reference channel of the block containing the sensor S

S = 1...24
i = 1...36

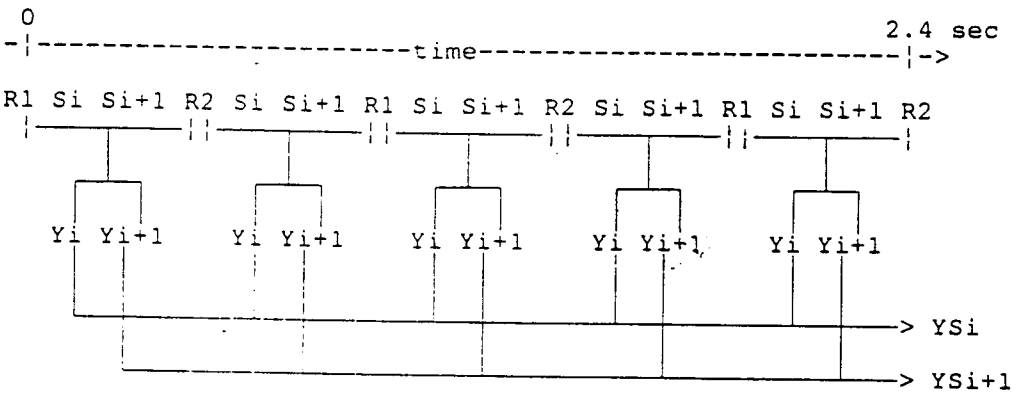
Double precision (32 bit) fract arithmetic shall be used for computation of above formula.

NOTE : The formula for computing of Yi has been inverted with respect to PPI specification as the HASI-DPU-SW actually deals with sensor periods instead of frequencies.

IMPORTANT : **In the formula R1 is a reference with a lower frequency than R2.**

UR-3.1.13-4.4: The following special sequence of raw frequency measurement shall be performed to allow the YSi production rate of 1 every 1.2 sec as stated in UR-3.1.13-4 (*) :

The sensor measurements of session steps i and i+1 are performed in couples sharing the reference channels measurements thus needing only 16 raw frequency measurements for a pair of YSi and YSi+1 performed in 2.4 seconds :



(*) : Since each YSi data is obtained from 16 raw frequency measurement, each taking between 120-140 msec, a straight-forward readout sequence would take between 1.9-2.2 seconds for each YSi.

UR-3.1.13-4.5: Each complete session measurement set of 36 YSi shall be inserted in a time-stamped, stand-alone TM packet together with the raw data value of last two reference channels R1, R2 read; i.e. there shall be a one-to-one correspondence between sessions and PPI TM packets. The particular data formats (1 for each session type) are defined in the HASI IDS.

HEALTH-CHECK SESSIONS

UR-3.1.13-5: HEALTH CHECK Sessions shall include up to two different types (from 0 to 1 or from G to H). Each of them defines a sequence **{Fh}** of 37 frequency channels raw data (either sensor or reference) acquired at regular distance in 6 seconds (that corresponds to a regular sampling rate of 6.2 Hz).

UR-3.1.13-5.1: The physical channel S(i,j) to be used for each step i of each HEALTH-CHECK session j shall be mapped by means of an EEPROM updatable table of the form:

S = f(i,j)

j : 1...2
i : 1...37
S : 1...24

The default PROM values are in the ANNEX B.

UR-3.1.13-5.2: Each **Fi** frequency raw data shall be a 24 bit unsigned integer value of the timer corresponding to the frequency period measured.

UR-3.1.13-5.3: Each complete HEALTH-CHECK SESSION measurement set of 37 Fi shall be inserted in a time-stamped, stand-alone TM packet i.e. : there shall be a one-to-one correspondence between HEALTH-CHECK SESSIONS and PPI TM packets. The particular data formats (1 for each session type) are defined in the HASI IDS.

HOUSEKEEPING MEASUREMENTS

UR-3.1.13-6: The two housekeeping voltage shall be sampled at a slow rate (every 2 sec) in order to approximatively fit the residue 0.5 bit/sec allocated bit rate i.e.:

16 bit (average) each 64 sec shall be allocated for each sample.

HKV1	16 bit	@0.015625Hz
HKV2	16 bit	@0.015625Hz
Total	32 bit	@0.015625Hz = 0.5 bit/sec

PPI BIT RATE UTILIZATION SUMMARY

BIT RATE ALLOCATED = 28 bit/sec
(0.5 packet/cmds cycle = 896 bit * 0.5 / 16 = 28 bit/sec)

FREQUENCY MEASURES = 27.509 bit/sec
(896 * 7)/(5*Tn + 2*Thc)

HOUSEKEEPING MEAS. = 0.5 bit/sec
(32bit @0.015625Hz)

UR-3.1.13-6.1 The two HK voltages shall be checked every 2 sec respect to a range and this result shall be transmitted in the HC2S health check report.

HKV1 range is 4.5v to 5.5v
HKV2 range is 2.5v to 7.5v

3.1.14 PWA MANAGEMENT

The HASI-DPU-SW shall manage the PWA activities by only means of information exchanging through the DPU-PWA data link depicted in the PWA and DPU specifications.

The main tasks of the data link between PWA and DPU are:

- PWA to receive currently updated (at least every 2 sec) mission information and HASI-DPU-SW status.
- PWA to periodically send scientific data according to the received mission information and the HASI-DPU-SW status.

UR-3.1.14-1 PWA operational modes (from the HASI-DPU-SW point of view i.e. data production) shall be fully driven by the STATUS BLOCK (SB) information ALWAYS provided by the HASI-DPU-SW. Contents of SB shall comprise the DDBL information plus HASI-DPU-SW internal events and states necessary to PWA.

UR-3.1.14-2 PWA shall **ALWAYS** provide 2 data packets for each SB from HAS-DPU-SW (according to the PWA I/F requirements i.e. 16 data packets every CDMS cycle) without regard of mission or HASI-DPU-SW status.

UR-3.1.14-2.1 The number of science/test/HC data packets shall vary with resolution of 1 CDMS cycle ONLY according to the HASI-DPU-SW STATUS as defined in the following table:

HASI-DPU-SW STATUS	PWA SEND	REMARKS
ENTRY	16 HC for CDMS cycle	Time < Tdata
DESCENT 1st phase	16 HC for CDMS cycle	Time < TdataH
DESCENT 2nd phase	(12 SC/TEST + 4 HC) for CDMS cycle	Time < Tradar
DESCENT 3rd phase	(13.5 SC/TEST + 2.5 HC) for CDMS cycle	Untill last Km
IMPACT	(13.5 SC/TEST + 2.5 HC) for CDMS cycle	Untill IMPACT
SURFACE	(12 SC/TEST + 4 HC) for CDMS cycle	Time < Tloss

UR-3.1.14-2.2 The Science (SC) and test (TEST) data packets shall be always re-coded and queued for TM transmission to CDMS.
The Health Check (HC) data packets shall be always garbled after RX check.

UR-3.1.14-2.3 For health-check purposes, PWA data flow toward HASI-DPU-SW in compliance with mission time and phase shall indicate correct working of PWA. The PWA status bit of the STATUS WORD shall be updated accordingly and PWA data link status shall be monitored in the Housekeeping TM packets.

UR-3.1.14-2.4 As TM packets redundancy shall be fully managed by PWA, HASI-DPU-SW shall forward PWA packets to CDMUs without redundancy according to the reception order of each couple: the first to CDMU A and the second to CDMU B.

UR-3.1.14-3 No special test commands are required by PWA over the data-line: PWA test commands defined in PWA specification and in HASI-IDS (AD-16) shall be uplinked to DPU by CDMS or EGSE/PIFS (respectively after or during the HASI-AIV).

PWA test commands shall be routed from HASI-DPU-SW to PWA by means of a special parameter contained in the STATUS BLOCK (SB) sent by the HASI-DPU-SW during the CHECKOUT modes.

UR-3.1.14-4 During CHECKOUT phases the PWA test actions (in case of routing of telecommands depicted above) shall be transparent to the HASI-DPU-SW that shall proceed the same simulated descent functions.
NOTE THAT TELECOMMANDS ARE FORESEEN ONLY FOR SPECIAL INVESTIGATION PURPOSES (I.E. CONTINGENCIES) AND THAT THE BIT RATE ALLOCATED FOR SIMULATED DESCENT IS THE SAME OF THE REAL DESCENT (I.E. THE CDMS SHALL PERFORM ALWAYS THE SAME POLLING SCHEME).

REMARKS: NOTE that during the CHECK-OUT the Status Block information may not follow the Nominal descent evolution E.G. MISSION TIME and HASI-DPU-SW Status may change without continuity (According to EID-A).

3.1.15 BOOMS RELEASE
(MCA ACTIVATION)

UR-3.1.15-1 The HASI-DPU-SW shall attempt to perform the booms release twice during the DESCENT phase by means of MCA devices activation :

- first try at **Td1** instant
- second try at **Td2** instant

of UR-3.1.1-2 General Mission timeline definition.

UR-3.1.15-2 For each boom release attempt the HASI-DPU-SW shall repeat the following MCAs power drivers switch activation-deactivation sequence for 3 consecutive times with 1 second of time interval between each of them (see MCA I/F description in chapter 3.2.2.7) :

repeat 3 consecutive times the following burst of MCA1 and MCA2 activations and deactivations (via I/O locations of 3.2.2.7):

A- readout MCA status

B- activate MCA1

C- 50 msec after A, readout MCA1 status and deactivate MCA1

D- wait at least 10 msec

E- activate MCA2

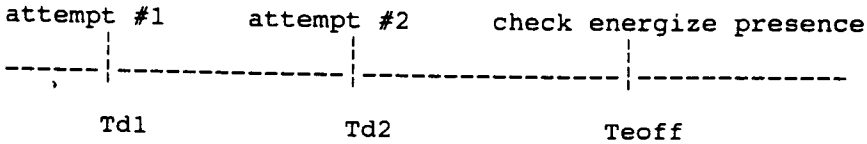
F- 50 msec after D, readout MCA2 status and deactivate MCA2.

UR-3.1.15-3 DELETED

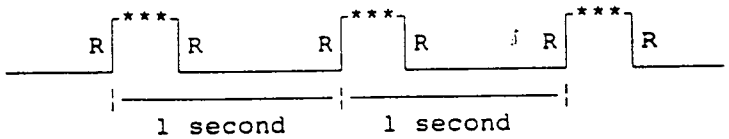
UR-3.1.15-4 The trace of the MCA's status during the MCA activation/deactivation sequence shall be reported in the EVENT log HK TM packets.

UR-3.1.15-5 The timing requirements specified in this chapter shall be respected with a tolerance of +1 **msec.**

BOOMS RELEASE



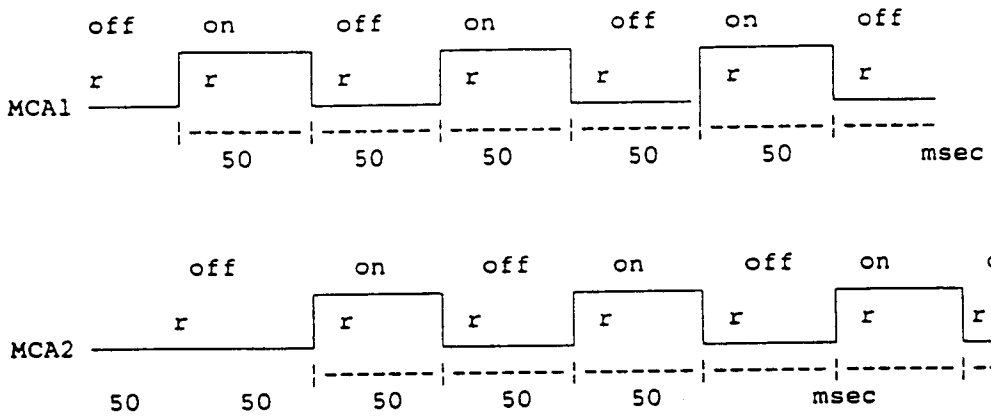
BOOM DEPLOY ATTEMPT



* = MCAs activation deactivation sequence

R = MCA status readout

MCA ACTIVATION-DEACTIVATION SEQUENCE



r = MCA status readout

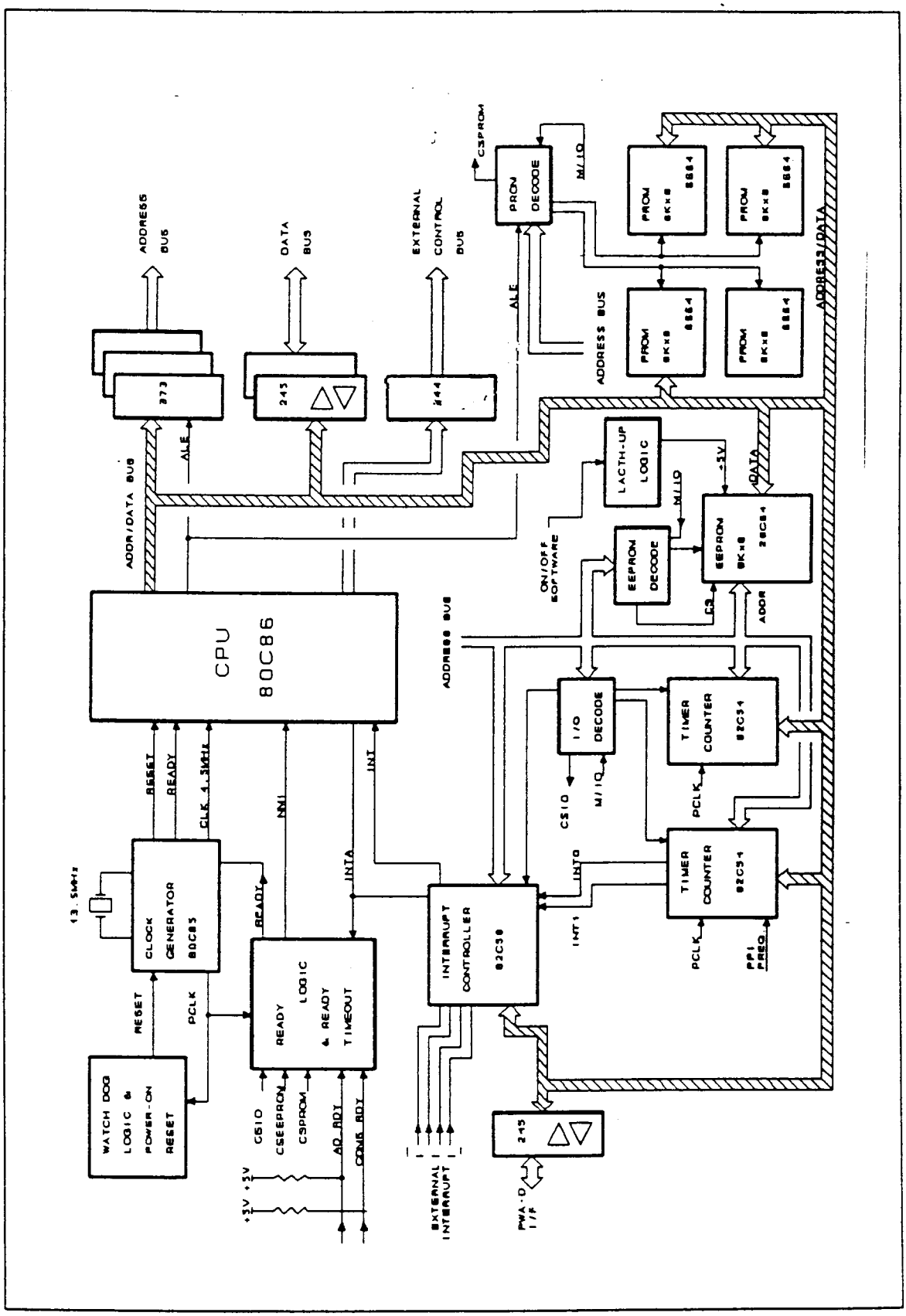
3.2 CONSTRAINTS REQUIREMENTS

3.2.1 CPU BOARD

The CPU module implements functions of elaboration and control of experiment in the HASI DPU.
The functions in this module are:

- Central Processing Unit.
- Clock generator.
- Interrupt controller.
- Prom memory.
- EEPROM memory with Latch-Up protection logic.
- Watch-Dog and Ready timeout logic.
- Six programmable timers/counters.
- Eight bits parallel port with handshake,forPWA interfacing.
- Bus interface to other DPU module.

A block diagram is showed hereafter.


CPU
80C86
ADDRESS BUS
DATA BUS
EXTERNAL CONTROL BUS
ADDR/DATA BUS
ALE
CLOCK GENERATOR 82C83
WATCH DOG LOGIC & POWER-ON RESET
READY LOGIC & READY TIMEOUT
INTERRUPT CONTROLLER 82C59
TIMER COUNTER 82C54
I/O DECODE
PROM DECODE
EEPROM DECODE
LATCH-UP LOGIC
EEPROM 8Kx8 28C64
PROM 8Kx8 8864
ON/OFF SOFTWARE
RESET
READY
CLK 4.5MHz
NMI
INT
INTA
PCLK
CS10
CSEEPROM
CSPROM
AD RDY
CONF RDY
EXTERNAL INTERRUPT
PWR-D I/F
373
245
244

3.2.1.1 CPU

A sixteen bit 80C86 cpu is used, working at clock frequency of 4.5 MHz.

This CPU operates in the minimum mode, it can address 1 MByte of memory and 64 Kbyte of I/O.

Memory address range : 00000-FFFFF

I/O address range: 0000-FFFF

These addresses are referred to byte locations.

Both word and byte accesses can be performed, both in read and in write cycles, in memory and I/O spaces.

Word accesses are done in two different modes:

a) even addresses: the two bytes of the word are read or written in a single cycle;

b) odd addresses: two consecutive byte cycles are performed, the first one for the LSbyte, the second one for the MSbyte.

In the DPU EPDH:

1) PROM memory (code memory and constant data) is byte or word addressable.

2) EEPROM memory (data and program patches) is byte addressable.

3) RAM memory (variable data and stack) is byte or word addressable.
NO PERMANENT DEFECTIVE LOCATION ARE FORESEEN (the high rel HS65758RH is latchup free)

4) The I/O peripherals on CPU board are byte addressable; on the other EPDH boards same peripherals are word addressable.
The 80C86 cpu uses a local time multiplexed address-data bus for memory and I/O spaces.

Octal latches (HCTS373) controlled by CPU signal ALE (address latch enable) are used to latch the addresses during cycles.

The CPU board includes the following functions:

INTR: (interrupt request) the interrupts generated by peripherals are masked and prioritized by the programmable interrupt controller (82C59A); this device generates the INTR signal to the cpu.

NMI: (non-maskable interrupt) this interrupt request is not maskable internally by software; its priority is higher than INTR request. In the HASI-DPU-SW this interrupt is used to control failure situations during read or write cycles on peripherals (memory or I/O) internal or external to the CPU board.

RESET: this signal initializes in a definite state the cpu and all devices in the boards.

This function has a higher priority than NMI function.
This function is activated in the following cases:

- Power on.
- Software Watch-Dog timeout.

HOLD: this signal is used by DMAC (dma controller, in the CDMS I/F board), to request control of the system bus. When a DMA request is made the DMAC issues the HOLD signal to inform the cpu. The cpu indicates to DMAC that it has relinquished control of the system bus with activation of HOLDA signal.

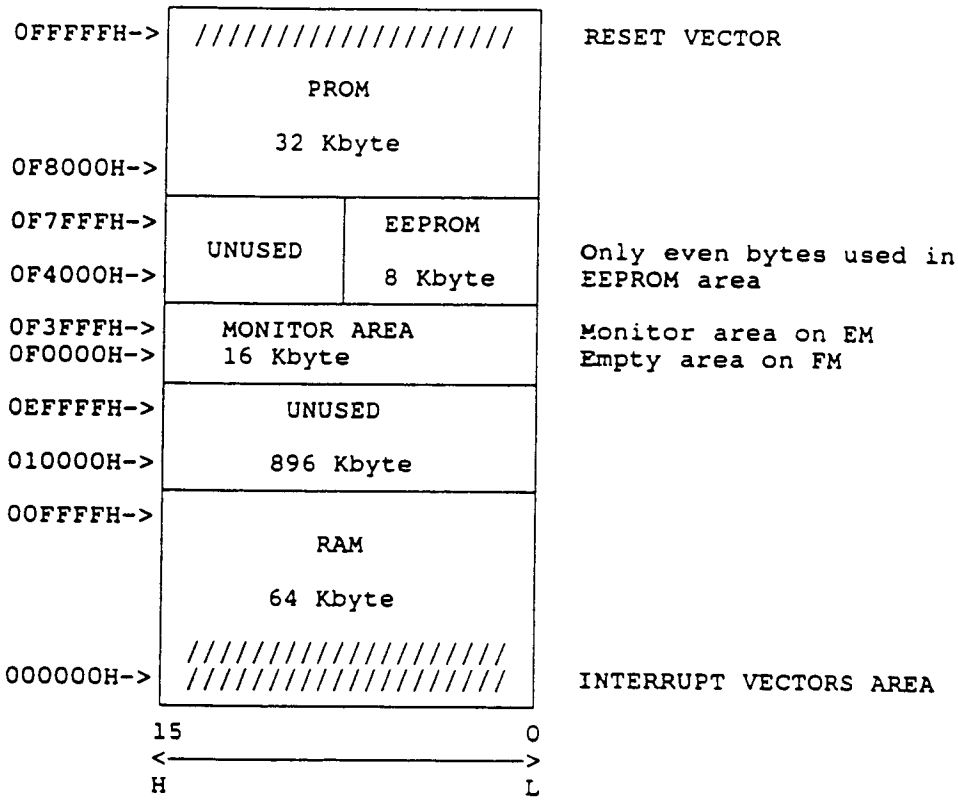
Clock Generator:

All the timing signals which are needed for the operation of the cpu and peripherals are derived from a 13.5 MHz clock signal.
This signal is generated by a crystal and by a clock generator (HS-82C85).
This device generates the cpu clock (4.5 MHz) duty cycle 33%;
peripheral clock (2.25 MHz) duty cycle 50% and synchronizes the reset and ready inputs.

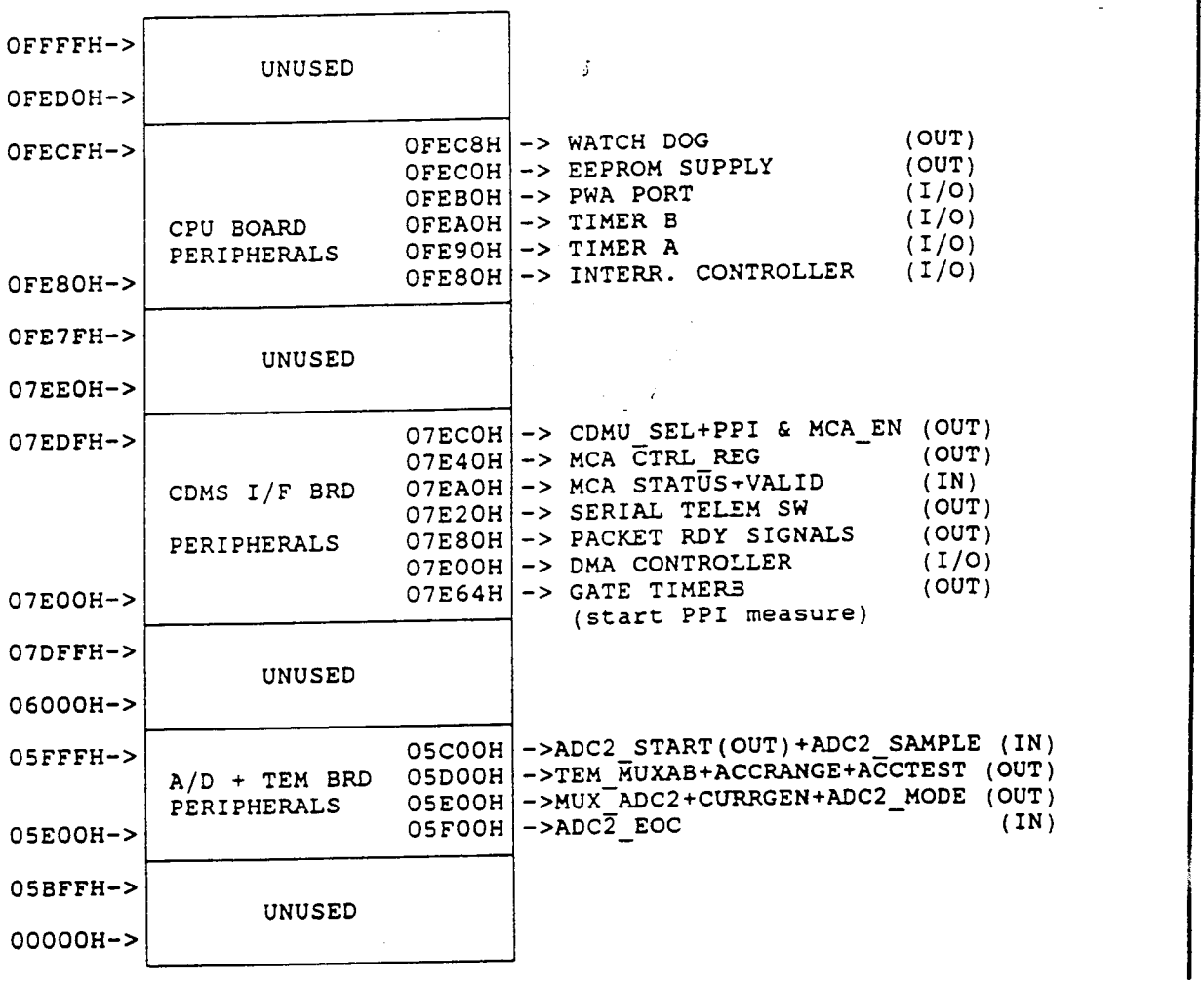
3.2.1.2 ADDRESSES SPACE

PROM	32Kb	F8000 - FFFFF
EEPROM only even address (8Kb)	16Kb	F4000 - F7FFF are used
MONITOR	16Kb	FF000 - F3FFF
NMI	896Kb	10000 - F0C00
RAM	64Kb	00000 - 0FFFF
I/O	64Kb	00000 - 0FFFF

EPDH Memory Map



EPDH I/O Map


0FFFFH->
UNUSED
0FED0H->
0FECFH->
CPU BOARD PERIPHERALS
0FEC8H -> WATCH DOG (OUT)
0FEC0H -> EEPROM SUPPLY (OUT)
0FEB0H -> PWA PORT (I/O)
0FEA0H -> TIMER B (I/O)
0FE90H -> TIMER A (I/O)
0FE80H -> INTERR. CONTROLLER (I/O)
0FE80H->
0FE7FH->
UNUSED
07EE0H->
07EDFH->
CDMS I/F BRD PERIPHERALS
07EC0H -> CDMU_SEL+PPI & MCA_EN (OUT)
07E40H -> MCA CTRL_REG (OUT)
07EA0H -> MCA STATUS+VALID (IN)
07E20H -> SERIAL TELEM SW (OUT)
07E80H -> PACKET RDY SIGNALS (OUT)
07E00H -> DMA CONTROLLER (I/O)
07E64H -> GATE TIMER3 (OUT)
(start PPI measure)
07E00H->
07DFFH->
UNUSED
06000H->
05FFFH->
A/D + TEM BRD PERIPHERALS
05C00H ->ADC2_START(OUT)+ADC2_SAMPLE (IN)
05D00H ->TEM_MUXAB+ACCRANGE+ACCTEST (OUT)
05E00H ->MUX_ADC2+CURRGEN+ADC2_MODE (OUT)
05F00H ->ADC2_EOC (IN)
05E00H->
05BFFH->
UNUSED
00000H->
75

3.2.1.3 EXTERNAL INTERRUPTS

A programmable interrupt controller (82C59A) is used. This device handles 8 interrupt sources with prioritization and selective enable/disable capability.

All the interrupt inputs shall be programmed for edge detection.

CPU INTERRUPT LINE	VECTOR OFFSET (priority)
INT EOP DMA	2
EOP TM I/F x 2	
EOP ML I/F x 1	
EOP ACC S.D. x 1	
INT BCP	1
INT PWA TX	5
INT PWA RX	3
INT PPI	4
INT EEPROM LATCH-UP	6
INT PERIODICAL TIMER	0
FAULT LINE	7

3.2.1.4 EEPROM SEEQ 28C64 pag 6÷39 MAN SEEQ 1990

This memory is used for variable data which must be mantained during power-off.
One 8 Kbytes chip is used, type 28C64; this component is not latch-up free, a circuitry for power control of this component is implemented in the CPU module which provides:

- power on/off control under software command.

- current limiting and automatic power off in case of latch-up, in order to prevent damage of the component; this event generates an interrupt request to the CPU.
A proper circuitry is provided in order to separate all signals in case of EEprom power-off, so that all the other function can still operate.

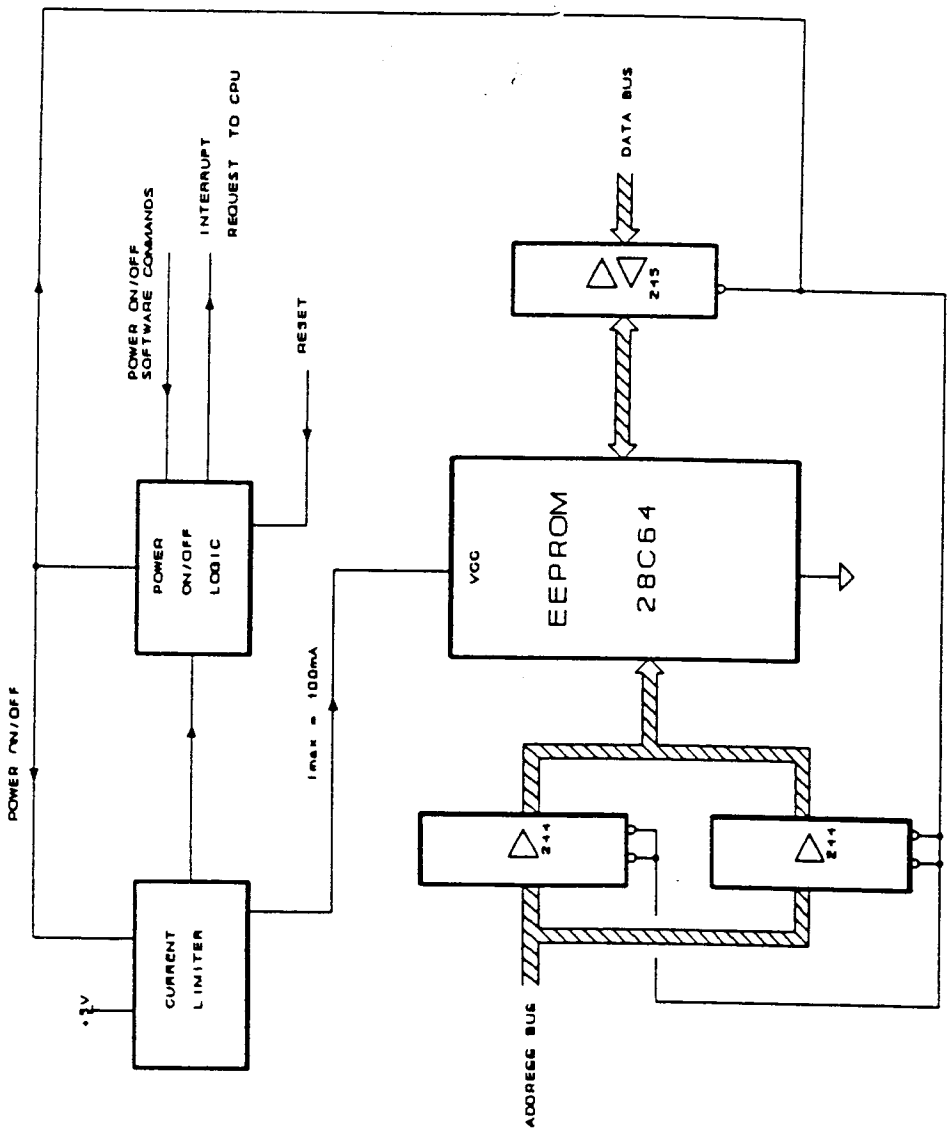
SUMMARY OF FEATURES:

- 8K x 8bit
- switched off at CPU RESET
- byte operations only (MEMORY INSTRUCTION)
- switch on at least 10 msec before operations (R/W)
- switch off (after operation) is possible after end of writing cycle (at least 10 msec)
- READ operations: no constraints
- WRITE operations: 10 msec min of STATUS polling before any accesses after a write operation
- automatic switch off upon latch-up event detected with INT6 generation
- switch on/off I/O register : byte access @FEC0
bit 0 : 0 = OFF 1 = ON

The memory map for this area is: F4000-F7FFF but only 8 Kbytes (even addresses) are usable.

A block diagram is showed hereafter

EEPROM POWER ON/OFF and LATCHUP PROTECTION LOGIC



3.2.1.5 INTERRUPT CONTROLLER HARRIS HS82C59A
MANUAL HARRIS DIGITAL MILITARY 1989 pg 5-62

- base address I/O FE80
- register R/W operations: I/O word access
(0 used, 1 not used)

3.2.1.6 PROGRAMMABLE TIMER/COUNTER HARRIS HS82C54
MANUAL HARRIS DIGITAL MILITARY 1989 pg 5-19

- base address I/O TIMER A FE90
- base address I/O TIMER B FEA0
- register R/W operations: I/O word access
(0 used, 1 not used)

TIMER A

- TIMER 0 of TIMER A provides INT0 (sw use)
(periodical mode 2)

- TIMER 1 of TIMER A started by BCP (sw use)
(mode 5 HW trigger)

- TIMER 2 of TIMER A to be programmed for generation of 3200Hz ACC sampling rate
(periodical mode 3, 3200.6 hz effective,
init count = 0x2BF)

TIMER B

The whole TIMER B is devoted to PPI frequency measurement

- TIMER 0 of TIMER B prescaler to TIMER 1 **(mode 2)**

- TIMER 1 of TIMER B measures PPI frequency periods
(mode 0)

- TIMER 2 of TIMER B controls PPI measures.
(mode 1)

- start count TIMER 2 of TIMER B (gate triggering) occur when bit D0 of I/O address 7E64H rises from 0 to 1

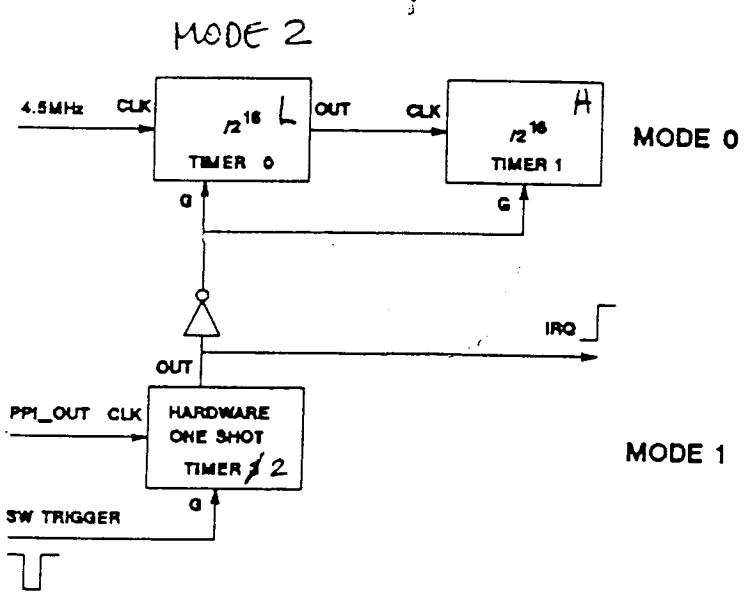
CLOCK TIMER A

- TIMER 0 4.5/2 MHz peripheral clock
- TIMER 1 4.5/2/128 " " "
- TIMER 2 4.5/2 MHz " " "

CLOCK TIMER B

- TIMER 0 CPU clock 4.5 MHz peripheral clock
- TIMER 1 CPU clock 4.5 " " "
- TIMER 2 CPU clock PPI frequency signal

TIMER B: PPI MEASURES of 1 frequency channel



UR-3.2.1.6-1: To measure a PPI frequency channel (after selected according to chapter 3.2.2.8) :

1) set TIMER 0 and 1 (T0=L=0x0000, T1=H=0xFFFF)
2) preset TIMER 2 = N
3) sw start TIMER 2; count begins
4) after N PPI_OUT pulses (i.e. N frequency periods) :

   4.1) TIMER 0 and 1 stop
   4.2) TIMER 2 stops
   4.3) an interrupt request INT 4 is generated

5) TIMER 1 chained with TIMER 0 contains the N PPI_OUT pulses time duration as int 32 bit with resolution of 1/4.5Mhz;
the corresponding frequency F may be computed as follow:
   F = 4.5 Mhz * N/COUNTER
   COUNTER = 1's complement of ((TIMER1 chained TIMER0) - 1)

NOTE : PPI_OUT waveform is always present

UR-3.2.1.6-2: As the relative accuracy of the PPI_OUT period measurement is given by 4.5Mhz CLK / MEAS. time i.e.: (1/4.5*10E6)/(N/PPI_OUT), the parameter N must be selected for each frequency to be measured in order to meet the accuracy required (2*10E-6 at present) and to keep the measurement time as equal as possible for each frequency measured (at least 100 msec are required for correct sensor integration time).
As the frequency range to be measured is not known in advance a fast preliminary rough measure should be performed in order to determine the most suitable value of N and a timeout of the order of 100 msec must be provided to avoid deadlocks under channels faults.

The following table shows typical values of N for nominal frequency ranges 1..30 Khz

ACCURACY = PPI_OUT/(N * 4.5*10E6)

MEAS_TIME = N/PPI_OUT

Hence : N = PPI_OUT/(4.5*10E6 * ACC)

if ACC = 2*10E-6 then N > PPI_OUT/9

Typical values :

PPI_OUT (Khz)	N	MEAS. TIME (msec)
1	110	110
10	1100	110
30	3300	110

3.2.1.7 PWA INTERFACE REGISTER

An eigth bits bidirectional parallel port is provided in the cpu board forcommunications between the EPDH and PWA-D electronics.
This interface is designed for operation using an 82C55 parallel port interface in the PWA.
The EPDH is the master of the communications, i.e. the timing of data exchange are determined by EPDH using an interrupt technique.
The data port is normally three-stated and becomes active only during read or write operations.
Four handshake signals are provided in order to control the data flow over the eigth bits parallel bus:

- **PWA strobe:** (output) a low level on this signal enables the EPDH output data buffer; write data can be latched in the PWA-D on the rising edge of this signal.
(to the 82C55 STB input).

- **PWA ack:** (output) a low level on this signal enables the PWA-D output data buffer; data are read by EPDH on the rising edge of this signal.
(to the 82C55 ACK input).

- **PWA ibf:** (input) this signal is low when the PWA-D input port is ready to accept new data; an interrupt to the EPDH cpu is generated on the falling edge of this signal, i.e. when the PWA-D has read the last data.
(to the 82C55 IBF output).

- **PWA obf:** (input) this signal goes low when new data are written in the PWA-D output buffer; an interrupt to the EPDH cpu is
generated on the falling edge of this signal.
(to the 82C55 OBF output).

SUMMARY OF FEATURES :

- R/W (RX/TX) register I/O address = FEB0
- ONE R or W operation at a time allowed
- data exchange flow syncronization not provided (controlled by sw protocol)
- PWA writing 1 byte generates INT 3 (RX)
- PWA reading 1 byte generates INT 5 (TX)

Word access (0 not used, 1 used)
Byte access @ FEB1 (base + 1)

3.2.1.8 WATCH DOG LOGIC

This logic consists of a binary counter which is clocked by a square wave signal with a 56uS period, (this signal is generated by a frequency division by 256 of the PCLK signal, 2.25 MHz); the counter generates the timeout signal after 4096 pulses, about 0.466 sec, if the software does not reset it performing an I/O byte write cycle at address FEC0.

In the event of timeout a hardware reset is issued to the cpu and to all the peripherals; a flag is provided to inform the software in the reset procedure whether the hardware reset was generated by a power-on or by a timeout condition.

SUMMARY OF FEATURES :

- I/O register address = FEC8H byte, write any value

- if 0.466 Sec. elapsed since last write generates CPU reset and raises IR7 of 82C59 inputs

3.2.1.9 NMI (READY TIMEOUT) LOGIC

This logic controls the generation of the READY signal by all the memory or peripheral devices addressed by the cpu or the DMAC.
Hardware failures in the address bus or in the address decoding logic (either in the cpu module or in the slave modules) can be detected for all cycles.
A binary counter is used, clocked by the PCLK signal,(2.25 MHz); the READY timeout signal is generated whenever the addressed memory or I/O device does not respond in less than about 8uS; in case of ready timeout, the ready signal to the cpu is forced active so that the cpu can proceed with execution, and an NMI request is generated

SUMMARY OF FEATURES :

- The NMI interrupt is generated when :

i) a failure condition on memory or I/O operation is detected
or

ii) an access is attempted to non-existent memory locations defined with NMI in chapter 3.2.1.2

or

iii) an access is attempted to I/O locations not existent, i.e. not listed in chapter 3.2.1.2.

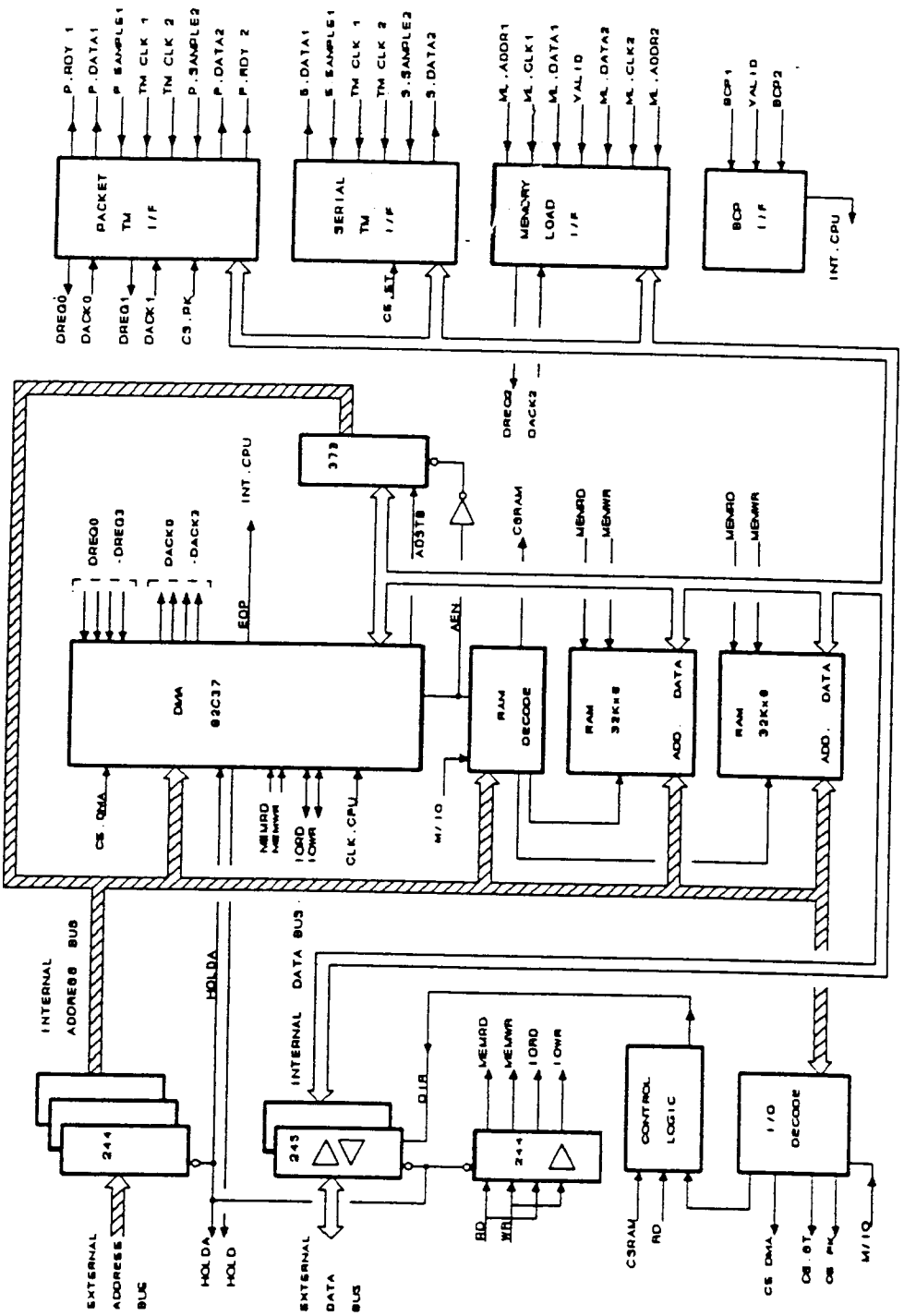
3.2.2 CDMS I/F BOARD

The CDMS I/F module implements function of communication with the two CDMU units.
This module also includes the DMAC (dma controller), the RAM memory and other functions of monitoring and driving.

The main functios of this module are:

- RAM memory.
- DMAC (dma controller).
- CDMU interfaces:
    - Status interface.
    - Packet interface.
    - Memory Load interface.
    - BCP interface.
- MCA timing.
- MCA monitor.
- PPI commands.

A block diagram is showed hereafter :


P.RDY 1
P.DATA1
P.SAMPLE1
TM CLK 1
TM CLK 2
P.SAMPLE2
P.DATA2
P.RDY 2
PACKET TM I/F
S.DATA1
S.SAMPLE1
TM CLK 1
TM CLK 2
S.SAMPLE2
S.DATA2
SERIAL TM I/F
M.ADDR1
M.CLK1
M.DATA1
VALID
M.DATA2
M.CLK2
M.ADDR2
MEMORY LOAD I/F
BCP1
VALID
BCP2
BCP I/F
INT.CPU
DREQ0
DACK0
DREQ1
DACK1
C3.PK
CS.BT
DREQ2
DACK2
373
INT.CPU
DREQ0
-DREQ3
DACK0
-DACK3
EOP
DMA 82C37
AEN
RAM DECODE
RAM 32Kx8
DATA
ADD.
CS.DMA
MEMRD
MEMWR
IORD
IOWR
CLK.CPU
M/IO
C3RAM
INTERNAL ADDRESS BUS
HOLDA
INTERNAL DATA BUS
244
245
DIR
CONTROL LOGIC
I/O DECODE
RD
WR
EXTERNAL ADDRESS BUS
HOLD
EXTERNAL DATA BUS
CS DMA
CS BT
CS PK

3.2.2.1 STATUS WORD

The Status Word interface is a serial digital data channel which provides monitor data to CDMU.

Two indipendent interfaces are realized for ensure full rendundance, but the same data are avaiable on them.

For each interface, the differential lines interfacing with the CDMU are:

DATA line to CDMU.
SAMPLE line from CDMU.
CLOCK line from CDMU.(shared with Packet I/F channel).

The status interface is composed of : a 16 bit register (common to both interfaces) containing the status word data, and two serial shift register (one for each interface).

At the DPU reset data in the status word register are cleared by hardware, the software sets a bit in the register at the program start. The CDMU can verify the correct start of the program.

The data written in the status word register is continuosly loaded in the shift register.
A control logic is provided in order to stop loading of shift-register when the CDMU begins to read the data.In this case the data read by CDMU is the last written by the CPU.

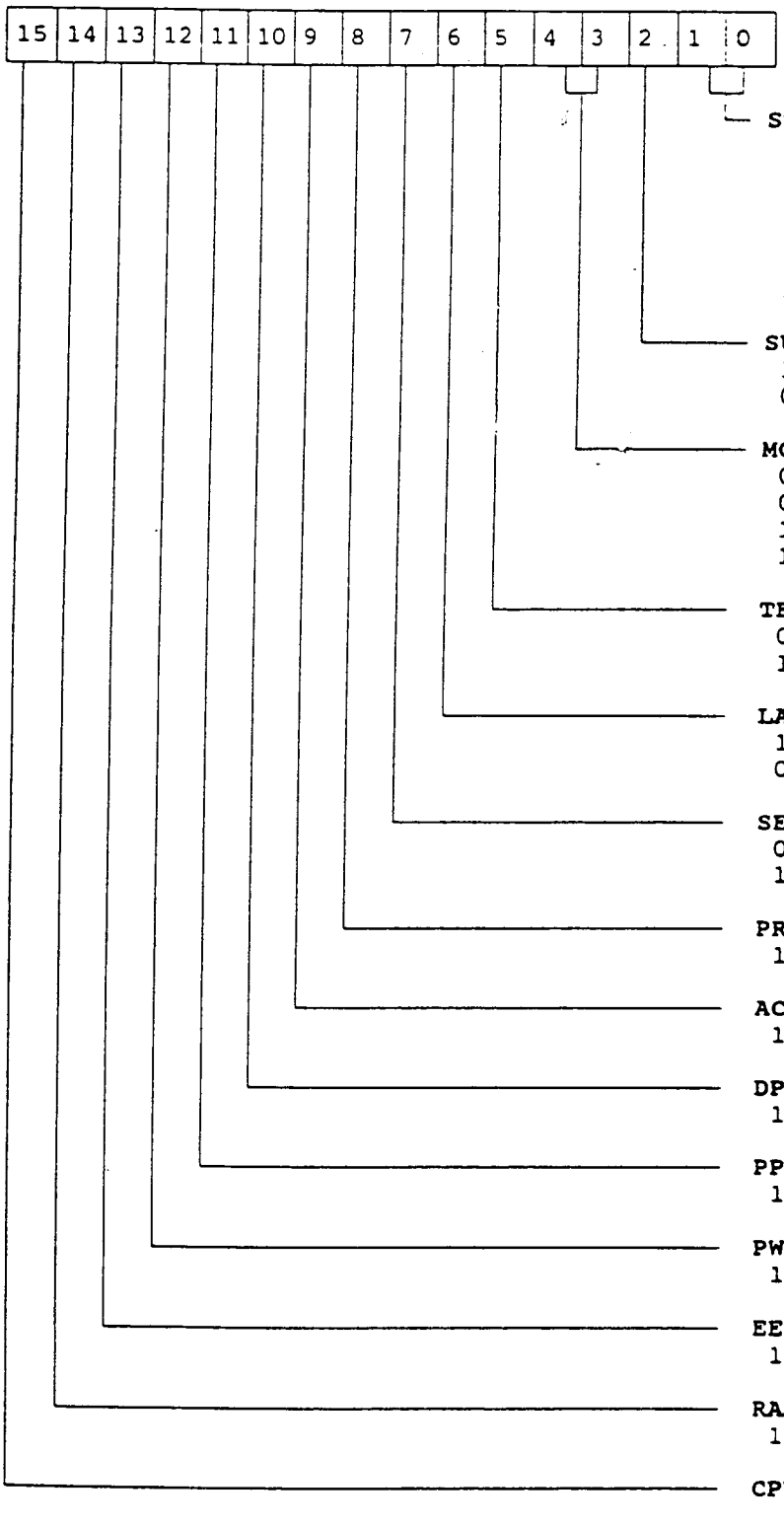
When one of the two CDMU requires a status word transmission it activates the corresponding SAMPLE line (this line is deactivated by the CDMU when transmission of the status word is completed), and supplies the clock signal to shift-out the data from the shift-register.

The address of status word register is : 7E20.

SUMMARY OF FEATURES :

- 16 bit register I/O access word instructions
- all 16 bit cleared at Power-on reset
- read each 16 Sec. by CDMUs (CDMS cycle rate)
- I/O address 7E20

LAYOUT BIT ASSIGNEMENT



3.2.2.2 PACKET TM I/F

The Packet tm i/f is a serial digital data channel to send the science data packet to the CDMU.
Two fully indipendent i/f are available on the CDMS I/F board.
For each interface, the differential lines interfacing with the CDMU are:
DATA line to CDMU.
SAMPLE line from CDMU.
PACKET READY line to CDMU: sw command, only this.
CLOCKline fromCDMU.(shared with StatusI/F channel).

Each interface is composed of a 16 bit shift register.When a packet of data is available, the HASI-DPU-SW sets the PACKET READY line to the CDMU; one for each word the CDMU asserts the SAMPLE signal to the DPU; this signal generates a dma- request to the DMAC; data is transferred from memory to the Packet tm serial shift register by DMAC, then the CDMU supplies the clock signal to shift-out the data from the shift register (refer to figure 3.6.4.9b section 3.6 of EID part A).

The addresses for setting the Packet-Ready lines are:

Packet Ready line A : set writing to address 7E80 (D0=1)
Packet Ready line B : set writing to address 7E80 (D1=1)

SUMMARY OF FEATURES :

- 2 PACKET TM I/F : 1 for CDMU A 1 for CDMU B

- PACKET TRANFERRED BY DMA CHANNELS:
  0 for CDMU A 1 for CDMU B

- PACKET READY SIGNALED BY ENABLING "PACKET READY" LINES AT ADDRESS 7E80 (byte I/O)
  bit 0 set/reset enable/disable data ready A
  bit 1 set/reset enable/disable data ready B

- DMA STARTS ACTUAL TRANSFER UPON CDMU POLLING :
after HASI-DPU-SW asserts one PACKET READY LINE the concerned CDMU asserts the related sample line and collects data tranferred by DMA channel, the PACKET READY LINE is reset on the falling edge of the sample line (i.e. just when the first word transfer is initiated).

- DMA may provide EOP INT #2 (low priority) for each channel

- PACKET READY LINES ARE INACTIVE (0) AT RESET, EITHER COLD AT W.D.

3.2.2.3 ML+BCP LINE SELECTION MUX

The two memory load lines A/B and the two BCP lines A/B selected by one dedicated MUX

- MUX I/O address = 7EC0 byte access (shared location)
- bit # 4 of 7EC0 = 0/1 --> lines B/A are selected
- lines B are selected at Power-on reset

3.2.2.4 MEMORY LOAD I/F

This interface is used to transmit command and data (or program patches) from the CDMUs to the DPU.
Two indipendent channels are used, one for each CDMU, with separate line receivers.

Data received from CDMU are 1 complemented.

The following lines are used for data transmission:

DATA line to CDMU-A.
ADDRESS line from CDMU-A.
CLOCKline from CDMU-A.

DATA line to CDMU-B.
ADDRESS line from CDMU-B.
CLOCKline from CDMU-B.

The HUYGENS Probe is operating with both CDMUs active.
The Processor VALID is provided to give experimenter indication of HEALTH of CDMU-A only.
The HASI-DPU-SW (HASI Experiment) has active one CDMU (ML lines) at a time.
The HASI-DPU-SW decides which of the two CDMU channel with the criteria given in UR-3.1.3-2.1 and in UR-3.1.8.

The selected channel is connected to the serial-to-parallel converter (SIPO), which uses two 8 bit shift registers (54HCT299); incoming data are shifted in by clock pulses.

Data is read from these devices using DMAC (channel 2); a DMA tranfer request is generated for each rising edge of the ADDRESS line.

Map of the I/O registers for Memory Load I/F:

VALID read	(RD)	7EA0	D3=0 line A health
			D3=1 line A not health

3.2.2.5 BCP I/F

This i/f is used in the DPU to receive the Broadcast Pulse; this signal which is generated by the CDMU synchronizes the activities of the experiments.
As for the M/L interface, two indipendent channels are used, one for each CDMU, with separate line receivers; again, the LINE MUX selects which of the two channels use.

The BCP pulse is used in the HASI-DPU-SW:

- to generate an interrupt to the CPU.

- to clear a time counter; this counter is used to measure the elapsed time since the last BCP by reading it "on the fly", while counting, this counter is implemented in the CPU board, using one of the three timer/counters in the 82C54 device (Mode 5 - hardware triggered strobe).

SUMMARY OF FEATURES :

- upon receiption of BCP pulse from selected line (8Hz rate) generates INT #1 and clears timer 1 of TIMER A

3.2.2.6 VALID I/F

Map of the I/O registers for VALID I/F:

VALID read	(RD)	7EA0	D3=1 line A health D3=0 line A not health

3.2.2.7 DMA HS82C37A MANUAL HARRIS DIG. MIL. 1989 pag 5-3

This device (HS-82C37A) is used for fast data transfer from CDMU to DPU RAM memory (Memory Load i/f channels A/B) and from DPU RAM memory to CDMU (Packet i/f channels A/B), the DMAC also executes data transfer from ACC, ADC to DPU memory.

The four programmable channels on this DMAC are used in this order:

- channel 0: memory to I/O - Packet i/f line A
- channel 1: memory to I/O - Packet i/f line B
- channel 2: I/O to memory - Memory Load i/f line A/B
- channel 3: I/O to memory - ACC sampling

The first three channels are dedicated to CDMU interfacing.

The other DMAC channel is dedicated to ACC data transfer, in this case the ACC data, sampled by an A/D converter in the AD+TEM module , are transferred to DPU I/F RAM memory driven by timer A2 (about 3200 hz)

All the DMA data tranfers are composed of 16 bit data words, the data are located in memory even addresses.

The handshake between DMAC and CPU is made by HOLD/HOLDA signals.
When a device requires a data transfer to or from memory, it generates a dma-request on its dedicate dma channel.
The DMAC sends a HOLD request to the CPU; when the CPU swicthes to HOLD state, it answers to DMAC with the activation of HOLDA signal (HOLD Acknowledge), this signal indicates that the CPU has relinqueshed control of system busses to DMAC.

In case of CDMU data transfer (DMA channels 0,1,2) the CDMS I/F module bus interface is completely disabled (Address/Data bus and RD/WR control lines from CPU) and the data are transferred to or from CDMS I/F and RAM memory.

In the case of ACC data transfer Address bus andRD/WR control lines from CPU are disabled and the data from AD+TEM board are transferred to CDMS memory.

The software can program the DMAC in order to generate an interrupt request at the end of transfer operation. (EOP function, INT #2)

The base address for reading and programming the internal register of DMAC is : 7E00 (I/O byte access on even address).

- 4 channels programmable for I/O ↔ memory transfer

- base I/O address 7E00 byte access.

3.2.2.8 MCA I/F

- 2 bit of an 8 bit register used for driving of MCA1 and MCA2
- base address = 7ED0 (used in common) I/O byte
- bit # 7 drives MCA 2 set = on
- bit # 6 drives MCA 1 set = on
- 1 bit register used for MCA driving enable
- base address = 7EC0 byte I/O access
- bit # 0 set enable MCA driving
- 3 bit of a 4 bit register used for MCA status reading
- base address = 7EB0 i/o BYTE (used in common)
- bit # 0 set/reset → absence/presence of MCA energise
- bit # 1 set/reset → MCA 1 not activated/activated
- bit # 2 set/reset → MCA 2 not activated/activated

(- bit # 3 used by TEM A/D EOC)

Since the MCA activation is a critical function, some protection is expected in the MCAs command interface design. The MCA power interface is distinguished from this circuit; it is located in the DC/DC converter module. The power driver is commanded by two indipendent signals. Two separated registers are foreseen:

- control register (MCA_CNTRLREG) has the following function: to select the MCA to be activated (MCA_SEL bit), to enable the activation register (MCA_ENABLE bit) and to command OFF the activation signals (MCA_OFF bit).

- activation register (MCA_ACTREG) generates the start of the MCA activation pulse.

Both registers are reset at power-on or after watch-dog timeout. This guarantees that the electronic switches in the MCAs power driver are OFF even if the software crashes. The following control_sequence shall be performed to execute the MCA activation procedure.

MCA pulse generation:

1) reset MCA_SEL bit, set MCA_ENABLE and MCA_OFF bits in control register.
2) clear MCA_ACTREG.

at this point the MCA driver is active...

...after the wished pulse duration time

3) the MCA_DRIVER may be deactivated by reset of MCA_OFF bit in control register MCA_CNTRLREG

After the MCAs pulses sequence generation the software resets the MCA_ENABLE and MCA_OFF bits in the control register as safety measure.

NOTE: to initiate the MCA activation, the software must write in two different memory location. This guarantees unexpected commands.

MCAs monitor interface

In the MCA power driver, the activation is enabled by two distinguished relays. Each MCA activation signal (generated by the MCAs command interface) pulls the relevant relay coil via a transistor. Each relay has two contacts: one enables the MCA power driver and the other can be used to monitor if the relay has been switched-on. The status of the these two relays is observed by software reading the MCAs monitor register bits, MCA_STATUS. The MCA power driver monitors the Protected Power presence via a relay; in fact the Protected Power supplies a relay coil and one of the two contacts are used to monitor it in the MCA monitor interface. The software checks this reading a bit the MCAs monitor interface.

MCA_CNTRLREG : 7EC0 byte

MCA_SEL	D7: 0 = MCA1, 1 = MCA2 selected
MCA_ENABLE	D6: 1 = enable, 0 = disable sequence
MCA_OFF	D5: 1 = enable control sequence, 0 = switch off immediately MCA driver and disable control sequence

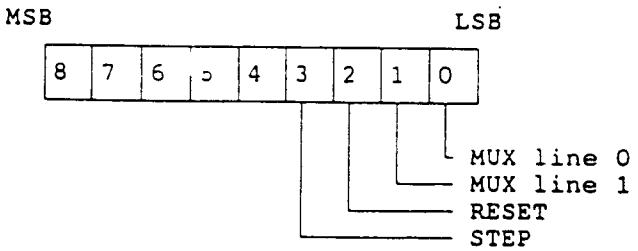
MCA_ACTREG : 7E40 byte

MCA_STATUS : 7EA0 byte shared

MCA_ENER	D0: 0 = presence, 1 = absent
MCA1_MON	D1: 0 = relay active, 1 = relay disactive
MCA2_MON	D2: 0 = relay active, 1 = relay disactive

3.2.2.9 PPI FREQUENCY CHANNEL SELECTION REGISTERS

- bit # 0..3 of an 8 bit I/O Write register (address = 7EC0h) are used for selecting the PPI frequency to be measured



- bit #0 and #1 select one among blocks 0..3 according to the following table :

block #	bit #1	bit#0
3	0	0
2	0	1
1	1	0
0	1	1

- bit #2 set : assert reset line

- bit #3 set : assert step line.

SELECTION OF A PPI FREQUENCY CHANNEL:
(from PPI specification document HASI-FMI-SYS-DOC-004 issue 1.0 of 29.4.93)

1) (not to be performed if block already selected)
select a frequency block 0..3 writing the MUX block selection pattern on bit #0,#1 as table above,
wait 10 microsecond before next operations 2) or 3)
wait 1 millisecond before next operations PPI_OUT measure

2) (mandatory if block selection performed) dispose PPI_OUT line to first freqency channel of the current block by means of a square wave clear-set on bit #2 (RESET line) with clear duration (line low) of at least 10 microsecond

Distance from another step or reset must be at least 10 microsecond

3) (not mandatory) dispose PPI_OUT line to NEXT frequency channel of the current block by means of a square wave clear-set on bit #3 (STEP line) with clear (line low) duration at least 10 microsecond.

Distance from another step or reset must be at least 10 microsecond

AT THE LAST CHANNEL OF THE BLOCK THE RESET OPERATION MUST BE PERFORMED IF RESTART FROM FIRST CHANNEL IS WISHED

4) T1 = at least 15 millisecond after 1) or 2) or 3) the desired frequency channel shall be stable at PPI_OUT line and the measurement of chapter 3.2.1.6 may be performed.

T1 > 15 --> fine

T1 > 2 --> rough

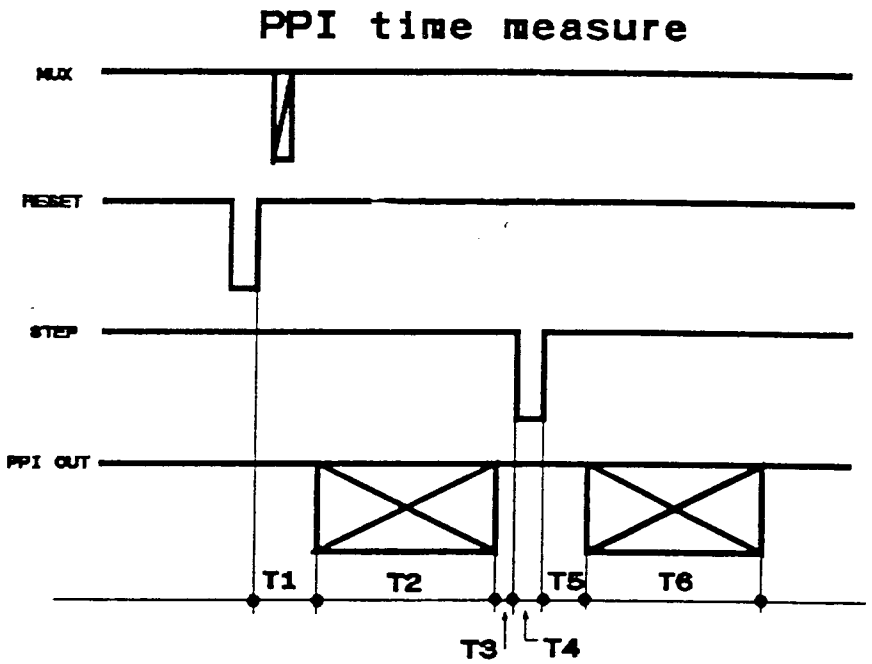


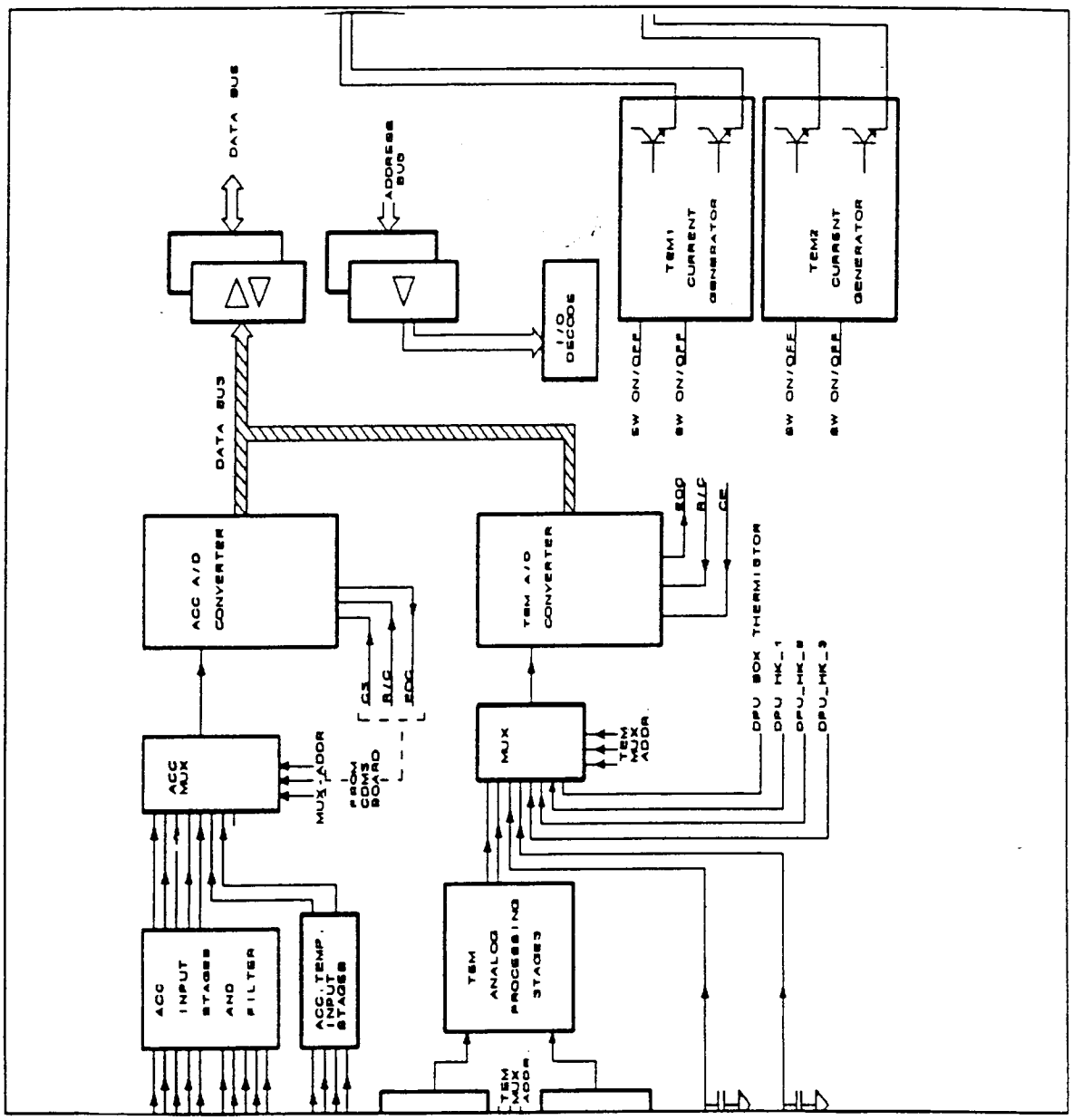
Figura 15 PPI TIMINGS

3.2.3 A/D + TEM BOARD

UR-3.2.3.1 GENERAL DESCRIPTION

The A/D + TEM board implements the functions of analog processing and acquisition for ACC and TEM sensors and other housekeeping signals.

A block diagram for this board is shown hereafter :



3.2.3.2 ADC 1

UR-3.2.3.2 ADC 1 (ACC SECTION)

The ACC section is composed of :

- five differential input stage (unity gain) for ACC signals.
- five low-pass filters.
- two differential input stages (unity gain) for ACC temperature signals.
- an eigth inputs multiplexer stage.
- A/D converter.
- Range control signals i/f.

A block diagram for ACC interface is shown in figure 17:

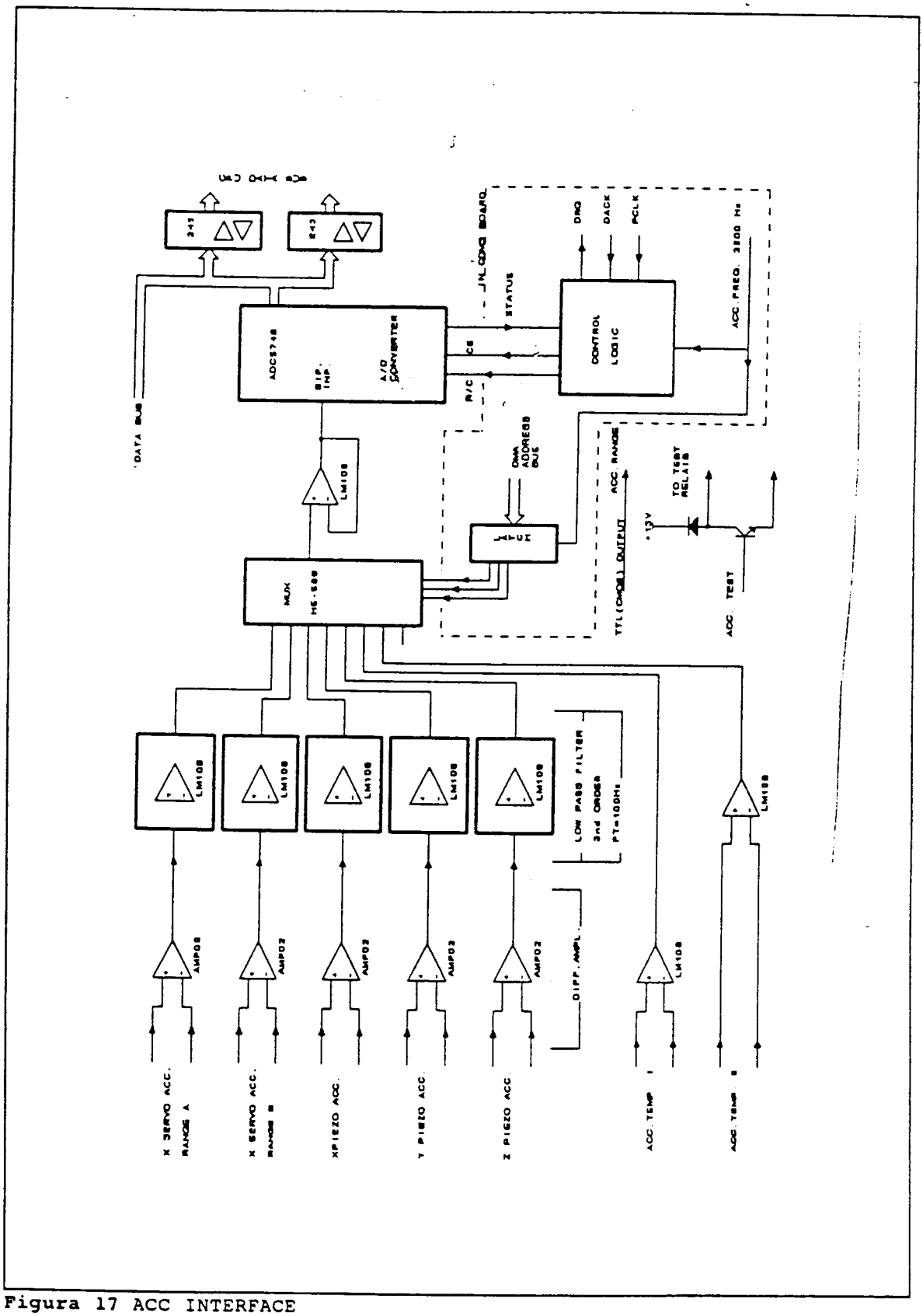


Figura 17 ACC INTERFACE

Input stages and filtering.

A differential instrumentation amplifier with unity gain (type LM108) is used for each of the five ACC channels:
The output of these amplifiers are connected to the low pass filter (Butteworth type filters) are used with unity gain, the -3 dB cut-off frequency is for all channels 100 Hz.

ACC temperature input stages.

Two differential instrumentation amplifiers with unity gain (LM108) are used for the ACC temperature signals.

Multiplexer stage.

An 8 inputs analog multiplexer (HS508A) selects the analog channel for A/D conversion as the following table:

Channel	Signal	MEMO ADD (words)
0	X servo low gain	1
1	X servo high gain	2
2	X piezo	3
3	Y piezo	4
4	Z piezo	5
5	Temperature 1	6
6	Temperature 2	7
7	Signal Gnd	8 or 0

Since ACC acquisition is performed using DMA technique for minimum CPU and software overhead, the channel selection is under DMAC control. The number of the selected channel is directly related to the DMA generated memory address (bits A3,A2,A1 select the analog channel (offset of one word as in above table); A0 is not used since word transfer cycles are executed.).

A/D conversion

A monolithic 12 bit bipolar Analog-to-Digital (± 10 v) converter is used (AD574A type), using the successive approximation technique; the clock is internally generated and one conversion requires about 35µs. This converter is controlled by a hardware logic; this logic triggers a periodic conversion (3200 Hz) and controls the A/D readout and the related DMA channel.

3.2.3.3 ACC XSERVO RANGE SELECTION

UR-3.2.3.3 ACC XSERVO RANGE SELECTOR

One digital CMOS-5V output signal is implemented in the A/D+TEM board in order to switch the X-servo range in the ACC sensor electronics.

- 1 bit of an 8 bit register (used in common) select FINE/COARSE range (bit D6 at 5D00 I/O address)

3.2.3.4 ACC XSERVO TEST SWITCH

UR-3.2.3.4 DELETED

3.2.3.5 RESOLUTION

UR-3.2.3.5 RESOLUTION

The resolution (LSB weight) is:

$$\frac{10V}{2048} = 5 \text{ mVolts} .$$

for the 7 measurement channels.

UR-3.2.3.6 ADC 2 (TEM & HK ADC CHAIN)

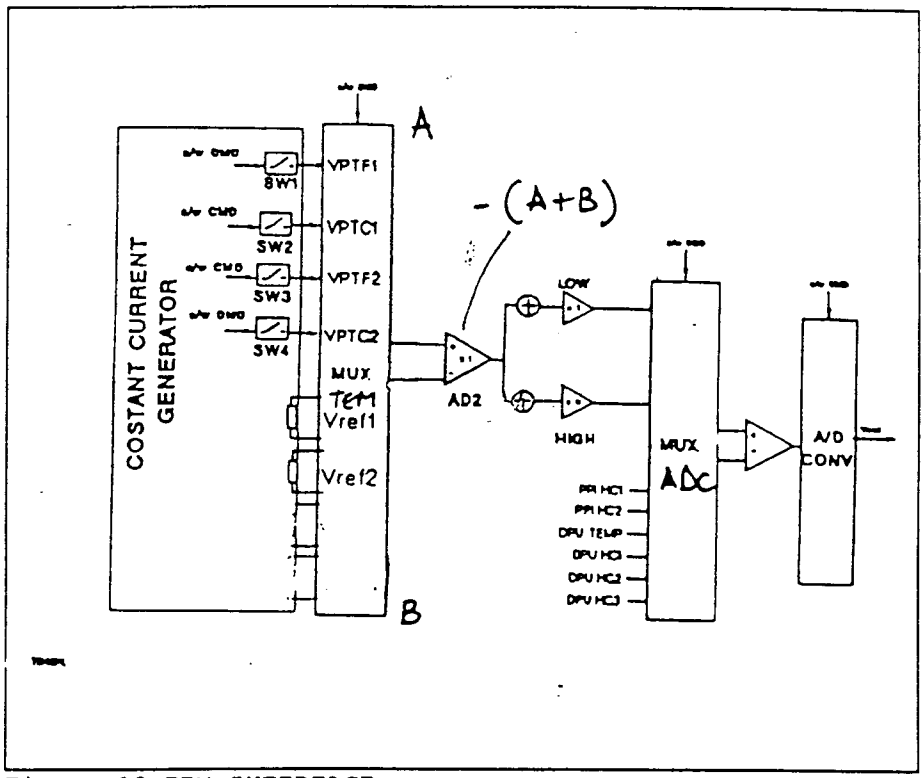


Figura 18 TEM INTERFACE

- single shot 12 bit sample unipolar in range 0÷10V

- conversion is driven by Start Of Conversion - End Of Conversion command - acknowledge

UR-3.2.3.6.1 A/D Start/End conversion

1. Reset bit D7 at 5E00H I/O address (set conversion mode)

2. Write any bit pattern at 5C00H I/O address (start of conversion)

3. Set bit D7 at 5E00H I/O address (set readout mode)

4. Reading bit D0 at 5F00H I/O address: if bit = 0 the conversion is ended (wait of END conversion)

5. 12 bit sample precision are read as 16 bit word right justified at 5C00H I/O address.

UR-3.2.3.6.2 MUX addresses

MUX TEM A (differential) Register at 5D00 I/O address

D2	D1	D0	Ch.	
0	0	0	$+V_{PTF1}$	FINE1
0	0	1	$+V_{PTC1}$	COARSE1
0	1	0	$+V_{PTF2}$	FINE2
0	1	1	$+V_{PTC2}$	COARSE2
1	0	0	$-V_{REF1}$	RIF.range (100k-330k)
1	0	1	$-V_{REF2}$	RIF.range (60k-110k)
1	1	0	$+V_{REF1}$	RIF.range (100k-330k)
1	1	1	$+V_{REF2}$	RIF.range (60k-110k)

MUX TEM B (differential) Register at 5D00 I/O address

D5	D4	D3	Ch.	
0	0	0	$+V_{PTF1}$	FINE1
0	0	1	$+V_{PTC1}$	COARSE1
0	1	0	$+V_{PTF2}$	FINE2
0	1	1	$+V_{PTC2}$	COARSE2
1	0	0	$-V_{REF1}$	RIF.range (100k-330k)
1	0	1	$-V_{REF2}$	RIF.range (60k-110k)
1	1	0	$+V_{REF1}$	RIF.range (100k-330k)
1	1	1	$+V_{REF2}$	RIF.range (60k-110k)

MUX AD (C) (single ended) Register at 5E00 I/O address

D2	D1	D0	Ch.
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

0 MUX TEM OUT X LOW GAIN 60K ÷ 110K RANGE
1 MUX TEM OUT X HIGH GAIN 100K ÷ 330K RANGE
2 PPI HK V1
3 PPI HK V2
4 DPU HC3 + 5 Vdc (HK of + 5V power supply)
5 DPU HC2 + 7.5 Vdc (HK of + 15V power supply)
6 DPU HC1 + 7.5 Vdc (HK of + 15V power supply)
7 DPU BOX TEMP

UR-3.2.3.7 TEM CURRENT GENERATOR SWITCHING SEQUENCES

- after h/w reset the current generators are OFF.

- only 1 current generator at time is switched on.
50 msec of maximum switch-on time shall be foreseen (for each 1.5 sec period ?).

UR-3.2.3.7.1 Switch-on

1 - select sensor PTx current generator using the D3, D4 and D5 bits (according to the below table) of register at 5E00H I/O address.

2 - wait 100 μsec (maximum = 300 μsec).

3 - set D6 bit at 5E00H I/O address.

NOTE: x = F1, C1, F2, C2

UR-3.2.3.7.2 Switch-off

1 - reset D6 bit at 5E00H I/O address.

2 - wait: min 2msec, max 4msec.

3 - reset D3, D4 and D5 bit at 5E00H I/O address.

D5	D4	D3	5E00H I/O write
0	0	0	RESET
0	0	1	unused
0	1	0	unused
0	1	1	unused
1	0	0	TEM1 COARSE (PTC1)
1	0	1	TEM1 FINE (PTF1)
1	1	0	TEM2 COARSE (PTC2)
1	1	1	TEM2 FINE (PTF2)

3.2.3.8 TEM READING

UR-3.2.3.8.1 TEM reading methode

The temperature measurement consistes to inject a current in the sensor head and a reference resistor and measure the two voltages V_{PTF}, V_{REF}.

Infact, supponing that the current is constant during the measure, from the ratio:

$$\frac{V_{PT}}{V_{REF}} = \frac{I\ R_{TF}}{I\ R_{REF}} = \frac{R_{TF}}{R_{REF}}$$

will be obtained the temperature.

The HASI-DPU-SW measures the following voltages:
$(2(V_{PT} - V_{REF}))$ and $(2V_{REF})$ and it sends them to ground via TM.

At ground these values shall be processed via:

$\frac{(2(V_{PT} - V_{REF}))}{(2V_{REF})} + 1$ to obtain the above formula this methode compensates the gain errors of TEM analog chain.

The temperature shall be measured in two ranges with different performances:

Range 100k - 330k
(LOW GAIN CHANNEL) with resolution of 0.07k

Range 60k - 110k
(HIGH GAIN CHANNEL) with resolution of 0.02k

3.2.3.8.2 (SENSOR AND REFERENCE) AND OFFSET MEASUREMENT

UR-3.2.3.8.2.1 Measurement of (sensor and reference)

$(2(V_{PTx} - V_{REFy}))$ and $(2V_{REFy})$

1. Switch on current generator x (according to 3.2.3.7.1)
2. Set MUX AD C on channel 0 or 1 depending on selected gain channel
3. Set MUX TEM A on ($+V_{PTx}$) channel
4. Set MUX TEM B on ($-V_{REFy}$) depending on selected gain channel
5. Wait at least 10 msec
6. Read 8 times and sum the values (RES. = ADC LSB / 8)
7. Set MUX TEM A on ($-V_{REFy}$) channel
8. Set MUX TEM B on ($+V_{PTx}$) channel
9. Wait at least 10 msec
10. Read 8 times and sum the values (RES. = ADC LSB / 8)
11. $2(V_{PTx} - V_{REFy}) = V_{1M} + V_{2M}$
12. Set MUX TEM A on ($+V_{REFy}$) channel
13. Set MUX TEM B on ($+V_{REFy}$) channel
14. Wait at least 10 msec
15. Read 8 times and obtain $2V_{REFy}$ (RES. = ADC LSB / 8)
16. Switch off current generator x (according to 3.2.3.7.2)

NOTE1: x = F1, C1, F2, C2 ; y = low, high

NOTE2: the $V_{PTx} - V_{REFy}$ value is 16 bits

UR-3.2.3.8.2.2 Measurement of (sensor and ref) offsets

Executes points from 2 to 15 of 3.2.3.8.2.1 (i.e. current generators remain switched off).

3.2.4 PWA DATA LINK PROTOCOL

UR-3.2.4-1 The phisycal level of the PWA interface consists in a 8 bit parallel port that allows exchanging of information only in one direction at a time. The HW provide signals for completions of read (RX) or write (TX) single byte operations.

UR-3.2.4-2 As the DPU HW does not provide any information about the current busyness of the line, the two communicating processes (DPU and PWA) shall synchronize the messages exchange on a time basis and a predefined order of TALK/LISTEN states transition as depicted here after.

- At Power on/reset HASI-DPU-SW shall configure as TALKER and PWA as LISTENER

- The HASI-DPU-SW shall transmit 1 SB every 2 seconds with 100 msec accuracy.

- PWA doesn't transmit data blocks until it receives a complete SB.

- PWA transmits ALWAYS two data blocks (nominally 2 TM packets) between two SB, soon after the reception of the SB and 0.5 sec before the next (rough values)

- The HASI-DPU-SW in case of I/F conflicts, discovered by means of a 100 msec timeout on the device either when TALKING or LISTENING, shall reconfigure itself as a **2 second period** TALKER.

- PWA in case of I/F conflicts, discovered by means of a 150 msec timeout on the device when TALKING, shall reconfigure itself as a LISTENER.

The following figures summarize the above sentences.

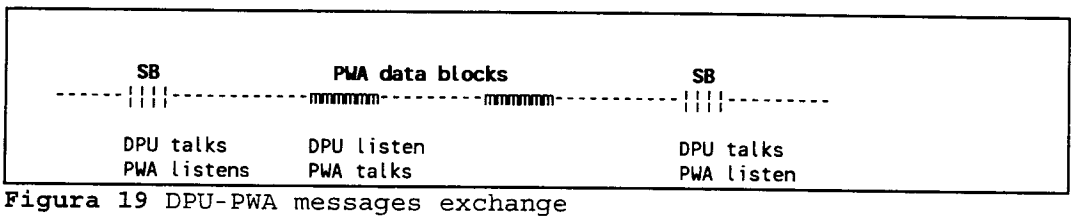


Figura 19 DPU-PWA messages exchange

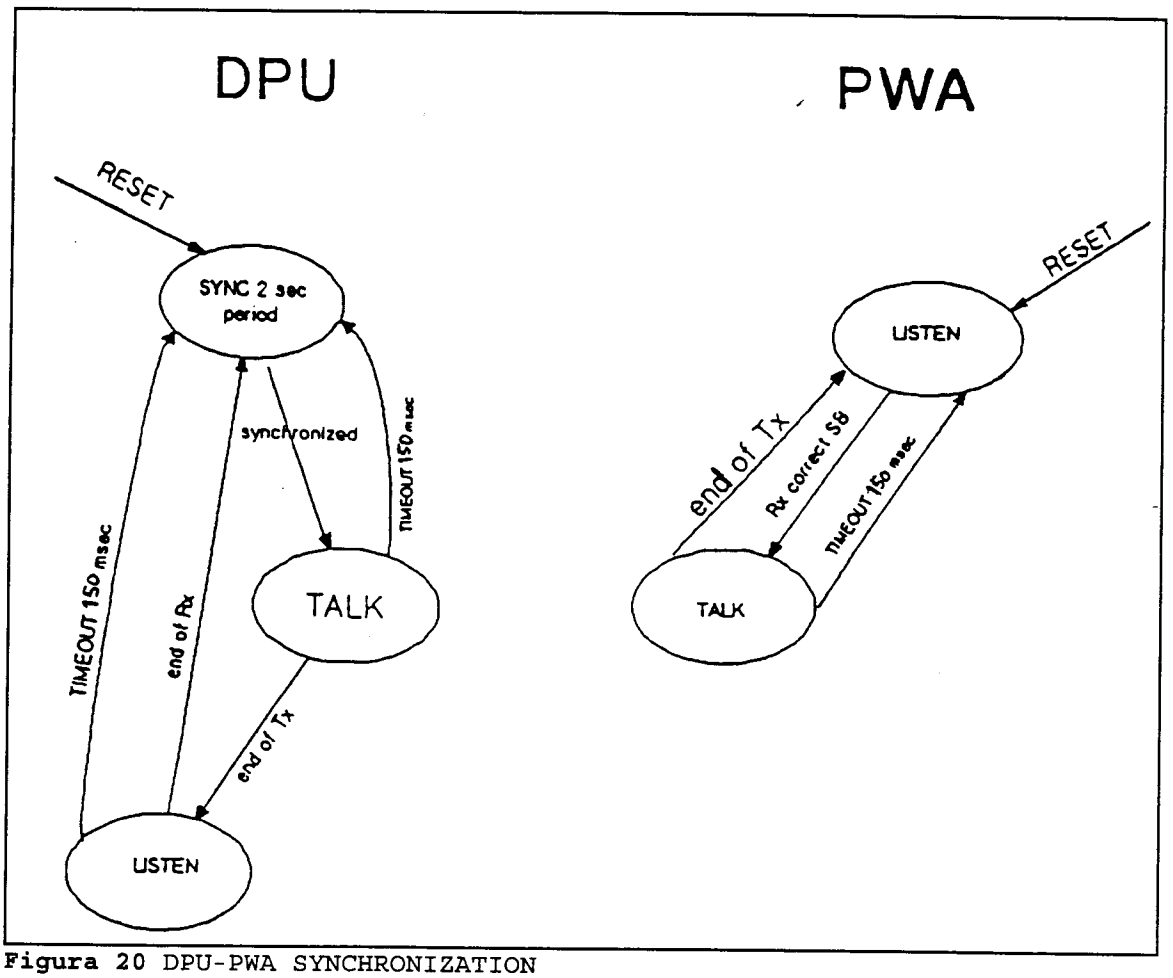


Figura 20 DPU-PWA SYNCHRONIZATION

UR-3.2.4-3: For each timed out or uncorrectly received PWA data block the HASI-DPU-SW shall :

- Tx it to the CDMS flagged as "CORRUPTED" after TdataH (i.e. only after DESCENT 1st).

- record the event in the mission history data (e.g. using the SEQUENCE count and/or the MISSION time)

UR-3.2.4-4: PWA ---> HASI-DPU-SW TM packets lay-out

The data block sent by PWA shall be conform to Standard ESA TM packets of 120 bytes composed as follows:

- HEADER (6 bytes)
- DATA FIELD HEADER (1 byte)
- DATA FIELD (112 bytes)
- XOR (1 byte)

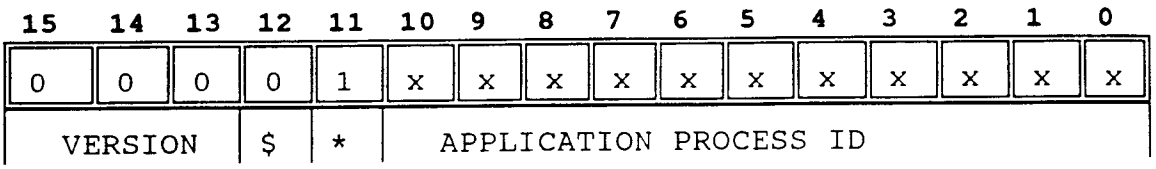
BYTE #	VALUE	MEANING
1		**PACKET IDENTIFIER (ver + flags + app proc id)**
2		
3	high	**PACKET SEQUENCE COUNT**
4	low	
5	high	**PACKET LENGTH (fixed to 115)**
6	low	
7	data type	**DATA FIELD HEADER**
8	112 bytes	**DATA FIELD**
...		
119		
120	XOR 1-119	**PACKET ERROR CONTROL**

UR-3.2.4-4.1 3 different application ID shall be foreseen in the PACKET ID field to distinguish between

- SCIENCE data packets
- TEST data packets
- HC data packets

The following figure detail the PACKET ID field.

PACKET IDENTIFICATION FIELD DETAILED



x := variable 0 / 1

$: 0 means Telemetry packet

* : 1 means data field header present

UR-3.2.4-4.2 The PWA SCIENCE data packets shall be identified by the packet id = **083F hex** (APPLICATION PROCESS ID = **00000111111b**)

UR-3.2.4-4.3 The PWA TEST data packets shall be identified by the packet id = **0FE0 hex** (APPLICATION PROCESS ID = **11111100000b**)

UR-3.2.4-4.4 The PWA HEALTH CHECK data packets shall be identified by the packet id = **0800 hex** (APPLICATION PROCESS ID = **00000000000b**)

UR-3.2.4-5 The DATA type (DATA TYPE FIELD HEADER) shall distinguish different data packets.

UR-3.2.4-5.1 The DATA type shall be in range 128 to 159 (decimal value). The meaning of each Data type field header is reported in the "TM packet DATA FORMATS LIST" in the IDS Annex 1 page 7.

UR-3.2.4-6 HASI-DPU-SW ---> PWA TC packets lay-out

The STATUS BLOCK sent by HASI-DPU-SW to PWA shall be conform to Standard ESA TC packets of 15 bytes composed as follows:

- HEADER (6 bytes)
- DATA FIELD (8 bytes)
- XOR (1 byte)

BYTE #	VALUE	MEANING
1	0001 0000	PACKET IDENTIFIER (ver + flags + app proc id)
2	1111 1111	
3	11 + high	PACKET SEQUENCE COUNT
4	low	
5	high	PACKET LENGTH (fixed to 9)
6	low	
7	from DDBL	DDBL MISSION PHASE
8	0-255	TEST COMMAND PARAMETER (*)
9	high	MISSION TIME (same DDBL format)
10	low	
11	from DDBL	PROBE ALTITUDE (from DDBL)
12		
13	from DDBL	PROBE SPIN RATE (from DDBL)
14	HASI-DPU STATUS	
15	XOR 1-14	PACKET ERROR CONTROL

(*) : 0 means no test command present
N means test command # N present

UR-3.2.4-6.1 MISSION TIME contained in bytes 9-10 of HASI-DPU-SW STATUS BLOCK shall be related to the trasmission time of byte 1 with an accuracy less than 1 BCP (125 msec).

UR-3.2.4-6.2 HASI-DPU-SW STATUS shall distiguished acccording to the following table

CONTENTS	MISSION PHASE
0	ENTRY
1	DESCENT 1st phase
2	DESCENT 2nd phase
3	DESCENT 3rd phase
4	(PRE)IMPACT
5	SURFACE

3.2.5 SW IN FLIGHT MANTAINANCE

3.2.5.1 MEMORY UPLOADING

UR-3.2.5.1-1: HASI MEMORY UPLOADING (physical address)

Within the RAM/EEPROM area defined in chapter 3.2.1.2, the HASI-DPU-SW shall be capable to replace the contents of the **physical addresses** specified in the "HASI LOAD MEMORY" Telecommand with the memory contents specified ibidem.

UR-3.2.5.1-2: DELETED

UR-3.2.5.1-3: DELETED

3.2.5.2 MEMORY DUMP

UR-3.2.5.2-1: The HASI-DPU-SW shall be capable to download via TM I/F every (SEGMENT;OFFSET) physical address defined in chapter 3.2.1.2 (EMPTY areas included) specified in the "DUMP MEMORY" Telecommand.

UR-3.2.5.2-2: DELETED

UR-3.2.5.2-3: DELETED

UR-3.2.5.2-4: For each "DUMP MEMORY" telecommand received a number of MEMORY DUMP TM packets shall be generated and transmitted to CDMS according to the NUMREC argument specified in the telecommand itself. A blocking factor may be defined in the HASI IDS to specify correspondance between dump records and TM packets.

UR-3.2.5.2-5: The MEMORY DUMP function completes when :

- the total number of records (or blocks) required by the TC arguments has been dumped

3.2.5.3 PROGRAM PARAMETERS UPLOADING

UR-3.2.5.3-1: DELETED

UR-3.2.5.3-2: DELETED

UR-3.2.5.3-3: DELETED

3.2.5.4 PROGRAM BLOCK UPLOADING

UR-3.2.5.4-1: DELETED

UR-3.2.5.4-2: DELETED

UR-3.2.5.4-3: DELETED.

3.2.6 QUALITY REQUIREMENTS

3.2.6.1 STANDARDS & METHODS

Refer to AD-2 ("HASI Software Project Plan issue 1" HASI-PL-OG-004).

3.2.6.2 TOOLS

Refer to AD-2 ("HASI Software Project Plan issue 1" HASI-PL-OG-004).

3.2.6.3 RELIABILITY REQUIREMENTS

UR-3.2.6.3-1: According to QUALITATIVE SPECIFICATION of software requirements defined in ESA-PSS-01-230 issue 1 the HASI-DPU-SW functions required in this document shall be grouped in the following categories :

high reliability (i.e. : the probability is .90 that the MTBF is 1,000 hours or more) :

- STARTUP
- TITAN DESCENT up to IMPACT subphase
- TELECOMMAND EXECUTION
- BOOM RELEASE

nominal reliability (i.e. : the probability is .80 that the MTBF is 200 hours or more) :

- TITAN DESCENT after IMPACT subphase
- ALL REMAINING SOFTWARE

APPENDIX A : LIST OF TBD

ANNEX 1 :

DPU SW INTERFACE DATA SHEET

- Telemetry Packets description
- Telecommand Packets description

TELEMETRY PACKET MANAGENENT

The TM packets shall be sent by DPU to CDMU's (each channel is indipendently and transmit at full CDMU polling rate) according to mission time as described in the following scheme.

1) During DPU Startup (~ 16 sec) no TM packet is sent.

2) Up to TdataH TM packets are sent to CDMUs while their copies are kept in the DPU memory.

3) After TdataH TM packets are sent to CDMUs without storing any copy (nominal transmission).

4) As soon as the TC is received by DPU (in CHECKOUT mode) the TM shall be managed as in pto 3) without regard of mission time.

The TC packets shall be accepted and executed by DPU only in CHECKOUT MODE.

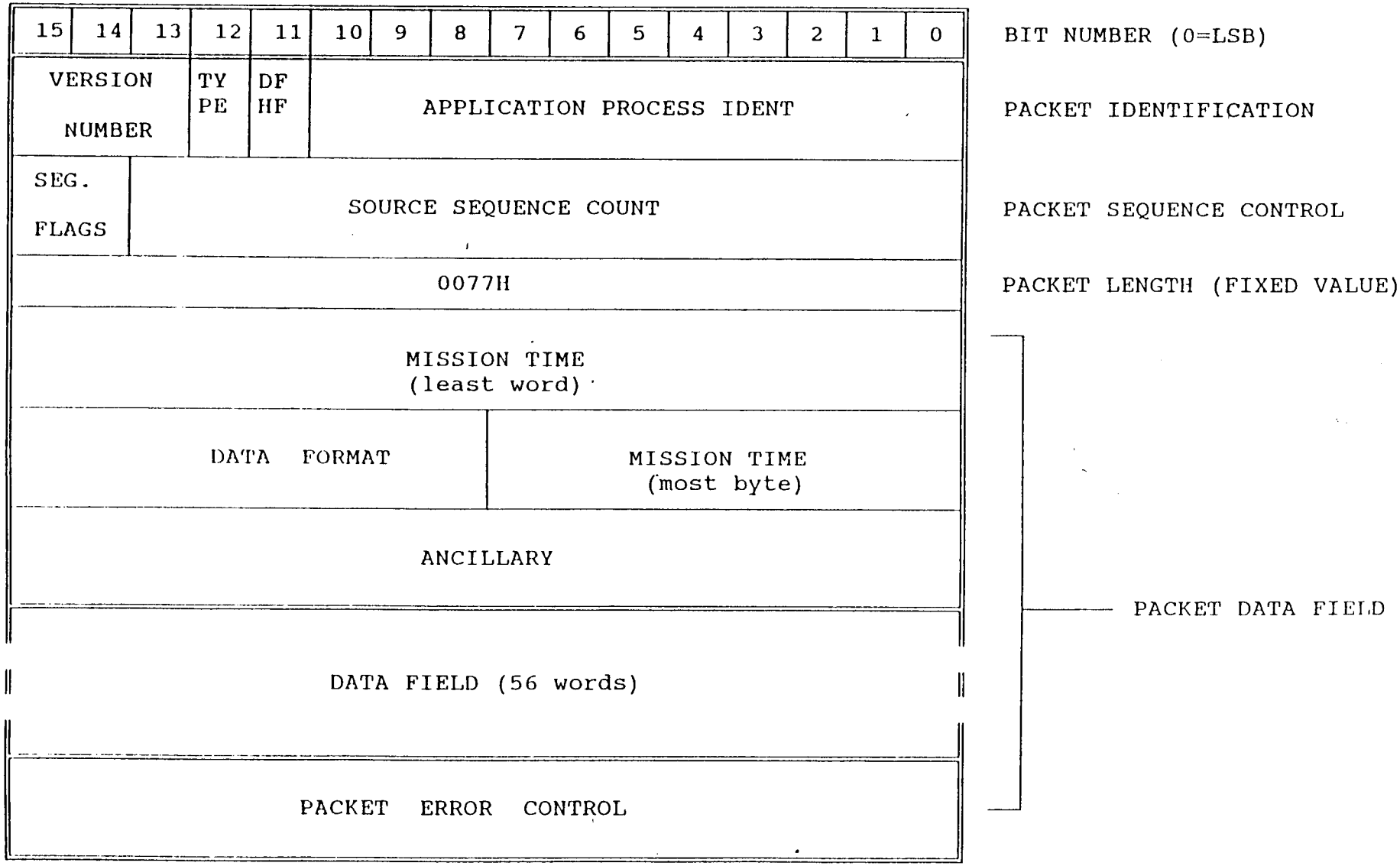


FIGURE A : TELEMETRY PACKET DESCRIPTION

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FIELDS CONTENT (referring to FIGURE A)

- **PACKET IDENTIFICATION** (16 bit): This field is divided into VERSION NUMBER, TYPE, DATA FIELD HEADER FLAG and APPLICATION PROCESS IDENT.

  VERSION NUMBER (3 bit): It's a 3-bit field occupying the three most significant bit of a packet structure.
  The Version Number is fixed to :
  Bit 15 through 13 = 0 0 0

  TYPE (1bit): It indicates either Telemetry Type or Telecommand Type. In this case bit 12 = 0.

  DATA FIELD HEADER FLAG (1bit): It indicates the presence or absence of a Data Field within the PACKET DATA FIELD. In this case bit 11 = 1.

  APPLICATION PROCESS IDENT (11 bit): It's an 11-bit field uniquely identifying phisical source. In this case: bit 10 through 0

  11110010001 for CDMUA
  11110110001 for CDMUB.

- **PACKET SEQUENCE CONTROL** (16 bit): This field is divided into SEGMENTATION FLAGS and SOURCE SEQUENCE COUNT.

  SEGMENTATION FLAGS (2 bit): In the TM Packet the Segmentation Flags shall always be set to "all one".
  . Bit 15 through 14 = 1 1

  SEQUENCE COUNT (14 bit): It counts the number of packets sent. It resets after 16384 packets or after an experiment power up.

- **PACKET LENGTH** (16 bit): It's a 16-bit field which specifies the number of octets contained within the Packet Data Field. The number is a binary value C:

  C = [(Number of octets in Packet Data Field)-1]

  In this case bit 15 through 0 :

  0000000001110111

- **PACKET DATA FIELD** (960 bit): This field is divided into MISSION TIME, DATA FORMAT, DATA FIELD and PACKET ERROR CONTROL.

  MISSION TIME (24 bit): Is the MISSION TIME interval (DDB counter, see EID A sect 2.2.3) when the first source data contained in the DATA FIELD was created.
  Resolution is LSB=1msec.

other data contained in the DATA FIELD can be easily computed according to their positions.

DATA FORMAT (8 bit): This field is divided into SOURCE NAME, TYPE NAME. It encodes the source and the type of data contained in the DATA FIELD.
The 256 possible data format codes are listed in the following TM PACKET DATA FORMAT LIST.

SOURCE NAME bit 7 - bit 5 (3 bit): It defines the source generating data.

SOURCE TYPE bit 4 - bit 0 (5 bit): It defines the type of data.

ANCILLARY (16 bit): This field is divided INDEX and STATUS PACKET.

(L) INDEX (8 bit): It shall contain the index of the last valid byte when incomplete, "0" otherwise.

(H) DATA STATUS (8 bit): It shall contain the information about the DATA PACKET FIELD:

bit 6 - bit 7: spare

bit 5: original bit; 1 means: this packet has been redunded by one or more packet (refered to ENTRY PHASE)

bit 3 - bit 4: TT same of DDBL; referred to MISSION TIME:

01 = before T0
10 = after T0

bit 2: spare

bit 1: redundance bit; 1 means: this packet is a redundance of another packet (i.e. it is maintained in the memory)

bit 0: incomplete = 1, complete = 0

DATA FIELD (896 bit): This field shall contain the sampled data. The format of the data depends on the DATA FORMAT field contents. The possible data formats are depicted in the following pages.

PACKET ERROR CONTROL (16 bit): It is the XOR function computed on all the words starting from PACKET IDENTIFICATION (included) till the last DATA in the DATA FIELD, i.e. from WORD 0 to WORD 61 (extremes included).

TM PACKET DATA FORMATS LIST

FORMAT CODE	FORMAT NAME		BINARY VALUE		FILL RATE (sec)	DATA FIELD (bit)	XREF PAGE no.
	SOURCE	TYPE	SOURCE	TYPE			
0	DPU	STARTUP	000	00000	ONCE	11*80	9
1	DPU	spare	000	*			
2	DPU	spare	000	*			
3	DPU	HK EVENT LOG	000	00011	N.A.	16*56	11
4	DPU	spare	000	00100			
5	DPU	HC RATE 2 sec	000	00101	112	56*16	14
6	DPU	spare	000	00110			
7	DPU	DPU BOXTEM	000	00111	896	56*16	16
8 - 31	DPU	Spare	000	*			
32	ACC	SCDS.E	001	00000	16.64	52*(16+1)	18
33	ACC	SCDS.D	001	00001	12.48	52*(16+1)	20
34	ACC	SCDS.R	001	00010	29.647	52*(16+1)	22
35	ACC	SCDP.X	001	00011	34.72	56*16	24
36	ACC	SCDP.Y	001	00100	34.72	56*16	26
37	ACC	SCDP.Z	001	00101	34.72	56*16	28
38	ACC	HKD1	001	00110	571.43	56*16	30
39	ACC	HKD2	001	00111	571.43	56*16	32
40	ACC	STD2.XS	001	01000	378.88	37*24	34
41	ACC	STD2.XP	001	01001	378.88	37*24	36
42	ACC	STD2.YP	001	01010	378.88	37*24	38
43	ACC	STD2.ZP	001	01011	378.88	37*24	40
44-47	ACC	spare	001	*			
48	ACC	ID1	001	10000	0.28	56*16	42
49	ACC	ID2	001	10001	0.28	56*16	44
50	ACC	ID3	001	10010	0.28	56*16	46

TM PACKET DATA FORMATS LIST

FORMAT CODE	FORMAT NAME		BINARY VALUE		FILL RATE (sec)	DATA FIELD (bit)	XREF PAGE no.
	SOURCE	TYPE	SOURCE	TYPE			
51 - 63	ACC	spare	001	*			
64	PPI	SESSION #0	010	00000	43.2	36*24 + 16+16	48
65	PPI	SESSION #1	010	00001	43.2	36*24 + 16+16	51
66	PPI	SESSION #2	010	00010	43.2	36*24 + 16+16	52
67-69	PPI	spare	010	*			
70	PPI	HC SESSION #0	010	00110	5.55	37*24	53
71	PPI	HC SESSION #1	010	00111	5.55	37*24	55
72	PPI	HKV	010	01000	1792	28 * (16+16)	56
73 - 95	PPI	spare	010	*			
96	TEM	F1	011	00000	90	18*48	58
97	TEM	spare	011	*			
98	TEM	C1	011	00010	90	18*48	61
99	TEM	spare	011	*			
100	TEM	F2	011	00100	90	18*48	62
101	TEM	spare	011	*			
102	TEM	C2	011	00110	90	18*48	63
103 - 127	TEM	spare	011	*			
128	PWA	EM SCIENCE DATA	100	00000	6/7 pck every 16 sec	112*8	64
129	PWA	CORRUPTED PACKET	100	00001	SPORADIC	112*8	65
130	PWA	TEST DATA (EM+FM)	100	00010	6/7 pck every 16 sec	112*8	66
131	PWA	FM SCIENCE DATA type 0 ACDC	100	00011	6/7 pck every 16 sec	112*8	67
132	PWA	FM SCIENCE DATA type 1 ACDCAU	100	00100	6/7 pck every 16 sec	112*8	68
133	PWA	FM SCIENCE DATA type 2 RADAR	100	00101	6/7 pck every 16 sec	112*8	69
134	PWA	FM SCIENCE DATA type 3 MI	100	00110	6/7 pck every 16 sec	112*8	70
135	PWA	FM SCIENCE DATA type 4 RP	100	00111	6/7 pck every 16 sec	112*8	71
136 - 159	PWA	FM SCIENCE DATA type 5 - 28	100	01000 - 11111			

160	TC REPORT	TC ECHO	101	00000	ONCE	16+55*16	72
161	TC REPORT	MEMORY DUMP TM	101	00001	3	32+864	73
162	TC REPORT	MEMORY LOAD ECHO	101	00010	3	32+864	75
163 - 191	TC REPORT	spare	101	*			
192 - 225	spare	spare	*	*			

DATA FORMAT #0

TITLE : MEMORY STARTUP TEST REPORTS

SOURCE NAME : DPU

TYPE NAME : STARTUP #0

BIT UTILIZATION :

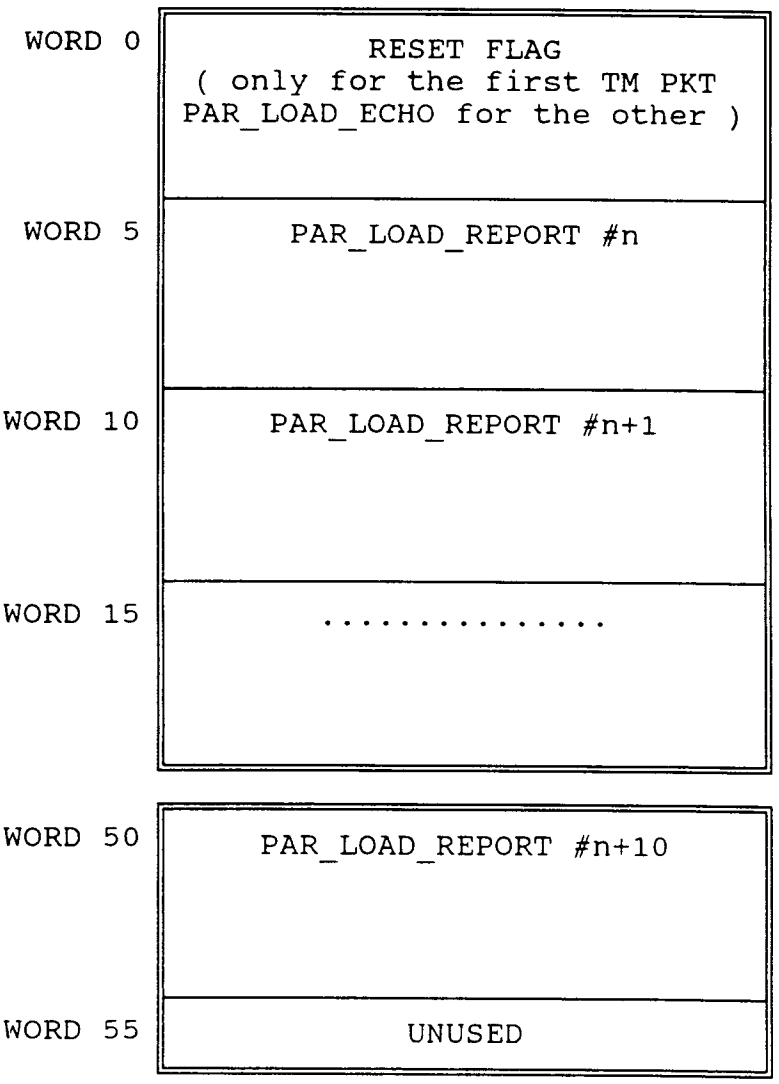
used	880 bit	(55 Word)	98.2%
unused	16 bit	(1 Word)	1.8%

FILL RATE : ONCE The # of packets varies according to the # of parameters containned in the EEPROM

DATA FIELD CONTENTS :

RESET FLAG + 10 PARLOAD REPORT OR 11 PARLOADREPORT

DATA FIELD LAYOUT :



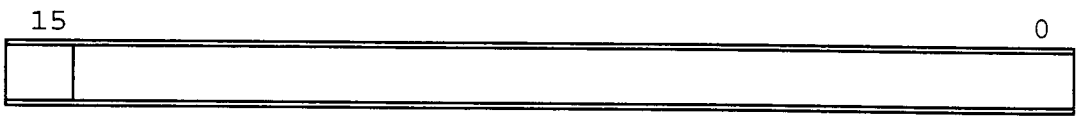
SUBFIELD NAME : RESET FLAG
SUBFIELD DESCR: Ascii string
SUBFIELD SIZE : 80 bit
SUBFIELD LAYOUT:

2° char	1° char
4° char	3° char
6° char	5° char
8° char	7° char
10° char	9° char

SUBFIELD NAME : PAR_LOAD_REPORT
SUBFIELD DESCR: parameter loading report EEPROM
SUBFIELD SIZE : 80 bit
SUBFIELD LAYOUT:

WORD 1	LOAD RESULT + PAR NUMBER
WORD 2	PAR SIZE (byte)
WORD 3	PAR POINT ADDRESS
WORD 4	
WORD 5	PAR CRC

SUBFIELD NAME : LOAD RESULT + PAR NUMBER
SUBFIELD DESCR: Loading result flag and progressive number of parameter
SUBFIELD SIZE : 16 bit
SUBFIELD LAYOUT:



bit #15 LOAD RESULT 0 = NOK 1 = OK

bit #14 - 0 PAR PROGRESSIVE NUMBER 0 - 32767

DATA FORMAT #3

TITLE : (OCCURRED) EVENT REPORT

SOURCE NAME : DPU

TYPE NAME : HK EVENT LOG

BIT UTILIZATION : used 896 bit (56 Word) 100%
unused 0 bit (0 Word)

FILL RATE : N.A. MAX 64 events for each event code

DATA FIELD CONTENTS:

EVENT (MISSION) TIME	32 bit (2 Word)
TT FLAG	8 bit (0.5 Word)
EVENT DATA	8 bit (0.5 Word)
EVENT #	8 bit (0.5 Word)

DATA FIELD LAYOUT :

M3 M2 M1 M0 = EVENT (MISSION) TIME
(4 byte ordered MS=M3, LS=M0)

TT = TT FLAG

ED = EVENT DATA

EN = EVENT #

word 0	ENa	EDa
word 1	M1a	M0a
word 2	M3a	M2a
word 3	EDb	TTa
word 4	M0b	ENb
word 5	M2b	M1b
word 6	TTb	M3b

word 55	TTz	M3z

SUBFIELD NAME : EVENT (MISSION)TIME
SUBFIELD DESCR: Time measured when event is happened
SUBFIELD SIZE : 1 DoubleWord (32 bits)
SUBFIELD LAYOUT: Mission Time in msec.

SUBFIELD NAME : TT FLAG
SUBFIELD DESCR: Flag
SUBFIELD SIZE : 0.5 Word (8 bits)
SUBFIELD LAYOUT: BEFORE_T0 = 1, AFTER_T0 = 2

SUBFIELD NAME : EVENT #
SUBFIELD DESCR: Event code
SUBFIELD SIZE : 8 bits
SUBFIELD LAYOUT: the following TABLE defines the event codes

Event Code	Binary value	Event Name
0	00000000	T0
1	00000001	TWRONG
2	00000010	spare
3	00000011	spare
4	00000100	TIMPACT
5	00000101	DDBL nok line A
6	00000110	DDBL nok line B
7	00000111	UNKNOWN TC
8	00001000	TC RX uncorrect
9	00001001	PWA LINK ERROR
10	00001010	MCA READOUT
11	00001011	EEPROM LATCH-UP
12	00001100	PPI RANGE FAIL
13	00001101	ADC1 FAILURE
14	00001110	ADC2 FAILURE
15	00001111	spare
16	00010000	PPI timeout
17	00010001	spare
18	00010010	ACC range set COARSE
19	00010011	EEPROM SWITCHED
20	00010100	EEPROM LOCKED

SUBFIELD NAME : EVENT DATA

SUBFIELD DESCR: Event happened detailed

SUBFIELD SIZE : 8 bit

SUBFIELD LAYOUT: the following TABLE defines the event data

EVENT DATA for PWA

Decimal value	Binary value	Mnemonic
0	00000000	Invalid Packet Id
1	00000001	Invalid Sequence Count
2	00000010	Invalid Packet Length
3	00000011	Invalid Packet Error Control
4	00000100	Invalid Data Field Header
5	00000101	Timeout

EVENT DATA for MCA

Decimal value	Binary value	Mnemonic
var	00000XYZ	Mca Report
	Z : MCA ENERGY PRES	0 = ON 1 = OFF
	Y : MCA1 ACTIVE	0 = ON 1 = OFF
	X : MCA2 ACTIVE	0 = ON 1 = OFF

EVENT DATA for EEPROM SWITCHED

Decimal value	Binary value	Mnemonic
var	0	OFF
	1	ON

DATA FORMAT #5

TITLE : Health Check Report

SOURCE NAME : DPU

TYPE NAME : HC RATE 2 SEC (0.5 Hz)

BIT UTILIZATION : used 896 bit (56 Word) 100%
unused 0 bit (0 Word)

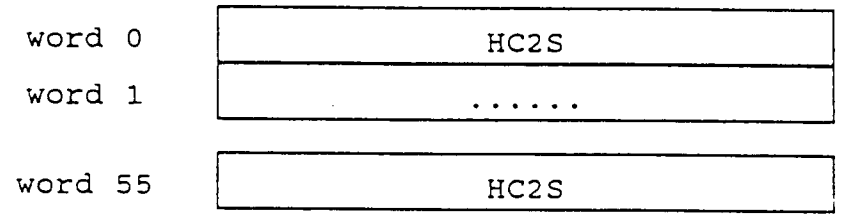
FILL RATE : 112 sec (0.14 TM / cycle CDMS)

DATA FIELD CONTENTS:

56 HC RATE 2 SEC subfields of 16 bit (1 Word) each

DATA FIELD LAYOUT :

HC2S = HC RATE 2 SEC (1 Word)

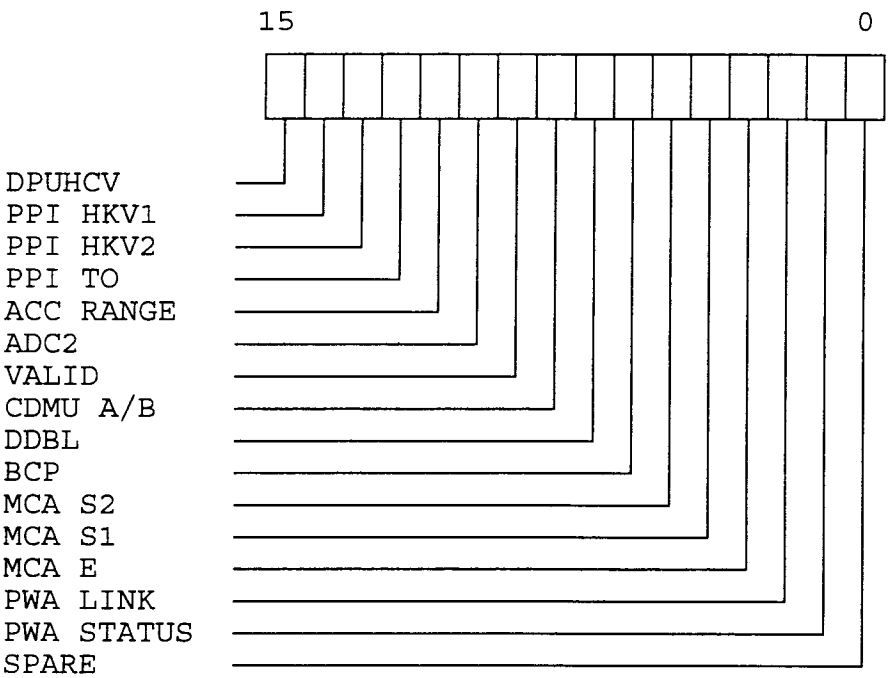


SUBFIELD NAME : HC2S

SUBFIELD DESCR : Health check every 2 sec

SUBFIELD SIZE : 16 bit

SUBFIELD LAYOUT :



bit #15	DPUHCV1/V2/V3	: DPU health check	ok=1, nok=0
bit #14	(PPI HKV1)	: PPI HKV1 helth check	ok=1, nok=0
bit #13	(PPI HKV2)	: PPI HKV2 helth check	ok=1, nok=0
bit #12	(PPI TO)	: PPI timeout HC	ok=1, nok=0
bit #11	ACC RANGE	: Range	high=1,low=0
bit #10	(ADC2)	: ADC 2 converter HC	ok=1, nok=0
bit #9	(VALID)	: valid line readout	B=1, A=0
bit #8	(CDMU A/B)	: current CDMU selection	A=0, B=1
bit #7	(DDBL)	: DDBL line failure	ok=1, nok=0
bit #6	(BCP)	: BCP line failure	ok=1, nok=0
bit #5	(MCA S2)	: MCA 2 STATUS	ON=0, OFF=1
bit #4	(MCA S1)	: MCA 1 STATUS	ON=0, OFF=1
bit #3	(MCA E)	: energize presence HC	ON=0, OFF=1
bit #2	(PWA LINK)	: PWA data link HC	ok=1, nok=0
bit #1	(PWA STATUS)	: PWA status HC	S=1, T=0

DATA FORMAT #7

TITLE : DPU Box Temperature (16 sec rate)

SOURCE NAME : DPU

TYPE NAME : DPU BOX TEM

BIT UTILIZATION : used 896 bit (56 Word) 100%
unused 0 bit (0 Word)

FILL RATE : 896 sec (0.0178 TM / cycle CDMS)

DATA FIELD CONTENTS:

56 DPU BOX TEM subfields of 16 bit (1 Word) each

DATA FIELD LAYOUT :

DPU BOX TEM (1 word)

word 0	DPU-BOX-TEM
word 1	.....
word 55	DPU-BOX-TEM

SUBFIELD NAME :	DPU BOX TEM
SUBFIELD DESCR :	Measure of DPU box internal temperature
SUBFIELD SIZE :	16 bit
SUBFIELD LAYOUT :	UNSIGNED INTEGER
	Resolution : LSB = ADC2 LSB/8

DATA FORMAT #32

TITLE : XSERVO ENTRY 3.125 Hz
(Sum of 32 samples at 100 Hz of Xservo best channel)

SOURCE NAME : ACC

TYPE NAME : SCDS.E

BIT UTILIZATION :

used	884 bit	(53 Words)	98.7%
unused	12 bit	(1 Word)	1.3%

FILL RATE : 16.64 sec (1.04 TM / cycle CDMS)

DATA FIELD CONTENTS:

52 SCDS.E 16 bit (1 Word)
52 SCDS.E_FLAG 1 bit (0.0625 Word)

DATA FIELD LAYOUT :

word 0	SCDS.E #0	
word 1	.....	
word 51	SCDS.E #51	
word 52	# 15	# 0
word 53	# 31	# 16
word 54	# 47	# 32
word 55	UNUSED	#51 #48

SCDS.E FLAG

SUBFIELD NAME : SCDS.E
SUBFIELD DESCR : Xservo values
SUBFIELD SIZE : 16 bit
SUBFIELD LAYOUT : INTEGER ~~U~~signed
Resolution: (ADC LSB * 2 / 32)
(2 because one rigth shift adj.;
32 because 32 SUMs)

SUBFIELD NAME : SCDS.E_FLAG
SUBFIELD DESCR : Channel selection flag

high = 1
low = 0

DATA FORMAT #33

TITLE : XSERVO DESCENT(4.167 Hz)
(Sum of 24 samples at 100 Hz of XServo best channel)

SOURCE NAME : ACC

TYPE NAME : SCDS.D

BIT UTILIZATION :

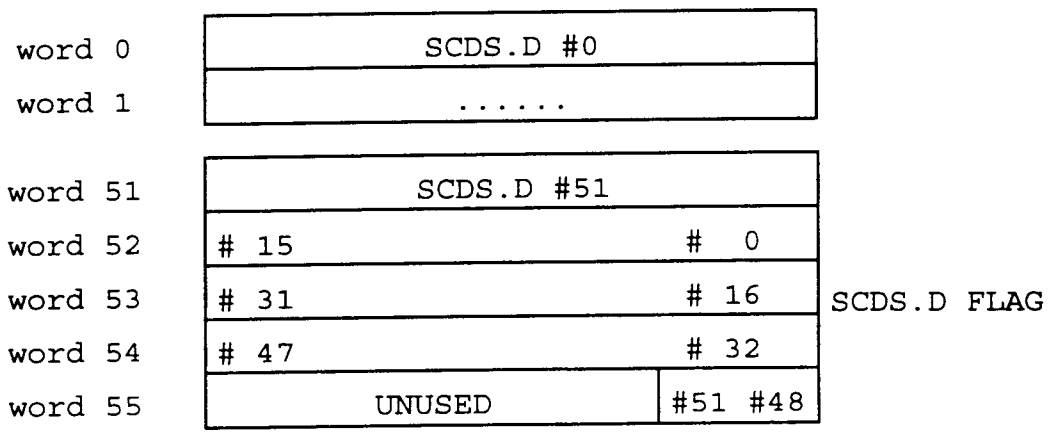
used	884 bit	(53 Words)	98.7%
unused	12 bit	(1 Word)	1.3%

FILL RATE : 12.48 sec (1.282 TM / cycle CDMS)

DATA FIELD CONTENTS:

52 SCDS.D 16 bit (1 Word)
52 SCDS.D_FLAG 1 bit (0.0625 Word)

DATA FIELD LAYOUT :



SUBFIELD NAME : SCDS.D
SUBFIELD DESCR : XSERVO values
SUBFIELD SIZE : 16 bit
SUBFIELD LAYOUT : INTEGER
Resolution: (ADC LSB * 2 / 24)
(2 because one rigth shift adj.;
24 because 24 SUMs)

SUBFIELD NAME : SCDS.D_FLAG
SUBFIELD DESCR : Channel selection flag

high = 1
low = 0

DATA FORMAT #34

TITLE : XSERVO RADAR (1.754 Hz)
(Sum of 57 samples at 100 Hz of Xservo best channel)

SOURCE NAME : ACC

TYPE NAME : SCDS.R

BIT UTILIZATION :

used	884 bit	(53 Words)	98.7%
unused	12 bit	(1 Word)	1.3%

FILL RATE : 29.647 sec (0.54 TM / cycle CDMS)

DATA FIELD CONTENTS:

52	SCDS.R	16 bit (1 Word)
52	SCDS.R_FLAG	1 bit (0.0625 Word)

DATA FIELD LAYOUT :

word 0	SCDS.R #0		
word 1	.....		
word 51	SCDS.R #51		
word 52	# 15	# 0	
word 53	# 31	# 16	SCDS.R FLAG
word 54	# 47	# 32	
word 55	UNUSED	#51 #48	

SUBFIELD NAME : SCDS.R
SUBFIELD DESCR : Xservo values
SUBFIELD SIZE : 16 bit
SUBFIELD LAYOUT : INTEGER
Resolution: (ADC LSB * 4 / 57)
(4 because two rigth shift adj.;
57 because 57 SUMs)

SUBFIELD NAME : SCDS.R_FLAG
SUBFIELD DESCR : Channel selection flag

high = 1
low = 0

DATA FORMAT #35

TITLE : XPIEZO (1.6129 Hz)
(Sum of 31 samples at 50 Hz of Xpiezo best channel)

SOURCE NAME : ACC

TYPE NAME : SCDPX

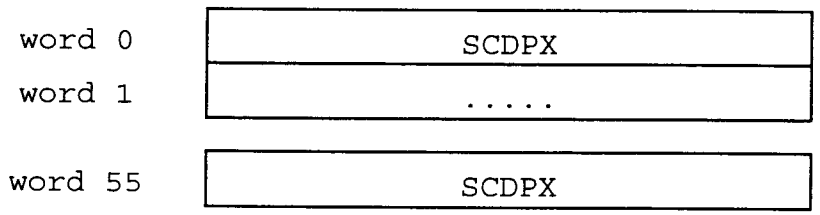
BIT UTILIZATION : used 896 bit (56 Words) 100%

FILL RATE : 34.72 sec (0.461 TM / cycle CDMS)

DATA FIELD CONTENTS:

56 SCDPX 16 bit (1 Word)

DATA FIELD LAYOUT :



SUBFIELD NAME : SCDPX
SUBFIELD DESCR : Xpiezo values
SUBFIELD SIZE : 16 bit
SUBFIELD LAYOUT : INTEGER
Resolution: (ADC LSB * 2 / 31)
(2 because one rigth shift adj.;
31 because 31 SUMs)

DATA FORMAT #36

TITLE : YPIEZO (1.6129 Hz)
(Sum of 31 samples at 50 Hz of Ypiezo best channel)

SOURCE NAME : ACC

TYPE NAME : SCDPY

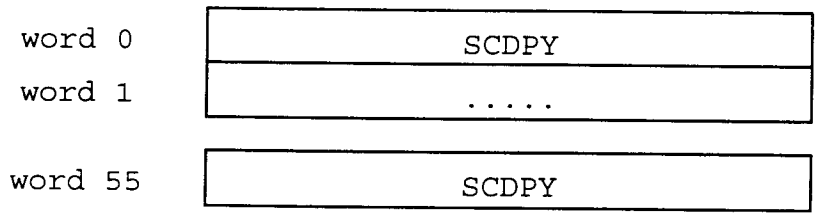
BIT UTILIZATION : used 896 bit (56 Words) 100%

FILL RATE : 34.72 sec (0.461 TM / cycle CDMS)

DATA FIELD CONTENTS:

56 SCDPY 16 bit (1 Word)

DATA FIELD LAYOUT :



SUBFIELD NAME : SCDPY
SUBFIELD DESCR : Ypiezo values
SUBFIELD SIZE : 16 bit
SUBFIELD LAYOUT : INTEGER ;
Resolution : (ADC LSB * 2 / 31)
(2 because one rigth shift adj.;
31 because 31 SUMs)

14

DATA FORMAT #37

TITLE : ZPIEZO (1.6129 Hz)
(Sum of 31 samples at 50 Hz of Zpiezo best channel)

SOURCE NAME : ACC

TYPE NAME : SCDPZ

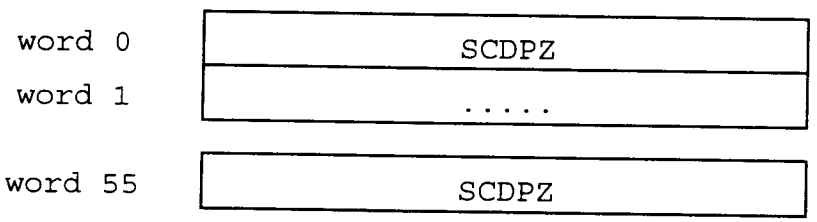
BIT UTILIZATION : used 896 bit (56 Words) 100%

FILL RATE : 34.72 sec (0.461 TM / cycle CDMS)

DATA FIELD CONTENTS:

56 SCDPZ 16 bit (1 Word)

DATA FIELD LAYOUT :



SUBFIELD NAME : SCDPZ
SUBFIELD DESCR : Zpiezo values
SUBFIELD SIZE : 16 bit signed
SUBFIELD LAYOUT : INTEGER;
Resolution : (ADC LSB * 2 / 31)
(2 because one rigth shift adj.;
31 because 31 SUMs)

DATA FORMAT #38

TITLE : Sum of 16 RD6 (Temp1) (0.098Hz)

SOURCE NAME : ACC

TYPE NAME : HKD1

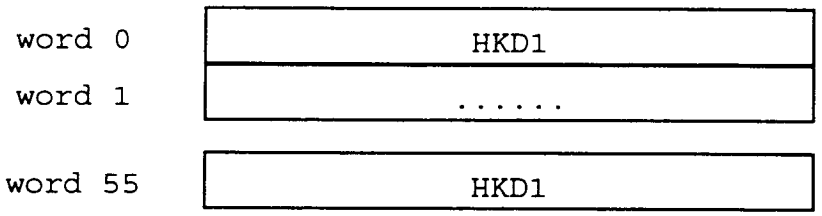
BIT UTILIZATION : used 896 bit (56 Words) 100%
unused 0 bit (0 Word)

FILL RATE : 571.43 sec (0.028 TM / cycle CDMS)

DATA FIELD CONTENTS:

56 HKD1 16 bit (1 Word)

DATA FIELD LAYOUT :



SUBFIELD NAME : HKD1

SUBFIELD DESCR : -

SUBFIELD SIZE : 16 bit

SUBFIELD LAYOUT : Sum of 16 consecutive samples;
Integer;
Resolution : (ADC LSB * 1 / 16)
(16 because 16 SUMs)

DATA FORMAT #39

TITLE : Sum of 16 RD7 (Temp2) (0.098Hz)

SOURCE NAME : ACC

TYPE NAME : HKD2

BIT UTILIZATION : Same of DATA FORMAT #38

FILL RATE : Same of DATA FORMAT #38

DATA FIELD CONTENTS:

56 HKD2 16 bit (1 Word)

DATA FIELD LAYOUT :

word 0	HKD2
word 1	.....
word 55	HKD2

SUBFIELD NAME : HKD2
SUBFIELD DESCR : -
SUBFIELD SIZE : 16 bit
SUBFIELD LAYOUT : sum of 16 consecutive samples;
INTEGER;
Resolution : Same of DATA FORMAT #38

DATA FORMAT #40

TITLE : Sum of 128 samples Xservo @ 12.5 Hz (0.098 Hz)

SOURCE NAME : ACC

TYPE NAME : STD2_XS

BIT UTILIZATION :

used	888 bit	(55.5 Words)	99.1%
unused	8 bit	(0.5 Word)	0,9%

FILL RATE : 378.88 sec (0.0422 TM / cycle CDMS)

DATA FIELD CONTENTS:

37 STD2_XS	24 bit	(1.25 Word)
UNUSED	8 bit	(0.5 Word)

$S2_x$ $S1_x$ $S0_x$ = STD2_XS (3 byte ordered MS = S2,LS = S0)

x = 0 .. 36, z = 36

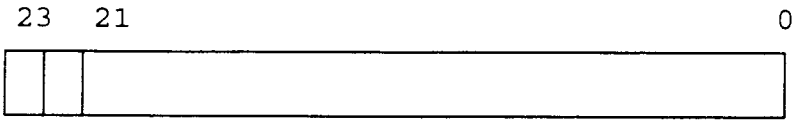
word 0	S1a	S0a
word 1	S0b	S2a
word 2	S2b	S1b
word 3	S1c	S0c
word 4	...	...
word 55	UNUSED	S2z

SUBFIELD NAME : STD2_XS

SUBFIELD DESCR : -

SUBFIELD SIZE : 24 bit

SUBFIELD LAYOUT :



bit #23	Channel selection flag :0 = LOW 1 = HIGH
bit #22	spare
bit #21...0	Xservo value INTEGER 22BIT;
	Resolution = (ADC LSB * 1 / 128)
	(128 because 128 SUMs)

DATA FORMAT #41

TITLE : Sum of 128 samples Xpiezo @12.5 (0.098 Hz)

SOURCE NAME : ACC

TYPE NAME : STD2_XP

BIT UTILIZATION : Same of data format #40

FILL RATE : Same of data format #40

DATA FIELD CONTENTS:

37 STD2_XP 24 bit (1.25 Word)
UNUSED 8 bit (0.5 Word)

$S2_x$ $S1_x$ $S0_x$ = STD2_XP (3 byte ordered MS = S2,LS = S0)

x = 0 .. 36, z = 36

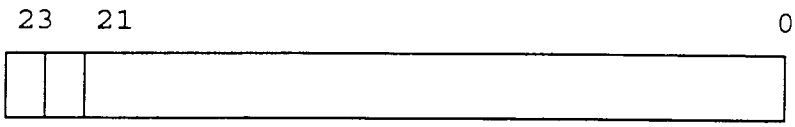
word 0	S1a	S0a
word 1	S0b	S2a
word 2	S2b	S1b
word 3	S1c	S0c
word 4	...	...
word 55	UNUSED	S2z

SUBFIELD NAME : STD2_XP

SUBFIELD DESCR : -

SUBFIELD SIZE : 24 bit

SUBFIELD LAYOUT :



bit #23..22 spare
bit #21...0 Xpiezo value INTEGER 22BIT;
Resolution = (ADC LSB * 1 / 128)
(128 because 128 SUMs)

DATA FORMAT #42

TITLE : Sum of 128 samples Ypiezo @ 12.5 Hz(0.098 Hz)

SOURCE NAME : ACC

TYPE NAME : STD2_YP

BIT UTILIZATION : Same of data format #40

FILL RATE : Same of data format #40

DATA FIELD CONTENTS:

37 STD2_YP 24 bit (1.25 Word)
UNUSED 8 bit (0.5 Word)

$S2_x$ $S1_x$ $S0_x$ = STD2_YP (3 byte ordered MS = S2,LS = S0)

x = 0 .. 36, z = 36

word 0	S1a	S0a
word 1	S0b	S2a
word 2	S2b	S1b
word 3	S1c	S0c
word 4	...	...
word 55	UNUSED	S2z

SUBFIELD NAME : STD2_YP

SUBFIELD DESCR : -

SUBFIELD SIZE : 24 bit

SUBFIELD LAYOUT : Same of data format #41

DATA FORMAT #43

TITLE : Sum of 128 samples Zpiezo @12.5 Hz (0.098 Hz)

SOURCE NAME : ACC

TYPE NAME : STD2_ZP

BIT UTILIZATION : Same of data format #40

FILL RATE : Same of data format #40

DATA FIELD CONTENTS:

37 STD2_ZP 24 bit (1.25 Word)
UNUSED 8 bit (0.5 Word)

$S2_x$ $S1_x$ $S0_x$ = STD2_ZP (3 byte ordered MS = S2,LS = S0)

x = 0 .. 36, z = 36

word 0	S1a	S0a
word 1	S0b	S2a
word 2	S2b	S1b
word 3	S1c	S0c
word 4	...	...
word 55	UNUSED	S2z

SUBFIELD NAME : STD2_ZP

SUBFIELD DESCR : -

SUBFIELD SIZE : 24 bit

SUBFIELD LAYOUT : Same of data format #41

DATA FORMAT #48

TITLE : 200 Hz impact trace data of Xpiezo

SOURCE NAME : ACC

TYPE NAME : ID1

BIT UTILIZATION :

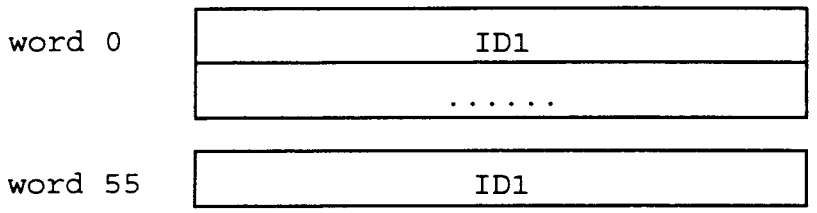
used	896 bit	(56 Words)	100%
unused	0 bit	(0 Words)	0%

FILL RATE : 0.28 sec (NOT APPLICABLE TM / cycle CDMS)

DATA FIELD CONTENTS:

56 ID1 16 bit (1 Word)

DATA FIELD LAYOUT :

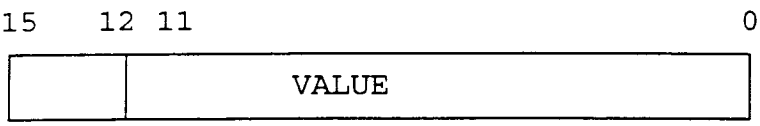


SUBFIELD NAME : ID1

SUBFIELD DESCR : -

SUBFIELD SIZE : 16 bit

SUBFIELD LAYOUT : Lowest part in lowest WORD :



bit #15..12 UNUSED
bit #11..0 VALUE SIGNED INTEGER;
Resolution : LSB = ADC LSB;

DATA FORMAT #49

TITLE : 200 Hz impact trace data of Ypiezo

SOURCE NAME : ACC

TYPE NAME : ID2

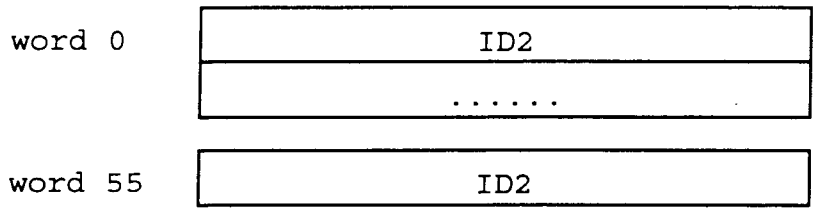
BIT UTILIZATION : Same of data format #48

FILL RATE : Same of data format #48

DATA FIELD CONTENTS:

56 ID2 16 bit (1 Word)

DATA FIELD LAYOUT :



SUBFIELD NAME : ID2

SUBFIELD DESCR : -

SUBFIELD SIZE : 16 bit

SUBFIELD LAYOUT : Same of data format #48

DATA FORMAT #50

TITLE : 200 Hz impact trace data of Zpiezo

SOURCE NAME : ACC

TYPE NAME : ID3

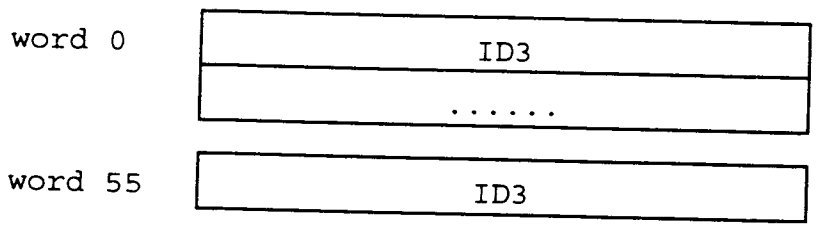
BIT UTILIZATION : Same of data format #48

FILL RATE : Same of data format #48

DATA FIELD CONTENTS:

56 ID3 16 bit (1 Word)

DATA FIELD LAYOUT :



SUBFIELD NAME : ID3

SUBFIELD DESCR : -

SUBFIELD SIZE : 16 bit

SUBFIELD LAYOUT : Same of data format #48

DATA FORMAT #64

TITLE : YSi statistical data of SESSION #0 (couples @ 0.417 Hz)

SOURCE NAME : PPI

TYPE NAME : NORMAL SESSION #0 (A)

BIT UTILIZATION : used 896 bit (56 Word) 100%
unused 0 bit (0 Word)

FILL RATE : 43.2 sec

DATA FIELD CONTENTS:

36 YSi + R1 + R2	896 bit (56 Word)
YSi (i=1..36)	24 bit (1.5 Word)
R1	16 bit (1 Word)
R2	16 bit (1 Word)

DATA FIELD LAYOUT :

Y2 Y1 Y0 = YSi (3 byte ordered MS=Y2, LS=Y0)

R1 (1 word)

R2 (1 word)

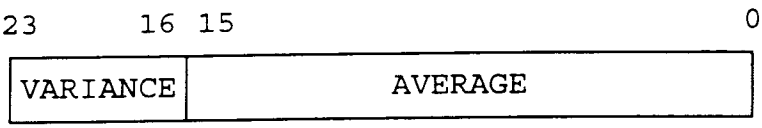
word 0	Y1a	Y0a
word 1	Y0b	Y2a
word 2	Y2b	Y1b
word 3	Y1c	Y0c
word 4	...	...
word 54	R1	
word 55	R2	

SUBFIELD NAME : YSi

SUBFIELD DESCR : YSi = VARIANCE + AVERAGE

SUBFIELD SIZE : 24 bit

SUBFIELD LAYOUT : Lowest bits in lowest WORD :



bit #23..16 (VARIANCE) unsigned integer (8 bit);
square of standard deviation
Resolution : LSB = .953674*10E-6 (2^{-18});

bit #15..0 (AVERAGE) integer (16 bit);
Resolution : LSB = .305175*10E-4 (2^{-15})
(i.e. range -1 .. +1);

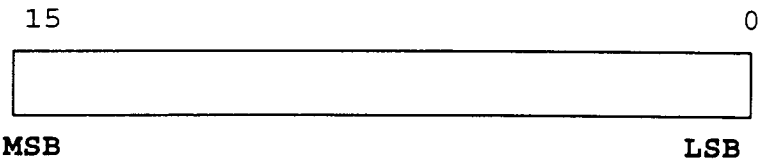
SUBFIELD NAME : R1

SUBFIELD DESCR : The last L.S. 16 bit of counter value readout of 1st reference channel * ALFA / PRESCALER

ALFA = 2^{10}
PRESCALER varies with frequency

SUBFIELD SIZE : 16 bit

SUBFIELD LAYOUT :



bit #15..0 (R1) unsigned integer (16 bit);
Resolution : LSB = .2170138889*10E-11 sec
(1/(4.5 Mhz * ALFA));

ALFA = 2^{10} = 1024

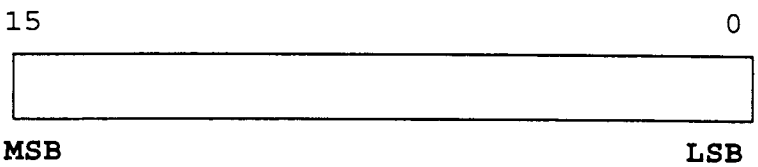
SUBFIELD NAME : R2

SUBFIELD DESCR : The last L.S. 16 bit of counter value readout of 2nd reference channel * ALFA / PRESCALER

ALFA = 2^{10} = 1024
PRESCALER varies with frequency

SUBFIELD SIZE : 16 bit

SUBFIELD LAYOUT :



bit #15..0 (R2) unsigned integer (16 bit);
Resolution : LSB = same of R1;

DATA FORMAT #65

TITLE : YSi statistical data of SESSION #1 (couples @ 0.417 Hz)

SOURCE NAME : PPI

TYPE NAME : NORMAL SESSION #1 (B)

BIT UTILIZATION : Same of NORMAL SESSION #0 (#64 data format)

FILL RATE : Same of NORMAL SESSION #0 (#64 data format)

DATA FIELD CONTENTS: Same of NORMAL SESSION #0 (#64 data format)

DATA FIELD LAYOUT : Same of NORMAL SESSION #0 (#64 data format)

DATA FORMAT #66

TITLE : YSi statistical data of SESSION #2 (couples @ 0.417 Hz)

SOURCE NAME : PPI

TYPE NAME : NORMAL SESSION #2 (C)

BIT UTILIZATION : Same of NORMAL SESSION #0 (#64 data format)

FILL RATE : Same of NORMAL SESSION #0 (#64 data format)

DATA FIELD CONTENTS: Same of NORMAL SESSION #0 (#64 data format)

DATA FIELD LAYOUT : Same of NORMAL SESSION #0 (#64 data format)

DATA FORMAT #70

TITLE : RAW DATA of HC SESSION #0 @ 6.666666 Hz (150 msec)

SOURCE NAME : PPI

TYPE NAME : HC SESSION #0 (G)

BIT UTILIZATION : used 888 bit (55.5 Words) 99.1%
unused 8 bit (0.5 Word 0.9%

FILL RATE : 5.55 sec

DATA FIELD CONTENTS:

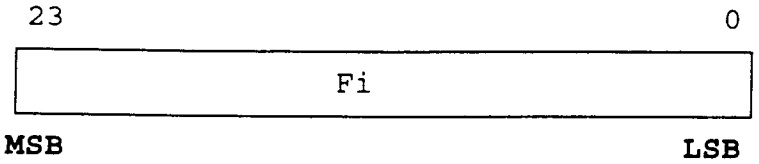
37 Fi subfields of 24 bit (1.5 Word) each

DATA FIELD LAYOUT :

$F2_x$ $F1_x$ $F0_x$ = Fi (3 byte ordered MS=F2, LS=F0)
x = 0 .. 36 ; z = 36

word 0	F1a	F0a
word 1	F0b	F2a
word 2	F2b	F1b
word 3	F1c	F0c
word 4	...	...
word 55	UNUSED	F2z

SUBFIELD NAME : Fi
SUBFIELD DESCR : Counter value readout of a raw phisical channel
SUBFIELD SIZE : 24 bit
SUBFIELD LAYOUT :



bit #23..0 (Fi) unsigned integer (24 bit);
Resolution : LSB = .2170138889*10E-11 sec
(1/(4.5 Mhz * ALFA));

ALFA = 2^{10} = 1024

DATA FORMAT #71

TITLE : Fi RAW DATA of HC SESSION #1 @ 6.666666 Hz

SOURCE NAME : PPI

TYPE NAME : HC SESSION #1 (H)

BIT UTILIZATION : Same of HC SESSION #0 (#70 data format)

FILL RATE : Same of HC SESSION #0 (#70 data format)

DATA FIELD CONTENTS: Same of HC SESSION #0 (#70 data format)

DATA FIELD LAYOUT : Same of HC SESSION #0 (#70 data format)

DATA FORMAT #72

TITLE : Housekeeping voltages 1 & 2 (64 sec = 0.015625 Hz)
(32 words @ 0.5 Hz)

SOURCE NAME : PPI

TYPE NAME : HKV

BIT UTILIZATION : used 896 bit (56 Words) 100%
unused 0 bit (0 Word)

FILL RATE : 1792 sec (0.00893 TM / cycle CDMS)

DATA FIELD CONTENTS:

28 (HKV1 + HKV2) 16 bit + 16 bit (1 Word + 1 Word)

DATA FIELD LAYOUT :

$HKV2_x$ (1 word)

$HKV1_x$ (1 word)

x = 0 .. 27, z = 27

word 0	HKV1a
word 1	HKV2a
word 3	HKV1b
word 4	HKV2b
word 55	HKV2z

SUBFIELD NAME : HKV1/HKV2
SUBFIELD DESCR : average of x samples

SUBFIELD SIZE : 16 bit
SUBFIELD LAYOUT : UNSIGNED INT;
Resolution : LSB = ADC LSB * 1/16

DATA FORMAT #96

TITLE : Offset and value of SENSOR HEAD 1 thermistor FINE and its reference, measured every 5 sec(0.2 Hz)

SOURCE NAME : TEM

TYPE NAME : F1

BIT UTILIZATION : used 896 bit (56 Words) 100%

FILL RATE : 90 sec (0.178 TM / cycle CDMS)

DATA FIELD CONTENTS:

18 TEM subfields of 48 bit (3 Word) each
2 OFFSET subfields of 16 bit (1 word) each

DATA FIELD LAYOUT :

T5x T4x T3x T2x T1x T0x = TEM (6 byte ordered MS=T5,LS=T0)
x = 0 .. 17, z = 17
OVFMEAN = 2 byte
OVRMEAN = 2 byte

word 0	T1a	T0a
word 1	T3a	T2a
word 2	T5a	T4a
word 3	...	...
word 4	...	...

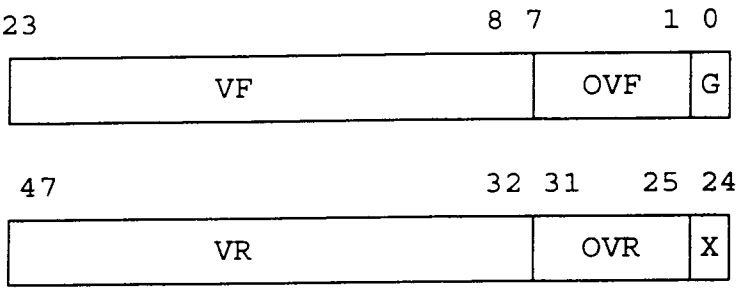
word 54	OVFMEAN
word 55	OVRMEAN

SUBFIELD NAME : TEM

SUBFIELD DESCR : TEM = VR + OVR + X + VF + OVF + G

SUBFIELD SIZE : 48 bit

SUBFIELD LAYOUT :



SUBFIELD NAME : G

SUBFIELD DESCR : gain selection flag
(1 = H, 0 = L)

SUBFIELD SIZE : 1 bit

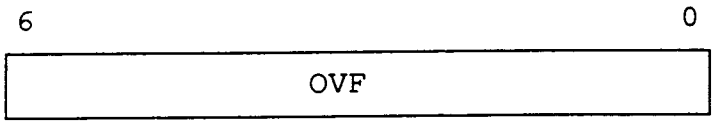
SUBFIELD LAYOUT : -

SUBFIELD NAME : OVF

SUBFIELD DESCR offset thermistor voltage

SUBFIELD SIZE : 7 bit

SUBFIELD LAYOUT :



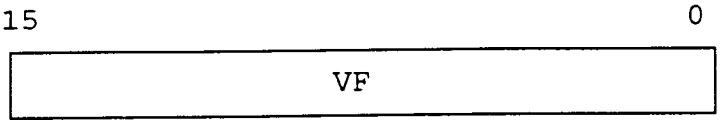
bit #6..0 : unsigned integer;
Resolution = ADC LSB /4;

SUBFIELD NAME : VF

SUBFIELD DESCR : voltage V_{TERM}

SUBFIELD SIZE : 16 bit

SUBFIELD LAYOUT :



bit #15..0 : unsigned integer;
Resolution = ADC LSB/8;

SUBFIELD NAME : X

SUBFIELD DESCR : spare bit

SUBFIELD SIZE : 1 bit

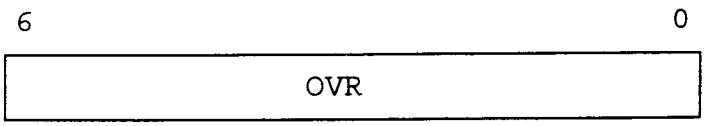
SUBFIELD LAYOUT : -

SUBFIELD NAME : OVR

SUBFIELD DESCR offset reference voltage

SUBFIELD SIZE : 7 bit

SUBFIELD LAYOUT :



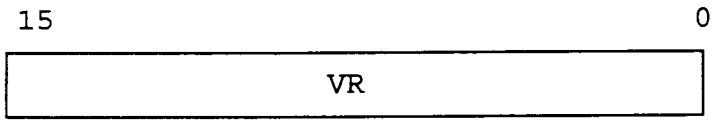
bit #7..0 : unsigned integer;
Resolution = ADC LSB /4;

SUBFIELD NAME : VR

SUBFIELD DESCR : voltage V_{REF}

SUBFIELD SIZE : 16 bit

SUBFIELD LAYOUT :



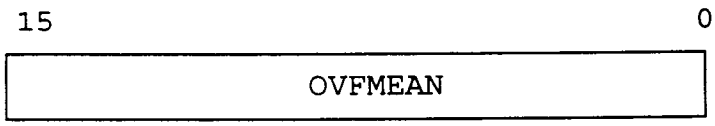
bit #15..0 : unsigned integer;
Resolution = ADC LSB/8;

SUBFIELD NAME : OVFMEAN

SUBFIELD DESCR : offset thermistor voltage
(average (running mean) of thermistor voltage
offset @108 sec)

SUBFIELD SIZE : 16 bit

SUBFIELD LAYOUT :



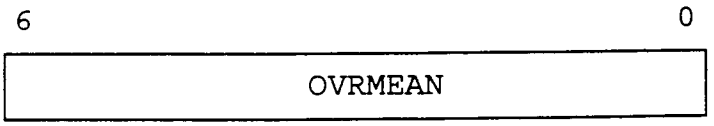
bit #15..0 : unsigned integer; Resolution = ADC LSB /8;

SUBFIELD NAME : OVRMEAN

SUBFIELD DESCR offset reference voltage
(average (running mean) of reference voltage
offset @108 sec)

SUBFIELD SIZE : 16 bit

SUBFIELD LAYOUT :



bit #15..0 : unsigned integer; Resolution = ADC LSB /8;

DATA FORMAT #98

TITLE : Offset and value of SENSOR HEAD 1 thermistor COARSE and its reference, measured every 5 sec (0.2 Hz)

SOURCE NAME : TEM

TYPE NAME : C1

BIT UTILIZATION : Same of F1 (#96 data format)

FILL RATE : Same of F1 (#96 data format)

DATA FIELD CONTENTS: Same of F1 (#96 data format)

DATA FIELD LAYOUT : Same of F1 (#96 data format)

DATA FORMAT #100

TITLE : Offset and value of SENSOR HEAD 2 thermistor FINE and its reference, measured every 5 sec (0.2 Hz)

SOURCE NAME : TEM

TYPE NAME : F2

BIT UTILIZATION : Same of F1 (#96 data format)

FILL RATE : Same of F1 (#96 data format)

DATA FIELD CONTENTS: Same of F1 (#96 data format)

DATA FIELD LAYOUT : Same of F1 (#96 data format)

DATA FORMAT #102

TITLE : Offset and value of SENSOR HEAD 2 thermistor COARSE and its reference, measured every 5 sec (0.2 Hz)

SOURCE NAME : TEM

TYPE NAME : C2

BIT UTILIZATION : Same of F1 (#96 data format)

FILL RATE : Same of F1 (#96 data format)

DATA FIELD CONTENTS: Same of F1 (#96 data format)

DATA FIELD LAYOUT : Same of F1 (#96 data format)

DATA FORMAT #128

TITLE : Pwa EM science data

SOURCE NAME : PWA

TYPE NAME : EM SCIENCE DATA

BIT UTILIZATION : used 896 bit (56 Words) 100%
unused 0 bit (0 Word)

FILL RATE : 6/7 packets every 16 sec

DATA FIELD CONTENTS:

PWA SCIENCE DATA 896 bit (56 Word)
PWA 112 bytes science packet data field

DATA FIELD LAYOUT :

$PWAD_x$ = pwa data bytes numbered in reception order

x = 0 .. 111

	15 ... 8	7 ... 0
WORD 0	PWAD1	PWAD0
WORD 1	PWAD3	PWAD2
WORD 55	PWAD111	PWAD110

DATA FORMAT #129

TITLE : Pwa corrupted data

SOURCE NAME : PWA

TYPE NAME : CORRUPTED DATA

BIT UTILIZATION : used 896 bit (56 Words) 100%
unused 0 bit (0 Word)

FILL RATE : sporadic

DATA FIELD CONTENTS:

PWA SCIENCE DATA 896 bit (56 Word)
PWA 112 bytes packet data field

DATA FIELD LAYOUT : Same of EM SCIENCE DATA (#128 data format)

DATA FORMAT #130

TITLE : Pwa test data (EM + FM)

SOURCE NAME : PWA

TYPE NAME : TEST DATA

BIT UTILIZATION : used 896 bit (56 Words) 100%
unused 0 bit (0 Word)

FILL RATE : 6/7 packets every 16 sec

DATA FIELD CONTENTS:

PWA TEST DATA 896 bit (56 Word)

PWA 112 bytes packet data field

DATA FIELD LAYOUT : Same of EM SCIENCE DATA (#128 data format)

DATA FORMAT #131

TITLE : Pwa FM science data - ACDC

SOURCE NAME : PWA

TYPE NAME : FM SCIENCE DATA ACDC

BIT UTILIZATION : used 896 bit (56 Words) 100%
unused 0 bit (0 Word)

FILL RATE : 6/7 packets every 16 sec

DATA FIELD CONTENTS:

PWA SCIENCE DATA 896 bit (56 Word)
PWA 112 bytes science packet data field

DATA FIELD LAYOUT :

$PWAD_x$ = pwa data bytes numbered in reception order

x = 0 .. 111

	15 — 8	7 — 0
WORD 0	PWAD1	PWAD0
WORD 1	PWAD3	PWAD2
WORD 55	PWAD111	PWAD110

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DATA FORMAT #132

TITLE : Pwa FM science data - ACDCDAU

SOURCE NAME : PWA

TYPE NAME : FM SCIENCE DATA ACDCAU

BIT UTILIZATION : used 896 bit (56 Words) 100%
unused 0 bit (0 Word)

FILL RATE : 6/7 packets every 16 sec

DATA FIELD CONTENTS:

PWA SCIENCE DATA 896 bit (56 Word)
PWA 112 bytes science packet data field

DATA FIELD LAYOUT : Same of FM SCIENCE DATA ACDC (#131 data format)

DATA FORMAT #133

TITLE : Pwa FM science data - RADAR

SOURCE NAME : PWA

TYPE NAME : FM SCIENCE DATA RADAR

BIT UTILIZATION : used 896 bit (56 Words) 100%
unused 0 bit (0 Word)

FILL RATE : 6/7 packets every 16 sec

DATA FIELD CONTENTS:

PWA SCIENCE DATA 896 bit (56 Word)
PWA 112 bytes science packet data field

DATA FIELD LAYOUT : Same of FM SCIENCE DATA ACDC (#131 data format)

DATA FORMAT #134

TITLE : Pwa FM science data - MI

SOURCE NAME : PWA

TYPE NAME : FM SCIENCE DATA MI

BIT UTILIZATION : used 896 bit (56 Words) 100%
unused 0 bit (0 Word)

FILL RATE : 6/7 packets every 16 sec

DATA FIELD CONTENTS:

PWA SCIENCE DATA 896 bit (56 Word)
PWA 112 bytes science packet data field

DATA FIELD LAYOUT : Same of FM SCIENCE DATA ACDC (#131 data format)

DATA FORMAT #135

TITLE : Pwa FM science data - RP

SOURCE NAME : PWA

TYPE NAME : FM SCIENCE DATA RP

BIT UTILIZATION : used 896 bit (56 Words) 100%
unused 0 bit (0 Word)

FILL RATE : 6/7 packets every 16 sec

DATA FIELD CONTENTS:

PWA SCIENCE DATA 896 bit (56 Word)
PWA 112 bytes science packet data field

DATA FIELD LAYOUT : Same of FM SCIENCE DATA ACDC (#131 data format

DATA FORMAT #160

TITLE : Telecommand echo

SOURCE NAME : TC

TYPE NAME : ECHO

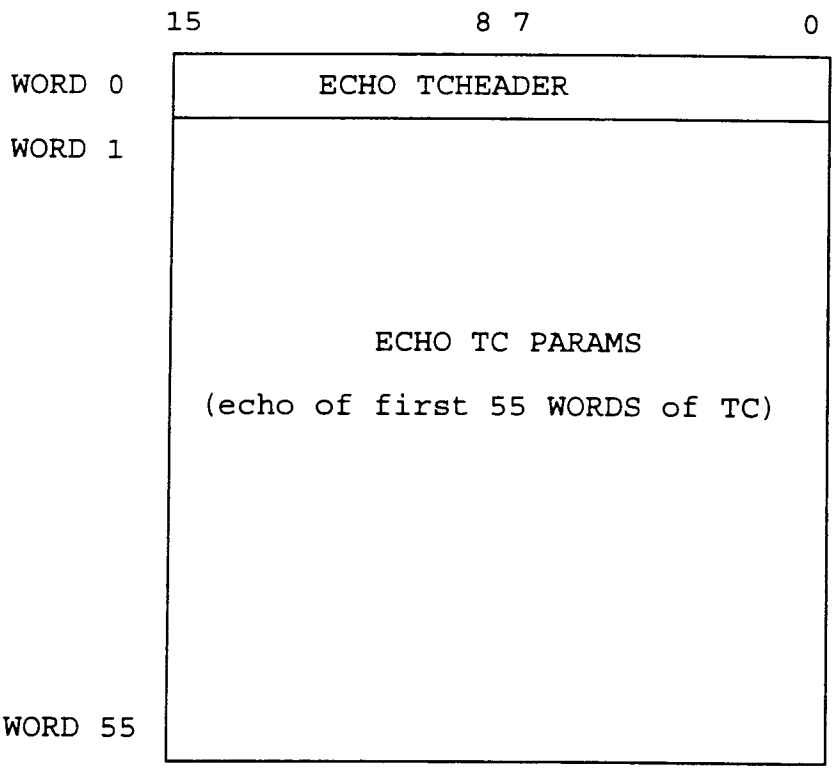
BIT UTILIZATION : used 896 bit (56 word)

FILL RATE : once every received tc

DATA FIELD CONTENTS:

ECHO TCHEADER 16 bit (1 Word)
ECHO TC PARAMS 880 bit (55 Word)

DATA FIELD LAYOUT :



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DATA FORMAT #161

TITLE : MEMORY DUMP TM

SOURCE NAME : TC REPORT

TYPE NAME : MEMORY DUMP

BIT UTILIZATION : used 896 bit (56 word) 100%
unused 0 bit

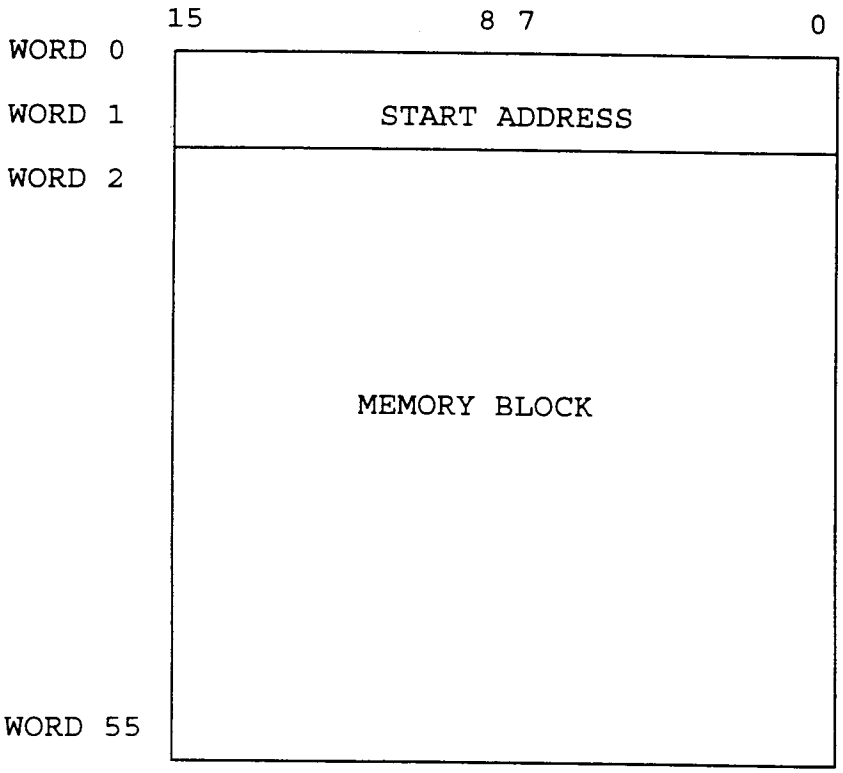
FILL RATE : 3 SEC (FORCED) (~5 TM/cycle)

DATA FIELD CONTENTS:

START ADDRESS 32 bit (2 Word)

MEMORY BLOCK 864 bit (54 Word)

DATA FIELD LAYOUT :

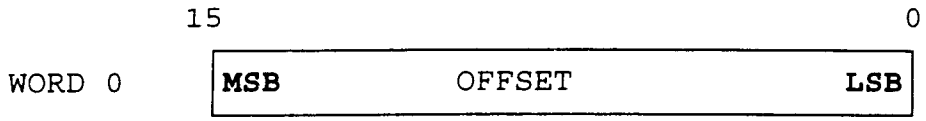


SUBFIELD NAME : START ADDRESS

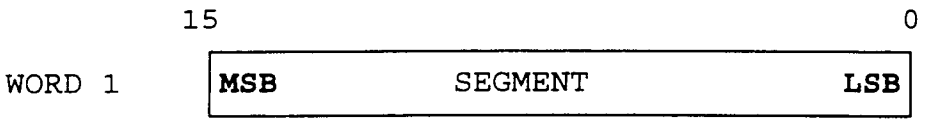
SUBFIELD DESCR Start address of MEMORY BLOCK subfield composed of 2 Word SEGMENT+OFFSET (80X86 FORMAT)

SUBFIELD SIZE : 32 bit (2 Word)

SUBFIELD LAYOUT :



WORD 0 : 16 bit OFFSET to SEGMENT



WORD 1 : 80x86 Segment Address Paragraph Aligned (i.e. multiple of 16);

SUBFIELD NAME : MEMORY BLOCK

SUBFIELD DESCR : 54 consecutive memory words starting from START ADDRESS

SUBFIELD SIZE : 864 bit (54 Word)

SUBFIELD LAYOUT : WORD 2..WORD 55 : array of 54 Word

DATA FORMAT #162

TITLE : Echo of loaded phisical location (word size)

SOURCE NAME : TC REPORT

TYPE NAME : MEMORY LOAD ECHO

BIT UTILIZATION : Same of MEMORY DUMP TM (#161 data format)

FILL RATE : Same of MEMORY DUMP TM (#161 data format)

DATA FIELD CONTENTS:

Same of MEMORY DUMP TM (#161 data format)

DATA FIELD LAYOUT :

Same of MEMORY DUMP TM (#161 data format)

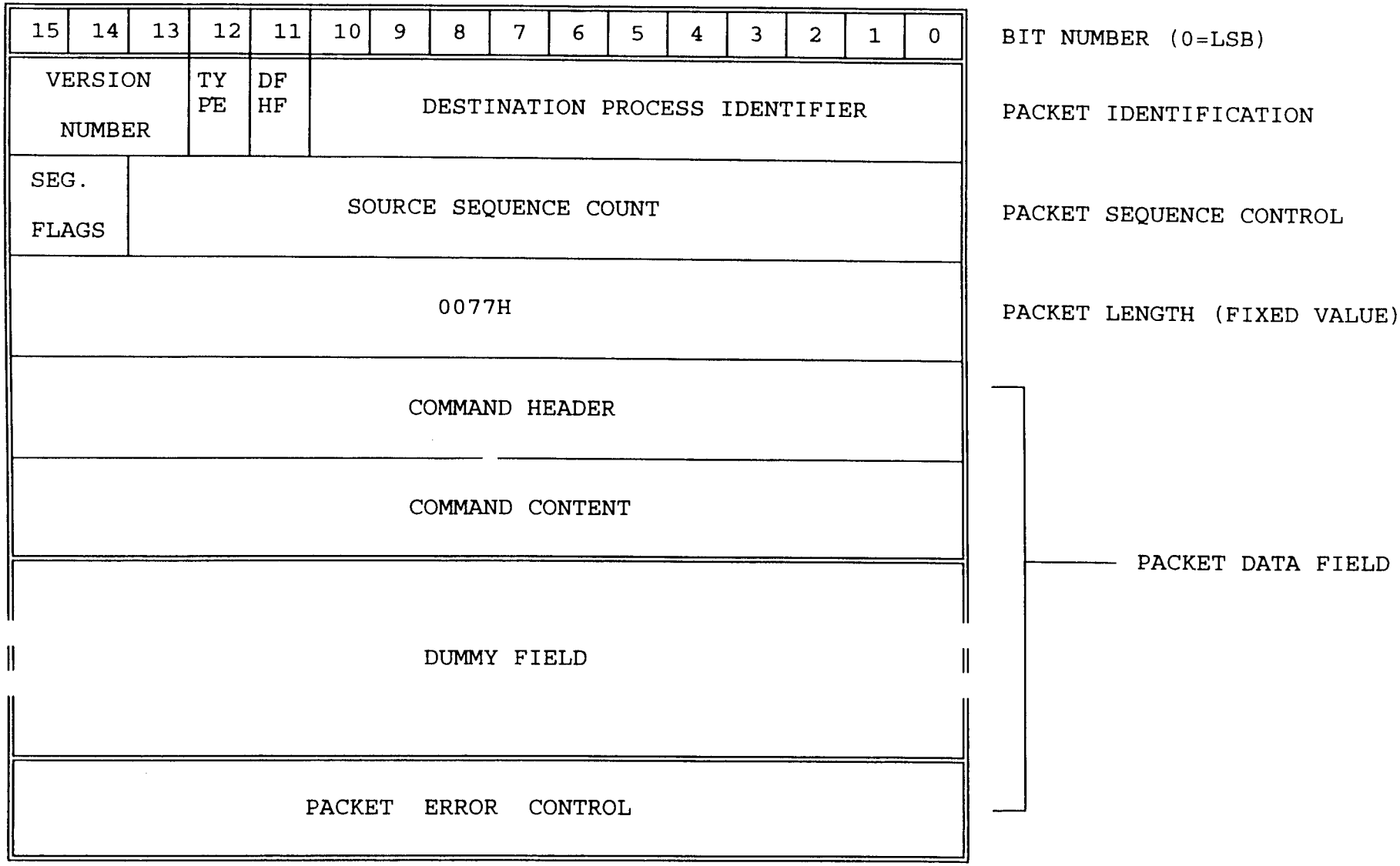


FIGURE B : TELECOMMAND PACKET DESCRIPTION

FIELDS CONTENT (referring to FIGURE B)

- **PACKET IDENTIFICATION** (16 bit): This field is divided into VERSION NUMBER, TYPE, DATA FIELD HEADER FLAG and DESTINATION PROCESS IDENTIFIER

  VERSION NUMBER (3 bit): It's a 3-bit field occupying the three most significant bit of a packet structure.

  The Version Number is fixed to :

  Bit 15 through 13 = 0 0 0

  TYPE (1bit): It indicates either Telemetry Type or Telecommand Type. In this case bit 12=1.

  DATA FIELD HEADER FLAG (1bit): It indicates the presence or absence a Data Field within the PACKET DATA FIELD. In this case bit 11 = 1.

  DESTINATION PROCESS IDENT (11 bit): It's an 11-bit field uniquely identifying phisical destinations. In this case: bit 10 through 0

  11110010001 for HASI LINE A
  11110110001 for HASI LINE B.

- **PACKET SEQUENCE CONTROL** (16 bit): This field is divided into SEGMENTATION FLAGS and SOURCE SEQUENCE COUNT.

  SEGMENTATION FLAGS (2 bit): In the TC Packet the Segmentation Flags shall always be set to "all one".

  . Bit 15 through 14 = 1 1

  SEQUENCE COUNT (14 bit): It counts the number of packets sent. It resets after 16384 packets or after an experiment power up.

- **PACKET LENGTH** (16 bit): It's a 16-bit field which specifies the number of octets contained within the Packet Data Field. The number is a binary value C:

  C = [(Number of octets in Data Field)-1]

  In this case bit 15 through 0 :

  0000000001110111

- **PACKET DATA FIELD** (960 bit): This field is divided into COMMAND HEADER, COMMAND CONTENT, DUMMY FIELD and PACKET ERROR CONTROL.

  COMMAND HEADER (16 bit): 16 bit pattern identifying the command and encoding the COMMAND CONTENT layout

  COMMAND CONTENT (variable): variable number of command parameters whos layout depend on

  DUMMY FIELD (variable) : variable number of ZERO value words to fill 126 byte fixed length of the Telecommand packet

  PACKET ERROR CONTROL (16 bit): It is the XOR function computed on all the words starting from PACKET IDENTIFICATION (included) till the last DATA in the DATA FIELD, i.e. from WORD 0 to WORD 61 (extremes included).

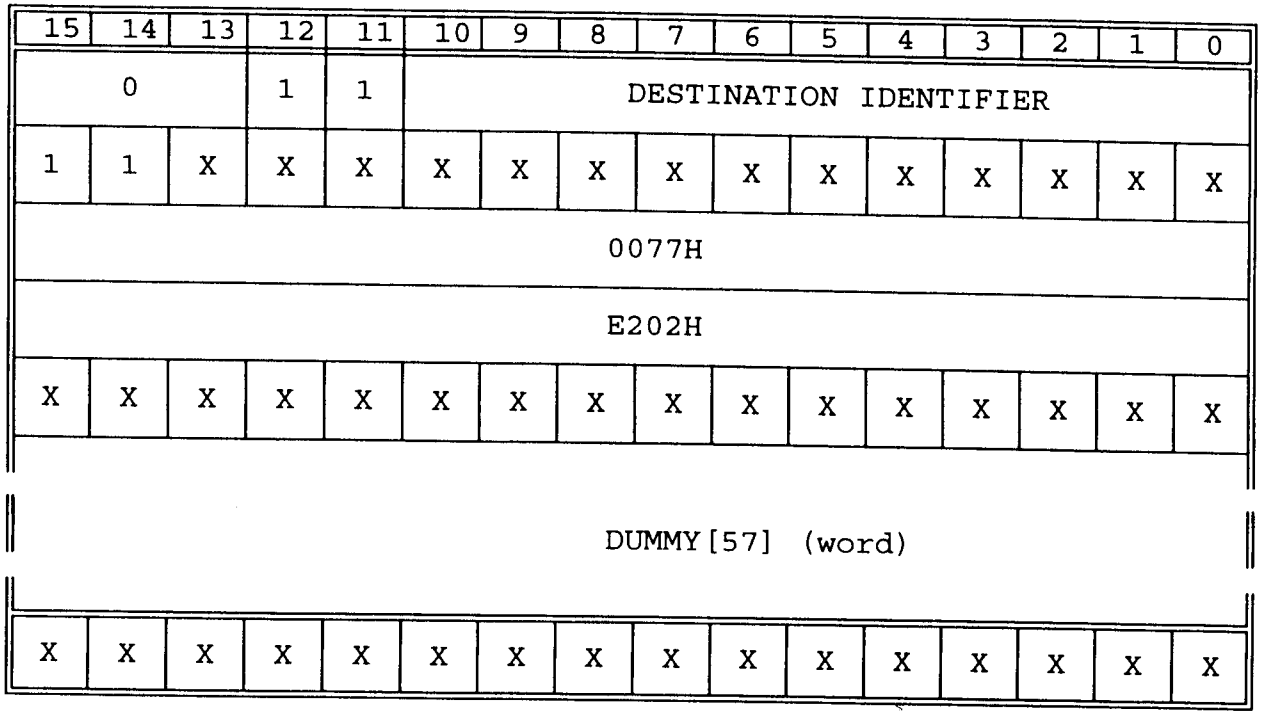
HASI SOFT RESET

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0			1	1	DESTINATION IDENTIFIER											BIT NUMBER (0=LSB)
																PACKET IDENTIFICATION
1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PACKET SEQUENCE COUNT
0077H																PACKET LENGTH
E200H																COMMAND HEADER
DUMMY[58] (word)																
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PACKET ERROR CONTROL (CRC 16)

NAME: SOFT RESET
ID, TYPE: E200, M
FUNCTION: Whole experiment software reset
REMARK: the length of the whole TC PACKET is fixed to 126 bytes

A87

HASI TEST MODE



NAME: TEST MODE
ID, TYPE: E202, M
FUNCTION: Performs a test of the HASI experiment communication
CONTENT: TEST MODE: = 0 --> STATUS WORD test BIT is reset
TEST MODE: <> 0 --> STATUS WORD test BIT is set

REMARK: the length of the whole TC PACKET is fixed to 126 bytes

A98

HASI PWA TEST

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0			1	1	DESTINATION IDENTIFIER											PACKET IDENTIFICATION
1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PACKET SEQUENCE COUNT
0077H																PACKET LENGTH
E201H																COMMAND HEADER
PWA CMD																COMMAND CONTENT
DUMMY[57] (word)																
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PACKET ERROR CONTROL (CRC 16)

BIT NUMBER (0=LSB)

NAME: TEST PWA
ID, TYPE: E201, M
FUNCTION: Dispatches test command PWA CMD to PWA
CONTENT: PWA CMD = 0: no PWA TEST, PWA CMD = N: PWA TEST #N (N = 0 to 32)

REMARK: the length of the whole TC PACKET is fixed to 126 bytes

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HASI MEMORY DUMP

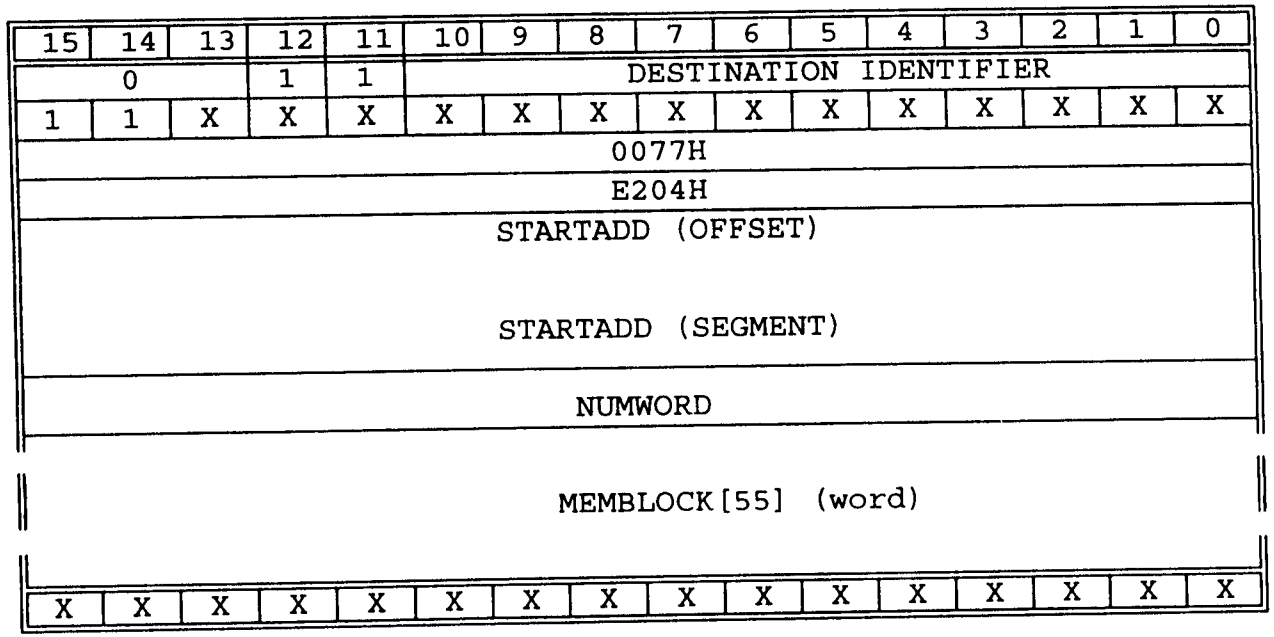
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	0		1	1	DESTINATION IDENTIFIER											PACKET IDENTIFICATION
1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PACKET SEQUENCE COUNT
0077H																PACKET LENGTH
E203H																COMMAND HEADER
STARTADD (OFFSET)																COMMAND CONTENT
STARTADD (SEGMENT)																
NUMRECORD																
DUMMY[55] (word)																
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PACKET ERROR CONTROL (CRC 16)

NAME: **MEMORY DUMP**
ID, TYPE: **E203, M**
FUNCTION: **Performs dumping of memory starting from STARTADD**
CONTENT: **NUMRECORD + STARTADD SEGMENT + STARTADD OFFSET**
- STARTADD OFFSET: 16 bit OFFSET to SEGMENT
- STARTADD SEGMENT: 80x86 CPU segment address paragraph aligned
- NUMRECORD: Number of memory blocks of 55 word size to be dumped

REMARK: **the length of the whole TC PACKET is fixed to 126 bytes**

202

HASI MEMORY LOAD



BIT NUMBER (0=LSB)
PACKET IDENTIFICATION
PACKET SEQUENCE COUNT
PACKET LENGTH
COMMAND HEADER

COMMAND CONTENT

PACKET ERROR CONTROL (CRC 16)

NAME: **MEMORY LOAD - EEPROM or RAM AREA**
ID, TYPE: **E204, M**
FUNCTION: **Loads one block in memory locations either in EEPROM or RAM**
CONTENT: **STARTADD SEGMENT + STARTADD OFFSET + NUMWORD + MEMBLOCK**

- STARTADD OFFSET : 16 bit OFFSET to SEGMENT
- STARTADD SEGMENT : 80x86 CPU segment address paragraph aligned
- NUMWORD: Number of words to be load
- MEMBLOCK: Array of NUMWORD words to be loaded (55 word)

REMARK: **the length of the whole TC PACKET is fixed to 126 bytes**

ANNEX 2 :

PPI SESSION TABLES DEFAULT

- PPI Normal session tables default
- PPI Health Check session tables default

The HASI PPI Normal session tables default

Ordinal		A (low) Sensor	Chn	B (medium) Sensor	Chn	C (high pressure) Sensor	Chn
1	S	P 1.1	1	P 2.7	15	P 1.1	1
2	S	P 1.8	8	P 2.8	16	P 1.8	8
3	H	P 3.7	23	P 1.1	1	P 2.7	15
4	H	P 3.8	24	P 1.8	8	P 2.8	16
5		T 1.3	3	T 1.3	3	T 1.3	3
6		P 1.6	6	P 1.6	6	P 1.6	6
7	H	P 3.7	23	P 1.1	1	P 2.7	15
8	H	P 3.8	24	P 1.8	8	P 2.8	16
9	S	P 1.1	1	P 2.7	15	P 1.1	1
10	S	P 1.8	8	P 2.8	16	P 1.8	8
11	H	P 3.7	23	P 1.1	1	P 2.7	15
12	H	P 3.8	24	P 1.8	8	P 2.8	16
13		T 2.3	11	T 2.3	11	T 2.3	11
14		P 2.1	9	P 2.1	9	P 2.1	9
15	H	P 3.7	23	P 1.1	1	P 2.7	15
16	H	P 3.8	24	P 1.8	8	P 2.8	16
17	S	P 1.1	1	P 2.7	15	P 1.1	1
18	S	P 1.8	8	P 2.8	16	P 1.8	8
19	H	P 3.7	23	P 1.1	1	P 2.7	15
20	H	P 3.8	24	P 1.8	8	P 2.8	16
21		T 3.3	19	T 3.3	19	T 3.3	19
22		C 3.1	17	C 3.1	17	C 3.1	17
23	H	P 3.7	23	P 1.1	1	P 2.7	15
24	H	P 3.8	24	P 1.8	8	P 2.8	16
25	S	P 1.1	1	P 2.7	15	P 1.1	1
26	S	P 1.8	8	P 2.8	16	P 1.8	8
27	H	P 3.7	23	P 1.1	1	P 2.7	15
28	H	P 3.8	24	P 1.8	8	P 2.8	16
29		P 2.7	15	P 3.7	23	P 3.7	23
30		P 2.8	16	P 3.8	24	P 3.8	24
31	H	P 3.7	23	P 1.1	1	P 2.7	15
32	H	P 3.8	24	P 1.8	8	P 2.8	16
33	S	P 1.1	1	P 2.7	15	P 1.1	1
34	S	P 1.8	8	P 2.8	16	P 1.8	8
35	H	P 3.7	23	P 1.1	1	P 2.7	15
36	H	P 3.8	24	P 1.8	8	P 2.8	16

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The HASI PPI Health Check session tables default

Ordinal	HC session G Sensor	Chn	HC session H Sensor	Chn
1	R 1.5	5	P 1.1	1
2	P 1.1	1	P 1.1	1
3	P 1.8	8	P 1.1	1
4	R 1.2	2	P 1.1	1
5	P 1.1	1	P 1.1	1
6	P 1.8	8	P 1.1	1
7	R 1.5	5	P 1.1	1
8	P 1.1	1	P 1.1	1
9	R 2.5	13	P 1.1	1
10	P 2.7	15	P 1.1	1
11	P 2.8	16	P 1.1	1
12	R 2.2	10	P 1.1	1
13	P 2.7	15	P 1.1	1
14	P 2.8	16	P 1.1	1
15	R 2.5	13	R 1.2	2
16	P 2.7	15	T 1.3	3
17	P 2.8	16	C 1.4	4
18	R 3.5	21	R 1.5	5
19	P 3.7	23	P 1.6	6
20	P 3.8	24	C 1.7	7
21	R 3.2	18	P 1.8	8
22	P 3.7	23	P 2.1	9
23	P 3.8	24	R 2.2	10
24	R 3.5	21	T 2.3	11
25	P 3.7	23	C 2.4	12
26	T 1.3	3	R 2.5	13
27	C 1.4	4	C 2.6	14
28	P 1.6	6	P 2.7	15
29	C 1.7	7	P 2.8	16
30	P 2.1	9	C 3.1	17
31	T 2.3	11	R 3.2	18
32	C 2.4	12	T 3.3	19
33	C 2.6	14	C 3.4	20
34	C 3.1	17	R 3.5	21
35	T 3.3	19	C 3.6	22
36	C 3.4	20	P 3.7	23
37	C 3.6	22	P 3.8	24