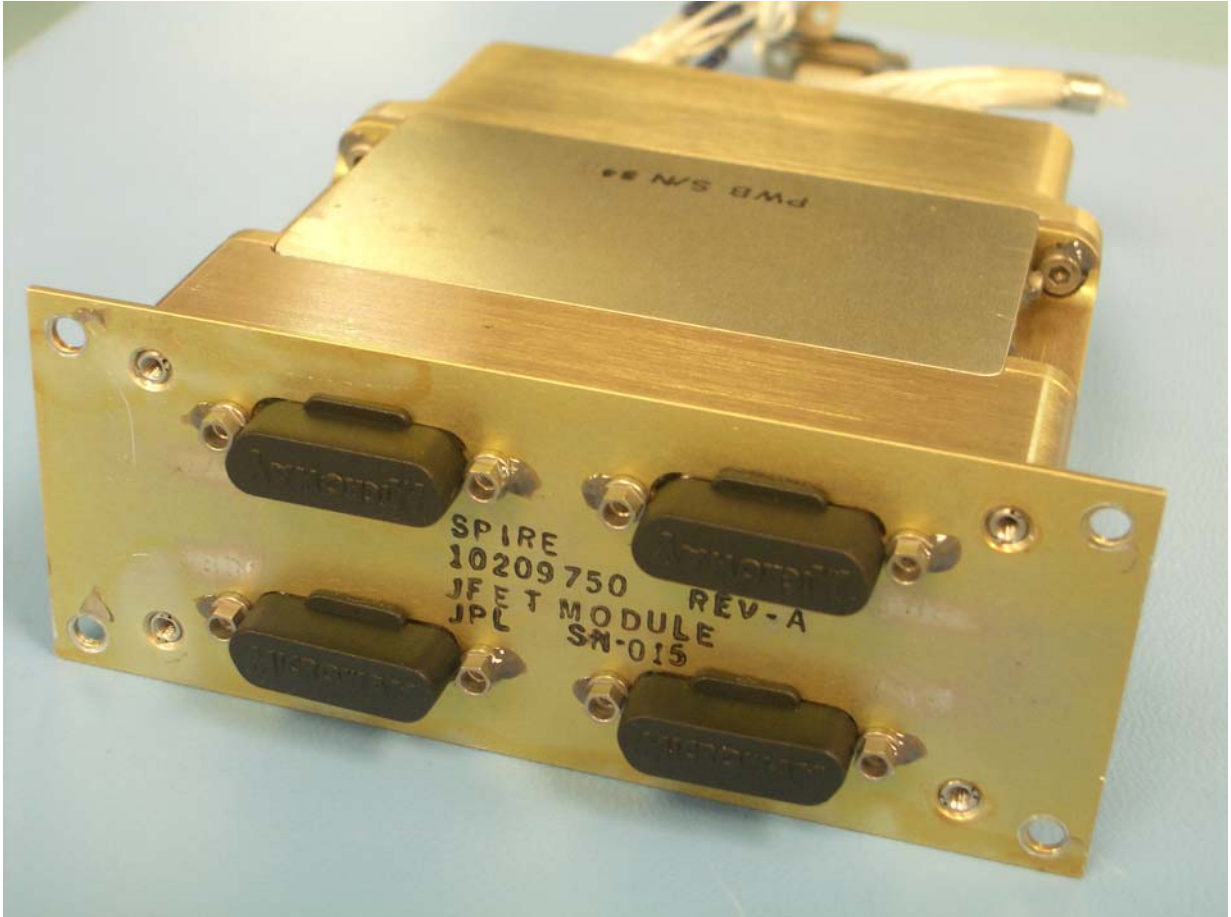


Assembly / Subsystem		PEM			Phone		Section		Date
SPIRE		Martin Herman			(818) 354-8541		386		3 February, 2005
Drawing/ Part No.	Dwg. Rev.	Nomenclature			Serial No.	Model	Type	Final IR No.	Mass (Meas. / Req.)
10209750-1	B	JFET Module			015	FLIGHT	N/A	923847	276.9 gm / 305 gm
Check applicable answer and provide explanation in remarks column		Y	N	N	Remarks		Data Attachments		Signature & Date
1. Are all drawings and specifications complete, approved, released and frozen?		X					14. Latest Top Assembly drawings <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None		Cognizant Engineer <i>[Signature]</i> 2/18/05
2. Do the released drawings and specifications reflect all approved changes?		X					15. List of open ECRs <input type="checkbox"/> Attached <input checked="" type="checkbox"/> None		PEM Martin H 2/18/05
3. Is hardware identical to other hardware delivered? If no, provide difference list.		X					16. Waivers (RFW request for waiver) <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None		QA Engineer 2/18/05 <i>[Signature]</i>
4. Does the hardware meet its functional requirements, specifications, waivers, ICDS?		X			EIDP attached. Also see item # 8 attachments.		17. Open MRB <input type="checkbox"/> Attached <input checked="" type="checkbox"/> None		Environments/Reliability J - 1 - el 2/18/05
5. Are all IR and MRB dispositioned and concurred by QA?		X					18. Open PFR on this H/W <input type="checkbox"/> Attached <input checked="" type="checkbox"/> None		Mission Assurance Mgr. J - 1 - el 2/18/05
6. Is complete as-built list information included in the build book?		X					19. Open PFR on similar H/W <input type="checkbox"/> Attached <input checked="" type="checkbox"/> None		Project Office J - 1 - el 2/18/05
7. Have all required environmental tests & analyses been completed?		X			ETAS attached		20. Handling Document → See Item 11 <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None		<i>[Signature]</i> 2/18/05
8. Is all required assembly and/or subsystem level functional testing complete?		X			Performance Test Data Attached. Also see EIDP in item # 4.		21. Shortage List <input type="checkbox"/> Attached <input checked="" type="checkbox"/> None		
9. Have all piece parts, processes and materials been approved by JPL?		X					22. Requirements Verification Matrix <input checked="" type="checkbox"/> Attached (See #4, #7, #8) <input type="checkbox"/> None		
10. Does this hardware meet all contamination control requirements?		X			Parts, processes and MIUL met all contamination control and out-gassing requirements.		23. Qualification Status <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None		
11. Are all shipping containers, shipping and special handling procedures ready?		X			See Attached Document D-26790		24. Mate / Demate Record <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None		
12. Is additional work required to bring this hardware to flight readiness?			X				25. Operating Log <input checked="" type="checkbox"/> Attached (See Item # 24) <input type="checkbox"/> None		
13. Is this hardware acceptable for flight?		X					26. MICD <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None		



RAL EIDP Table of Contents Versus JPL HRCR Check List Item Numbers

RAL EIDP Section Number	RAL EIDP Title	JPL HRCR Check List Item Number	Notes
1	Shipping Documents		Shipper and Final IR
2	Transportation, Packing, Handling & Integration Procedures	11	Special Handling Document D-26790
3	Certificate of Conformance / Delivery Review Board MOM		HRCR book is the C of C
4	As Built Configuration Status List	1 & 2	Assembly Drawings
5	List of Waivers	4	RFW (request for waiver) Attached
6	Copies of Waivers	4 & 7	RFW (request for waiver) Attached
7	List of Non-Conformance Reports		See RFW in 4 & 7
8	Copies of Non-Conformance Reports		See RFW in 4 & 7
9	Cleanliness Statement		Final IR QA Inspection
10	Operational Manual		NA
11	Top Level Drawings (inc. Family Tree)	14	Top Assembly Drawing
12	Interface Drawings	26	MICD Drawing
13	Functional, Block & Mechanical Drawings		NA
14	Electrical Circuit Drawings		NA
15	Serialized Components List		In build books – not shipped
16	Mass Properties/ Power Budget	HRCR Check List Page 1	Mass listed in HRCR check list
17	Qualification Status List / Test Matrix	23	Qualification Unit Test Matrix
18	Test Reports	4, 7, 8, 23	
19	Open Work / Deferred Work / Open Tests		NA
20	Calibration Data		NA
21	Historical Record	23	Qualification Unit Test Matrix
22	Manufacturing Logbook(s)		In build books – not shipped
23	Operating Time / Cycle Record	25	
24	Connector Mating Record	24	
25	Age Sensitive Items Record		NA
26	Pressure Vessels – History/Test Record		NA
27	Temporary Installation Record		NA
28	Reference List of EIDPs (Lower level)		NA
29	Other Useful Information		NA

JPL Hardware Requirements
Certification Review (HRCR)

Junction Field Effect Transistor (JFET)
Flight Module

10209750-1 S/N 015

SPIRE Element
Herschel Space Observatory Project

February 3, 2005

Configuration of Module, Boards & Membranes

Module 10209750-1	S/N 15	S/N 15
PWB 10209760-1	S/N 34	S/N 35
Membrane 10209758-1	J6.4.1	J6.4.4

Attachment of HRCR Items #1 Drawing Release Status

ALL ASSEMBLY & PARTS DRAWINGS ARE RELEASED IN PDMS

Released Drawings:

- 10209719-1 assembly built per released Rev. A drawing (studlock)**
- 10209722-1 assembly built per released Rev. B drawing (interface drawing)**
- 10209750-1 assembly built per released Rev. B drawing (module assy)**
- 10209751-1 assembly built per released Rev. B drawing (chassis 1)**
- 10209752-1 assembly built per released Rev. A drawing (chassis 2)**
- 10209753-1 assembly built per released Rev. A drawing (chassis 3)**
- 10209754-1 assembly built per released Rev. C drawing (mount)**
- 10209756-1 assembly built per released Rev. B drawing (chassis lid)**
- 10209757-1 assembly built per released Rev. A drawing (membrane)**
- 10209758-1 assembly built per released Rev. A drawing (membrane assy)**
- 10209759-1,-2,-4 redlined Rev. B drawing (gasket)**
- 10209760-1 assembly built per released Rev. C drawing (board assembly)**
- 10209761-1 assembly built per released Rev. C drawing (solder connector)**
- 10209769-1 assembly built per released Rev. A drawing (stiffener)**
- 10209777-1 assembly built per released Rev. B drawing (board)**
- 10209858-2 assembly built per released Rev. A drawing (special fastener)**
- 10217636-1 assembly built per released Rev. A drawing (clip)**

Attachment of HRCR Item #4: EIDP

EIDP Coveragepage For JFET Testing

Unit Identification						
Name	:	JFET PFM Module				
Part #	:	10209750-1				
S/N	:	#015				

Environmental Testing						
	Axes Tested	Temp	Duration/# of Cycle	Requirement	Source	Waiver
Random Vibration Test	X, Y, Z	Rm T	1 min/axis	X, Y, Z	SSSD, JFET-DES-07	
High Level Sine Vibe Test	None	NA	NA	X, Y, Z	SSSD, JFET-DES-07	HR-SP-JPL-RFW-005
Bakeout	NA	80 C	28 hrs	> 24 HRS		
Thermal Cycles	NA	RmT to 80 K	2	Minimum 1	D-20549	

Performance Characteristics						
		Specification		Source	Waiver	
Power needed for <11 bad channels (Min Perf.)	8.11 mW	11 mW for CQM, 7 mW for PFMFS		SSSD, JFET-TEC-05, JFET-PER-02	HR-SP-JPL-RFW-004	
Power needed for <4 bad channels (Design Value)	8.24 mW	11 mW for CQM, 7 mW for PFMFS		SSSD, JFET-TEC-05, JFET-PER-02		
Power needed for 100 % Yield per unit	9.14 mW	NA		NA		
Median Noise at < 11 bad chs.	10.17 nV/rtHz	<15 nV/rtHz	<7 nV/rtHz	SSSD, JFET-PER-01		
Median Noise at < 4 bad chs.	8.88 nV/rtHz	Min	Design	SSSD, JFET-PER-01		
Median Noise at 100 % Yield.	7.30 nV/rtHz	Performance	Value	SSSD, JFET-PER-01		
# of Channels over the max. offset voltage	0	< 15 mV		SSSD, BDA-DRCU-27		
Common Mode Rejection Ratio	< -80 dB by design, as measured in EM4 unit			SSSD, BDA-DRCU-11		

Board Level Details						
	Board SN 034 (JAA-JDD)		Board SN 035 (JAA'-JDD')		Source	
# Channels Tested	24		24			
Median Noise at 3.5 mW	19.35 nV/rtHz		15.92 nV/rtHz		SSSD, JFET-PER-01	
# of good channels at 3.5 mW	9	37.5% Yield	11	45.8% Yield	SSSD, JFET-PER-02	
Power Needed for 100 % Yield	4.72		4.42 mW		SSSD, JFET-PER-02	
Median Noise at High Power (w/ 100 % Yield)	7.32 nV/rtHz		7.24 nV/rtHz		SSSD, JFET-PER-01	
Median Gain at High Power	0.98		0.98		NA	
Heater Resistance, 4K Reference value	2.92 kΩ		3.01 kΩ		NA	

Definitions						
Good Channels	: Noise less than a min. performance value of 15 nV/rtHz					
Yield	: # of Good Channels / 24					

Filenames						
Noise Measurements	: JFET_Mod15_brd34, 35_Noise_perf.pdf					
Source Voltages (RmT, 4K)	: JFET Module 12,15 voltage data.pdf					

Notes						
1) The Base temperature for all performance characterization was 4K						
2) All Noise Measurements were made with the inputs shorted to ground						
3) Type of membranes:		SN034: 33% Overetched Perforated		SN035: 31% Overetched Perforated		

Attachment of HRCR Item # 4: RFW (request for waiver)

		RFW/RFD Number:	HR-SP-JPL-RFW-016	
Spacecraft / Project	Herschel	Originator's Name	Steve Tseng	
System / Experiment / Model	1.1 SPIRE	Signature / Date		
Sub-System	detectors	Request Type (Highlight applicable request)	Waiver (RFW)	Deviation (RFD)
Assembly	JFET modules	1.1.1.1 <u>Organisation</u>	Jet Propulsion Laboratory	
Sub-Assembly		Ref. Doc. / Drwg No.	SPIRE-JPL-PRJ-000456	
Item		References		
Serial No.				
RFW/RFD Title	JFET Power Dissipation s/n 015			

End Items(s) Affected (Hardware, Software)				
Name	CI-Number	Model(s)		
JFET Module p/n 10209750 s/n 015		PFM		
Requirement / Interface Documents Affected				
Specification/Drawing Title	Number	Issue	Date	App. Paragraph
BDA-SSSD	SPIRE-JPL-PRJ-0004456	3.2	7/1/03	JFET-PER-01 JFET-PER-02 JFET-TEC-05
Description of Deviation / Discrepancy / Non-Conformance				
<p>Requirement states that dissipation of photometer JFETs is to be less than 7 mW average, while supplying 90% of channels with voltage noise < 15 nV/rHz according to BDA-SSSD JFET-PER-01, JFET-PER-02, JFET-TEC-05. Measured JFET performance of the JFETs indicates that 8.11 mW of power dissipation will be required to meet the specified yield and noise performance specifications.</p>				
Other Items or Requirements (Potentially) Affected				
<p>Overall sensitivity of the bolometer sub-system is affected by JFET noise performance. JFET power dissipation impacts the heat sink temperature of the 3He refrigerator and may in turn increase the base detector temperature. Dissipation of JFETs affects power dissipation on cryostat.</p>				
Need for RFW/RFD and Rationale for Acceptance				
<p>Measured JFET performance of JFETs indicates that 8.11 mW of power dissipation will be required to meet the specified yield and noise performance specifications. JPL is unable to significantly alter the JFET fabrication process in order to meet the power specification without undue risk to the stated PFM/FS delivery dates. Furthermore, JPL requests a full system optimisation to revisit the noise and power requirements on the JFETs. The JFET modules can meet the noise design value with 100 % yield at 9.14 mW.</p>				
	Approved	Rejected	Name	Date
Engineering:				
Product Assurance:				
CCB-Chairman:				
Principal Investigator				
Product Assurance:				
Co-Investigator				
Prime Contractor				
ESA Project Office				

Attachment of HRCR Item #7: RFW (request for waiver)

RFW/RFD Number:	HR-SP-JPL-RFW-005
------------------------	--------------------------

Spacecraft / Project	Herschel	Originator's Name	Kalyani Sukhatme	
System / Experiment / Model	SPIRE	Signature / Date		
Sub-System	detectors	Request Type (Highlight applicable request)	Waiver (RFW)	Deviation (RFD)
Assembly		Organisation	Jet Propulsion Laboratory	
Sub-Assembly		Ref. Doc. / Drwg No.	SPIRE-JPL-PRJ-000456	
Item		References		
Serial No.				
RFW/RFD Title	BDA and JFET module sine test deletion			

End Items(s) Affected (Hardware, Software)		
Name	CI-Number	Model(s)
Bolometric Detector Assemblies JFET Modules		CQM, PFM, FS CQM, PFM, FS

Requirement / Interface Documents Affected				
Specification/Drawing Title	Number	Issue	Date	App. Paragraph
BDA-SSSD (SPIRE-JPL-PRJ-000456)		3.2	Jan 7, 2003	BDA-DES-10, JFET-DES-07

Description of Deviation / Discrepancy / Non-Conformance
 High Level Sine- Vibe Test is not performed on these units

Other Items or Requirements (Potentially) Affected

Need for RFW/RFD and Rationale for Acceptance
 The hardware has to be qualified under a cold vibration test and is installed in the cold vibration facility for the purpose of the test. The high level sine vibration test configuration will put the hardware and the personnel at risk since the cold vibration facility is not structurally capable of withstanding the high levels. Obtaining additional resources (cost and schedule) for developing a new set-up is not feasible at this time.

	Approved	Rejected	Name	Date
JPL Engineering:				
JPL Product Assurance:				
CCB-Chairman:				
Principal Investigator				
Product Assurance:				
Co-Investigator				
Prime Contractor				
ESA Project Office				

Attachment of HRCR Item #7: ETAS (environmental test summary)

ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)						
AUTHORIZATION SECTION						
PROJECT Herschel			LOG NO. HS037			
SYSTEM/ASSEMBLY TITLE S JFET Modules S/N 12,15				DATE ISSUED 2/03/05		
REFERENCE DESIGNATION NUMBER		PART NO. (IF MULTIPLE, ATTACH LIST) 10209750-1		REV.	SERIAL NO. 012, 015	
HARDWARE TYPE <input type="checkbox"/> EM QUAL <input checked="" type="checkbox"/> FLIGHT <input type="checkbox"/> FLIGHT SPARE <input type="checkbox"/> OTHER			PRE-ENVIRONMENTAL INSPECTION REPORT NUMBER (ATTACH IR)			
WIRING HARNESS <input type="checkbox"/> EM QUAL <input type="checkbox"/> FLIGHT <input type="checkbox"/> EM <input type="checkbox"/> SE			PART NO.	REV.	SERIAL NO.	
TEST DESCRIPTION (CHECK ALL APPLICABLE) <input type="checkbox"/> SINE VIBRATION <input type="checkbox"/> PYROSHOCK <input type="checkbox"/> ACOUSTIC <input type="checkbox"/> EMC <input type="checkbox"/> OTHER _____ <input type="checkbox"/> RANDOM VIBRATION <input checked="" type="checkbox"/> THERMAL VAC. <input type="checkbox"/> THERMAL ATMOSPHERE			TYPE OF TEST <input type="checkbox"/> QUALIFICATION <input type="checkbox"/> FLIGHT ACCEPTANCE <input checked="" type="checkbox"/> PROTO FLIGHT <input type="checkbox"/> RETEST			
WILL ALL TESTS/LEVELS/DURATIONS REQUIRED BY THE PROJECT DOCUMENTS BE PERFORMED ON THIS UNIT? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) ENTER PROJ. DOC. NO. AND REV. _____						
HAS THE UNIT PASSED ALL PRE-ENVIRONMENTAL FUNCTIONAL TESTS? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION _____						
HAVE ALL DESIGN ANALYSES BEEN COMPLETED AND REQUIRED CHANGES BEEN IMPLEMENTED? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION _____						
IS THE TEST ARTICLE IDENTICAL TO OTHER FLIGHT UNITS? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION _____						
ARE ALL PFRs AGAINST THIS UNIT CLOSED? <input type="checkbox"/> YES <input checked="" type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION PFR's in process of closure. All issues have been addressed and qualified. See PFR # Z84742 and Z84924						
HAVE ALL WAIVERS AND ECRs BEEN APPROVED AND ARE THEY INCORPORATED? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION _____						
TEST AUTHORIZED BY						
COGNIZANT ENGINEER 		DATE 2/7/05	TECHNICAL MGR./INSTR MRG./PI PREP REP 		DATE 2/7/05	
			ENVIRONMENTAL REQUIREMENTS ENG. 		DATE 2-7-05	
SUMMARY SECTION						
TEST AGENCY (IF MULTIPLE, ATTACH SUMMARY AND TEST DATES) JPL Building 144		TEST INITIATION DATE 11/11/04		ACCUMULATED OPERATING HOURS PRIOR TO FIRST ENVIRONMENTAL TEST		
SERIAL NUMBERS ACTUALLY TESTED SN 12 & 15		TEST TERMINATION DATE		OPERATING HOURS DURING ENVIRONMENTAL EXPOSURE		
TEST DESCRIPTION						
VIBRATION AXES: X Y Z SINE VIBRATION <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> RANDOM VIBRATION <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>		ACOUSTIC <input type="checkbox"/>	PYROSHOCK SHOCK AXES: X Y Z <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> SHOCKS/AXIS: _____		<input checked="" type="checkbox"/> THERMAL VACUUM PRESSURE: <10E-5 <77K h.R.T. 1 cycle NO OF CYCLES: 1 1	<input type="checkbox"/> TEMPERATURE ATMOSPHERE <input type="checkbox"/> OTHER
EMC <input type="checkbox"/> ESD <input type="checkbox"/> COND. SUSC. <input type="checkbox"/> RAD. SUSC.		<input type="checkbox"/> COND. EMIS. <input type="checkbox"/> RAD. EMIS.		<input type="checkbox"/> ISOLATION <input type="checkbox"/> MAGNETICS	TEMP. LEVEL (°c) AND ACCUMULATED DURATION (HRS.) HOT: _____°c _____h COLD: _____°c _____h HOT: _____°c _____h COLD: _____°c _____h	
WERE THERE ANY PFRs GENERATED DURING ENVIRONMENTAL TESTS? <input type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST)			LIST PFR NOS. / BRIEF EXPLANATION			
ARE THE POST ENVIRONMENTAL DAMAGE INSPECTIONS COMPLETE? <input type="checkbox"/> YES <input type="checkbox"/> NO (IF YES, ATTACH A COPY OF THE INSPECTION REPORTS. IF NO, ATTACH EXPLANATION)			LIST PFR NOS. / BRIEF EXPLANATION			
WERE ALL PLANNED TESTS/LEVELS/DURATIONS ACHIEVED? <input type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST)			LIST PFR NOS. / BRIEF EXPLANATION			
<input type="checkbox"/> TESTS HAVE NOT BEEN SUCCESSFULLY COMPLETED. SEE THE ATTACHED SUMMARY FOR ACTIONS THAT NEED TO BE TAKEN.						
COGNIZANT ENGINEER		DATE	TECHNICAL MGR./INSTR MRG./PI PREP REP		DATE	
			ENVIRONMENTAL REQUIREMENTS ENG.		DATE	
<input checked="" type="checkbox"/> HARDWARE HAS SUCCESSFULLY COMPLETED THE ENVIRONMENTAL TESTS LISTED ON THIS FORM OR REMAINING ACTIONS HAVE BEEN TAKEN, INCLUDING RETEST.						
COGNIZANT ENGINEER 		DATE 2/7/05	TECHNICAL MGR./INSTR MRG./PI PREP REP 		DATE 2/7/05	
			ENVIRONMENTAL REQUIREMENTS ENG. 		DATE 2-7-05	

Attachment of HRCR Item #7: ETAS (environmental test summary)

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ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)

OTHER AUTHORIZATION PROVISIONS AND EXPLANATIONS

2 to 3 vacuum thermal cycles will also be completed.

3-axis vibrate was completed and is carried on AIDS#'s 243946 and 244164, ETAS#'s HSO31 nad HSO32.

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Attachment of HRCR Item #7: ETAS (environmental test summary)

ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)							
ENVIRONMENTAL TEST SUMMARY							
HARDWARE	S/N	ETAS	TEST ENVIRONMENT LEVELS & DURATION	DATE TEST PERFORMED	TEST AGENCY	PASS/ FAIL	COMMENTS
SPIRE JFET (10209750-1)	012,01 5	HSO37	1 2-3 vacuum thermal cycles. <10E-5 mbar, <70K to RT .				

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Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise For Module 15

JFET SOURCE VOLTAGE MEASUREMENT

Post Vibe, post bake, SN12,15 module, gm dewar, rm T.

PERF TEST Post Vibe, post bake, SN12,15 module, gm dewar, Helium.

Date		11/5/2004	11/5/2004	11/5/2004	11/5/2004	11/9/2004	11/9/2004	11/9/2004	11/9/2004
T. plate		Rm T	Rm T	Rm T	Rm T	4K	4K	4K	4K
Vdd		3	3	3	3	3	3	3	3
Vss		-1.5	1.5	-1.5	-1.5	-1.5	1.5	-1.5	-1.5
Idd		1.0288	0.9858	1.22	1.1346	0.9691	0.9247	1.1077	1.0211
Iss		1.0269	0.9839	1.2181	1.1327	0.9608	0.9258	1.1088	1.0223
SN		22	23	34	35	22	23	34	35
Channel #		DELTA	DELTA	DELTA	DELTA	DELTA	DELTA	DELTA	DELTA
1	a	1.002	0.973	0.977	1.125	0.691	0.643	0.685	0.629
	b	0.999	0.976	0.978	1.123	0.684	0.647	0.684	0.626
2	a	1.041	1.587	1.039	0.746	0.729	1.283	0.749	0.434
	b	1.043	1.578	1.038	0.741	0.734	1.277	0.745	0.428
3	a	1.037	1.516	1.214	1.198	0.725	1.209	0.930	0.901
	b	1.042	1.524	1.211	1.198	0.730	1.216	0.927	0.901
4	a	0.981	0.980	0.894	1.149	0.662	0.649	0.599	0.849
	b	0.980	0.977	0.889	1.149	0.662	0.644	0.595	0.852
5	a	1.420	0.965	1.781	0.921	1.102	0.630	1.520	0.618
	b	1.429	0.965	1.793	0.928	1.109	0.632	1.534	0.624
6	a	1.745	1.727	0.974	0.960	1.466	1.405	0.661	0.657
	b	1.758	1.714	0.972	0.961	1.477	1.391	0.661	0.657
7	a	0.974	1.342	0.996	1.108	0.651	1.021	0.689	0.808
	b	0.970	1.335	1.000	1.107	0.648	1.014	0.695	0.805
8	a	1.000	0.897	0.962	0.820	0.682	0.565	0.666	0.509
	b	0.999	0.896	0.966	0.825	0.680	0.558	0.669	0.515
9	a	0.984	1.415	1.048	1.286	0.638	1.093	0.749	0.992
	b	0.965	1.422	1.045	1.279	0.641	1.099	0.744	0.984
10	a	0.973	1.058	0.981	1.314	0.649	0.727	0.683	1.020
	b	0.972	1.058	0.978	1.319	0.647	0.726	0.681	1.023
11	a	0.969	0.527	1.157	0.970	0.637	0.168	0.856	0.651
	b	0.972	0.515	1.155	0.968	0.642	0.156	0.857	0.650
12	a	0.971	0.918	1.311	0.950	0.641	0.673	1.024	0.639
	b	0.973	0.927	1.318	0.947	0.644	0.682	1.030	0.635
13	a	0.970	1.414	1.011	0.971	0.645	1.097	0.708	0.653
	b	0.972	1.405	1.011	0.974	0.649	1.089	0.708	0.656
14	a	1.246	0.961	1.061	0.987	0.933	0.622	0.754	0.673
	b	1.240	0.963	1.064	0.986	0.929	0.625	0.757	0.671
15	a	1.307	0.962	1.172	0.847	0.992	0.613	0.877	0.519
	b	1.292	0.962	1.176	0.845	0.982	0.615	0.882	0.516
16	a	1.534	1.749	0.745	1.113	1.242	1.451	0.422	0.805
	b	1.540	1.759	0.757	1.114	1.246	1.461	0.434	0.804
17	a	1.116	1.002	1.145	0.991	0.808	0.675	0.851	0.682
	b	1.123	1.008	1.144	0.988	0.813	0.680	0.849	0.679
18	a	0.981	1.095	1.146	1.067	0.646	0.769	0.856	0.762
	b	0.960	1.094	1.152	1.064	0.641	0.770	0.861	0.756
19	a	0.931	0.970	0.889	0.506	0.619	0.641	0.594	0.181
	b	0.934	0.970	0.888	0.498	0.622	0.642	0.591	0.173
20	a	0.963	0.846	1.119	0.980	0.633	0.515	0.824	0.652
	b	0.964	0.849	1.116	0.976	0.636	0.519	0.824	0.649
21	a	0.965	1.641	1.164	1.358	0.650	1.341	0.874	1.071
	b	0.964	1.631	1.169	1.359	0.648	1.331	0.880	1.071
22	a	1.022	1.672	1.256	1.044	0.712	1.373	0.970	0.743
	b	1.026	1.667	1.255	1.043	0.714	1.370	0.972	0.743
23	a	1.007	0.961	1.700	0.963	0.694	0.639	1.437	0.657
	b	1.007	0.960	1.711	0.960	0.696	0.633	1.449	0.655
24	a	0.982	1.708	1.059	0.981	0.668	1.407	0.769	0.670
	b	0.983	1.695	1.055	0.981	0.668	1.396	0.767	0.674

Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise

Board S/N 034 in Module S/N 015

	Pwr1	Pwr2	Pwr3	Pwr4	Pwr5	Pwr5b	Pwr7	Pwr8	Pwr9	Pwr10	Pwr11	Pwr12	Pwr13	Pwr14
Vdd (V)	2.5	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.82	2.84	2.87	2.8
Vss (V)	-1.5	-1.7	-1.8	-1.5	-1.4	-1.45	-1.47	-1.46	-1.48	-1.25	-1.45	-1.45	-1.45	-1.45
Vdd' (V)	2.205	2.477	2.49	2.503	2.518	2.51	2.507	2.508	2.505	2.535	2.529	2.549	2.578	2.509
Vss' (V)	-1.212	-1.385	-1.298	-1.21	-1.124	-1.1667	-1.1841	-1.1754	-1.1926	-0.9929	-1.1667	-1.1664	-1.1664	-1.1665
Idd (mA)	1.1353	1.2431	1.1935	1.1431	1.0929	1.118	1.128	1.123	1.133	1.0169	1.1185	1.1189	1.1197	1.1179
Iss (mA)	1.0967	1.2032	1.1538	1.1034	1.0534	1.0784	1.0884	1.0834	1.0934	0.9778	1.0788	1.0792	1.08	1.0783
I (mA)	1.116	1.22315	1.17365	1.12325	1.07315	1.0982	1.1082	1.1032	1.1132	0.99735	1.09865	1.09905	1.09985	1.0981
P (mW)	3.813372	4.7238053	4.4467862	4.17062725	3.906266	4.03775194	4.09047702	4.06352688	4.11618832	3.518551065	4.060280805	4.08341037	4.11827834	4.03606655

	Channel Num	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	
15	Channel: 1	7.25	6.63	7.29	7.36	6.89	7.51	5.51	6.60	6.67	7.70	6.85	7.19	6.57	5.61
14	Channel: 2	20.95	9.40	12.63	11.83	17.29	14.91	13.23	15.81	12.17	25.80	12.55	12.05	10.74	13.46
13	Channel: 3	23.13	8.25	9.89	12.62	22.89	17.25	14.94	14.44	15.32	25.46	15.32	15.41	14.39	19.17
12	Channel: 4	7.80	7.33	6.39	6.36	7.56	6.04	6.77	7.89	6.77	15.64	5.14	6.65	7.55	7.09
10	Channel: 5	7.68	7.04	5.61	6.01	5.18	6.00	7.29	5.27	6.34	8.07	5.63	5.93	8.12	5.66
9	Channel: 6	15.19	9.70	13.71	14.51	13.97	15.22	14.72	12.66	14.04	22.84	14.75	14.17	12.73	15.07
8	Channel: 7	15.87	7.61	8.00	9.57	12.75	10.74	9.67	9.21	10.78	31.31	11.88	10.21	10.09	11.43
7	Channel: 8	6.29	6.58	7.97	7.43	7.24	6.48	7.10	5.97	4.94	7.94	5.46	7.63	7.67	5.90
6	Channel: 9	7.67	12.84	11.56	9.10	6.99	8.91	8.86	8.51	7.28	7.68	8.82	9.92	9.74	8.18
5	Channel: 10	22.10	12.23	11.88	13.39	17.74	16.95	16.15	15.55	14.87	17.78	15.40	16.86	17.30	14.61
4	Channel: 11	9.71	8.34	8.46	8.27	9.79	8.67	9.08	7.31	7.37	20.65	8.58	8.16	11.04	8.61
3	Channel: 12	16.51	7.30	9.97	11.97	16.15	15.03	14.53	13.22	13.96	28.38	12.45	12.67	16.23	14.49
28	Channel: 13	12.36	7.67	8.43	9.14	9.26	11.53	9.65	9.93	9.10	11.17	10.04	10.56	9.59	8.60
27	Channel: 14	20.74	7.23	7.49	11.80	18.68	12.30	11.28	11.54	9.54	36.05	12.63	12.71	13.36	11.37
26	Channel: 15	17.70	7.27	8.27	9.50	12.71	10.23	8.98	9.49	8.36	47.45	9.02	10.20	9.71	10.18
25	Channel: 16	10.90	5.99	6.72	7.98	9.10	6.87	7.78	7.74	7.57	20.12	7.64	8.80	7.25	7.26
24	Channel: 17	18.85	7.31	6.81	14.41	15.27	15.19	12.55	15.24	14.26	20.66	14.27	14.82	16.84	14.41
23	Channel: 18	18.03	6.52	9.33	12.51	16.97	15.04	11.38	14.87	13.02	32.09	12.63	12.14	12.12	14.07
22	Channel: 19	14.11	7.85	7.67	9.69	11.52	10.61	9.01	9.41	9.47	18.59	10.39	10.01	9.57	12.52
21	Channel: 20	6.79	5.56	7.62	6.40	7.64	7.58	6.28	6.92	6.39	11.92	5.56	7.60	6.82	6.15
19	Channel: 21	55.55	14.67	19.34	33.31	51.83	40.98	38.62	44.99	41.44	64.83	41.75	36.89	37.97	50.45
18	Channel: 22	8.85	7.38	6.37	9.24	6.88	6.55	6.57	6.31	6.58	9.12	7.24	6.55	6.22	6.81
17	Channel: 23	7.57	5.71	6.12	6.88	5.66	5.47	6.67	5.85	6.72	11.12	6.16	6.53	5.50	6.58
16	Channel: 24	8.09	6.59	9.38	7.88	8.12	7.82	6.90	7.23	7.03	11.33	8.11	8.17	9.02	9.37
	Median	13.24	7.32	8.13	9.37	10.66	10.42	9.03	9.31	8.73	19.35	9.53	10.11	9.73	9.78
	Overall Mean	14.99	8.04	8.04	10.71	13.25	11.83	10.98	11.33	10.83	21.40	11.18	11.33	11.51	11.96
	Good Mean	8.85	8.04	8.59	9.73	8.83	8.72	9.49	9.02	9.24	9.56	9.32	9.65	9.39	9.64
	MP Req'd					15									
	Yield	0.54	1.00	0.96	0.96	0.67	0.71	0.92	0.83	0.92	0.38	0.88	0.88	0.83	0.88
	# Good Ch.	13	24	23	23	16	17	22	20	22	9	21	21	20	21
	# Bad Ch.	11	0	1	1	8	7	2	4	2	15	3	3	4	3

Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise

Board S/N 035 in Module S/N 015

	Pwr1	Pwr2	Pwr3	Pwr4	Pwr5	Pwr5b	Pwr7
Vdd (V)	2.8	2.8	2.8	2.8	2.8	2.8	2.8
Vss (V)	-1.5	-1.6	-1.55	-1.7	-1.57	-1.65	-1.35
Vdd' (V)	2.527	2.515	2.521	2.5016	2.518	2.508	2.545
Vss' (V)	-1.2319	-1.32	-1.276	-1.407	-1.293	-1.363	-1.1
Idd (mA)	1.051	1.0653	1.075	1.1478	1.0847	1.1236	0.9772
Iss (mA)	1.0168	1.0994	1.0407	1.1133	1.0502	1.0891	0.9434
I (mA)	1.0339	1.08235	1.05785	1.13055	1.06745	1.10635	0.9603
P (mW)	3.88632671	4.15081225	4.01665645	4.41886773	4.06805195	4.28268085	3.5002935

Channel Num			Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	
15	Channel: 1	7.94	9.94	15.60	8.06	8.43	8.59	12.88
14	Channel: 2	8.24	5.46	8.12	6.59	7.09	6.79	15.02
13	Channel: 3	6.89	5.30	6.94	6.83	6.02	5.77	9.37
12	Channel: 4	7.49	7.69	6.85	8.81	7.94	8.80	9.02
10	Channel: 5	12.47	7.91	9.43	7.24	9.49	6.72	33.50
9	Channel: 6	6.06	5.38	6.67	6.40	5.82	6.53	6.88
8	Channel: 7	15.84	7.73	10.69	6.92	10.17	6.93	23.09
7	Channel: 8	6.97	5.83	7.55	5.47	6.70	6.77	8.81
6	Channel: 9	26.80	19.64	23.86	11.78	20.62	13.92	33.02
5	Channel: 10	10.17	8.70	8.25	6.78	7.95	9.20	12.89
4	Channel: 11	10.08	9.20	7.49	10.40	9.65	9.61	9.91
3	Channel: 12	19.74	12.38	13.89	7.24	13.37	8.14	36.82
28	Channel: 13	11.07	8.13	11.67	8.42	10.74	9.03	18.65
27	Channel: 14	18.31	14.19	16.04	10.49	16.92	12.86	36.78
26	Channel: 15	45.18	24.40	30.21	10.93	27.32	15.37	85.29
25	Channel: 16	9.51	8.23	8.43	5.82	7.50	7.61	17.77
24	Channel: 17	14.61	8.89	10.56	5.82	9.23	7.74	27.82
23	Channel: 18	12.53	11.62	11.47	9.09	11.20	9.60	23.21
22	Channel: 19	8.63	8.50	7.25	7.14	6.84	7.28	14.23
21	Channel: 20	12.03	11.06	10.94	13.11	12.17	13.23	12.64
19	Channel: 21	20.04	14.62	16.68	7.37	16.08	9.97	24.00
18	Channel: 22	5.30	6.66	5.01	6.34	5.71	6.35	7.58
17	Channel: 23	6.76	6.05	6.35	5.70	8.42	6.61	16.82
16	Channel: 24	6.51	8.58	6.88	7.63	7.31	6.38	8.98
	Median	10.12	8.54	8.93	7.24	8.83	7.94	15.92
	Overall Mean	12.88	9.84	11.12	7.93	10.53	8.74	21.04
	Good Mean	9.07	8.73	8.65	7.93	8.59	8.45	10.29
	MP Req'd					15		
	Yield	0.75	0.92	0.79	1.00	0.83	0.96	0.46
	# Good Ch.	18	22	19	24	20	23	11
	# Bad Ch.	6	2	5	0	4	1	13

Attachment of HRCR Item # 9: SPIRE MIUL Cover Page

MIUL = Material Identification & Utilization List

Declared Materials List's and Processes List are not included in this HRCR

Materials and Processes List

SPIRE

JPL D-25725

REV B
1/05/04

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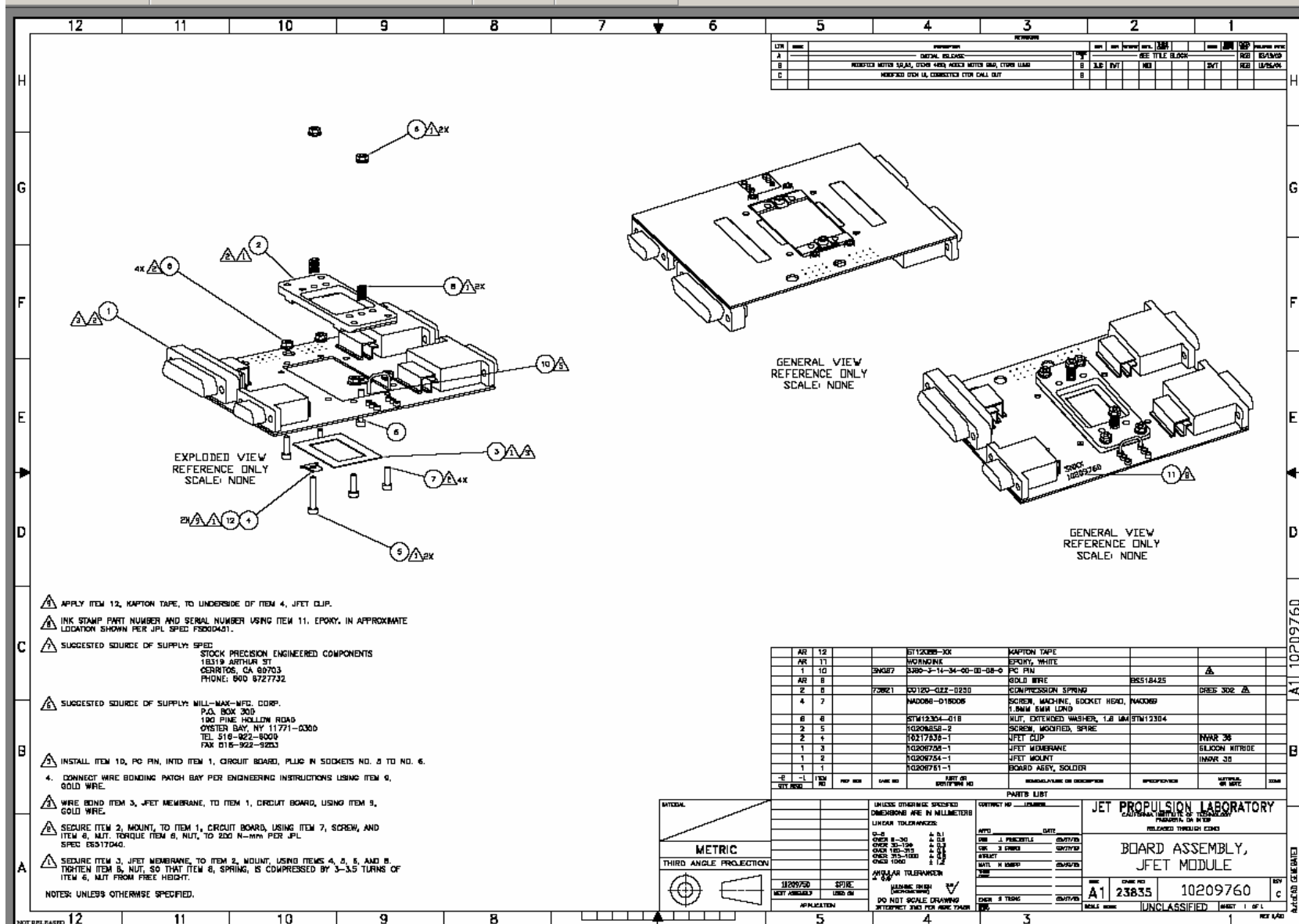
Reviewed by:


M. Knopp M&P Engineer

Attachment of HRCR Item # 11:

**See End of This HRCR Package for
“JFET Module Handling Document”**

Attachment of HRCR Item # 14: JFET Module Top Assembly Drawing 10209750-1



Attachment of HRCR Item # 23: Qualification Compliance Test

Qualification Model JFET Module

EIDP Coveragepage For JFET Testing						
Unit Identification						
Name	:	JFET QM Module				
Part #	:	10209750-1				
S/N	:	#001				
Environmental Testing						
		Axes Tested	Temperature	Duration/# of Cycle	Requirement	Source Waiver
Random Vibration Test		X, Y, Z	100 K	2 min/axis	X, Y, Z	SSSD, JFET-DES-07
High Level Sine Vibe Test		None	NA	NA	X, Y, Z	SSSD, JFET-DES-07 HR-SP-JPL- RFW_005
Bakeout		NA	80 C	72 Hours	80C, 72 Hrs	D-20549
Thermal Cycles		NA	RmT to 80 K	27	Minimum 15	D-20549
Performance Characteristics						
			Specification		Source	Waiver
Power needed for <11 bad channels (Min Perf.)	9.1 mW		11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	RFW in process
Power needed for <4 bad channels (Design Value)	10.8 mW		11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	
Power needed for 100 % Yield per unit	13.5 mW		NA		NA	
Median Noise at < 11 bad chs.	7.13 nV/rtHz	<15 nV/rtHz			SSSD, JFET-PER-01	
Median Noise at < 4 bad chs.	6.1 nV/rtHz	Min		<7 nV/rtHz	SSSD, JFET-PER-01	
Median Noise at 100 % Yield.	6.97 nV/rtHz	Performance		Design Value	SSSD, JFET-PER-01	
# of Channels over the max. offset voltage	0	< 15 mV for CQM < 15 mV for PFM/FS			SSSD, BDA-DRCU-27	
Common Mode Rejection Ratio	< -80 dB by design, as measured in EM4 unit				SSSD, BDA-DRCU-11	
Board Level Detail						
		Board SN 001			Source	
# Channels Tested	:	24				
Median Noise at 3.5 mW	:	18 nV/rtHz			SSSD, JFET-PER-01	
# of good channels at 3.5 mW	:	7	29% Yield		SSSD, JFET-PER-02	
Power Needed for 100 % Yield	:	6.75 mW			SSSD, JFET-PER-02	
Median Noise at High Power (w/ 100 % Yield)	:	6.97 nV/rtHz			SSSD, JFET-PER-01	
Median Gain at High Power	:	0.98			NA	
Definitions						
Good Channels	:	Noise less than a min. performance value of 15 nV/rtHz				
Yield	:	# of Good Channels / 24				
Filenames						
Noise Measurements	:	QualJFETPostVibeNoise_Summary.pdf				
Notes						
1) The Base temperature for all performance characterization was 4K						
2) All Noise Measurements were made with the inputs shorted to ground						

Attachment of HRCR Item # 24 & #25: Mate/Demate & Operation Logs

Hardware ID JFET S/N 12,15							
Date	Time	AIDS	Power	Mate	Demate	Transport	Notes
11/5/04		244299		X		X	103 → 183
11/5/04		"	X				.5 hr each board, warm S.V.
11/5/04		"					pump out
11/9/04		"					transfer LN2 (77K)
11/9/04		"					transfer helium (4K)
11/9/04		"	X				4 hours, board 34, noise data
11/10/04		"	X				8 hrs, " "
11/11/04		"	X				1 hr, " "
11/11/04		"	X				8 hrs, board 35, noise data
11/12/04		"	X				2 hrs, board 34, gain data, CMRR
11/12/04		"	X				3 hrs, board 35, gain, CMRR
11/12/04		"					begin warm-up
11/16/04		"		X	X		switch connector to fix prob. w/ S/N 12
11/16/04		"					pump out
11/17/04		"					go to LN2, helium
11/19/04		"	X				prob fixed (GSE)
11/19/04		"	X				6 hrs, board 22, noise data
11/22/04		"	X				2 hrs, board 22, noise data
11/22/04		"	X				6 hrs, board 23, noise data
11/23/04		"	X				2 hrs, " "
11/23/04		"	X				3 hrs, " gain, CMRR
11/23/04		"	X				3 hrs, board 22, gain, CMRR
11/30/04		"	X				.5 hrs each board, warm S.V.
12/1/04		"			X	X	183 → 103

Attachment of HRCR Items # 24 & # 25: Mate/Demate & Operation Logs (PWB S/N 035)

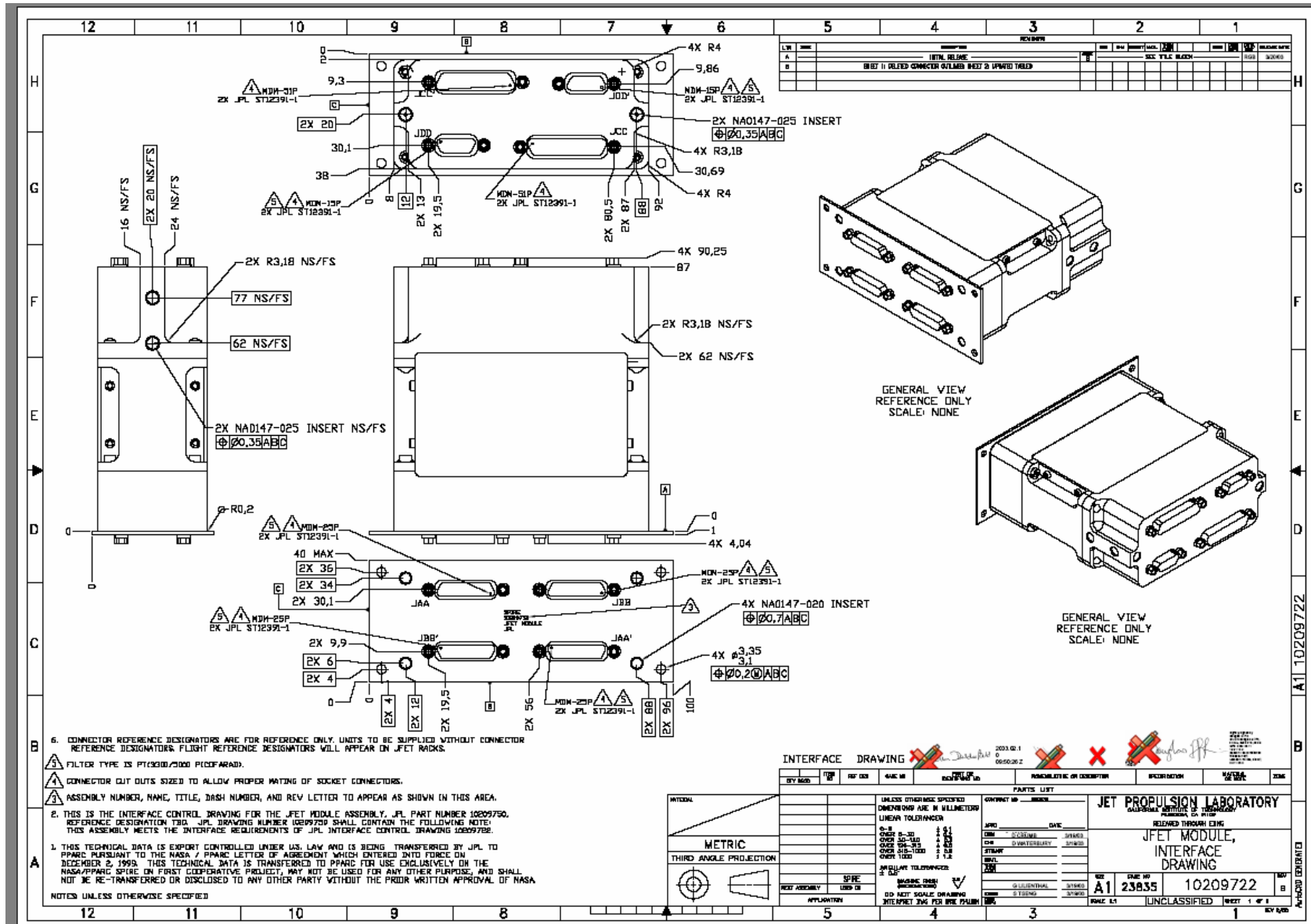
OPERATION LOG SHEET -- SPIRE JFET BOARDS MODULE

Mod. 15

DEVICE (BRD) S/N: 35 (49) PROJECT: SPIRE/JFET BOARD USE THE "NOTE" COLUMN TO DESCRIBE ACTIONS

DATE	TIME	TECH	PWR ON	PWR OFF	MATE				DEMATE				TRANSFERT	NOTE
					JAA	JBB	JCC	JDD	JAA	JBB	JCC	JDD		
7-15-04	7:00AM	103199			✓	✓	✓	✓						GND & CHASSIS - SAVER ON
7-19-04		103199												GND & CHASSIS ? "
8-16-04		103199												GND & CHASSIS TEST
8-16-04		103199												SOURCE - SAVER ON
8-19-04		103199												GND & CHASSIS "
8-19-04		103199	✓	✓										SOURCE TEST "
10-18-04		ST NW			✓	✓	✓	✓			✓	✓		GND & CHASSIS
10-18-04		ST NW	✓	✓			✓	✓	✓	✓				SOURCE TEST
10-21-04		ST NW			✓	✓	✓	✓			✓	✓		GND & CHASSIS
10-21-04		ST NW	✓	✓			✓	✓			✓	✓		SOURCE TEST
10-25-04		ST NW			✓	✓	✓	✓			✓	✓		GND & CHASSIS
							✓	✓	✓	✓				SOURCE TEST

Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 1 of 2)



Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 2 of 2)

	12	11	10	9	8	7	6	5	4	3	2	1				
H	JAA JFET OUTPUT 1B			JAB JFET OUTPUT 2A			JCC JFET INPUT 1			JDD JFET SERVICE 1			JCD' JFET INPUT 2			
	PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		
	1	SIGNAL M+		1	SIGNAL M+		1	BIAS V+		1	VSS		1	BIAS V+		
	2	SIGNAL N+		2	SIGNAL N+		2	BIAS V-		2	V+		2	BIAS V-		
	3	SIGNAL P+		3	SIGNAL P+		3	SIGNAL Y+		3	H+		3	SIGNAL Y+		
	4	SIGNAL R+		4	SIGNAL R+		4	SIGNAL W-		4	V-		4	SIGNAL W-		
	5	SIGNAL S+		5	SIGNAL S+		5	SIGNAL V+		5	V-		5	SIGNAL V+		
	6	SIGNAL T+		6	SIGNAL T+		6	SIGNAL T+		6	H+		6	SIGNAL T+		
	7	SIGNAL U-		7	SIGNAL U-		7	SIGNAL S-		7	V+		7	SIGNAL S-		
	8	SIGNAL V-		8	SIGNAL V-		8	SIGNAL P+		8	VSS		8	SIGNAL P+		
	9	SIGNAL W-		9	SIGNAL W-		9	SIGNAL N-		9	BIAS GND		9	SIGNAL N-		
	10	SIGNAL X-		10	SIGNAL X-		10	SIGNAL L-		10	Voh		10	SIGNAL L-		
	11	SIGNAL Y-		11	SIGNAL Y-		11	SIGNAL K+		11	H-		11	SIGNAL K+		
	12	SIGNAL Z-		12	SIGNAL Z-		12	SIGNAL I-		12	CHASSIS GND		12	SIGNAL I-		
	13	FPU GND		13	FPU GND		13	SIGNAL H+		13	H-		13	SIGNAL H+		
	14	SIGNAL M-		14	SIGNAL M-		14	SIGNAL F+		14	Voh		14	SIGNAL F+		
	15	SIGNAL N-		15	SIGNAL N-		15	SIGNAL E-		15	BIAS GND		15	SIGNAL E-		
	16	SIGNAL P-		16	SIGNAL P-		16	SIGNAL C+		JDD' JFET SERVICE 2				16	SIGNAL C+	
	17	SIGNAL R-		17	SIGNAL R-		17	SIGNAL B-		PIN #	PIN PURPOSE		17	SIGNAL B-		
	18	SIGNAL S-		18	SIGNAL S-		18	SIGNAL A-		1	VSS'		18	SIGNAL A-		
	19	SIGNAL T-		19	SIGNAL T-		19	BIAS GND		2	V+		19	BIAS GND'		
	20	SIGNAL U+		20	SIGNAL U+		20	SIGNAL Z+		3	H+		20	SIGNAL Z+		
	21	SIGNAL V+		21	SIGNAL V+		21	SIGNAL X-		4	V-		21	SIGNAL X-		
	22	SIGNAL W+		22	SIGNAL W+		22	SIGNAL W+		5	V-		22	SIGNAL W+		
	23	SIGNAL X+		23	SIGNAL X+		23	SIGNAL U-		6	H+		23	SIGNAL U-		
24	SIGNAL Y+		24	SIGNAL Y+		24	SIGNAL T-		7	V+		24	SIGNAL T-			
25	SIGNAL Z+		25	SIGNAL Z+		25	SIGNAL R+		8	VSS'		25	SIGNAL R+			
G	JBB JFET OUTPUT 1A			JBB' JFET OUTPUT 2B			JCC' JFET INPUT 2			JDD' JFET SERVICE 2			JCD' JFET INPUT 2			
	PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		
	1	SIGNAL A+		1	SIGNAL A+		26	SIGNAL P-		9	BIAS GND'		26	SIGNAL P-		
	2	SIGNAL B+		2	SIGNAL B+		27	SIGNAL M+		10	Voh'		27	SIGNAL M+		
	3	SIGNAL C+		3	SIGNAL C+		28	SIGNAL L+		11	H-		28	SIGNAL L+		
	4	SIGNAL D+		4	SIGNAL D+		29	SIGNAL J-		12	CHASSIS GND'		29	SIGNAL J+		
	5	SIGNAL E+		5	SIGNAL E+		30	SIGNAL I+		13	H-		30	SIGNAL I+		
	6	SIGNAL F+		6	SIGNAL F+		31	SIGNAL G-		14	Voh'		31	SIGNAL G-		
	7	SIGNAL G-		7	SIGNAL G-		32	SIGNAL F-		15	BIAS GND'		32	SIGNAL F-		
	8	SIGNAL H-		8	SIGNAL H-		33	SIGNAL D+		33	BIAS GND'		33	SIGNAL D+		
	9	SIGNAL I-		9	SIGNAL I-		34	SIGNAL C-		34	BIAS GND'		34	SIGNAL C-		
	10	SIGNAL J-		10	SIGNAL J-		35	SIGNAL A+		35	BIAS GND'		35	SIGNAL A+		
	11	SIGNAL K-		11	SIGNAL K-		36	SIGNAL Z-		36	BIAS GND'		36	SIGNAL Z-		
	12	SIGNAL L-		12	SIGNAL L-		37	SIGNAL Y-		37	BIAS GND'		37	SIGNAL Y-		
	13	FPU GND		13	FPU GND		38	SIGNAL X+		38	BIAS GND'		38	SIGNAL X+		
	14	SIGNAL A-		14	SIGNAL A-		39	SIGNAL V-		39	BIAS GND'		39	SIGNAL V-		
	15	SIGNAL B-		15	SIGNAL B-		40	SIGNAL U+		40	BIAS GND'		40	SIGNAL U+		
	16	SIGNAL C-		16	SIGNAL C-		41	SIGNAL S+		41	BIAS GND'		41	SIGNAL S+		
	17	SIGNAL D-		17	SIGNAL D-		42	SIGNAL R-		42	BIAS GND'		42	SIGNAL R-		
	18	SIGNAL E-		18	SIGNAL E-		43	SIGNAL N+		43	BIAS GND'		43	SIGNAL N+		
	19	SIGNAL F-		19	SIGNAL F-		44	SIGNAL M-		44	BIAS GND'		44	SIGNAL M-		
	20	SIGNAL G+		20	SIGNAL G+		45	SIGNAL K-		45	BIAS GND'		45	SIGNAL K-		
	21	SIGNAL H+		21	SIGNAL H+		46	SIGNAL J+		46	BIAS GND'		46	SIGNAL J+		
	22	SIGNAL I+		22	SIGNAL I+		47	SIGNAL H-		47	BIAS GND'		47	SIGNAL H-		
	23	SIGNAL J+		23	SIGNAL J+		48	SIGNAL G+		48	BIAS GND'		48	SIGNAL G+		
24	SIGNAL K+		24	SIGNAL K+		49	SIGNAL E+		49	BIAS GND'		49	SIGNAL E+			
25	SIGNAL L+		25	SIGNAL L+		50	SIGNAL D-		50	BIAS GND'		50	SIGNAL D-			
25	SIGNAL L+		25	SIGNAL L+		51	SIGNAL B+		51	BIAS GND'		51	SIGNAL B+			
F	JBB JFET OUTPUT 1A			JBB' JFET OUTPUT 2B			JCC' JFET INPUT 2			JDD' JFET SERVICE 2			JCD' JFET INPUT 2			
	PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		
	1	SIGNAL A+		1	SIGNAL A+		26	SIGNAL P-		9	BIAS GND'		26	SIGNAL P-		
	2	SIGNAL B+		2	SIGNAL B+		27	SIGNAL M+		10	Voh'		27	SIGNAL M+		
	3	SIGNAL C+		3	SIGNAL C+		28	SIGNAL L+		11	H-		28	SIGNAL L+		
	4	SIGNAL D+		4	SIGNAL D+		29	SIGNAL J-		12	CHASSIS GND'		29	SIGNAL J+		
	5	SIGNAL E+		5	SIGNAL E+		30	SIGNAL I+		13	H-		30	SIGNAL I+		
	6	SIGNAL F+		6	SIGNAL F+		31	SIGNAL G-		14	Voh'		31	SIGNAL G-		
	7	SIGNAL G-		7	SIGNAL G-		32	SIGNAL F-		15	BIAS GND'		32	SIGNAL F-		
	8	SIGNAL H-		8	SIGNAL H-		33	SIGNAL D+		33	BIAS GND'		33	SIGNAL D+		
	9	SIGNAL I-		9	SIGNAL I-		34	SIGNAL C-		34	BIAS GND'		34	SIGNAL C-		
	10	SIGNAL J-		10	SIGNAL J-		35	SIGNAL A+		35	BIAS GND'		35	SIGNAL A+		
	11	SIGNAL K-		11	SIGNAL K-		36	SIGNAL Z-		36	BIAS GND'		36	SIGNAL Z-		
	12	SIGNAL L-		12	SIGNAL L-		37	SIGNAL Y-		37	BIAS GND'		37	SIGNAL Y-		
	13	FPU GND		13	FPU GND		38	SIGNAL X+		38	BIAS GND'		38	SIGNAL X+		
	14	SIGNAL A-		14	SIGNAL A-		39	SIGNAL V-		39	BIAS GND'		39	SIGNAL V-		
	15	SIGNAL B-		15	SIGNAL B-		40	SIGNAL U+		40	BIAS GND'		40	SIGNAL U+		
	16	SIGNAL C-		16	SIGNAL C-		41	SIGNAL S+		41	BIAS GND'		41	SIGNAL S+		
	17	SIGNAL D-		17	SIGNAL D-		42	SIGNAL R-		42	BIAS GND'		42	SIGNAL R-		
	18	SIGNAL E-		18	SIGNAL E-		43	SIGNAL N+		43	BIAS GND'		43	SIGNAL N+		
	19	SIGNAL F-		19	SIGNAL F-		44	SIGNAL M-		44	BIAS GND'		44	SIGNAL M-		
	20	SIGNAL G+		20	SIGNAL G+		45	SIGNAL K-		45	BIAS GND'		45	SIGNAL K-		
	21	SIGNAL H+		21	SIGNAL H+		46	SIGNAL J+		46	BIAS GND'		46	SIGNAL J+		
	22	SIGNAL I+		22	SIGNAL I+		47	SIGNAL H-		47	BIAS GND'		47	SIGNAL H-		
	23	SIGNAL J+		23	SIGNAL J+		48	SIGNAL G+		48	BIAS GND'		48	SIGNAL G+		
24	SIGNAL K+		24	SIGNAL K+		49	SIGNAL E+		49	BIAS GND'		49	SIGNAL E+			
25	SIGNAL L+		25	SIGNAL L+		50	SIGNAL D-		50	BIAS GND'		50	SIGNAL D-			
25	SIGNAL L+		25	SIGNAL L+		51	SIGNAL B+		51	BIAS GND'		51	SIGNAL B+			
E	JBB JFET OUTPUT 1A			JBB' JFET OUTPUT 2B			JCC' JFET INPUT 2			JDD' JFET SERVICE 2			JCD' JFET INPUT 2			
	PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		
	1	SIGNAL A+		1	SIGNAL A+		26	SIGNAL P-		9	BIAS GND'		26	SIGNAL P-		
	2	SIGNAL B+		2	SIGNAL B+		27	SIGNAL M+		10	Voh'		27	SIGNAL M+		
	3	SIGNAL C+		3	SIGNAL C+		28	SIGNAL L+		11	H-		28	SIGNAL L+		
	4	SIGNAL D+		4	SIGNAL D+		29	SIGNAL J-		12	CHASSIS GND'		29	SIGNAL J+		
	5	SIGNAL E+		5	SIGNAL E+		30	SIGNAL I+		13	H-		30	SIGNAL I+		
	6	SIGNAL F+		6	SIGNAL F+		31	SIGNAL G-		14	Voh'		31	SIGNAL G-		
	7	SIGNAL G-		7	SIGNAL G-		32	SIGNAL F-		15	BIAS GND'		32	SIGNAL F-		
	8	SIGNAL H-		8	SIGNAL H-		33	SIGNAL D+		33	BIAS GND'		33	SIGNAL D+		
	9	SIGNAL I-		9	SIGNAL I-		34	SIGNAL C-		34	BIAS GND'		34	SIGNAL C-		
	10	SIGNAL J-		10	SIGNAL J-		35	SIGNAL A+		35	BIAS GND'		35	SIGNAL A+		
	11	SIGNAL K-		11	SIGNAL K-		36	SIGNAL Z-		36	BIAS GND'		36	SIGNAL Z-		
	12	SIGNAL L-		12	SIGNAL L-		37	SIGNAL Y-		37	BIAS GND'		37	SIGNAL Y-		
	13	FPU GND		13	FPU GND		38	SIGNAL X+		38	BIAS GND'		38	SIGNAL X+		
	14	SIGNAL A-		14	SIGNAL A-		39	SIGNAL V-		39	BIAS GND'		39	SIGNAL V-		
	15	SIGNAL B-		15	SIGNAL B-		40	SIGNAL U+		40	BIAS GND'		40	SIGNAL U+		
	16	SIGNAL C-		16	SIGNAL C-		41	SIGNAL S+		41	BIAS GND'		41	SIGNAL S+		
	17	SIGNAL D-		17	SIGNAL D-		42	SIGNAL R-		42	BIAS GND'		42	SIGNAL R-		
	18	SIGNAL E-		18	SIGNAL E-		43	SIGNAL N+		43	BIAS GND'		43	SIGNAL N+		
	19	SIGNAL F-		19	SIGNAL F-		44	SIGNAL M-		44	BIAS GND'		44	SIGNAL M-		
	20	SIGNAL G+		20	SIGNAL G+		45	SIGNAL K-		45	BIAS GND'		45	SIGNAL K-		
	21	SIGNAL H+		21	SIGNAL H+		46	SIGNAL J+		46	BIAS GND'		46	SIGNAL J+		
	22	SIGNAL I+		22	SIGNAL I+		47	SIGNAL H-		47	BIAS GND'		47	SIGNAL H-		
	23	SIGNAL J+		23	SIGNAL J+		48	SIGNAL G+		48	BIAS GND'		48	SIGNAL G+		
24	SIGNAL K+		24	SIGNAL K+		49	SIGNAL E+		49	BIAS GND'		49	SIGNAL E+			
25	SIGNAL L+		25	SIGNAL L+		50	SIGNAL D-		50	BIAS GND'		50	SIGNAL D-			
25	SIGNAL L+		25	SIGNAL L+		51	SIGNAL B+		51	BIAS GND'		51	SIGNAL B+			
D	JBB JFET OUTPUT 1A			JBB' JFET OUTPUT 2B			JCC' JFET INPUT 2			JDD' JFET SERVICE 2			JCD' JFET INPUT 2			
	PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		
	1	SIGNAL A+		1	SIGNAL A+		26	SIGNAL P-		9	BIAS GND'		26	SIGNAL P-		
	2															

Attachment of HRCR Item # 11:

SPIRE

Handling Document

Field Effect Transistor (JFET) Module

10209750-1

Prepared by: Kalyani Sukhatme

10 September, 2003

Hardware Handling Guidelines

Contamination: Open shipment suitcase in a FED-STD-209 Class 10,000 clean room (ISO 14644-1 class 7) or better. Handle hardware with gloves.

ESD: Handle with grounding straps, ESD-safe gloves and ESD smocks at an ESD-safe workstation. Maintain shorting plugs on the unit whenever ESD is a concern. Refer to attached electrical handling document for other important safety precautions.

Fragile: Do not drop or otherwise shock the hardware including the shipping suitcase and container.

Humidity Sensitive: Place hardware in a humidity controlled Class 10,000 clean room. Maintain humidity level at 35%-50% RH typical, for ESD safety.

SPIRE JFET Electrical Handling Document

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1. Introduction

This document provides guidelines for electrical handling for the SPIRE JFET Module.

1.1 Hardware Description

Each JFET module has two sets of 24 JFET channels. The JFET channels are populated on 1.0 micron thick Silicon Nitride membranes which provides thermal isolation. The operating temperature for these JFETs is ~120 K. The process of powering up the JFETs dissipates heat into the membrane resulting in a temperature increase with respect to the base temperature (4K to 10 K). Higher the power dissipation, higher is the temperature of the JFETs.

Each JFET channel consists of a matched pair of FETs (Figure 1.1-1) with a requirement for the offset voltage of less than **15 mV** between the matched pair. [The characteristic offset voltage is the difference between the source voltages (V_{sa} and V_{sb} with respect to ground) of the two FETs.]

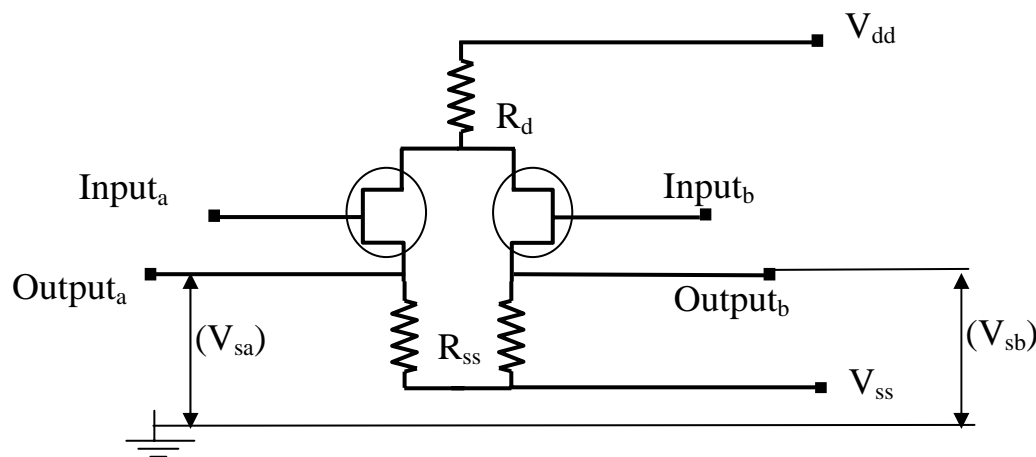


Figure 1.1-1

The Gates of the JFETs are the ‘Inputs’ of the circuit and the Sources (V_{sa} and V_{sb}) of the JFETs are the outputs, as marked in Figure 1.1-1. V_{dd} and V_{ss} are the power lines for the circuit.

Handling

1. **The JFET Module is Contamination Sensitive:** Handle the unit with Gloves only in a FED-STD-209 Class 100000 clean room (ISO 14644-1 class 7) or better.
2. **The JFET Module is ESD Sensitive:** Please handle with appropriate ESD hardware handling procedures. Handle with grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.
3. **The JFET Module is Fragile:** Please do not drop or otherwise shock the unit. Please DO NOT remove the cover of the JFET Module.

Power ON Procedure

1. The JFET Module should be powered on **WITH the shorting plugs** (JPL Supplied Protection connectors) in place and with the **inputs shorted to ground**. Pins #9 and #15 on the 15-pin MDM connectors on the JFET Module are the bias grounds on the module. These pins should also be shorted to the power supply ground. The unit may be powered up without the shorting plug only when the inputs are connected to the detector system.

Under no circumstances the unit should be powered up without the inputs shorted to ground either via the shorting plug (JPL Supplied) or via the detector system.

2. Do not exceed a voltage of +5 V for the Vdd line and -5 V for the Vss line of the JFET Module.
3. When removing the shorting plugs from the unit for installation into the instrument, please use standard ESD precautions including grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.

Electrical Check-out Test: Characteristic Offset Voltage Measurement

- 1) Verify that the gates of the JFET channels (Inputs) are shorted together and grounded.
- 2) Apply the power supply ground to the bias ground pins on the unit (Pins 9 and 15 on the 15-pin MDM connectors)
- 3) Power on the JFET modules with Vdd = +3 V and Vss = -1.5 V
- 4) Verify that the handheld multimeter is in calibration.
- 5) Connect one side of the handheld multimeter to ground (Power supply ground).
- 6) And measure the voltage with respect to ground of each side (V_{sa} and V_{sb}) of each channel.
- 7) Calculate the characteristic offset voltage (V_{offset}) for each channel (V_{offset}= V_{sa}-V_{sb})
- 8) Compare the values for each of the channels with the specific datasheet provided with the unit.
The datasheets accompanying the unit also provides the values for the drain and source currents for a similar test performed at JPL.

REFER TO MEASURED SOURCE VOLTAGE DATA FOR ACTUAL HARDWARE. Here is an example of the source voltage values and the drain and the source currents obtained for such a test at room temperature are given in the Table 4-1

T, JFET	rm T	
Vdd	3 V	
Vss	-1.5 V	
Idd	1.564 mA	
Iss	1.5686 mA	
Channel #	(V)	DELTA (V)
1	1.130	0
	1.130	
2	1.075	0.001
	1.074	
3	0.781	0.001
	0.780	
4	1.088	0.005
	1.093	
5	0.834	0.001
	0.833	
6	1.012	0.003
	1.015	
7	0.785	0.002
	0.787	
8	1.148	0.004
	1.144	
9	0.753	0
	0.753	

10	0.693	0.008
	0.701	
11	1.110	0.004
	1.114	
12	0.758	0.001
	0.759	
13	0.832	0.002
	0.830	
14	1.264	0.001
	1.265	
15	1.206	0
	1.206	
16	0.818	0.001
	0.819	
17	0.526	0.005
	0.521	
18	1.423	0
	1.423	
19	0.773	0.002
	0.775	
20	0.873	0.004
	0.877	
21	1.387	0.006
	1.393	
22	1.417	0.003
	1.420	
23	0.887	0.002
	0.889	
24	0.888	0.003
	0.891	

- END OF -
Attachment of HRCR Item # 11:
JFET Module Handling Document

END OF
HRCR PACKAGE