JPL Hardware Requirements Certification Review – SPIRE Element No. D-30475

Assembly / Subsystem		PEM		Phone		Section		Date
SPIRE		Martin Herman		(818) 354-8541		386		3 February, 2005
Drawing/ Part No.	Dwg. Rev.	Nomenclature		Serial No.	Model	Type	Final IR No.	Mass (Meas. / Req.)
10209750-1	B	JFET Module		014	FLIGHT	N/A	923847	280.6 gm / 305 gm

Check applicable answer and provide explanation in remarks column	YES	NO	NA	Remarks	Data Attachments	Signature & Date
1. Are all drawings and specifications complete, approved, released and frozen?	X				14. Latest Top Assembly drawings ☒ Attached ☐ None	Cognizant Engineer 2/18/05
2. Do the released drawings and specifications reflect all approved changes?	X				15. List of open ECRs ☐ Attached ☒ None	PEM 2/18/05
3. Is hardware identical to other hardware delivered? If no, provide difference list.	X				16. Waivers (RFW request for waiver) ☒ Attached ☐ None	QA Engineer 2/18/05
4. Does the hardware meet its functional requirements, specifications, waivers, ICDs?	X			EIDP attached. Also see item # 8 attachments.	17. Open MRB ☐ Attached ☒ None	Environments/Reliability 2/18/05
5. Are all IR and MRB dispositioned and concurred by QA?	X				18. Open PFR on this H/W ☐ Attached ☒ None	Mission Assurance Mgr. 2/18/05
6. Is complete as-built list information included in the build book?	X				19. Open PFR on similar H/W ☐ Attached ☒ None	Project Office 2/18/05
7. Have all required environmental tests & analyses been completed?	X			ETAS attached	20. Handling Document → See Item 11 ☒ Attached ☐ None	PI 2/18/05
8. Is all required assembly and/or subsystem level functional testing complete?	X			Performance Test Data Attached. Also see EIDP in item # 4.	21. Shortage List ☐ Attached ☒ None	
9. Have all piece parts, processes and materials been approved by JPL?	X				22. Requirements Verification Matrix ☒ Attached (See #4, #7, #8) ☐ None	
10. Does this hardware meet all contamination control requirements?	X			Parts, processes and MIUL met all contamination control and out-gassing requirements.	23. Qualification Status ☒ Attached ☐ None	
11. Are all shipping containers, shipping and special handling procedures ready?	X			See Attached Document D-26790	24. Mate / Demate Record ☒ Attached ☐ None	
12. Is additional work required to bring this hardware to flight readiness?		X			25. Operating Log ☒ Attached (See Item # 24) ☐ None	
13. Is this hardware acceptable for flight?	X				26. MICD ☒ Attached ☐ None	

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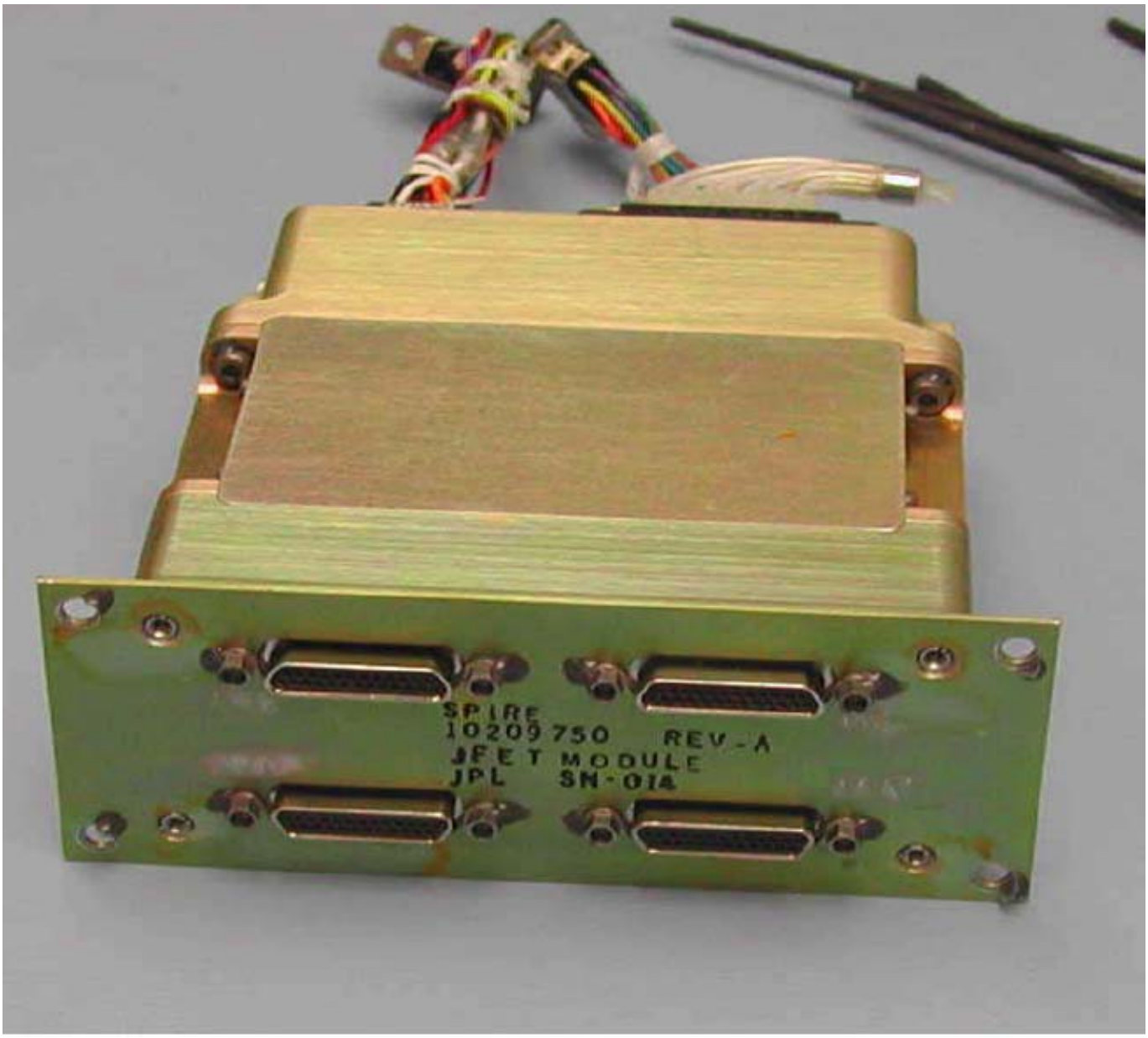

SPIRE JFET Module S/N 014

RAL EIDP Table of Contents Versus JPL HRCR Check List Item Numbers

RAL EIDP Section Number	RAL EIDP Title	JPL HRCR Check List Item Number	Notes
1	Shipping Documents		Shipper and Final IR
2	Transportation, Packing, Handling & Integration Procedures	11	Special Handling Document D-26790
3	Certificate of Conformance / Delivery Review Board MOM		HRCR book is the C of C
4	As Built Configuration Status List	1 & 2	Assembly Drawings
5	List of Waivers	4	RFW (request for waiver) Attached
6	Copies of Waivers	4 & 7	RFW (request for waiver) Attached
7	List of Non-Conformance Reports		See RFW in 4 & 7
8	Copies of Non-Conformance Reports		See RFW in 4 & 7
9	Cleanliness Statement		Final IR QA Inspection
10	Operational Manual		NA
11	Top Level Drawings (inc. Family Tree)	14	Top Assembly Drawing
12	Interface Drawings	26	MICD Drawing
13	Functional, Block & Mechanical Drawings		NA
14	Electrical Circuit Drawings		NA
15	Serialized Components List		In build books – not shipped
16	Mass Properties/ Power Budget	HRCR Check List Page 1	Mass listed in HRCR check list
17	Qualification Status List / Test Matrix	23	Qualification Unit Test Matrix
18	Test Reports	4, 7, 8, 23	
19	Open Work / Deferred Work / Open Tests		NA
20	Calibration Data		NA
21	Historical Record	23	Qualification Unit Test Matrix
22	Manufacturing Logbook(s)		In build books – not shipped
23	Operating Time / Cycle Record	25	
24	Connector Mating Record	24	
25	Age Sensitive Items Record		NA
26	Pressure Vessels – History/Test Record		NA
27	Temporary Installation Record		NA
28	Reference List of EIDPs (Lower level)		NA
29	Other Useful Information		NA

JPL Hardware Requirements Certification Review (HRCR)

Junction Field Effect Transistor (JFET) Flight Module

10209750-1 S/N 014

SPIRE Element
Herschel Space Observatory Project

February 3, 2005

Configuration of Module, Boards & Membranes

Module 10209750-1	S/N 14	S/N 14
PWB 10209760-1	S/N 36	S/N 37
Membrane 10209758-1	J6.15.2	J6.15.1

Attachment of HRCR Items #1
Drawing Release Status

ALL ASSEMBLY & PARTS DRAWINGS ARE RELEASED IN PDMS

Released Drawings:

10209719-1 assembly built per released Rev. A drawing (studlock)

10209722-1 assembly built per released Rev. B drawing (interface drawing)

10209750-1 assembly built per released Rev. B drawing (module assy)

10209751-1 assembly built per released Rev. B drawing (chassis 1)

10209752-1 assembly built per released Rev. A drawing (chassis 2)

10209753-1 assembly built per released Rev. A drawing (chassis 3)

10209754-1 assembly built per released Rev. C drawing (mount)

10209756-1 assembly built per released Rev. B drawing (chassis lid)

10209757-1 assembly built per released Rev. A drawing (membrane)

10209758-1 assembly built per released Rev. A drawing (membrane assy)

10209759-1,-2,-4 redlined Rev. B drawing (gasket)

10209760-1 assembly built per released Rev. C drawing (board assembly)

10209761-1 assembly built per released Rev. C drawing (solder connector)

10209769-1 assembly built per released Rev. A drawing (stiffener)

10209777-1 assembly built per released Rev. B drawing (board)

10209858-2 assembly built per released Rev. A drawing (special fastener)

10217636-1 assembly built per released Rev. A drawing (clip)

Attachment of HRCR Item #4: EIDP

EIDP Coverpage For JFET Testing

Unit Identfication		
Name	:	JFET PFM Module
Part #	:	10209750-1
S/N	:	#014

Environmemtal Testing

	Axes Tested	Temp	Duration/# of Cycle	Requirement	Source	Waiver
Random Vibration Test	X, Y, Z	Rm T	1 min/axis	X, Y, Z	SSSD, JFET-DES-07	
High Level Sine Vibe Test	None	NA	NA	X, Y, Z	SSSD, JFET-DES-07	HR-SP-JPL-RFW-005
Bakeout	NA	80 C	25 hrs	> 24 HRS		
Thermal Cycles	NA	RmT to 80 K	2	Minimum 1	D-20549	

Performance Characteristics

		Specification		Source	Waiver
Power needed for <11 bad channels (Min Perf.)	6.9 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	HR-SP-JPL-RFW-004
Power needed for <4 bad channels (Design Value)	7.35 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	
Power needed for 100 % Yield per unit	9.14 mW	NA		NA	
Median Noise at < 11 bad chs.	11.63 nV/rtHz	<15 nV/rtHz Min Performance	<7 nV/rtHz Design Value	SSSD, JFET-PER-01	
Median Noise at < 4 bad chs.	10.24 nV/rtHz			SSSD, JFET-PER-01	
Median Noise at 100 % Yield.	9.23 nV/rtHz			SSSD, JFET-PER-01	
# of Channels over the max. offset voltage	0	< 15 mV		SSSD, BDA-DRCU-27	
Common Mode Rejection Ratio	< -60 dB by design, as measured in EM4 unit			SSSD, BDA-DRCU-11	

Board Level Details

		Board SN 036 (JAA-JDD)		Board SN 037 (JAA'-JDD')		Source
# Channels Tested	:	36		37		
Median Noise at 3.5 mW	:	9.24 nV/rtHz		12.37 nV/rtHz		SSSD, JFET-PER-01
# of good channels at 3.5 mW	:	22	92% Yield	18	75 % Yield	SSSD, JFET-PER-02
Power Needed for 100 % Yield	:	4.01 mW		5.14 mW		SSSD, JFET-PER-02
Median Noise at High Power (w/ 100 % Yield)		9.20 nV/rtHz		9.45 nV/rtHz		SSSD, JFET-PER-01
Median Gain at High Power		0.98		0.97		NA
Heater Resistance, 4K Reference value	:	2.51 kΩ		2.53 kΩ		NA

Definitions		
Good Channels	:	Noise less than a min. performance value of 15 nV/rtHz
Yield	:	# of Good Channels / 24
Filenames		
Noise Measurements	:	JFET_Mod14_Noise_data.pdf
Source Voltages (RmT, 4K)	:	JFET_Mod14_Source_Voltage_Data.pdf

Notes

1) The Base temperature for all performance characterization was 4K

2) All Noise Measurements were made with the inputs shorted to ground

3) Type of membranes: SN036: 36% Overetched Perforated; SN037: 30% Overetched Perforated

Attachment of HRCR Item # 4: RFW (request for waiver)

RFW/RFD Number:	HR-SP-JPL-RFW-015

Spacecraft / Project	Herschel	**Originator's Name**	Steve Tseng	
System / Experiment / Model	**1.1 SPIRE**	**Signature / Date**		
Sub-System	detectors	**Request Type** **(Highlight applicable request)**	Waiver (RFW)	Deviation (RFD)
Assembly	JFET modules	1.1.1.1 Organisation	Jet Propulsion Laboratory	
Sub-Assembly		**Ref. Doc. / Drwg No.**	SPIRE-JPL-PRJ-000456	
Item		**References**		
Serial No.				
RFW/RFD Title	**JFET Power Dissipation s/n 014**			

End Items(s) Affected (Hardware, Software)		
Name	**CI-Number**	**Model(s)**
JFET Module p/n 10209750 s/n 014		PFM

Requirement / Interface Documents Affected				
Specification/Drawing Title	**Number**	**Issue**	**Date**	**App. Paragraph**
BDA-SSSD	SPIRE-JPL-PRJ-0004456	3.2	7/1/03	JFET-PER-01 JFET-PER-02 JFET-TEC-05

Description of Deviation / Discrepancy / Non-Conformance

Requirement states that dissipation of photometer JFETs is to be less than 6.90 mW average, while supplying 90% of channels with voltage noise < 15 nV/rtHz according to BDA-SSSD JFET-PER-01, JFET-PER-02, JFET-TEC-05. Measured JFET performance of the JFETs indicates that 9.14 mW of power dissipation will be required to meet the specified yield and noise performance specifications.

Other Items or Requirements (Potentially) Affected

Overall sensitivity of the bolometer sub-system is affected by JFET noise performance. JFET power dissipation impacts the heat sink temperature of the 3He refrigerator and may in turn increase the base detector temperature. Dissipation of JFETs affects power dissipation on cryostat.

Need for RFW/RFD and Rationale for Acceptance

Measured JFET performance of JFETs indicates that 6.90 mW of power dissipation will be required to meet the specified yield and noise performance specifications. JPL is unable to significantly alter the JFET fabrication process in order to meet the power specification without undue risk to the stated PFM/FS delivery dates. Furthermore, JPL requests a full system optimisation to revisit the noise and power requirements on the JFETs. The JFET modules can meet the noise design value with 100 % yield at 9.14 mW.

	Approved	**Rejected**	**Name**	**Date**
Engineering:				
Product Assurance:				
CCB-Chairman:				
Principal Investigator				
Product Assurance:				
Co-Investigator				
Prime Contractor				
ESA Project Office				

Attachment of HRCR Item #7: RFW (request for waiver)

RFW/RFD Number:	HR-SP-JPL-RFW-005

Spacecraft / Project	Herschel	**Originator's Name**	Kalyani Sukhatme	
System / Experiment / Model	**SPIRE**	**Signature / Date**		
Sub-System	detectors	**Request Type** **(Highlight applicable request)**	Waiver (RFW)	Deviation (RFD)
Assembly		Organisation	Jet Propulsion Laboratory	
Sub-Assembly		**Ref. Doc. / Drwg No.**	SPIRE-JPL-PRJ-000456	
Item		**References**		
Serial No.				
RFW/RFD Title	**BDA and JFET module sine test deletion**			

End Items(s) Affected (Hardware, Software)		
Name	**CI-Number**	**Model(s)**
Bolometric Detector Assemblies JFET Modules		CQM, PFM, FS CQM, PFM, FS

Requirement / Interface Documents Affected				
Specification/Drawing Title	**Number**	**Issue**	**Date**	**App. Paragraph**
BDA-SSSD (SPIRE-JPL-PRJ-000456)		3.2	Jan 7, 2003	BDA-DES-10, JFET-DES-07

Description of Deviation / Discrepancy / Non-Conformance

High Level Sine- Vibe Test is not performed on these units

Other Items or Requirements (Potentially) Affected

Need for RFW/RFD and Rationale for Acceptance

The hardware has to be qualified under a cold vibration test and is installed in the cold vibration facility for the purpose of the test. The high level sine vibration test configuration will put the hardware and the personnel at risk since the cold vibration facility is not structurally capable of withstanding the high levels. Obtaining additional resources (cost and schedule) for developing a new set-up is not feasible at this time.

	Approved	**Rejected**	**Name**	**Date**
JPL Engineering:				
JPL Product Assurance:				
CCB-Chairman:				
Principal Investigator				
Product Assurance:				
Co-Investigator				
Prime Contractor				
ESA Project Office				

Attachment of HRCR Item #7: ETAS (environmental test summary)

ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)

AUTHORIZATION SECTION

PROJECT: Herschel		LOG NO.: HS035	
SYSTEM/ASSEMBLY TITLE: 4E JFET Modules S/N 13,14			DATE ISSUED: 12/03/04
REFERENCE DESIGNATION NUMBER	PART NO. (IF MULTIPLE, ATTACH LIST): 10209750-1	REV.	SERIAL NO.: 013,014

HARDWARE TYPE: ☐ EM QUAL ☒ FLIGHT ☐ FLIGHT SPARE ☐ OTHER — PRE-ENVIRONMENTAL INSPECTION REPORT NUMBER (ATTACH IR)

WIRING HARNESS: ☐ EM QUAL ☐ FLIGHT ☐ EM ☐ SE — PART NO. — REV. — SERIAL NO.

TEST DESCRIPTION (CHECK ALL APPLICABLE): ☐ SINE VIBRATION ☐ PYROSHOCK ☐ ACOUSTIC ☐ EMC ☐ OTHER ____ ☒ RANDOM VIBRATION ☒ THERMAL VAC. ☐ THERMAL ATMOSPHERE

TYPE OF TEST: ☐ QUALIFICATION ☐ FLIGHT ACCEPTANCE ☒ PROTO FLIGHT ☒ RETEST

WILL ALL TESTS/LEVES/DURATIONS REQUIRED BY THE PROJECT DOCUMENTS BE PERFORMED ON THIS UNIT?
☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) — ENTER PROJ. DOC. NO. AND REV. ____

HAS THE UNIT PASSED ALL PRE-ENVIRONMENTAL FUNCTIONAL TESTS?
☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) — BRIEF EXPLANATION

HAVE ALL DESIGN ANALYSES BEEN COMPLETED AND REQUIRED CHANGES BEEN IMPLEMENTED?
☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) — BRIEF EXPLANATION

IS THE TEST ARTICLE IDENTICAL TO OTHER FLIGHT UNITS?
☐ YES ☒ NO (IF NO, ATTACH EXCEPTIONS LIST) — BRIEF EXPLANATION Stiffeners have been added to the design and includedon this unit

ARE ALL PFRs AGAINST THIS UNIT CLOSED?
☐ YES ☒ NO (IF NO, ATTACH EXCEPTIONS LIST) — BRIEF EXPLANATION PFR's in process of closure. All issues have been addressed and qualified except for ongoing diagnosis of last two units (12,13)

HAVE ALL WAIVERS AND ECRs BEEN APPROVED AND ARE THEY INCORPORATED?
☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) — BRIEF EXPLANATION

TEST AUTHORIZED BY

COGNIZANT ENGINEER	DATE	TECHNICAL MGR./INSTR MRG./PI PREP REP	DATE	ENVIRONMENTAL REQUIREMENTS ENG.	DATE
[signature]	12/3/04	[signature]	12/3/04	[signature]	12-3-04

SUMMARY SECTION

TEST AGENCY (IF MULTIPLE, ATTACH SUMMARY AND TEST DATES)	TEST INITIATION DATE	ACCUMULATED OPERATING HOURS PRIOR TO FIRST ENVIRONMENTAL TEST
JPL Building 144	12/07/04	
SERIAL NUMBERS ACTUALLY TESTED	TEST TERMINATION DATE	OPERATING HOURS DURING ENVIRONMENTAL EXPOSURE

TEST DESCRIPTION

VIBRATION	ACOUSTIC	PYROSHOCK SHOCK	THERMAL VACUUM	TEMPERATURE ATMOSPHERE	OTHER
AXES: X Y Z SINE VIBRATION ☐☐☐ RANDOM VIBRATION ☒☒☒	☐	AXES: X Y Z ☐☐☐ SHOCKS/AXIS:	☒ PRESSURE: <10E-5 <77K NO OF CYCLES: ~~2~~ 1 cycle	NO OF CYCLES:	☐ ____

EMC ☐ COND. SUSC. ☐ COND. EMIS. ☐ ISOLATION
ESD ☐ RAD. SUSC. ☐ RAD. EMIS. ☐ MAGNETICS

TEMP. LEVEL (°c) AND ACCUMULATED DURATION (HRS.)
HOT: ____°c, ____h COLD: ____°c, ____h
HOT: ____°c, ____h COLD: ____°c, ____h

WERE THERE ANY PFRs GENERATED DURING ENVIRONMENTAL TESTS?
☐ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) — LIST PFR NOS. / BRIEF EXPLANATION

ARE THE POST ENVIRONMENTAL DAMAGE INSPECTIONS COMPLETE?
☐ YES ☐ NO (IF YES, ATTACH A COPY OF THE INSPECTION REPORTS. IF NO, ATTACH EXPLANATION) — LIST PFR NOS. / BRIEF EXPLANATION

WERE ALL PLANNED TESTS/LEVELS/DURATIONS ACHIEVED?
☐ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) — LIST PFR NOS. / BRIEF EXPLANATION

☐ TESTS HAVE NOT BEEN SUCCESSFULLY COMPLETED. SEE THE ATTACHED SUMMARY FOR ACTIONS THAT INEED TO BE TAKEN.

COGNIZANT ENGINEER	DATE	TECHNICAL MGR./INSTR MRG./PI PREP REP	DATE	ENVIRONMENTAL REQUIREMENTS ENG.	DATE

☐ HARDWARE HAS SUCCESSFULLY COMPLETED THE ENVIRONMENTAL TESTS LISTED ON THIS FORM OR REMAINING ACTIONS HAVE BEEN TAKEN, INCLUDING RETEST.

COGNIZANT ENGINEER	DATE	TECHNICAL MGR./INSTR MRG./PI PREP REP	DATE	ENVIRONMENTAL REQUIREMENTS ENG.	DATE
[signature]	2/7/05	[signature]	2/7/05	[signature]	2-7-05

Attachment of HRCR Item #7: ETAS (environmental test summary)

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ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)

OTHER AUTHORIZATION PROVISIONS AND EXPLANATIONS

This is a 3-axis warm vibration test (room temp) done on the JFET flight modules SN~~012~~ 014 and 013. The test will be done with the JFET unit mounted inside a mock-up JFET rack. The unit will be assessed both before and after the test with visual inspections and electrical checkouts. 3 response accelerometers will be mounted onto the JFET rack in order to give response data.

2 to 3 vacuum thermal cycles will also be completed.

S/N 14 passed vib and thermal

S/N 013 failed (Z-85374)-problem found during thermal cycle. Rework to be done & retested (ETAS 115036)

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Attachment of HRCR Item #7: ETAS (environmental test summary)

ENVIRONMENTAL TES JTHORIZATION AND SUMMARY (ETAS)
ENVIRONMENTAL TEST SUMMARY

HARDWARE	S/N	ETAS	TEST ENVIRONMENT LEVELS & DURATION	DATE TEST PERFORMED	TEST AGENCY	PASS/ FAIL	COMMENTS
SPIRE JFET (10209750-1)	013,014	HSO35	**X, Y, and Z** 1 minute Random Vibe Frequency [Hz] / Spec [g^2.Hz] 20 / 0.01 100 / 0.05 300 / 0.05 499 / 0.0214 500 / 0.0214 2000 / 0.00214 Each axis 1/4 g sine sweep 20-2000 Hz each axis 1 ~~2-3~~ vacuum thermal cycles, <10E-5 mbar, <70K				

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Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise
For Module 14

JFET SOURCE VOLTAGE MEASUREMENT

Date			12/8/2004		12/8/2004	
T, plate			4K		4K	
			4K		4K	
Vdd			3		3	
Vss			-1.5		-1.5	
Vdd'			2.676		2.68	
Vss'			-1.173		-1.176	
Idd			1.2443		1.2287	
Iss			1.2433		1.2301	
SN			36		37	
Channel #				DELTA		DELTA
1	a		0.713	0	0.755	0.003
	b		0.713		0.752	
2	a		0.743	0.004	0.747	0.006
	b		0.747		0.741	
3	a		0.718	0.003	0.760	0.002
	b		0.715		0.762	
4	a		0.713	0.003	0.721	0.001
	b		0.716		0.722	
5	a		0.715	0	0.740	0.004
	b		0.715		0.744	
6	a		0.710	0.001	0.712	0.007
	b		0.709		0.719	
7	a		0.738	0	0.769	0.004
	b		0.738		0.773	
8	a		0.696	0.002	0.695	0.005
	b		0.698		0.700	
9	a		0.690	0.003	0.734	0.005
	b		0.693		0.739	
10	a		0.798	0.003	0.786	0.007
	b		0.795		0.793	
11	a		0.797	0.001	0.745	0.007
	b		0.798		0.738	
12	a		1.129	0.011	0.738	0.001
	b		1.140		0.737	
13	a		0.786	0.01	0.731	0.004
	b		0.796		0.735	
14	a		0.743	0.005	0.754	0
	b		0.748		0.754	
15	a		0.748	0	0.658	0.003
	b		0.748		0.661	
16	a		0.795	0.004	0.634	0.003
	b		0.799		0.637	
17	a		0.722	0.006	0.758	0.009
	b		0.716		0.749	
18	a		0.754	0	0.592	0.002
	b		0.754		0.594	
19	a		0.714	0.002	0.780	0.006
	b		0.712		0.786	
20	a		0.716	0.004	0.704	0.002
	b		0.720		0.706	
21	a		0.743	0.005	0.740	0.004
	b		0.738		0.736	
22	a		0.747	0	0.801	0
	b		0.747		0.801	
23	a		0.680	0.001	0.775	0.005
	b		0.681		0.780	
24	a		1.015	0.003	0.696	0
	b		1.012		0.696	

Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise

Board S/N 036 in Module S/N 014

	Pwr1	Pwr2	Pwr3	Pwr4	Pwr10	Pwr11	Pwr12	Pwr13	Pwr14	Pwr15	Pwr16	Pwr17	Pwr18
Vdd (V)	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.79	2.78	2.75	2.7	2.73	2.8
Vss (V)	-1.4	-1.3	-1.2	-1.1	-1.17	-1.13	-1.1	-1.1	-1.1	-1.1	-1.1	-1.1	-1.25
Vdd' (V)	2.483	2.498	2.512	2.528	2.5168	2.5228	2.5278	2.5177	2.5077	2.4781	2.4285	2.4583	2.5053
Vss' (V)	-1.089	-1.003	-0.919	-0.833	-0.893	-0.855	-0.833	-0.833	-0.833	-0.833	-0.833	-0.833	-0.961
Idd (mA)	1.2197	1.162	1.1053	1.0468	1.088	1.0645	1.047	1.0468	1.0466	1.0457	1.0444	1.0452	1.1337
Iss (mA)	1.1831	1.126	1.0691	1.0111	1.0519	1.0285	1.0111	1.0109	1.0108	1.01	1.0089	1.0095	1.0974
I (mA)	1.2014	1.144	1.0872	1.02895	1.06995	1.0465	1.02905	1.02885	1.0287	1.02785	1.02665	1.02735	1.11555
P (mW)	4.2914008	4.005144	3.7301832	3.458301	3.6483155	3.5348677	3.4584312	3.4473677	3.4365781	3.4033141	3.348419	3.3813171	3.866831

Channel Num			Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz
Channel: 1	11.03	9.20	12.64	16.28	11.46	14.16	15.22	15.66	15.95	17.32	15.71	15.29	10.91
Channel: 2	7.52	9.45	10.06	8.56	5.67	7.83	7.27	8.64	6.77	6.95	7.41	6.16	6.50
Channel: 3	7.91	8.54	9.93	9.64	6.51	7.60	7.07	8.82	7.45	8.17	10.94	7.77	7.55
Channel: 4	10.27	10.41	9.63	10.23	6.52	7.27	7.67	8.22	6.22	6.35	7.42	6.49	6.43
Channel: 5	9.65	6.62	8.00	13.66	7.83	9.30	10.19	10.91	11.67	12.80	16.20	12.28	8.41
Channel: 6	7.59	8.90	10.50	12.28	10.18	13.62	13.23	13.46	14.10	14.44	17.53	16.59	7.95
Channel: 7	8.40	8.97	8.74	11.33	6.70	9.96	7.76	7.02	6.71	7.05	12.59	8.40	5.70
Channel: 8	8.14	8.39	8.55	11.56	6.85	8.91	10.61	8.07	8.30	8.18	13.85	10.59	7.67
Channel: 9	8.69	9.73	9.84	11.71	8.18	9.18	11.25	10.68	10.29	11.58	17.07	10.98	7.02
Channel: 10	10.17	12.66	21.83	29.68	25.86	31.61	35.91	36.11	36.50	31.24	37.25	37.31	18.70
Channel: 11	9.90	8.96	9.82	11.12	8.69	10.97	8.75	8.84	9.07	7.69	13.12	8.43	9.34
Channel: 12	7.80	9.21	13.31	18.03	10.44	11.70	15.85	15.01	15.83	18.67	17.50	20.19	8.88
Channel: 13	8.22	10.04	9.00	9.28	9.26	7.26	8.71	9.52	9.49	9.68	10.74	10.81	6.38
Channel: 14	9.39	9.78	8.92	10.59	8.25	8.30	11.76	10.08	10.17	9.55	14.39	11.99	6.52
Channel: 15	9.91	9.87	10.92	15.06	9.63	17.29	14.28	15.11	14.44	12.12	18.76	13.37	10.58
Channel: 16	7.31	8.91	8.17	9.69	8.93	7.89	9.01	9.04	6.87	7.65	9.05	10.74	6.91
Channel: 17	8.32	9.27	10.48	14.91	8.45	11.63	12.63	12.91	13.49	14.76	16.23	15.39	9.35
Channel: 18	12.25	10.42	11.24	14.53	12.02	10.86	11.16	13.93	12.71	15.00	17.25	13.85	10.21
Channel: 19	8.19	7.82	8.67	10.48	8.81	9.37	6.19	7.99	8.44	8.92	9.44	8.57	8.88
Channel: 20	8.33	7.44	8.34	10.14	6.50	8.45	6.62	7.04	7.30	7.14	7.21	7.89	7.45
Channel: 21	9.11	9.64	8.41	10.26	5.91	6.96	7.01	7.34	7.93	8.58	8.23	7.92	7.28
Channel: 22	11.54	8.97	8.23	10.93	7.25	8.64	9.94	11.60	11.25	11.45	11.70	10.60	6.66
Channel: 23	11.40	7.36	7.85	9.13	6.21	6.24	7.48	6.89	9.29	9.25	8.21	9.09	6.43
Channel: 24	11.60	9.88	8.96	12.70	7.91	9.86	10.91	9.54	10.31	11.89	13.22	14.59	7.06
Median	8.90	9.20	9.31	11.22	8.21	9.24	10.06	9.53	9.83	9.61	13.17	10.77	7.50
Overall Mean	9.28	9.19	10.09	12.57	8.92	10.62	11.10	11.35	11.27	11.52	13.79	12.30	8.28
Good Mean	9.28	9.19	9.58	11.14	8.18	9.36	9.50	9.53	9.63	9.71	10.50	10.03	7.83
MP Reqd Yield	**1.00**	**1.00**	**0.96**	**0.83**	**0.96**	**0.92**	**0.88**	**0.83**	**0.88**	**0.83**	**0.63**	**0.79**	**0.96**
# Good Ch.	24	24	23	20	23	22	21	20	21	20	15	19	23
# Bad Ch.	0	0	1	4	1	2	3	4	3	4	9	5	1

Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise

Board S/N 037 in Module S/N 014

	Pwr1	Pwr2	Pwr3	Pwr4	Pwr5	Pwr5b	Pwr7	Pwr8	Pwr9
Vdd (V)	2.74	2.8	2.8	2.8	2.7	2.7	2.7	2.7	2.7
Vss (V)	-1.31	-1.5	-1.6	-1.7	-1.3	-1.25	-1.2	-1.18	-1.15
Vdd' (V)	2.4414	2.4724	2.4574	2.4427	2.403	2.4102	2.4176	2.4206	2.4251
Vss' (V)	-1.016	-1.177	-1.262	-1.348	-1.008	-0.965	-0.923	-0.906	-0.881
Idd (mA)	1.1495	1.2601	1.3174	1.3739	1.1428	1.114	1.0851	1.0735	1.056
Iss (mA)	1.1149	1.225	1.2822	1.3384	1.1085	1.0797	1.051	1.0394	1.0219
I (mA)	1.1322	1.24255	1.2998	1.35615	1.12565	1.09685	1.06805	1.05645	1.03895
P (mW)	3.91446828	4.53456197	4.83447612	5.14075781	3.83959215	3.70208812	3.56792783	3.51438657	3.4348726

Channel Num			Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz
Channel: 1	12.03	8.11	10.61	8.71	16.62	11.69	14.13	13.34	9.95
Channel: 2	9.70	6.34	9.63	8.20	13.34	14.41	17.41	16.68	10.31
Channel: 3	24.00	8.36	8.94	9.71	32.05	35.34	45.94	51.52	52.97
Channel: 4	5.55	6.72	6.62	10.11	10.33	9.12	12.35	20.08	8.12
Channel: 5	7.48	6.14	7.83	10.78	17.56	7.57	7.88	14.44	9.74
Channel: 6	7.17	5.96	9.89	8.76	14.30	12.57	9.43	18.32	12.96
Channel: 7	6.76	5.94	8.19	10.76	9.85	11.71	9.48	11.27	9.10
Channel: 8	8.18	8.53	9.92	13.21	8.11	13.05	11.78	7.71	14.65
Channel: 9	6.38	8.79	11.59	7.26	7.60	12.87	16.33	18.46	23.72
Channel: 10	8.63	10.24	11.90	8.59	11.28	12.76	8.52	12.59	10.20
Channel: 11	12.28	6.95	7.04	7.02	13.38	13.91	10.64	9.25	15.09
Channel: 12	6.63	6.80	7.18	6.82	8.91	11.49	12.52	13.28	22.26
Channel: 13	8.49	5.72	7.03	6.61	10.18	10.23	9.52	12.14	14.34
Channel: 14	11.39	16.17	15.49	14.47	12.52	12.75	12.89	12.87	15.52
Channel: 15	17.59	15.34	9.45	10.92	20.93	18.22	15.37	10.58	12.77
Channel: 16	6.10	6.00	6.91	7.28	15.73	10.41	11.10	7.34	12.03
Channel: 17	7.29	5.32	6.71	9.26	7.87	14.13	14.34	8.34	11.60
Channel: 18	7.72	10.62	15.39	13.90	10.41	13.09	11.32	7.49	10.17
Channel: 19	7.20	10.35	11.27	8.35	11.30	16.30	9.47	7.73	15.24
Channel: 20	10.63	10.35	8.56	13.97	14.44	13.89	12.73	16.38	22.05
Channel: 21	6.24	6.38	7.37	9.04	12.24	7.64	12.12	6.31	13.71
Channel: 22	6.06	7.43	9.94	9.95	9.74	13.35	13.76	6.33	15.45
Channel: 23	7.91	5.79	14.52	10.12	12.12	11.66	14.48	12.13	19.17
Channel: 24	6.68	7.13	15.31	9.64	12.16	10.26	16.35	12.97	22.05
Median	7.60	7.04	9.54	9.45	12.14	12.75	12.44	12.37	14.03
Overall Mean	9.09	8.14	9.89	9.73	13.04	13.27	13.74	13.65	15.97
Good Mean	8.02	7.45	9.10	9.73	11.06	11.84	11.50	10.34	11.40
MP Reqd					15				
Yield	**0.92**	**0.92**	**0.88**	**1.00**	**0.79**	**0.88**	**0.79**	**0.75**	**0.58**
# Good Ch.	22	22	21	24	19	21	19	18	14
# Bad Ch.	2	2	3	0	5	3	5	6	10

Attachment of HRCR Item # 9: SPIRE MIUL Cover Page

MIUL = Material Identification & Utilization List

Declared Materials List's and Processes List are not included in this HRCR

Materials and Processes List

SPIRE

JPL D-25725

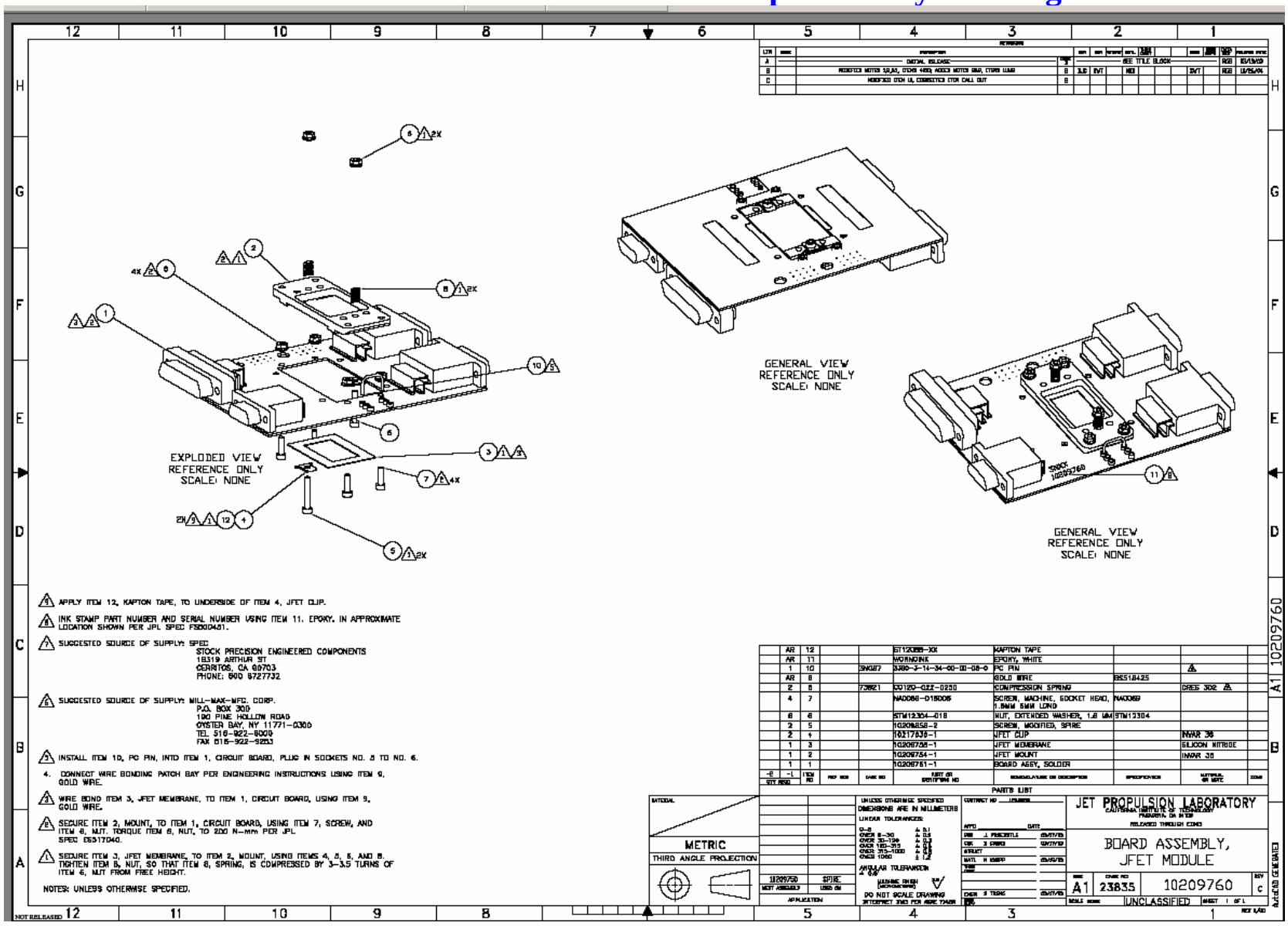
REV B
1/05/04

Reviewed by: _____
M. Knopp M&P Engineer

Attachment of HRCR Item # 11:

See End of This HRCR Package for "JFET Module Handling Document"

Attachment of HRCR Item # 14: JFET Module Top Assembly Drawing 10209750-1



Attachment of HRCR Item # 23: Qualification Compliance Test

Qualification Model JFET Module

EIDP Coverpage For JFET Testing

Unit Identfication		
Name	:	JFET QM Module
Part #	:	10209750-1
S/N	:	#001

Environmemtal Testing	Axes Tested	Temperature	Duration/# of Cycle	Requirement	Source	Waiver
Random Vibration Test	X, Y, Z	100 K	2 min/axis	X, Y, Z	SSSD, JFET-DES-07	
High Level Sine Vibe Test	None	NA	NA	X, Y, Z	SSSD, JFET-DES-07	HR-SP-JPL-RFW_005
Bakeout	NA	80 C	72 Hours	80C, 72 Hrs	D-20549	
Thermal Cycles	NA	RmT to 80 K	27	Minimum 15	D-20549	

Performance Characteristics		Specification		Source	Waiver
Power needed for <11 bad channels (Min Perf.)	9.1 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	RFW in process
Power needed for <4 bad channels (Design Value)	10.8 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	
Power needed for 100 % Yield per unit	13.5 mW	NA		NA	
Median Noise at < 11 bad chs.	7.13 nV/rtHz	<15 nV/rtHz Min Performance		SSSD, JFET-PER-01	
Median Noise at < 4 bad chs.	6.1 nV/rtHz		<7 nV/rtHz Design Value	SSSD, JFET-PER-01	
Median Noise at 100 % Yield.	6.97 nV/rtHz			SSSD, JFET-PER-01	
# of Channels over the max. offset voltage	0	< 15 mV for CQM < 15 mV for PFM/FS		SSSD, BDA-DRCU-27	
Common Mode Rejection Ratio	< -60 dB by design, as measured in EM4 unit			SSSD, BDA-DRCU-11	

Board Level Detail		Board SN 001		Source
# Channels Tested	:	24		
Median Noise at 3.5 mW	:	18 nV/rtHz		SSSD, JFET-PER-01
# of good channels at 3.5 mW	:	7	29% Yield	SSSD, JFET-PER-02
Power Needed for 100 % Yield	:	6.75 mW		SSSD, JFET-PER-02
Median Noise at High Power (w/ 100 % Yield)		6.97 nV/rtHz		SSSD, JFET-PER-01
Median Gain at High Power		0.98		NA

Definitions		
Good Channels	:	Noise less than a min. performance value of 15 nV/rtHz
Yield	:	# of Good Channels / 24
Filenames		
Noise Measurements	:	QualJFETPostVibeNoise_Summary.pdf

Notes	
1)	The Base temperature for all performance characterization was 4K
2)	All Noise Measurements were made with the inputs shorted to ground

Attachment of HRCR Item # 24 & #25: Mate/Demate & Operation Logs

Hardware ID JFET S/N 13, 14

Date	Time	AIDS	Power	Mate	Demate	Transport	Notes
11/24		244404					103 → 158
11/24		"					Pump out
11/26		"					90 to 80°C
11/27		"					turn heat off (25 hr bakeout)
11/28		"					158 → 183
11/30		"	X	X			.5 hr, each board, wrm S.V.
12/3		244448					install into shake facility
12/7		"				X	183 → 144
12/7							3 axis warm shake (pump out twice)
12/7		"				X	144 → 183
12/7		244449		X			install into grn dewar
12/8		"					pump out, 90 cold
12/9		"	X				4 hrs, brd 36, noise
12/10		"	X				10 hrs, " , "
12/13		"	X				10 hrs, brd 37, noise
12/14		"	X				3 hrs, " , "
12/14		"	X				3 hrs, " , gain, CMRR
12/14		"	X				3 hrs, brd 36, gain, CMRR
12/17					X	X	183 → 103

Attachment of HRCR Item # 24 & #25: Mate/Demate & Operation Logs (continued)

Hardware ID JFET S/N 14, 15

Date	Time	AIDS	Power	Mate	Demate	Transport	Notes
10/25/04	9A	244163				x	103 → [redacted] 158
10/26/04	4:30P	"					Pump out, start Bakeout to 80°C
10/28/04	10A	"				x	[redacted] 158 – 183
~~10/29~~	3P	244164	x				.5 hr each board, wrm S.V.
11/1	1030A	"				x	183 → 144
11/1	–	"					3 axis warm shake
11/2	Afternoon	"	–	–	–	–	Transfer to ESD bags
11/4	9:00a.m.	244170					Install into Green Dewar
11/4		"	x				.5 hr each board, wrm S.V.
11/4		"				x	183 → 103 (Mod 14 bad S.V.)
							PFR 284924

Attachment of HRCR Items # 24 & # 25: Mate/Demate & Operation Logs (PWB S/N 036)

OPERATION LOG SHEET -- SPIRE JFET BOARDS MODULE

Mod. 14

USE THE "NOTE" COLUMN TO DESCRIBE ACTIONS

DEVICE (BRD) S/N: 36 (50) PROJECT: SPIRE/ JFET BOARD

DATE	TIME	TECH	PWR ON	PWR OFF	MATE				DEMATE				TRANSFORT	NOTE
					JAA	JBB	JCC	JDD	JAA	JBB	JCC	JDD		
7-19-04					✓	✓	✓	✓						GND & CHASSIS - SAUER ON
9-23-04		NAN												GND & CHASSIS "
9-23-04		NAN	✓	✓										SOURCE TEST "
11-16-04		NAN	✓											GND & CHASSIS "
11-16-04		NAN	✓	✓										SOURCES TEST "
11-22-04		BOB / NAN					✓	✓	✓	✓	✓	✓		DEMATE SAUER INSTALL TO M. #14
11-23-04		NAN			✓	✓	✓	✓			✓	✓		GND & CHASSIS TEST
11-23-04		NAN	✓	✓			✓	✓	✓	✓	✓	✓		SOURCE TEST
11-24-04		NAN			✓	✓	✓	✓			✓	✓		GND & CHASSIS
11-24-04		NAN	✓	✓			✓	✓	✓	✓				SOURCE TEST

Attachment of HRCR Items # 24 & # 25: Mate/Demate & Operation Logs (PWB S/N 037)

OPERATION LOG SHEET -- SPIRE JFET BOARDS MODULE

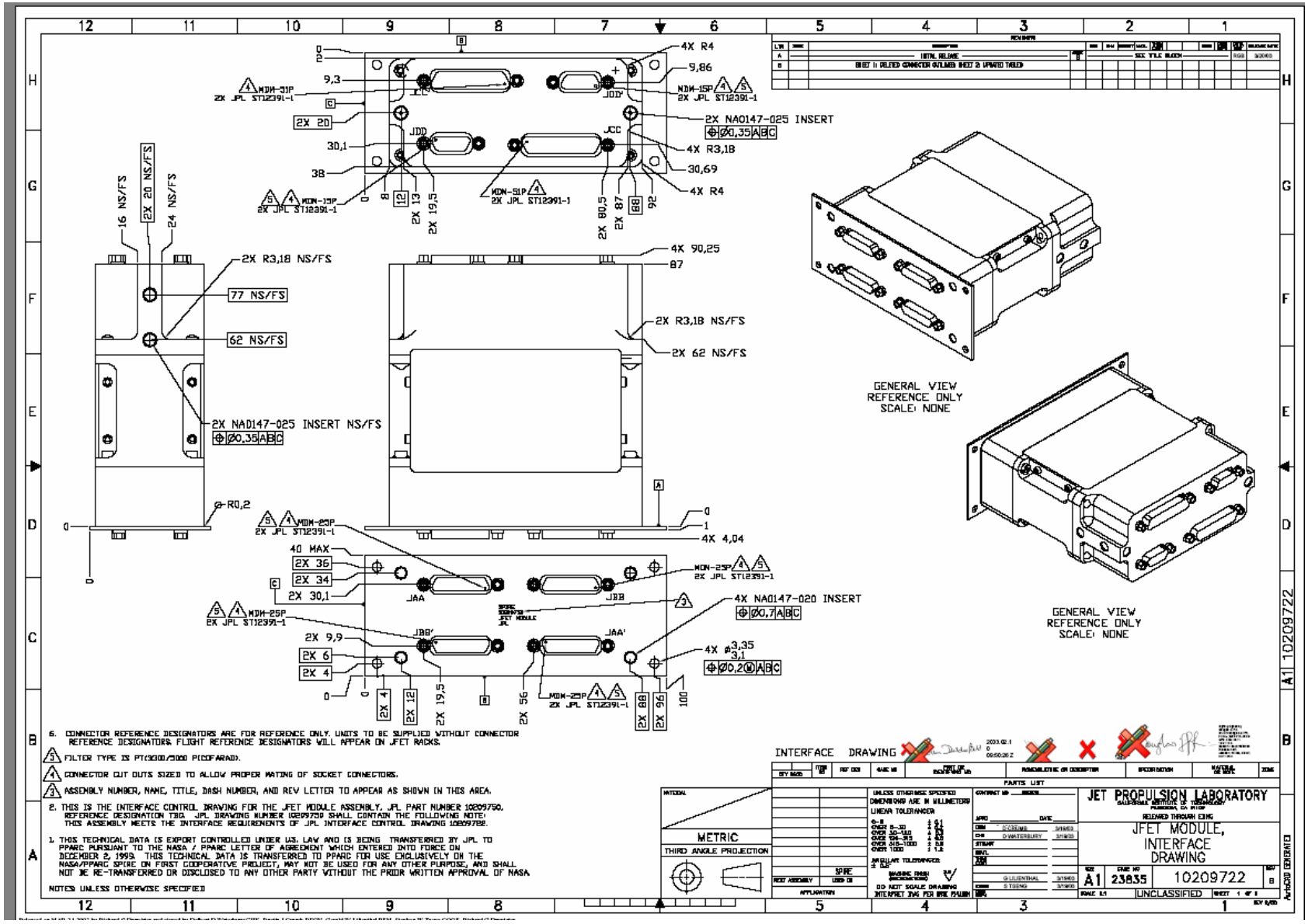
Mod. 14

USE THE "NOTE" COLUMN TO DESCRIBE ACTIONS

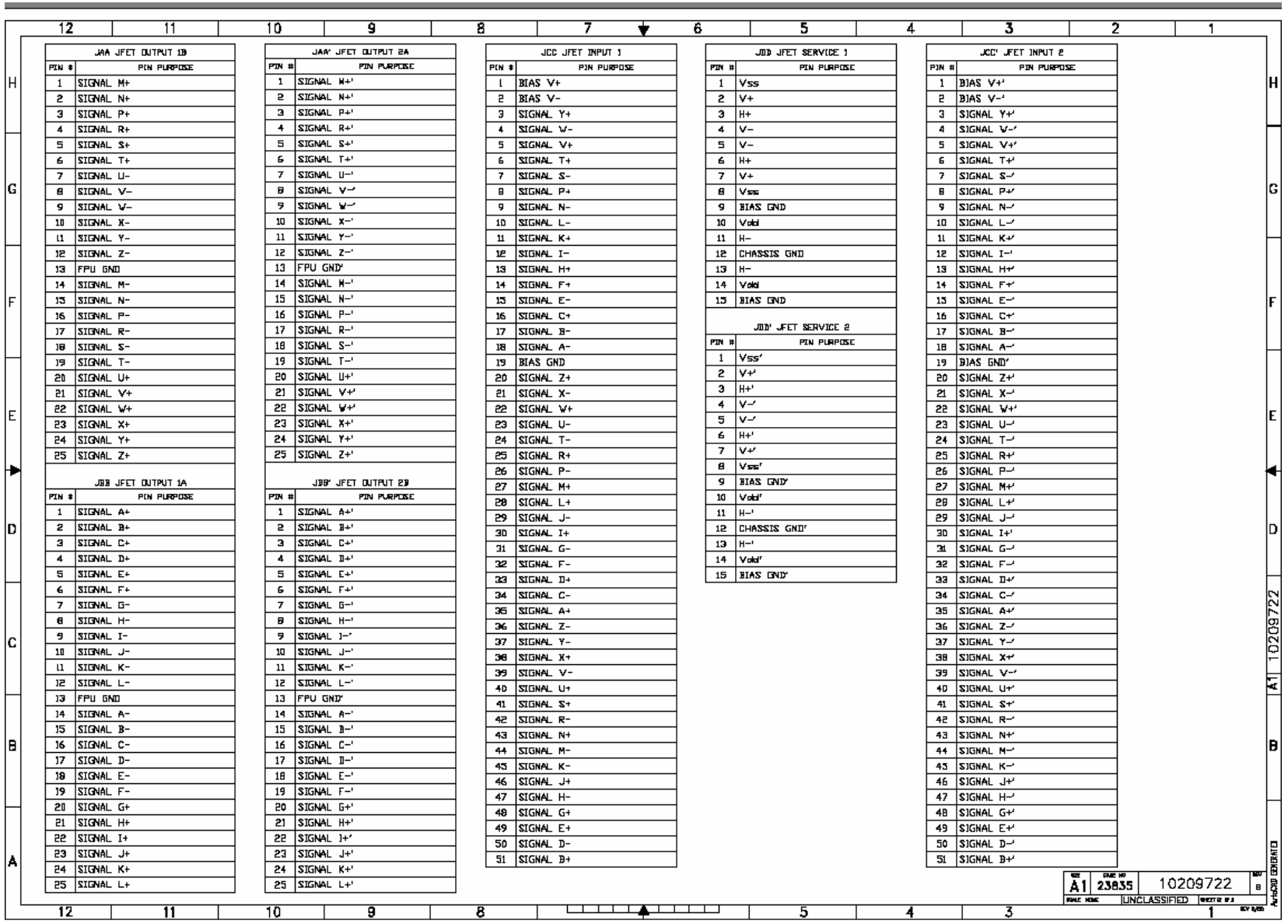
DEVICE (BRD) S/N: 37 (51) PROJECT: SPIRE/ JFET BOARD

DATE	TIME	TECH	PWR ON	PWR OFF	MATE JAA	MATE JBB	MATE JCC	MATE JDD	DEMATE JAA	DEMATE JBB	DEMATE JCC	DEMATE JDD	TRANSFORT	NOTE
7-30-4					✓	✓	✓	✓						GND & CHASSIS - SAUER-ON
9-23-4		NW												GND & CHASSIS - "
9-23-4		NW	✓	✓										SOURCE TEST "
11-16-4		NW												GND & CHASSIS "
11-16-4		NW	✓	✓										SOURCE TEST "
11-18-4		NW												GND & CHASSIS "
11-18-4		NW	✓	✓										SOURCE TEST "
11-18-4		NW												GND & CHASSIS "
11-18-4		NW	✓	✓										SOURCE TEST "
11-22-04		BDP/NW					✓	✓	✓	✓	✓	✓		INSTALL TO M.#14 DEMATE SAVERS
11-23-04		NW			✓	✓	✓	✓			✓	✓		GND & CHASSIS
11-23-04		NW	✓	✓			✓	✓	✓	✓	✓	✓		SOURCE TEST
11-24-04		NW			✓	✓	✓	✓			✓	✓		GND & CHASSIS
11-24-04		NW	✓	✓			✓	✓	✓	✓				SOURCE TEST

Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 1 of 2)



Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 2 of 2)



JAA JFET OUTPUT 1B

PIN #	PIN PURPOSE
1	SIGNAL M+
2	SIGNAL N+
3	SIGNAL P+
4	SIGNAL R+
5	SIGNAL S+
6	SIGNAL T+
7	SIGNAL U-
8	SIGNAL V-
9	SIGNAL W-
10	SIGNAL X-
11	SIGNAL Y-
12	SIGNAL Z-
13	FPU GND
14	SIGNAL M-
15	SIGNAL N-
16	SIGNAL P-
17	SIGNAL R-
18	SIGNAL S-
19	SIGNAL T-
20	SIGNAL U+
21	SIGNAL V+
22	SIGNAL W+
23	SIGNAL X+
24	SIGNAL Y+
25	SIGNAL Z+

JBB JFET OUTPUT 1A

PIN #	PIN PURPOSE
1	SIGNAL A+
2	SIGNAL B+
3	SIGNAL C+
4	SIGNAL D+
5	SIGNAL E+
6	SIGNAL F+
7	SIGNAL G-
8	SIGNAL H-
9	SIGNAL I-
10	SIGNAL J-
11	SIGNAL K-
12	SIGNAL L-
13	FPU GND
14	SIGNAL A-
15	SIGNAL B-
16	SIGNAL C-
17	SIGNAL D-
18	SIGNAL E-
19	SIGNAL F-
20	SIGNAL G+
21	SIGNAL H+
22	SIGNAL I+
23	SIGNAL J+
24	SIGNAL K+
25	SIGNAL L+

JAA' JFET OUTPUT 2A

PIN #	PIN PURPOSE
1	SIGNAL M+'
2	SIGNAL N+'
3	SIGNAL P+'
4	SIGNAL R+'
5	SIGNAL S+'
6	SIGNAL T+'
7	SIGNAL U-'
8	SIGNAL V-'
9	SIGNAL W-'
10	SIGNAL X-'
11	SIGNAL Y-'
12	SIGNAL Z-'
13	FPU GND'
14	SIGNAL M-'
15	SIGNAL N-'
16	SIGNAL P-'
17	SIGNAL R-'
18	SIGNAL S-'
19	SIGNAL T-'
20	SIGNAL U+'
21	SIGNAL V+'
22	SIGNAL W+'
23	SIGNAL X+'
24	SIGNAL Y+'
25	SIGNAL Z+'

JBB' JFET OUTPUT 2B

PIN #	PIN PURPOSE
1	SIGNAL A+'
2	SIGNAL B+'
3	SIGNAL C+'
4	SIGNAL D+'
5	SIGNAL E+'
6	SIGNAL F+'
7	SIGNAL G-'
8	SIGNAL H-'
9	SIGNAL I-'
10	SIGNAL J-'
11	SIGNAL K-'
12	SIGNAL L-'
13	FPU GND'
14	SIGNAL A-'
15	SIGNAL B-'
16	SIGNAL C-'
17	SIGNAL D-'
18	SIGNAL E-'
19	SIGNAL F-'
20	SIGNAL G+'
21	SIGNAL H+'
22	SIGNAL I+'
23	SIGNAL J+'
24	SIGNAL K+'
25	SIGNAL L+'

JCC JFET INPUT 1

PIN #	PIN PURPOSE
1	BIAS V+
2	BIAS V-
3	SIGNAL Y+
4	SIGNAL W-
5	SIGNAL V+
6	SIGNAL T+
7	SIGNAL S-
8	SIGNAL P+
9	SIGNAL N-
10	SIGNAL L-
11	SIGNAL K+
12	SIGNAL I-
13	SIGNAL H+
14	SIGNAL F+
15	SIGNAL E-
16	SIGNAL C+
17	SIGNAL B-
18	SIGNAL A-
19	BIAS GND
20	SIGNAL Z+
21	SIGNAL X-
22	SIGNAL W+
23	SIGNAL U-
24	SIGNAL T-
25	SIGNAL R+
26	SIGNAL P-
27	SIGNAL M+
28	SIGNAL L+
29	SIGNAL J-
30	SIGNAL I+
31	SIGNAL G-
32	SIGNAL F-
33	SIGNAL D+
34	SIGNAL C-
35	SIGNAL A+
36	SIGNAL Z-
37	SIGNAL Y-
38	SIGNAL X+
39	SIGNAL V-
40	SIGNAL U+
41	SIGNAL S+
42	SIGNAL R-
43	SIGNAL N+
44	SIGNAL M-
45	SIGNAL K-
46	SIGNAL J+
47	SIGNAL H-
48	SIGNAL G+
49	SIGNAL E+
50	SIGNAL D-
51	SIGNAL B+

JDD JFET SERVICE 1

PIN #	PIN PURPOSE
1	Vss
2	V+
3	H+
4	V-
5	V-
6	H+
7	V+
8	Vss
9	BIAS GND
10	Vdd
11	H-
12	CHASSIS GND
13	H-
14	Vdd
15	BIAS GND

JDD' JFET SERVICE 2

PIN #	PIN PURPOSE
1	Vss'
2	V+'
3	H+'
4	V-'
5	V-'
6	H+'
7	V+'
8	Vss'
9	BIAS GND'
10	Vdd'
11	H-'
12	CHASSIS GND'
13	H-'
14	Vdd'
15	BIAS GND'

JCC' JFET INPUT 2

PIN #	PIN PURPOSE
1	BIAS V+'
2	BIAS V-'
3	SIGNAL Y+'
4	SIGNAL W-'
5	SIGNAL V+'
6	SIGNAL T+'
7	SIGNAL S-'
8	SIGNAL P+'
9	SIGNAL N-'
10	SIGNAL L-'
11	SIGNAL K+'
12	SIGNAL I-'
13	SIGNAL H+'
14	SIGNAL F+'
15	SIGNAL E-'
16	SIGNAL C+'
17	SIGNAL B-'
18	SIGNAL A-'
19	BIAS GND'
20	SIGNAL Z+'
21	SIGNAL X-'
22	SIGNAL W+'
23	SIGNAL U-'
24	SIGNAL T-'
25	SIGNAL R+'
26	SIGNAL P-'
27	SIGNAL M+'
28	SIGNAL L+'
29	SIGNAL J-'
30	SIGNAL I+'
31	SIGNAL G-'
32	SIGNAL F-'
33	SIGNAL D+'
34	SIGNAL C-'
35	SIGNAL A+'
36	SIGNAL Z-'
37	SIGNAL Y-'
38	SIGNAL X+'
39	SIGNAL V-'
40	SIGNAL U+'
41	SIGNAL S+'
42	SIGNAL R-'
43	SIGNAL N+'
44	SIGNAL M-'
45	SIGNAL K-'
46	SIGNAL J+'
47	SIGNAL H-'
48	SIGNAL G+'
49	SIGNAL E+'
50	SIGNAL D-'
51	SIGNAL B+'

Attachment of HRCR Item # 11:

SPIRE

Handling Document

Field Effect Transistor (JFET) Module

10209750-1

Prepared by: Kalyani Sukhatme

10 September, 2003

Hardware Handling Guidelines

Contamination: Open shipment suitcase in a FED-STD-209 Class 10,000 clean room (ISO 14644-1 class 7) or better. Handle hardware with gloves.

ESD: Handle with grounding straps, ESD-safe gloves and ESD smocks at an ESD-safe workstation. Maintain shorting plugs on the unit whenever ESD is a concern. Refer to attached electrical handling document for other important safety precautions.

Fragile: Do not drop or otherwise shock the hardware including the shipping suitcase and container.

Humidity Sensitive: Place hardware in a humidity controlled Class 10,000 clean room. Maintain humidity level at 35%-50% RH typical, for ESD safety.

SPIRE JFET Electrical Handling Document

1. Introduction

This document provides guidelines for electrical handling for the SPIRE JFET Module.

1.1 Hardware Description

Each JFET module has two sets of 24 JFET channels. The JFET channels are populated on 1.0 micron thick Silicon Nitride membranes which provides thermal isolation. The operating temperature for these JFETs is ~120 K. The process of powering up the JFETs dissipates heat into the membrane resulting in a temperature increase with respect to the base temperature (4K to 10 K). Higher the power dissipation, higher is the temperature of the JFETs.

Each JFET channel consists of a matched pair of FETs (Figure 1.1-1) with a requirement for the offset voltage of less than **15 mV** between the matched pair. [The characteristic offset voltage is the difference between the source voltages (V_{sa} and V_{sb} with respect to ground) of the two FETs.]

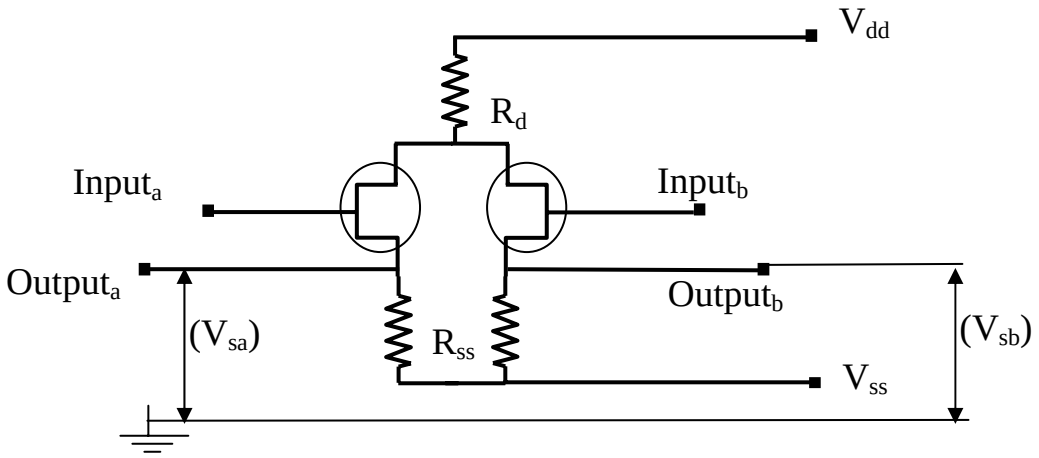


Figure 1.1-1

The Gates of the JFETs are the 'Inputs' of the circuit and the Sources (V_{sa} and V_{sb}) of the JFETs are the outputs, as marked in Figure 1.1-1. Vdd and Vss are the power lines for the circuit.

Handling

1. **The JFET Module is Contamination Sensitive**: Handle the unit with Gloves only in a FED-STD-209 Class 100000 clean room (ISO 14644-1 class 7) or better.

2. **The JFET Module is ESD Sensitive**: Please handle with appropriate ESD hardware handling procedures. Handle with grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.

3. **The JFET Module is Fragile**: Please do not drop or otherwise shock the unit. Please DO NOT remove the cover of the JFET Module.

Power ON Procedure

1. The JFET Module should be powered on **WITH the shorting plugs** (JPL Supplied Protection connectors) in place and with the **inputs shorted to ground.** Pins #9 and #15 on the 15-pin MDM connectors on the JFET Module are the bias grounds on the module. These pins should also be shorted to the power supply ground. The unit may be powered up without the shorting plug only when the inputs are connected to the detector system.

Under no circumstances the unit should be powered up without the inputs shorted to ground either via the shorting plug (JPL Supplied) or via the detector system.

2. Do not exceed a voltage of +5 V for the Vdd line and –5 V for the Vss line of the JFET Module.

3. When removing the shorting plugs from the unit for installation into the instrument, please use standard ESD precautions including grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.

Electrical Check-out Test: Characteristic Offset Voltage Measurement

1) Verify that the gates of the JFET channels (Inputs) are shorted together and grounded.
2) Apply the power supply ground to the bias ground pins on the unit (Pins 9 and 15 on the 15-pin MDM connectors)
3) Power on the JFET modules with Vdd = +3 V and Vss = -1.5 V
4) Verify that the handheld multimeter is in calibration.
5) Connect one side of the handheld multimeter to ground (Power supply ground).
6) And measure the voltage with respect to ground of each side (V_{sa} and V_{sb}) of each channel.
7) Calculate the characteristic offset voltage (V_{offset}) for each channel ($V_{offset}= V_{sa}-V_{sb}$)
8) Compare the values for each of the channels with the specific datasheet provided with the unit. The datasheets accompanying the unit also provides the values for the drain and source currents for a similar test performed at JPL.

REFER TO MEASURED SOURCE VOLTAGE DATA FOR ACTUAL HARDWARE. Here is an example of the source voltage values and the drain and the source currents obtained for such a test at room temperature are given in the Table 4-1

T, JFET	rm T	
Vdd	3 V	
Vss	-1.5 V	
Idd	1.564 mA	
Iss	1.5686 mA	
Channel #	(V)	DELTA (V)
1	1.130	0
	1.130	
2	1.075	0.001
	1.074	
3	0.781	0.001
	0.780	
4	1.088	0.005
	1.093	
5	0.834	0.001
	0.833	
6	1.012	0.003
	1.015	
7	0.785	0.002
	0.787	
8	1.148	0.004
	1.144	
9	0.753	0
	0.753	

10	0.693	0.008
	0.701	
11	1.110	0.004
	1.114	
12	0.758	0.001
	0.759	
13	0.832	0.002
	0.830	
14	1.264	0.001
	1.265	
15	1.206	0
	1.206	
16	0.818	0.001
	0.819	
17	0.526	0.005
	0.521	
18	1.423	0
	1.423	
19	0.773	0.002
	0.775	
20	0.873	0.004
	0.877	
21	1.387	0.006
	1.393	
22	1.417	0.003
	1.420	
23	0.887	0.002
	0.889	
24	0.888	0.003
	0.891	

- END OF -
Attachment of HRCR Item # 11:
JFET Module Handling Document

END OF

HRCR PACKAGE