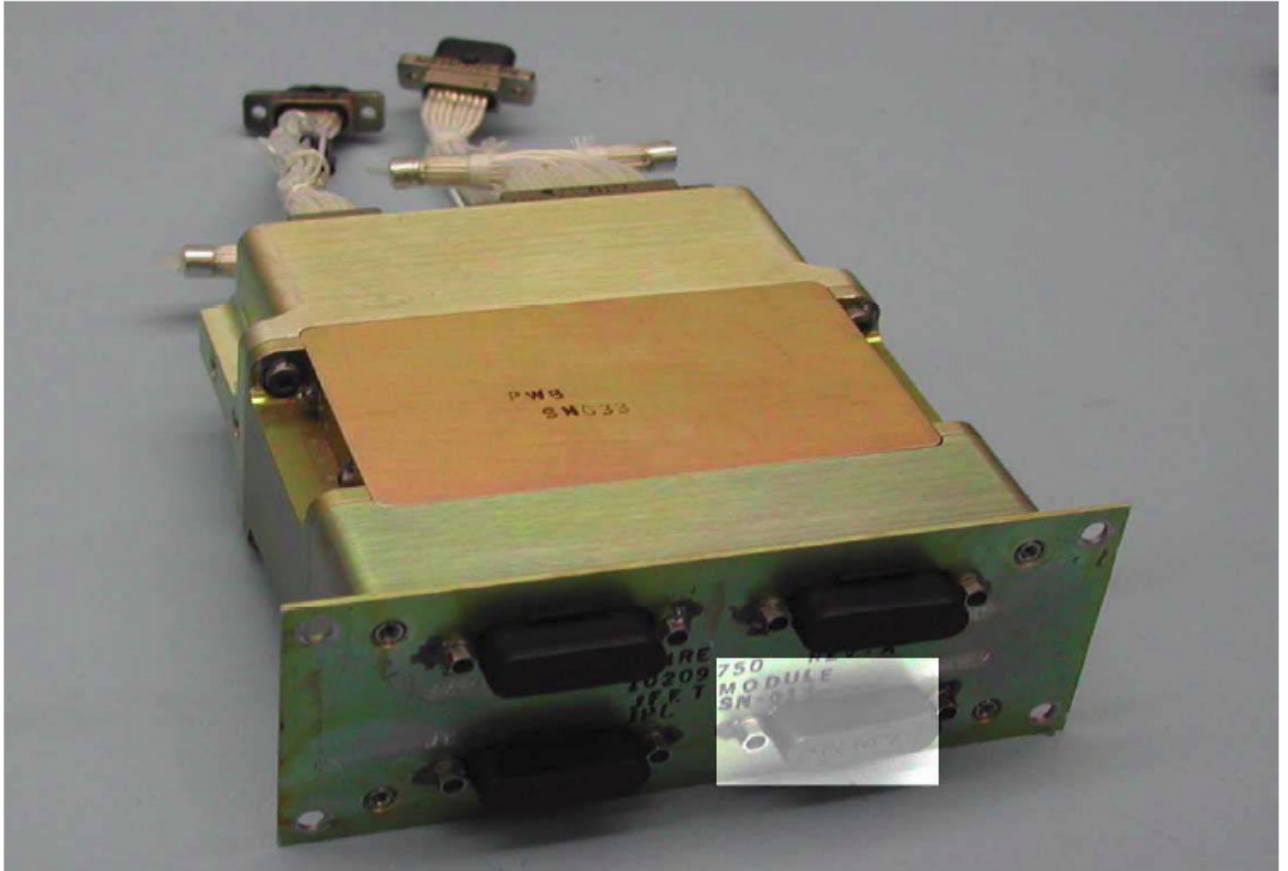


JPL Hardware Requirements Certification Review – SPIRE Element No. D-30474

Assembly / Subsystem		PEM	Phone	Section			Date	
SPIRE		Martin Herman	(818) 354-8541	386			3 February, 2005	
Drawing/ Part No.	Dwg. Rev.	Nomenclature	Serial No.	Model	Type	Final IR No.	Mass (Meas. / Req.)	
10209750-1	B	JFET Module	013	FLIGHT	N/A	923845	275.8 gm / 305 gm	
Check applicable answer and provide explanation in remarks column		Y E S	N O	N A	Remarks		Data Attachments	Signature & Date
1. Are all drawings and specifications complete, approved, released and frozen?		X					14. Latest Top Assembly drawings <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None	Cognizant Engineer <i>DeWisey 2/18/05</i>
2. Do the released drawings and specifications reflect all approved changes?		X					15. List of open ECRs <input type="checkbox"/> Attached <input checked="" type="checkbox"/> None	PEM <i>Martin H 2/18/05</i>
3. Is hardware identical to other hardware delivered? If no, provide difference list.		X					16. Waivers (RFW request for waiver) <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None	QA Engineer <i>Soreen Valente 2/18/05</i>
4. Does the hardware meet its functional requirements, specifications, waivers, ICDS?		X			EIDP attached. Also see item # 8 attachments.		17. Open MRB <input type="checkbox"/> Attached <input checked="" type="checkbox"/> None	Environments/Reliability <i>J - 1-ell 2/18/05</i>
5. Are all IR and MRB dispositioned and concurred by QA?		X					18. Open PFR on this H/W <input type="checkbox"/> Attached <input checked="" type="checkbox"/> None	Mission Assurance Mgr. <i>J - 1-ell 2/18/05</i>
6. Is complete as-built list information included in the build book?		X					19. Open PFR on similar H/W <input type="checkbox"/> Attached <input checked="" type="checkbox"/> None	Project Office <i>J - 1-ell 2/18/05</i>
7. Have all required environmental tests & analyses been completed?		X			ETAS attached		20. Handling Document → See Item 11 <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None	PI <i>James J. Bell 2/18/05</i>
8. Is all required assembly and/or subsystem level functional testing complete?		X			Performance Test Data Attached. Also see EIDP in item # 4.		21. Shortage List <input type="checkbox"/> Attached <input checked="" type="checkbox"/> None	
9. Have all piece parts, processes and materials been approved by JPL?		X					22. Requirements Verification Matrix <input checked="" type="checkbox"/> Attached (See #4, #7, #8) <input type="checkbox"/> None	
10. Does this hardware meet all contamination control requirements?		X			Parts, processes and MIUL met all contamination control and out-gassing requirements.		23. Qualification Status <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None	
11. Are all shipping containers, shipping and special handling procedures ready?		X			See Attached Document D-26790		24. Mate / Demate Record <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None	
12. Is additional work required to bring this hardware to flight readiness?			X				25. Operating Log <input checked="" type="checkbox"/> Attached (See Item # 24) <input type="checkbox"/> None	
13. Is this hardware acceptable for flight?		X					26. MICD <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None	



SPIRE JFET Module S/N 013

RAL EIDP Table of Contents Versus JPL HRCR Check List Item Numbers

RAL EIDP Section Number	RAL EIDP Title	JPL HRCR Check List Item Number	Notes
1	Shipping Documents		Shipper and Final IR
2	Transportation, Packing, Handling & Integration Procedures	11	Special Handling Document D-26790
3	Certificate of Conformance / Delivery Review Board MOM		HRCR book is the C of C
4	As Built Configuration Status List	1 & 2	Assembly Drawings
5	List of Waivers	4	RFW (request for waiver) Attached
6	Copies of Waivers	4 & 7	RFW (request for waiver) Attached
7	List of Non-Conformance Reports		See RFW in 4 & 7
8	Copies of Non-Conformance Reports		See RFW in 4 & 7
9	Cleanliness Statement		Final IR QA Inspection
10	Operational Manual		NA
11	Top Level Drawings (inc. Family Tree)	14	Top Assembly Drawing
12	Interface Drawings	26	MICD Drawing
13	Functional, Block & Mechanical Drawings		NA
14	Electrical Circuit Drawings		NA
15	Serialized Components List		In build books – not shipped
16	Mass Properties/ Power Budget	HRCR Check List Page 1	Mass listed in HRCR check list
17	Qualification Status List / Test Matrix	23	Qualification Unit Test Matrix
18	Test Reports	4, 7, 8, 23	
19	Open Work / Deferred Work / Open Tests		NA
20	Calibration Data		NA
21	Historical Record	23	Qualification Unit Test Matrix
22	Manufacturing Logbook(s)		In build books – not shipped
23	Operating Time / Cycle Record	25	
24	Connector Mating Record	24	
25	Age Sensitive Items Record		NA
26	Pressure Vessels – History/Test Record		NA
27	Temporary Installation Record		NA
28	Reference List of EIDPs (Lower level)		NA
29	Other Useful Information		NA

JPL Hardware Requirements
Certification Review (HRCR)

Junction Field Effect Transistor (JFET)
Flight Module

10209750-1 S/N 013

SPIRE Element
Herschel Space Observatory Project

February 3, 2005

Configuration of Module, Boards & Membranes

Module 10209750-1	S/N 13	S/N 13
PWB 10209760-1	S/N 33	S/N 39
Membrane 10209758-1	J6.10.6	J6.15.4

Attachment of HRCR Items #1 Drawing Release Status

ALL ASSEMBLY & PARTS DRAWINGS ARE RELEASED IN PDMS

Released Drawings:

- 10209719-1 assembly built per released Rev. A drawing (studlock)**
- 10209722-1 assembly built per released Rev. B drawing (interface drawing)**
- 10209750-1 assembly built per released Rev. B drawing (module assy)**
- 10209751-1 assembly built per released Rev. B drawing (chassis 1)**
- 10209752-1 assembly built per released Rev. A drawing (chassis 2)**
- 10209753-1 assembly built per released Rev. A drawing (chassis 3)**
- 10209754-1 assembly built per released Rev. C drawing (mount)**
- 10209756-1 assembly built per released Rev. B drawing (chassis lid)**
- 10209757-1 assembly built per released Rev. A drawing (membrane)**
- 10209758-1 assembly built per released Rev. A drawing (membrane assy)**
- 10209759-1,-2,-4 redlined Rev. B drawing (gasket)**
- 10209760-1 assembly built per released Rev. C drawing (board assembly)**
- 10209761-1 assembly built per released Rev. C drawing (solder connector)**
- 10209769-1 assembly built per released Rev. A drawing (stiffener)**
- 10209777-1 assembly built per released Rev. B drawing (board)**
- 10209858-2 assembly built per released Rev. A drawing (special fastener)**
- 10217636-1 assembly built per released Rev. A drawing (clip)**

Attachment of HRCR Item #4: EIDP

EIDP Coveragepage For JFET Testing

Unit Identification						
Name	:	JFET PFM Module				
Part #	:	10209750-1				
S/N	:	#013				

Environmental Testing						
	Axes Tested	Temp	Duration/# of Cycle	Requirement	Source	Waiver
Random Vibration Test	X, Y, Z	Rm T	1 min/axis	X, Y, Z	SSSD, JFET-DES-07	
High Level Sine Vibe Test	None	NA	NA	X, Y, Z	SSSD, JFET-DES-07	HR-SP-JPL-RFW-005
Bakeout	NA	80 C	25 hrs	> 24 HRS		
Thermal Cycles	NA	RmT to 80 K	2	Minimum 1	D-20549	

Performance Characteristics						
		Specification		Source	Waiver	
Power needed for <11 bad channels (Min Perf.)	7.15 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	HR-SP-JPL-RFW-004	
Power needed for <4 bad channels (Design Value)	8.39 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02		
Power needed for 100 % Yield per unit	8.96 mW	NA		NA		
Median Noise at < 11 bad chs.	10.02 nV/rHz	<15 nV/rHz Min Performance	<7 nV/rHz Design Value	SSSD, JFET-PER-01		
Median Noise at < 4 bad chs.	7.98 nV/rHz			SSSD, JFET-PER-01		
Median Noise at 100 % Yield.	6.77 nV/rHz			SSSD, JFET-PER-01		
# of Channels over the max. offset voltage	0	< 15 mV			SSSD, BDA-DRCU-27	
Common Mode Rejection Ratio	< -80 dB by design, as measured in EM4 unit				SSSD, BDA-DRCU-11	

Board Level Details						
	Board SN 033 (JAA-JDD)		Board SN 039 (JAA'-JDD')		Source	
# Channels Tested	24		24			
Median Noise at 3.5 mW	11.39 nV/rHz		9.32 nV/rHz		SSSD, JFET-PER-01	
# of good channels at 3.5 mW	16	66.7% Yield	18	75 % Yield	SSSD, JFET-PER-02	
Power Needed for 100 % Yield	4.5 mW		4.46 mW		SSSD, JFET-PER-02	
Median Noise at High Power (w/ 100 % Yield)	6.79 nV/rHz		6.73 nV/rHz		SSSD, JFET-PER-01	
Median Gain at High Power	0.98		0.97		NA	
Heater Resistance, 4K Reference value	2.98 kΩ		2.68 kΩ		NA	

Definitions						
Good Channels	:	Noise less than a min. performance value of 15 nV/rHz				
Yield	:	# of Good Channels / 24				

FileNames						
Noise Measurements	:	JFET_Mod13_Noise_perf.pdf				
Source Voltages (RmT, 4K)	:	JFET_Mod13_Source_Voltage_Data.pdf				

Notes						
1) The Base temperature for all performance characterization was 4K						
2) All Noise Measurements were made with the inputs shorted to ground						
3) Type of membranes:		SN033: 67 % Overetched (Solid)			SN039: 30 % Overetched (Perforated)	

Attachment of HRCR Item # 4: RFW (request for waiver)

		RFW/RFD Number:	HR-SP-JPL-RFW-014	
Spacecraft / Project	Herschel	Originator's Name	Steve Tseng	
System / Experiment / Model	1.1 SPIRE	Signature / Date		
Sub-System	detectors	Request Type (Highlight applicable request)	Waiver (RFW)	Deviation (RFD)
Assembly	JFET modules	1.1.1.1 <u>Organisation</u>	Jet Propulsion Laboratory	
Sub-Assembly		Ref. Doc. / Drwg No.	SPIRE-JPL-PRJ-000456	
Item		References		
Serial No.				
RFW/RFD Title	JFET Power Dissipation s/n 013			

End Items(s) Affected (Hardware, Software)		
Name	CI-Number	Model(s)
JFET Module p/n 10209750 s/n 013		PFM

Requirement / Interface Documents Affected				
Specification/Drawing Title	Number	Issue	Date	App. Paragraph
BDA-SSSD	SPIRE-JPL-PRJ-0004456	3.2	7/1/03	JFET-PER-01 JFET-PER-02 JFET-TEC-05

Description of Deviation / Discrepancy / Non-Conformance
 Requirement states that dissipation of photometer JFETs is to be less than 7 mW average, while supplying 90% of channels with voltage noise < 15 nV/rHz according to BDA-SSSD JFET-PER-01, JFET-PER-02, JFET-TEC-05. Measured JFET performance of the JFETs indicates that 7.15 mW of power dissipation will be required to meet the specified yield and noise performance specifications.

Other Items or Requirements (Potentially) Affected
 Overall sensitivity of the bolometer sub-system is affected by JFET noise performance. JFET power dissipation impacts the heat sink temperature of the 3He refrigerator and may in turn increase the base detector temperature. Dissipation of JFETs affects power dissipation on cryostat.

Need for RFW/RFD and Rationale for Acceptance
 Measured JFET performance of JFETs indicates that 7.15 mW of power dissipation will be required to meet the specified yield and noise performance specifications. JPL is unable to significantly alter the JFET fabrication process in order to meet the power specification without undue risk to the stated PFM/FS delivery dates. Furthermore, JPL requests a full system optimisation to revisit the noise and power requirements on the JFETs. The JFET modules can meet the noise design value with 100 % yield at 8.96 mW.

	Approved	Rejected	Name	Date
Engineering:				
Product Assurance:				
CCB-Chairman:				
Principal Investigator				
Product Assurance:				
Co-Investigator				
Prime Contractor				
ESA Project Office				

Attachment of HRCR Item #7: RFW (request for waiver)

RFW/RFD Number:	HR-SP-JPL-RFW-005
------------------------	--------------------------

Spacecraft / Project	Herschel	Originator's Name	Kalyani Sukhatme	
System / Experiment / Model	SPIRE	Signature / Date		
Sub-System	detectors	Request Type (Highlight applicable request)	Waiver (RFW)	Deviation (RFD)
Assembly		Organisation	Jet Propulsion Laboratory	
Sub-Assembly		Ref. Doc. / Drwg No.	SPIRE-JPL-PRJ-000456	
Item		References		
Serial No.				
RFW/RFD Title	BDA and JFET module sine test deletion			

End Items(s) Affected (Hardware, Software)		
Name	CI-Number	Model(s)
Bolometric Detector Assemblies JFET Modules		CQM, PFM, FS CQM, PFM, FS

Requirement / Interface Documents Affected				
Specification/Drawing Title	Number	Issue	Date	App. Paragraph
BDA-SSSD (SPIRE-JPL-PRJ-000456)		3.2	Jan 7, 2003	BDA-DES-10, JFET-DES-07

Description of Deviation / Discrepancy / Non-Conformance
 High Level Sine- Vibe Test is not performed on these units

Other Items or Requirements (Potentially) Affected

Need for RFW/RFD and Rationale for Acceptance
 The hardware has to be qualified under a cold vibration test and is installed in the cold vibration facility for the purpose of the test. The high level sine vibration test configuration will put the hardware and the personnel at risk since the cold vibration facility is not structurally capable of withstanding the high levels. Obtaining additional resources (cost and schedule) for developing a new set-up is not feasible at this time.

	Approved	Rejected	Name	Date
JPL Engineering:				
JPL Product Assurance:				
CCB-Chairman:				
Principal Investigator				
Product Assurance:				
Co-Investigator				
Prime Contractor				
ESA Project Office				

Attachment of HRCR Item #7: ETAS (environmental test summary)

Note: The initial S/N 013 module originally failed test due to a failure on board 10209760-1 S/N 030 (Ref. ETAS No. 035 and a closed PFR No. Z85374). The failed board S/N 030 was subsequently replaced by board 10209760-1 S/N 039 into module S/N 013. Then module S/N 013 was then vibrated and has passed final performance tested (see ETAS No.HS036).

ETAS No. HS036

ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)					
AUTHORIZATION SECTION					
PROJECT Herschel			LOG NO. HS036		
SYSTEM/ASSEMBLY TITLE JFET Modules S/N 13,44				DATE ISSUED 1/06/05	
REFERENCE DESIGNATION NUMBER		PART NO. (IF MULTIPLE, ATTACH LIST) 10209750-1		REV. SERIAL NO. 013, 014 <i>delete 014 1/7/05</i>	
HARDWARE TYPE <input type="checkbox"/> EM QUAL <input checked="" type="checkbox"/> FLIGHT <input type="checkbox"/> FLIGHT SPARE <input type="checkbox"/> OTHER			PRE-ENVIRONMENTAL INSPECTION REPORT NUMBER (ATTACH (R))		
WIRING HARNESS <input type="checkbox"/> EM QUAL <input type="checkbox"/> FLIGHT <input type="checkbox"/> EM <input type="checkbox"/> SE			PART NO.		SERIAL NO.
TEST DESCRIPTION (CHECK ALL APPLICABLE) <input type="checkbox"/> SINE VIBRATION <input type="checkbox"/> PYROSHOCK <input type="checkbox"/> ACOUSTIC <input type="checkbox"/> EMC <input type="checkbox"/> OTHER <input checked="" type="checkbox"/> RANDOM VIBRATION <input checked="" type="checkbox"/> THERMAL VAC. <input type="checkbox"/> THERMAL ATMOSPHERE			TYPE OF TEST <input type="checkbox"/> QUALIFICATION <input type="checkbox"/> FLIGHT ACCEPTANCE <input checked="" type="checkbox"/> PROTO FLIGHT <input checked="" type="checkbox"/> RETEST		
WILL ALL TESTS/LEVELS/DURATIONS REQUIRED BY THE PROJECT DOCUMENTS BE PERFORMED ON THIS UNIT? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) ENTER PROJ. DOC. NO. AND REV. _____					
HAS THE UNIT PASSED ALL PRE-ENVIRONMENTAL FUNCTIONAL TESTS? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION _____					
HAVE ALL DESIGN ANALYSES BEEN COMPLETED AND REQUIRED CHANGES BEEN IMPLEMENTED? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION _____					
IS THE TEST ARTICLE IDENTICAL TO OTHER FLIGHT UNITS? <input type="checkbox"/> YES <input checked="" type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION Stiffeners have been added to the design and included on this unit					
ARE ALL PFRs AGAINST THIS UNIT CLOSED? <input type="checkbox"/> YES <input checked="" type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION PFR's in process of closure. All issues have been addressed and qualified. See PFR # ZB5374					
HAVE ALL WAIVERS AND ECRs BEEN APPROVED AND ARE THEY INCORPORATED? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION _____					
TEST AUTHORIZED BY					
COGNIZANT ENGINEER <i>[Signature]</i>		DATE 1/7/05	TECHNICAL MGR./INSTR MRG./PI PREP REP <i>[Signature]</i>	DATE 1-7-05	ENVIRONMENTAL REQUIREMENTS ENG. <i>[Signature]</i>
SUMMARY SECTION					
TEST AGENCY (IF MULTIPLE, ATTACH SUMMARY AND TEST DATES) JPL Building 144		TEST INITIATION DATE 1/10/04		ACCUMULATED OPERATING HOURS PRIOR TO FIRST ENVIRONMENTAL TEST	
SERIAL NUMBERS ACTUALLY TESTED S/N 013		TEST TERMINATION DATE		OPERATING HOURS DURING ENVIRONMENTAL EXPOSURE	
TEST DESCRIPTION					
VIBRATION AXES: X Y Z SINE VIBRATION <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> RANDOM VIBRATION <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/>		ACOUSTIC <input type="checkbox"/>		PYROSHOCK SHOCK AXES: X Y Z <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> SHOCKS/AXIS: _____	
EMC <input type="checkbox"/> ESD <input type="checkbox"/> COND. SUSC. <input type="checkbox"/> RAD. SUSC.		<input type="checkbox"/> COND. EMIS. <input type="checkbox"/> RAD. EMIS.		<input type="checkbox"/> ISOLATION <input type="checkbox"/> MAGNETICS	
TEMP. LEVEL (°C) AND ACCUMULATED DURATION (HRS.) HOT: _____ °C, _____ h COLD: _____ °C, _____ h HOT: _____ °C, _____ h COLD: _____ °C, _____ h		<input checked="" type="checkbox"/> THERMAL VACUUM PRESSURE: <10E-5 <7K (to R.T.) NO OF CYCLES: 200 100		<input type="checkbox"/> TEMPERATURE ATMOSPHERE <input type="checkbox"/> OTHER	
WERE THERE ANY PFRs GENERATED DURING ENVIRONMENTAL TESTS? <input type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST)			LIST PFR NOS. / BRIEF EXPLANATION		
ARE THE POST ENVIRONMENTAL DAMAGE INSPECTIONS COMPLETE? <input type="checkbox"/> YES <input type="checkbox"/> NO (IF YES, ATTACH A COPY OF THE INSPECTION REPORTS. IF NO, ATTACH EXPLANATION)			LIST PFR NOS. / BRIEF EXPLANATION		
WERE ALL PLANNED TESTS/LEVELS/DURATIONS ACHIEVED? <input type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST)			LIST PFR NOS. / BRIEF EXPLANATION		
<input type="checkbox"/> TESTS HAVE NOT BEEN SUCCESSFULLY COMPLETED. SEE THE ATTACHED SUMMARY FOR ACTIONS THAT NEED TO BE TAKEN.					
COGNIZANT ENGINEER		DATE	TECHNICAL MGR./INSTR MRG./PI PREP REP	DATE	ENVIRONMENTAL REQUIREMENTS ENG. DATE
HARDWARE HAS SUCCESSFULLY COMPLETED THE ENVIRONMENTAL TESTS LISTED ON THIS FORM OR REMAINING ACTIONS HAVE BEEN TAKEN, INCLUDING RETEST.					
COGNIZANT ENGINEER <i>[Signature]</i>		DATE 2/7/05	TECHNICAL MGR./INSTR MRG./PI PREP REP <i>[Signature]</i>	DATE 2/7/05	ENVIRONMENTAL REQUIREMENTS ENG. <i>[Signature]</i>

ETAS No. HS036 (continued)

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ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)

OTHER AUTHORIZATION PROVISIONS AND EXPLANATIONS

This is a 3-axis warm vibration test (room temp) done on the JFET flight modules SN ~~012~~ and 013. The test will be done with the JFET unit mounted inside a mock-up JFET rack. The unit will be assessed both before and after the test with visual inspections and electrical checkouts. 3 response accelerometers will be mounted onto the JFET rack in order to give response data.

2 to 3 vacuum thermal cycles will also be completed.

This unit a 3-axis ambient vibe already completed. An electrical problem was discovered after vibe and PFR # ~~Z85274~~ was generated. The problematic channel was removed from the flight wiring scheme and replaced with a healthy channel. This vibe will act to qualify the unit for flight. This unit, therefore, will see 2x 3axis vibe tests.

Z85374 for additional rework.

ETAS No. HS036 (continued)

ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)		ENVIRONMENTAL TEST SUMMARY				PASS/ FAIL	COMMENTS													
HARDWARE	S/N	ETAS	TEST ENVIRONMENT LEVELS & DURATION	DATE TEST PERFORMED	TEST AGENCY															
SPIRE JFET (10209750-1)	013,01 4	HSO36	<p>X, Y, and Z 1 minute Random Vibe</p> <table border="1"> <thead> <tr> <th>Frequency [Hz]</th> <th>Spec [g².Hz]</th> </tr> </thead> <tbody> <tr> <td>20</td> <td>0.01</td> </tr> <tr> <td>100</td> <td>0.05</td> </tr> <tr> <td>300</td> <td>0.05</td> </tr> <tr> <td>499</td> <td>0.0214</td> </tr> <tr> <td>500</td> <td>0.0214</td> </tr> <tr> <td>2000</td> <td>0.00214</td> </tr> </tbody> </table> <p>Each axis 1/4 g sine sweep 20-2000 Hz each axis</p> <p>2-3 vacuum thermal cycles. <10E-5 mbar, <70K</p>	Frequency [Hz]	Spec [g ² .Hz]	20	0.01	100	0.05	300	0.05	499	0.0214	500	0.0214	2000	0.00214			
Frequency [Hz]	Spec [g ² .Hz]																			
20	0.01																			
100	0.05																			
300	0.05																			
499	0.0214																			
500	0.0214																			
2000	0.00214																			

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ETAS No. HS035

JPL ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)			
AUTHORIZATION SECTION			
PROJECT Herschel		LOG NO. HS035	
SYSTEM/ASSEMBLY TITLE HE JFET Modules S/N 13,14		DATE ISSUED 12/03/04	
REFERENCE DESIGNATION NUMBER	PART NO. (IF MULTIPLE, ATTACH LIST) 10209750-1	REV.	SERIAL NO. 013,014
HARDWARE TYPE <input type="checkbox"/> EM QUAL <input checked="" type="checkbox"/> FLIGHT <input type="checkbox"/> FLIGHT SPARE <input type="checkbox"/> OTHER		PRE-ENVIRONMENTAL INSPECTION REPORT NUMBER (ATTACH IR)	
WIRING HARNESS <input type="checkbox"/> EM QUAL <input type="checkbox"/> FLIGHT <input type="checkbox"/> EM <input type="checkbox"/> SE		PART NO.	SERIAL NO.
TEST DESCRIPTION (CHECK ALL APPLICABLE) <input type="checkbox"/> SINE VIBRATION <input type="checkbox"/> PYROSHOCK <input type="checkbox"/> ACOUSTIC <input type="checkbox"/> EMC <input type="checkbox"/> OTHER _____ <input checked="" type="checkbox"/> RANDOM VIBRATION <input checked="" type="checkbox"/> THERMAL VAC. <input type="checkbox"/> THERMAL ATMOSPHERE		TYPE OF TEST <input type="checkbox"/> QUALIFICATION <input type="checkbox"/> FLIGHT ACCEPTANCE <input checked="" type="checkbox"/> PROTO FLIGHT <input checked="" type="checkbox"/> RETEST	
WILL ALL TESTS/LEVELS/DURATIONS REQUIRED BY THE PROJECT DOCUMENTS BE PERFORMED ON THIS UNIT? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) ENTER PROJ. DOC. NO. AND REV. _____			
HAS THE UNIT PASSED ALL PRE-ENVIRONMENTAL FUNCTIONAL TESTS? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION _____			
HAVE ALL DESIGN ANALYSES BEEN COMPLETED AND REQUIRED CHANGES BEEN IMPLEMENTED? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION _____			
IS THE TEST ARTICLE IDENTICAL TO OTHER FLIGHT UNITS? <input type="checkbox"/> YES <input checked="" type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION Stiffeners have been added to the design and included on this unit			
ARE ALL PFRs AGAINST THIS UNIT CLOSED? <input type="checkbox"/> YES <input checked="" type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION PFRs in process of closure. All issues have been addressed and qualified except for ongoing diagnosis of last two units (12,13)			
HAVE ALL WAIVERS AND ECRs BEEN APPROVED AND ARE THEY INCORPORATED? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION _____			
TEST AUTHORIZED BY			
COGNIZANT ENGINEER <i>[Signature]</i>	DATE 12/3/04	TECHNICAL MGR./INSTR MRG./PI PREP REP <i>[Signature]</i>	ENVIRONMENTAL REQUIREMENTS ENG. DATE 12-3-04
SUMMARY SECTION			
TEST AGENCY (IF MULTIPLE, ATTACH SUMMARY AND TEST DATES) JPL Building 144	TEST INITIATION DATE 12/07/04	ACCUMULATED OPERATING HOURS PRIOR TO FIRST ENVIRONMENTAL TEST	
SERIAL NUMBERS ACTUALLY TESTED	TEST TERMINATION DATE	OPERATING HOURS DURING ENVIRONMENTAL EXPOSURE	
TEST DESCRIPTION			
VIBRATION AXES: X Y Z SINE VIBRATION <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> RANDOM VIBRATION <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/>	ACOUSTIC <input type="checkbox"/>	PYROSHOCK SHOCK AXES: X Y Z <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> SHOCKS/AXIS:	<input checked="" type="checkbox"/> THERMAL VACUUM PRESSURE: <10E-5 <77K NO OF CYCLES: 1000 1 cycle
EMC <input type="checkbox"/> ESD	<input type="checkbox"/> COND. SUSC. <input type="checkbox"/> RAD. SUSC.	<input type="checkbox"/> COND. EMIS. <input type="checkbox"/> RAD. EMIS.	<input type="checkbox"/> TEMPERATURE ATMOSPHERE <input type="checkbox"/> OTHER
WERE THERE ANY PFRs GENERATED DURING ENVIRONMENTAL TESTS? <input type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST)		LIST PFR NOS. / BRIEF EXPLANATION	
ARE THE POST ENVIRONMENTAL DAMAGE INSPECTIONS COMPLETE? <input type="checkbox"/> YES <input type="checkbox"/> NO (IF YES, ATTACH A COPY OF THE INSPECTION REPORTS. IF NO, ATTACH EXPLANATION)		LIST PFR NOS. / BRIEF EXPLANATION	
WERE ALL PLANNED TESTS/LEVELS/DURATIONS ACHIEVED? <input type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST)		LIST PFR NOS. / BRIEF EXPLANATION	
<input type="checkbox"/> TESTS HAVE NOT BEEN SUCCESSFULLY COMPLETED. SEE THE ATTACHED SUMMARY FOR ACTIONS THAT NEED TO BE TAKEN.			
COGNIZANT ENGINEER	DATE	TECHNICAL MGR./INSTR MRG./PI PREP REP	ENVIRONMENTAL REQUIREMENTS ENG. DATE
HARDWARE HAS SUCCESSFULLY COMPLETED THE ENVIRONMENTAL TESTS LISTED ON THIS FORM OR REMAINING ACTIONS HAVE BEEN TAKEN, INCLUDING RETEST.			
COGNIZANT ENGINEER <i>[Signature]</i>	DATE 2/7/05	TECHNICAL MGR./INSTR MRG./PI PREP REP <i>[Signature]</i>	ENVIRONMENTAL REQUIREMENTS ENG. DATE 2-7-05

ETAS No. HS035 (continued)



ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)

OTHER AUTHORIZATION PROVISIONS AND EXPLANATIONS

This is a 3-axis warm vibration test (room temp) done on the JFET flight modules SN⁰¹⁴~~012~~ and 013. The test will be done with the JFET unit mounted inside a mock-up JFET rack. The unit will be assessed both before and after the test with visual inspections and electrical checkouts. 3 response accelerometers will be mounted onto the JFET rack in order to give response data.

2 to 3 vacuum thermal cycles will also be completed.

S/N 14 passed vib and thermal

S/N 013 failed (285374) - problem found during thermal cycle.
Rework to be done & tested (ETAS HS035)

ETAS No. HS035 (continued)

ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)
ENVIRONMENTAL TEST SUMMARY

HARDWARE	S/N	ETAS	TEST ENVIRONMENT LEVELS & DURATION	DATE TEST PERFORMED	TEST AGENCY	PASS/ FAIL	COMMENTS														
SPIRE JFET (10209750-1)	013.01 4	HS035	<p>X, Y, and Z 1 minute Random Vibe</p> <table border="1"> <thead> <tr> <th>Frequency [Hz]</th> <th>Spec [g².Hz]</th> </tr> </thead> <tbody> <tr> <td>20</td> <td>0.01</td> </tr> <tr> <td>100</td> <td>0.05</td> </tr> <tr> <td>300</td> <td>0.05</td> </tr> <tr> <td>499</td> <td>0.0214</td> </tr> <tr> <td>500</td> <td>0.0214</td> </tr> <tr> <td>2000</td> <td>0.00214</td> </tr> </tbody> </table> <p>Each axis 1/4 g sine sweep 20-2000 Hz each axis</p> <p>1 -2-3 vacuum thermal cycles. <10E-5 mbar, <70K</p>	Frequency [Hz]	Spec [g ² .Hz]	20	0.01	100	0.05	300	0.05	499	0.0214	500	0.0214	2000	0.00214				
Frequency [Hz]	Spec [g ² .Hz]																				
20	0.01																				
100	0.05																				
300	0.05																				
499	0.0214																				
500	0.0214																				
2000	0.00214																				

PAGE 3 JPL 2683 R 1/88 FF

Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise For Module 13

JFET SOURCE VOLTAGE MEASUREMENT

Perf Test Post Vibe, post bake, SN13 module, grm dewar, Helium.

Date		1/20/2005		1/20/2005	
T _{plate}		4K		4K	
V _{dd}		3		3	
V _{ss}		-1.5		1.5	
V _{dd'}		2.729		2.688	
V _{ss'}		-1.224		-1.183	
V _{dd}		1.0458		1.204	
V _{ss}		1.0443		1.2029	
SN		33		39	
Channel #			DELTA		DELTA
1	a	0.942	0.007	0.551	0.006
	b	0.949		0.557	
2	a	0.663	0.007	0.779	0.003
	b	0.670		0.782	
3	a	0.786	0.009	1.062	0.005
	b	0.777		1.067	
4	a	1.603	0.014	0.787	0.001
	b	1.589		0.786	
5	a	0.602	0.012	1.001	0.001
	b	0.590		1.002	
6	a	1.274	0.013	0.721	0.005
	b	1.287		0.716	
7	a	0.672	0	0.921	0
	b	0.672		0.921	
8	a	1.215	0.011	0.733	0.002
	b	1.204		0.731	
9	a	1.465	0.006	0.972	0.007
	b	1.459		0.965	
10	a	0.860	0.002	0.544	0.008
	b	0.862		0.536	
11	a	0.679	0.008	0.839	0.001
	b	0.687		0.840	
12	a	0.762	0.002	1.036	0.001
	b	0.764		1.037	
13	a	0.998	0	0.765	0.003
	b	0.998		0.762	
14	a	0.739	0.001	0.281	0.004
	b	0.740		0.285	
15	a	0.710	0.007	0.672	0.002
	b	0.717		0.674	
16	a	0.693	0.002	0.667	0
	b	0.691		0.667	
17	a	0.719	0.002	0.771	0.001
	b	0.721		0.772	
18	a	0.677	0	0.804	0
	b	0.677		0.804	
19	a	0.978	0.006	0.699	0.001
	b	0.972		0.698	
20	a	0.868	0.003	0.713	0.001
	b	0.871		0.712	
21	a	0.679	0.002	0.919	0.004
	b	0.677		0.923	
22	a	0.676	0.002	0.849	0.005
	b	0.678		0.854	
23	a	0.707	0	0.699	0
	b	0.707		0.699	
24	a	0.671	0.002	0.707	0.003
	b	0.673		0.710	

Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise

Board S/N 033 in Module S/N 013

	Pwr1	Pwr2	Pwr3	Pwr4	Pwr5	Pwr5b	Pwr7	Pwr8	Pwr9	Pwr10	Pwr11
Vdd (V)	3	2.9	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8
Vss (V)	-1.5	-1.8	-1.7	-1.6	-1.65	-1.63	-1.55	-1.5	-1.4	-1.45	-1.35
Vdd' (V)	2.718	2.583	2.494	2.5066	2.5006	2.503	2.513	2.519	2.5309	2.5248	2.5369
Vss' (V)	-1.224	-1.488	-1.401	-1.3133	-1.3569	-1.33396	-1.2688	-1.2249	-1.1379	-1.1812	-1.0934
Idd (mA)	1.0864	1.2244	1.1761	1.1292	1.1527	1.1433	1.1056	1.0818	1.0352	1.0583	1.011
Iss (mA)	1.0442	1.1825	1.1342	1.0879	1.111	1.1019	1.0641	1.0407	0.9939	1.0173	0.9699
I (mA)	1.0653	1.20345	1.15515	1.10855	1.13185	1.1226	1.08485	1.06125	1.01455	1.0378	0.99045
P (mW)	4.1994126	4.89924495	4.49930925	4.234550145	4.36611138	4.307371296	4.10268573	3.973213875	3.72218104	3.8460868	3.595630635

Channel Num		Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz
Channel: 1	5.98	7.00	6.85	6.45	7.37	6.53	6.76	6.91	6.45	6.78	7.15
Channel: 2	7.59	6.62	6.46	7.33	7.45	5.50	6.73	7.37	12.20	10.87	13.27
Channel: 3	13.51	7.03	8.49	12.53	9.22	11.33	16.82	20.15	16.74	16.08	14.92
Channel: 4	5.68	4.70	5.02	6.52	5.48	4.91	5.55	6.13	6.02	5.38	6.25
Channel: 5	7.97	7.70	6.89	7.45	7.42	6.36	9.37	10.73	16.26	12.09	21.97
Channel: 6	5.87	5.52	5.52	5.89	5.26	5.80	7.09	6.96	9.42	8.30	12.01
Channel: 7	5.61	6.30	6.06	7.14	6.93	6.12	8.76	7.80	10.10	8.17	13.73
Channel: 8	5.24	5.89	6.48	5.04	5.88	5.94	5.93	5.56	6.01	6.13	5.44
Channel: 9	4.96	5.25	4.56	6.01	5.76	6.20	5.62	7.24	7.92	7.27	8.20
Channel: 10	22.43	7.45	11.04	18.05	14.87	17.01	25.80	30.10	43.71	40.94	43.01
Channel: 11	12.20	11.34	11.67	10.26	12.17	11.67	12.25	11.12	16.01	12.74	18.55
Channel: 12	13.78	9.82	12.77	13.96	13.07	14.28	14.22	13.15	12.18	12.40	9.92
Channel: 13	8.91	6.13	7.25	7.60	6.50	8.39	7.73	10.54	22.91	17.76	29.94
Channel: 14	8.79	13.83	14.76	10.88	11.10	11.31	9.93	8.99	9.33	9.69	8.62
Channel: 15	5.61	5.80	5.87	6.87	4.71	5.97	6.04	5.49	8.23	6.53	7.42
Channel: 16	10.43	8.73	9.23	9.83	9.35	10.60	12.05	12.54	11.45	11.58	15.57
Channel: 17	7.99	6.01	6.73	6.91	5.94	6.90	7.51	6.91	8.28	13.60	10.68
Channel: 18	8.93	6.39	6.10	9.46	7.99	8.53	11.53	11.52	11.26	15.13	10.12
Channel: 19	6.69	6.93	7.31	6.80	6.07	6.67	7.41	6.90	6.95	8.15	8.75
Channel: 20	5.87	6.78	5.35	5.20	6.92	5.55	5.64	5.78	7.54	6.42	9.21
Channel: 21	14.38	7.07	8.35	15.55	9.71	12.22	21.06	25.90	42.32	37.64	49.61
Channel: 22	25.96	8.36	12.77	19.63	18.32	21.40	23.67	37.33	43.57	36.72	45.54
Channel: 23	5.57	6.39	5.78	5.97	6.57	5.58	5.77	7.00	10.38	8.62	10.78
Channel: 24	7.12	7.03	6.30	5.73	6.97	6.98	6.58	6.79	9.48	7.29	8.45
Median	7.78	6.85	6.79	7.24	7.17	6.78	7.62	8.04	10.82	10.18	11.39
Overall Mean	9.46	7.25	7.82	9.05	8.38	8.82	10.41	11.68	15.00	13.47	16.52
Good Mean	8.12	7.25	7.82	7.80	7.94	7.88	8.12	8.34	9.32	8.84	9.64
MP Req'd					15						
Yield	0.92	1.00	1.00	0.88	0.96	0.92	0.83	0.83	0.71	0.75	0.67
# Good Ch.	22	24	24	21	23	22	20	20	17	18	16
# Bad Ch.	2	0	0	3	1	2	4	4	7	6	8

Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise

Board S/N 039 in Module S/N 013

	Pwr1	Pwr2	Pwr3	Pwr4	Pwr5	Pwr5b	Pwr7	Pwr8	Pwr9
Vdd (V)	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8
Vss (V)	-1.5	-1.4	-1.3	-1.2	-1.1	-1.15	-1.17	-1	-1.16
Vdd' (V)	2.479	2.4932	2.5074	2.5218	2.5361	2.529	2.5259	2.5509	2.5276
Vss' (V)	-1.184	-1.099	-1.013	-0.927	-0.841	-0.884	-0.902	-0.755	-0.893
Idd (mA)	1.236	1.1816	1.1264	1.0715	1.0156	1.0438	1.0549	0.9596	1.0495
Iss (mA)	1.1992	1.145	1.0901	1.0352	0.9795	1.0077	1.0188	0.9238	1.0133
I (mA)	1.2176	1.1633	1.10825	1.05335	0.99755	1.02575	1.03685	0.9417	1.0314
P (mW)	4.4600688	4.17880626	3.9014833	3.63279348	3.36882611	3.50088475	3.554218115	3.11316603	3.52800684

Channel Num			Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz
Channel: 1	7.41	9.60	6.33	10.01	10.19	9.07	6.90	14.55	7.79
Channel: 2	6.80	7.59	6.90	9.83	6.16	5.26	7.57	12.43	6.53
Channel: 3	5.31	6.73	8.54	13.49	18.95	15.28	14.78	17.30	16.88
Channel: 4	12.01	12.84	14.70	13.24	16.23	17.53	14.73	15.05	15.17
Channel: 5	9.02	10.94	15.62	21.46	21.38	18.11	16.58	33.71	19.00
Channel: 6	5.61	5.87	8.46	11.76	23.60	17.51	13.36	44.30	15.48
Channel: 7	7.34	8.93	6.29	5.81	8.65	6.88	7.45	15.41	5.78
Channel: 8	6.58	8.64	6.51	7.15	10.23	7.75	8.50	24.61	7.80
Channel: 9	7.01	5.94	6.46	5.71	6.96	7.52	5.60	11.33	6.10
Channel: 10	6.65	8.15	9.62	8.22	8.59	8.16	8.32	14.36	9.36
Channel: 11	6.56	8.20	9.83	13.21	16.03	13.70	10.83	33.50	13.80
Channel: 12	5.54	7.84	6.37	7.41	7.49	6.07	5.83	13.26	8.79
Channel: 13	12.10	14.19	13.11	11.40	16.36	14.21	13.47	20.24	12.53
Channel: 14	6.41	9.14	9.12	8.51	10.66	8.20	7.68	18.11	9.05
Channel: 15	11.78	19.69	36.78	39.73	39.37	43.94	41.28	28.49	41.29
Channel: 16	6.97	7.36	8.62	9.33	9.25	9.86	9.73	13.57	8.87
Channel: 17	9.88	16.83	28.79	46.50	48.22	50.44	54.57	48.85	52.42
Channel: 18	7.40	11.92	6.63	7.25	9.13	7.83	11.20	12.84	9.21
Channel: 19	5.93	11.77	7.53	9.04	10.39	9.93	7.50	13.38	8.15
Channel: 20	5.80	5.69	6.03	9.74	6.80	7.38	8.54	10.42	6.95
Channel: 21	6.60	5.94	6.30	8.89	6.73	7.98	6.51	10.68	9.23
Channel: 22	6.54	6.99	6.15	10.30	9.00	9.57	6.54	16.84	9.30
Channel: 23	7.27	5.16	6.22	13.36	7.58	11.46	10.42	11.37	11.39
Channel: 24	6.40	6.71	5.90	9.10	6.16	7.53	5.72	7.68	6.26
Median	6.73	8.18	7.22	9.79	9.72	9.32	8.52	14.80	9.22
Overall Mean	7.45	9.28	10.28	12.94	13.92	13.38	12.65	19.26	13.21
Good Mean	7.45	8.46	7.89	9.66	8.37	8.80	9.10	12.16	8.72
MP Req'd					15				
Yield	1.00	0.92	0.88	0.88	0.67	0.75	0.88	0.50	0.75
# Good Ch.	24	22	21	21	16	18	21	12	18
# Bad Ch.	0	2	3	3	8	6	3	12	6

Attachment of HRCR Item # 9: SPIRE MIUL Cover Page

MIUL = Material Identification & Utilization List

Declared Materials List and Processes List are not included in this HRCR

Materials and Processes List


SPIRE

JPL D-25725

REV B
1/05/04

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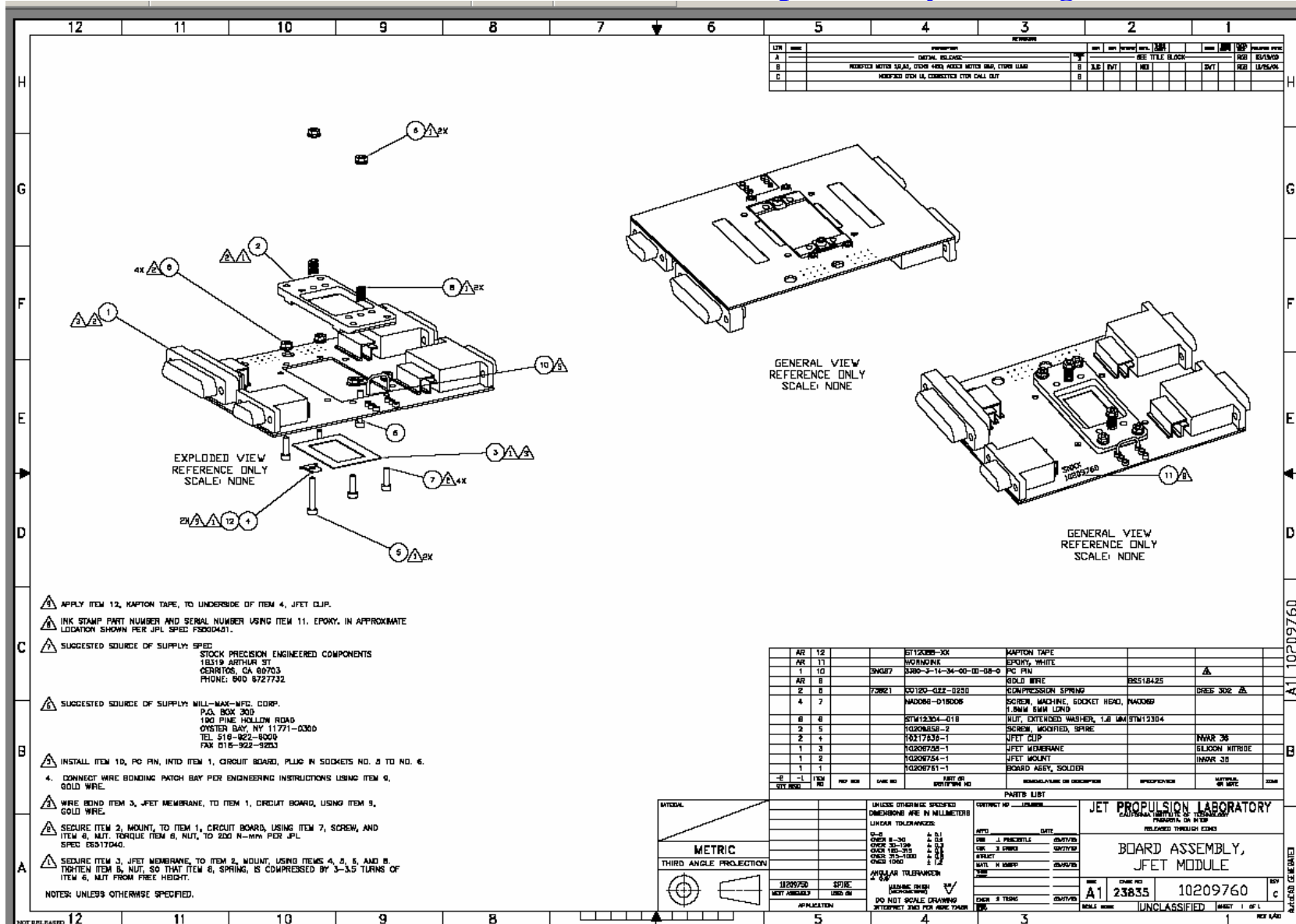
Reviewed by:


M. Knopp M&P Engineer

Attachment of HRCR Item # 11:

**See End of This HRCR Package for
“JFET Module Handling Document”**

Attachment of HRCR Item # 14: JFET Module Top Assembly Drawing 10209750-1



Attachment of HRCR Item # 23: Qualification Compliance Test

Qualification Model JFET Module

EIDP Coveragepage For JFET Testing						
Unit Identification						
Name	:	JFET QM Module				
Part #	:	10209750-1				
S/N	:	#001				
Environmental Testing						
		Axes Tested	Temperature	Duration/# of Cycle	Requirement	Source Waiver
Random Vibration Test		X, Y, Z	100 K	2 min/axis	X, Y, Z	SSSD, JFET-DES-07
High Level Sine Vibe Test		None	NA	NA	X, Y, Z	SSSD, JFET-DES-07 HR-SP-JPL-RFW_005
Bakeout		NA	80 C	72 Hours	80C, 72 Hrs	D-20549
Thermal Cycles		NA	RmT to 80 K	27	Minimum 15	D-20549
Performance Characteristics						
		Specification			Source	Waiver
Power needed for <11 bad channels (Min Perf.)	9.1 mW	11 mW for CQM, 7 mW for PFM/FS			SSSD, JFET-TEC-05, JFET-PER-02	RFW in process
Power needed for <4 bad channels (Design Value)	10.8 mW	11 mW for CQM, 7 mW for PFM/FS			SSSD, JFET-TEC-05, JFET-PER-02	
Power needed for 100 % Yield per unit	13.5 mW	NA			NA	
Median Noise at < 11 bad chs.	7.13 nV/rtHz	<15 nV/rtHz			SSSD, JFET-PER-01	
Median Noise at < 4 bad chs.	6.1 nV/rtHz	Min	<7 nV/rtHz		SSSD, JFET-PER-01	
Median Noise at 100 % Yield.	6.97 nV/rtHz	Performance	Design Value		SSSD, JFET-PER-01	
# of Channels over the max. offset voltage	0	< 15 mV for CQM < 15 mV for PFM/FS			SSSD, BDA-DRCU-27	
Common Mode Rejection Ratio	< -80 dB by design, as measured in EM4 unit				SSSD, BDA-DRCU-11	
Board Level Detail						
		Board SN 001			Source	
# Channels Tested	:	24				
Median Noise at 3.5 mW	:	18 nV/rtHz			SSSD, JFET-PER-01	
# of good channels at 3.5 mW	:	7	29% Yield		SSSD, JFET-PER-02	
Power Needed for 100 % Yield	:	6.75 mW			SSSD, JFET-PER-02	
Median Noise at High Power (w/ 100 % Yield)	:	6.97 nV/rtHz			SSSD, JFET-PER-01	
Median Gain at High Power	:	0.98			NA	
Definitions						
Good Channels	:	Noise less than a min. performance value of 15 nV/rtHz				
Yield	:	# of Good Channels / 24				
Filenames						
Noise Measurements	:	QualJFETPostVibeNoise_Summary.pdf				
Notes						
1) The Base temperature for all performance characterization was 4K						
2) All Noise Measurements were made with the inputs shorted to ground						

Attachment of HRCR Item # 24 & #25: Mate/Demate & Operation Logs (continued)

Hardware ID	FET	S/N	13, 14						
Date	Time	AIDS	Power	Mate	Demate	Transport			Notes
11/24		244404							103 → 158
11/24		"							Pump out
11/26		"							90 to 80°C
11/27		"							turn heat off (25 hr bakeout)
11/28		"							158 → 183
11/30		"	X	X					.5 hr, each board, w/m S.V.
12/3		244448							install into shake facility
12/7		"				X			183 → 144
12/7		"							3 axis warm shake (pump out twice)
12/7		"				X			144 → 183
12/7		244449		X					install photo grn down
12/8		"							pump out, 90 cold
12/9		"	X						4 hrs, brd 36, noise
12/10		"	X						10 hrs, " " "
12/13		"	X						10 hrs, brd 37, noise
12/14		"	X						3 hrs, " " "
12/14		"	X						3 hrs, " " , gain, CMRR
12/14		"	X						3 hrs, brd 36, gain, CMRR
12/17					X	X			183 → 103

Attachment of HRCR Items # 24 & # 25: Mate/Demate & Operation Logs (PWB S/N 033)

OPERATION LOG SHEET -- SPIRE JFET BOARDS MODULE

Mod. 13

USE THE "NOTE" COLUMN TO DESCRIBE ACTIONS
 DEVICE (BRD) S/N: 33 (47) PROJECT: SPIRE/JFET BOARD

DATE	TIME	TECH	PWR ON	PWR OFF	MATE				DEMATE				TRANSFERT	NOTE	
					JAA	JBB	JCC	JDD	JAA	JBB	JCC	JDD			
7-15-04	7:00AM	103199			✓	✓	✓	✓	✓						GND of CHASSIS - SAVER ON
7-19-04		NAN													GND CHASSIS - "
8-16-04	8:00	NAN													GND of CHASSIS "
8-16-04		NAN	✓	✓											SOURCE TEST "
8-22-04		NAN/PW							✓	✓	✓	✓			REMOVE SAVER
8-22-04		NAN			✓	✓	✓	✓	✓	✓	✓	✓			GND of CHASSIS TEST
9-16-04		ST			✓	✓	✓	✓							GND of CHASSIS TEST
9-16-04		ST	✓	✓			✓	✓			✓	✓			SOURCE TEST
9-23-04		ST			✓	✓	✓	✓			✓	✓			GND of CHASSIS
9-23-04		ST	✓	✓			✓	✓	✓	✓	1				SOURCE TEST
10-12-04		NAN			✓	✓	✓	✓			✓	✓			GND of CHASSIS
10-12-04		NAN	✓	✓			✓	✓	✓	✓					SOURCE TEST
11-11-04		NAN			✓	✓	✓	✓			✓	✓			GND of CHASSIS
11-11-04		NAN	✓	✓			✓	✓	✓	✓					SOURCE TEST
11-17-04		NAN			✓	✓	✓	✓			✓	✓			GND of CHASSIS
11-17-04		NAN	✓	✓			✓	✓			✓	✓			SOURCE TEST
12-17-04		NAN			✓	✓	✓	✓	✓		✓	✓			GND of CHASSIS
12-17-04		NAN	✓	✓			✓	✓	✓	✓	✓	✓			SOURCE TEST
1-3-05	7:00	NAN			✓	✓	✓	✓			✓	✓			GND of CHASSIS TEST
1-3-05	8:00	NAN	✓	✓			✓	✓	✓	✓	✓	✓			SOURCE TEST
1-6-05		NAN			✓	✓	✓	✓			✓	✓			GND of CHASSIS
1-6-05		NAN	✓	✓			✓	✓	✓	✓	✓	✓			SOURCE
1-7-05		NAN			✓	✓	✓	✓			✓	✓			GND of CHASSIS
1-7-05		NAN	✓	✓			✓	✓	✓	✓	✓	✓			SOURCE

Attachment of HRCR Items # 24 & # 25: Mate/Demate & Operation Logs (PWB S/N 039)

OPERATION LOG SHEET -- SPIRE JFET BOARDS MODULE

Mod. 13

USE THE "NOTE" COLUMN TO DESCRIBE ACTIONS
 DEVICE (BRD) S/N: 039 (53) PROJECT: SPIRE/JFET BOARD

DATE	TIME	TECH	PWR ON	PWR OFF	MATE				DEMATE				TRANSFERT	NOTE
					JAA	JBB	JCC	JDD	JAA	JBB	JCC	JDD		
9/17/04	8:30 AM	ST.			✓	✓	✓	✓	-	-	-	-		SERVER ON
9/23/04		NAN			-	-	-	-	-	-	-	-		GND/CHASSY TEST
9/23/04		NAN	✓	✓	-	-	-	-	-	-	-	-		SOURCE TEST
11/04/04		NAN			-	-	-	-	-	-	-	-		GND/CHASSY TEST
11/04/04		NAN	✓	✓	-	-	-	-	-	-	-	-		SOURCE TEST
11/11/04	9:45	NAN			✓	✓	✓	✓	✓	✓	✓	✓		REMOVE SERVER BOB.
11/11/04	10:00	NAN			✓	✓	✓	✓	✓	✓	✓	✓		GND & CHASSY TEST
11/11/04		NAN	✓	✓			✓	✓	✓	✓				SOURCE TEST
11/17/04	10:00	NAN			✓	✓	✓	✓			✓	✓		GND & CHASSIS TEST
11/17/04		NAN	✓	✓			✓	✓			✓	✓		SOURCE TEST
12/17/04		NAN			✓	✓	✓	✓			✓	✓		GND & CHASSIS TEST
12/17/04		NAN	✓	✓			✓	✓	✓	✓	✓	✓		SOURCE TEST
1/6/05		NAN			✓	✓	✓	✓			✓	✓		GND & CHASSIS
1/6/05		NAN	✓	✓			✓	✓	✓	✓	✓	✓		SOURCE TEST
1/7/05		NAN			✓	✓	✓	✓			✓	✓		GND & CHASSIS
1/7/05		NAN	✓	✓			✓	✓	✓	✓	✓	✓		SOURCE TEST

Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 2 of 2)

	12	11	10	9	8	7	6	5	4	3	2	1						
H	JAA JFET OUTPUT 1B			JAB JFET OUTPUT 2A			JCC JFET INPUT 1			JDD JFET SERVICE 1			JCD' JFET INPUT 2					
	PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE				
	1	SIGNAL M+		1	SIGNAL M+		1	BIAS V+		1	VSS		1	BIAS V+				
	2	SIGNAL N+		2	SIGNAL N+		2	BIAS V-		2	V+		2	BIAS V-				
	3	SIGNAL P+		3	SIGNAL P+		3	SIGNAL Y+		3	H+		3	SIGNAL Y+				
	4	SIGNAL R+		4	SIGNAL R+		4	SIGNAL W-		4	V-		4	SIGNAL W-				
	5	SIGNAL S+		5	SIGNAL S+		5	SIGNAL V+		5	V-		5	SIGNAL V+				
	6	SIGNAL T+		6	SIGNAL T+		6	SIGNAL T+		6	H+		6	SIGNAL T+				
	7	SIGNAL U-		7	SIGNAL U-		7	SIGNAL S-		7	V+		7	SIGNAL S-				
	8	SIGNAL V-		8	SIGNAL V-		8	SIGNAL P+		8	VSS		8	SIGNAL P+				
	9	SIGNAL W-		9	SIGNAL W-		9	SIGNAL N-		9	BIAS GND		9	SIGNAL N-				
	10	SIGNAL X-		10	SIGNAL X-		10	SIGNAL L-		10	Voh		10	SIGNAL L-				
	11	SIGNAL Y-		11	SIGNAL Y-		11	SIGNAL K+		11	H-		11	SIGNAL K+				
	12	SIGNAL Z-		12	SIGNAL Z-		12	SIGNAL I-		12	CHASSIS GND		12	SIGNAL I-				
	13	FPU GND		13	FPU GND		13	SIGNAL H+		13	H-		13	SIGNAL H+				
	14	SIGNAL M-		14	SIGNAL M-		14	SIGNAL F+		14	Voh		14	SIGNAL F+				
	15	SIGNAL N-		15	SIGNAL N-		15	SIGNAL E-		15	BIAS GND		15	SIGNAL E-				
	16	SIGNAL P-		16	SIGNAL P-		16	SIGNAL C+		JDD' JFET SERVICE 2				16	SIGNAL C+			
	17	SIGNAL R-		17	SIGNAL R-		17	SIGNAL B-		PIN #	PIN PURPOSE		17	SIGNAL B-				
	18	SIGNAL S-		18	SIGNAL S-		18	SIGNAL A-		1	VSS'		18	SIGNAL A-				
	19	SIGNAL T-		19	SIGNAL T-		19	BIAS GND		2	V+		19	BIAS GND'				
	20	SIGNAL U+		20	SIGNAL U+		20	SIGNAL Z+		3	H+		20	SIGNAL Z+				
	21	SIGNAL V+		21	SIGNAL V+		21	SIGNAL X-		4	V-		21	SIGNAL X-				
	22	SIGNAL W+		22	SIGNAL W+		22	SIGNAL W+		5	V-		22	SIGNAL W+				
	23	SIGNAL X+		23	SIGNAL X+		23	SIGNAL U-		6	H+		23	SIGNAL U-				
24	SIGNAL Y+		24	SIGNAL Y+		24	SIGNAL T-		7	V+		24	SIGNAL T-					
25	SIGNAL Z+		25	SIGNAL Z+		25	SIGNAL R+		8	VSS'		25	SIGNAL R+					
G	JBB JFET OUTPUT 1A			JBB' JFET OUTPUT 2B			JCC JFET INPUT 1			JDD JFET SERVICE 1			JCD' JFET INPUT 2					
	PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE				
	1	SIGNAL A+		1	SIGNAL A+		26	SIGNAL P-		9	BIAS GND'		26	SIGNAL P-				
	2	SIGNAL B+		2	SIGNAL B+		27	SIGNAL M+		10	Voh'		27	SIGNAL M+				
	3	SIGNAL C+		3	SIGNAL C+		28	SIGNAL L+		11	H-		28	SIGNAL L+				
	4	SIGNAL D+		4	SIGNAL D+		29	SIGNAL J-		12	CHASSIS GND'		29	SIGNAL J+				
	5	SIGNAL E+		5	SIGNAL E+		30	SIGNAL I+		13	H-		30	SIGNAL I+				
	6	SIGNAL F+		6	SIGNAL F+		31	SIGNAL G-		14	Voh'		31	SIGNAL G-				
	7	SIGNAL G-		7	SIGNAL G-		32	SIGNAL F-		15	BIAS GND'		32	SIGNAL F-				
	8	SIGNAL H-		8	SIGNAL H-		33	SIGNAL D+						33	SIGNAL D+			
	9	SIGNAL I-		9	SIGNAL I-		34	SIGNAL C-						34	SIGNAL C-			
	10	SIGNAL J-		10	SIGNAL J-		35	SIGNAL A+						35	SIGNAL A+			
	11	SIGNAL K-		11	SIGNAL K-		36	SIGNAL Z-						36	SIGNAL Z-			
	12	SIGNAL L-		12	SIGNAL L-		37	SIGNAL Y-						37	SIGNAL Y-			
	13	FPU GND		13	FPU GND		38	SIGNAL X+						38	SIGNAL X+			
	14	SIGNAL A-		14	SIGNAL A-		39	SIGNAL V-						39	SIGNAL V-			
	15	SIGNAL B-		15	SIGNAL B-		40	SIGNAL U+						40	SIGNAL U+			
	16	SIGNAL C-		16	SIGNAL C-		41	SIGNAL S+						41	SIGNAL S+			
	17	SIGNAL D-		17	SIGNAL D-		42	SIGNAL R-						42	SIGNAL R-			
	18	SIGNAL E-		18	SIGNAL E-		43	SIGNAL N+						43	SIGNAL N+			
	19	SIGNAL F-		19	SIGNAL F-		44	SIGNAL M-						44	SIGNAL M-			
	20	SIGNAL G+		20	SIGNAL G+		45	SIGNAL K-						45	SIGNAL K-			
	21	SIGNAL H+		21	SIGNAL H+		46	SIGNAL J+						46	SIGNAL J+			
	22	SIGNAL I+		22	SIGNAL I+		47	SIGNAL H-						47	SIGNAL H-			
	23	SIGNAL J+		23	SIGNAL J+		48	SIGNAL G+						48	SIGNAL G+			
24	SIGNAL K+		24	SIGNAL K+		49	SIGNAL E+						49	SIGNAL E+				
25	SIGNAL L+		25	SIGNAL L+		50	SIGNAL D-						50	SIGNAL D-				
F	JAA JFET OUTPUT 1B			JAB JFET OUTPUT 2A			JCC JFET INPUT 1			JDD JFET SERVICE 1			JCD' JFET INPUT 2					
	PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE				
	1	SIGNAL M+		1	SIGNAL M+		51	SIGNAL B+						51	SIGNAL B+			
	2	SIGNAL N+		2	SIGNAL N+													
	3	SIGNAL P+		3	SIGNAL P+													
	4	SIGNAL R+		4	SIGNAL R+													
	5	SIGNAL S+		5	SIGNAL S+													
	6	SIGNAL T+		6	SIGNAL T+													
	7	SIGNAL U-		7	SIGNAL U-													
	8	SIGNAL V-		8	SIGNAL V-													
	9	SIGNAL W-		9	SIGNAL W-													
	10	SIGNAL X-		10	SIGNAL X-													
	11	SIGNAL Y-		11	SIGNAL Y-													
	12	SIGNAL Z-		12	SIGNAL Z-													
	13	FPU GND		13	FPU GND													
	14	SIGNAL M-		14	SIGNAL M-													
	15	SIGNAL N-		15	SIGNAL N-													
	16	SIGNAL P-		16	SIGNAL P-													
	17	SIGNAL R-		17	SIGNAL R-													
	18	SIGNAL S-		18	SIGNAL S-													
	19	SIGNAL T-		19	SIGNAL T-													
	20	SIGNAL U+		20	SIGNAL U+													
	21	SIGNAL V+		21	SIGNAL V+													
	22	SIGNAL W+		22	SIGNAL W+													
	23	SIGNAL X+		23	SIGNAL X+													
24	SIGNAL Y+		24	SIGNAL Y+														
25	SIGNAL Z+		25	SIGNAL Z+														
E	JAA JFET OUTPUT 1B			JAB JFET OUTPUT 2A			JCC JFET INPUT 1			JDD JFET SERVICE 1			JCD' JFET INPUT 2					
	PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE				
	1	SIGNAL M+		1	SIGNAL M+													
	2	SIGNAL N+		2	SIGNAL N+													
	3	SIGNAL P+		3	SIGNAL P+													
	4	SIGNAL R+		4	SIGNAL R+													
	5	SIGNAL S+		5	SIGNAL S+													
	6	SIGNAL T+		6	SIGNAL T+													
	7	SIGNAL U-		7	SIGNAL U-													
	8	SIGNAL V-		8	SIGNAL V-													
	9	SIGNAL W-		9	SIGNAL W-													
	10	SIGNAL X-		10	SIGNAL X-													
	11	SIGNAL Y-		11	SIGNAL Y-													
	12	SIGNAL Z-		12	SIGNAL Z-													
	13	FPU GND		13	FPU GND													
	14	SIGNAL M-		14	SIGNAL M-													
	15	SIGNAL N-		15	SIGNAL N-													
	16	SIGNAL P-		16	SIGNAL P-													
	17	SIGNAL R-		17	SIGNAL R-													
	18	SIGNAL S-		18	SIGNAL S-													
	19	SIGNAL T-		19	SIGNAL T-													
	20	SIGNAL U+		20	SIGNAL U+													
	21	SIGNAL V+		21	SIGNAL V+													
	22	SIGNAL W+		22	SIGNAL W+													
	23	SIGNAL X+		23	SIGNAL X+													
24	SIGNAL Y+		24	SIGNAL Y+														
25	SIGNAL Z+		25	SIGNAL Z+														
D	JAA JFET OUTPUT 1B			JAB JFET OUTPUT 2A			JCC JFET INPUT 1			JDD JFET SERVICE 1			JCD' JFET INPUT 2					
	PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE				
	1	SIGNAL M+		1	SIGNAL M+													
	2	SIGNAL N+		2	SIGNAL N+													
	3	SIGNAL P+		3	SIGNAL P+													
	4	SIGNAL R+		4	SIGNAL R+													
	5	SIGNAL S+		5	SIGNAL S+													
	6	SIGNAL T+		6	SIGNAL T+													
	7	SIGNAL U-		7	SIGNAL U-													
	8	SIGNAL V-		8	SIGNAL V-													
	9	SIGNAL W-		9	SIGNAL W-													
	10	SIGNAL X-		10	SIGNAL X-													
	11	SIGNAL Y-		11	SIGNAL Y-													
	12	SIGNAL Z-		12	SIGNAL Z-													
	13	FPU GND		13	FPU GND													
	14	SIGNAL M-		14	SIGNAL M-													
	15	SIGNAL N-		15	SIGNAL N-													
	16	SIGNAL P-		16	SIGNAL P-													
	17	SIGNAL R-		17	SIGNAL R-													
	18	SIGNAL S-		18	SIGNAL S-													
	19	SIGNAL T-		19	SIGNAL T-													
	20	SIGNAL U+		20	SIGNAL U+													
	21	SIGNAL V+		21	SIGNAL V+													
	22	SIGNAL W+		22	SIGNAL W+													
	23	SIGNAL X+		23	SIGNAL X+													
24	SIGNAL Y+		24	SIGNAL Y+														
25	SIGNAL Z+		25	SIGNAL Z+														
C	JAA JFET OUTPUT 1B			JAB JFET OUTPUT 2A			JCC JFET INPUT 1			JDD JFET SERVICE 1			JCD' JFET INPUT 2					
	PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE		PIN #	PIN PURPOSE				
	1	SIGNAL M+		1	SIGNAL M+													
	2	SIGNAL N+		2	SIGNAL N+													
	3	SIGNAL P+		3	SIGNAL P+													
	4	SIGNAL R+		4	SIGNAL R+													
	5	SIGNAL S+		5	SIGNAL S+													
	6	SIGNAL T+		6	SIGNAL T+													
	7	SIGNAL U-		7	SIGNAL U-													
	8	SIGNAL V-		8	SIGNAL V-													

Attachment of HRCR Item # 11:

SPIRE

Handling Document

Field Effect Transistor (JFET) Module

10209750-1

Prepared by: Kalyani Sukhatme

10 September, 2003

Hardware Handling Guidelines

Contamination: Open shipment suitcase in a FED-STD-209 Class 10,000 clean room (ISO 14644-1 class 7) or better. Handle hardware with gloves.

ESD: Handle with grounding straps, ESD-safe gloves and ESD smocks at an ESD-safe workstation. Maintain shorting plugs on the unit whenever ESD is a concern. Refer to attached electrical handling document for other important safety precautions.

Fragile: Do not drop or otherwise shock the hardware including the shipping suitcase and container.

Humidity Sensitive: Place hardware in a humidity controlled Class 10,000 clean room. Maintain humidity level at 35%-50% RH typical, for ESD safety.

SPIRE JFET Electrical Handling Document

1	Introduction	1
1.1	Hardware Description	1
2	Handling.....	2
3	Power ON Procedure.....	2
4	Electrical Check-out Test: Characteristic Offset Voltage Measurement.....	3

1. Introduction

This document provides guidelines for electrical handling for the SPIRE JFET Module.

1.1 Hardware Description

Each JFET module has two sets of 24 JFET channels. The JFET channels are populated on 1.0 micron thick Silicon Nitride membranes which provides thermal isolation. The operating temperature for these JFETs is ~120 K. The process of powering up the JFETs dissipates heat into the membrane resulting in a temperature increase with respect to the base temperature (4K to 10 K). Higher the power dissipation, higher is the temperature of the JFETs.

Each JFET channel consists of a matched pair of FETs (Figure 1.1-1) with a requirement for the offset voltage of less than **15 mV** between the matched pair. [The characteristic offset voltage is the difference between the source voltages (V_{sa} and V_{sb} with respect to ground) of the two FETs.]

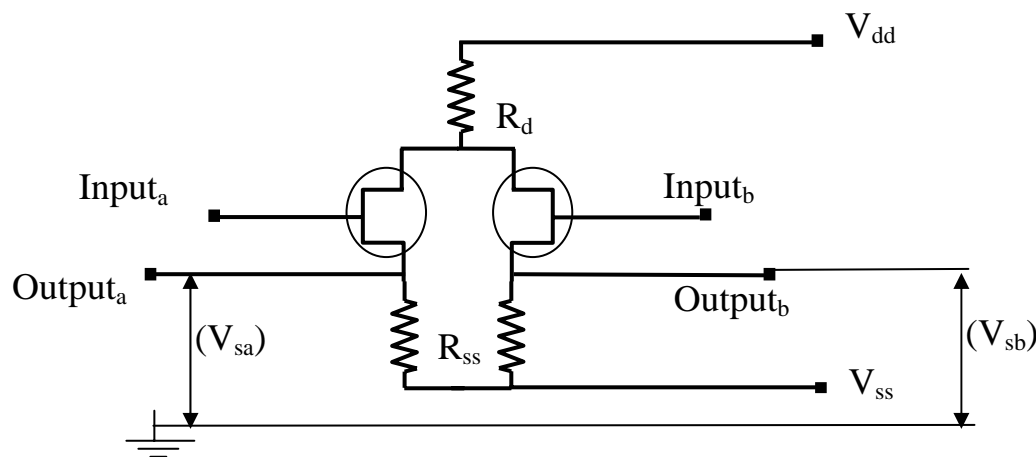


Figure 1.1-1

The Gates of the JFETs are the 'Inputs' of the circuit and the Sources (V_{sa} and V_{sb}) of the JFETs are the outputs, as marked in Figure 1.1-1. V_{dd} and V_{ss} are the power lines for the circuit.

Handling

1. **The JFET Module is Contamination Sensitive:** Handle the unit with Gloves only in a FED-STD-209 Class 100000 clean room (ISO 14644-1 class 7) or better.
2. **The JFET Module is ESD Sensitive:** Please handle with appropriate ESD hardware handling procedures. Handle with grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.
3. **The JFET Module is Fragile:** Please do not drop or otherwise shock the unit. Please DO NOT remove the cover of the JFET Module.

Power ON Procedure

1. The JFET Module should be powered on **WITH the shorting plugs** (JPL Supplied Protection connectors) in place and with the **inputs shorted to ground**. Pins #9 and #15 on the 15-pin MDM connectors on the JFET Module are the bias grounds on the module. These pins should also be shorted to the power supply ground. The unit may be powered up without the shorting plug only when the inputs are connected to the detector system.

Under no circumstances the unit should be powered up without the inputs shorted to ground either via the shorting plug (JPL Supplied) or via the detector system.

2. Do not exceed a voltage of +5 V for the Vdd line and -5 V for the Vss line of the JFET Module.
3. When removing the shorting plugs from the unit for installation into the instrument, please use standard ESD precautions including grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.

Electrical Check-out Test: Characteristic Offset Voltage Measurement

- 1) Verify that the gates of the JFET channels (Inputs) are shorted together and grounded.
- 2) Apply the power supply ground to the bias ground pins on the unit (Pins 9 and 15 on the 15-pin MDM connectors)
- 3) Power on the JFET modules with Vdd = +3 V and Vss = -1.5 V
- 4) Verify that the handheld multimeter is in calibration.
- 5) Connect one side of the handheld multimeter to ground (Power supply ground).
- 6) And measure the voltage with respect to ground of each side (V_{sa} and V_{sb}) of each channel.
- 7) Calculate the characteristic offset voltage (V_{offset}) for each channel (V_{offset}= V_{sa}-V_{sb})
- 8) Compare the values for each of the channels with the specific datasheet provided with the unit.
The datasheets accompanying the unit also provides the values for the drain and source currents for a similar test performed at JPL.

REFER TO MEASURED SOURCE VOLTAGE DATA FOR ACTUAL HARDWARE. Here is an example of the source voltage values and the drain and the source currents obtained for such a test at room temperature are given in the Table 4-1

T, JFET	rm T	
Vdd	3 V	
Vss	-1.5 V	
Idd	1.564 mA	
Iss	1.5686 mA	
Channel #	(V)	DELTA (V)
1	1.130	0
	1.130	
2	1.075	0.001
	1.074	
3	0.781	0.001
	0.780	
4	1.088	0.005
	1.093	
5	0.834	0.001
	0.833	
6	1.012	0.003
	1.015	
7	0.785	0.002
	0.787	
8	1.148	0.004
	1.144	
9	0.753	0
	0.753	

10	0.693	0.008
	0.701	
11	1.110	0.004
	1.114	
12	0.758	0.001
	0.759	
13	0.832	0.002
	0.830	
14	1.264	0.001
	1.265	
15	1.206	0
	1.206	
16	0.818	0.001
	0.819	
17	0.526	0.005
	0.521	
18	1.423	0
	1.423	
19	0.773	0.002
	0.775	
20	0.873	0.004
	0.877	
21	1.387	0.006
	1.393	
22	1.417	0.003
	1.420	
23	0.887	0.002
	0.889	
24	0.888	0.003
	0.891	

- END OF -
Attachment of HRCR Item # 11:
JFET Module Handling Document

END OF
HRCR PACKAGE