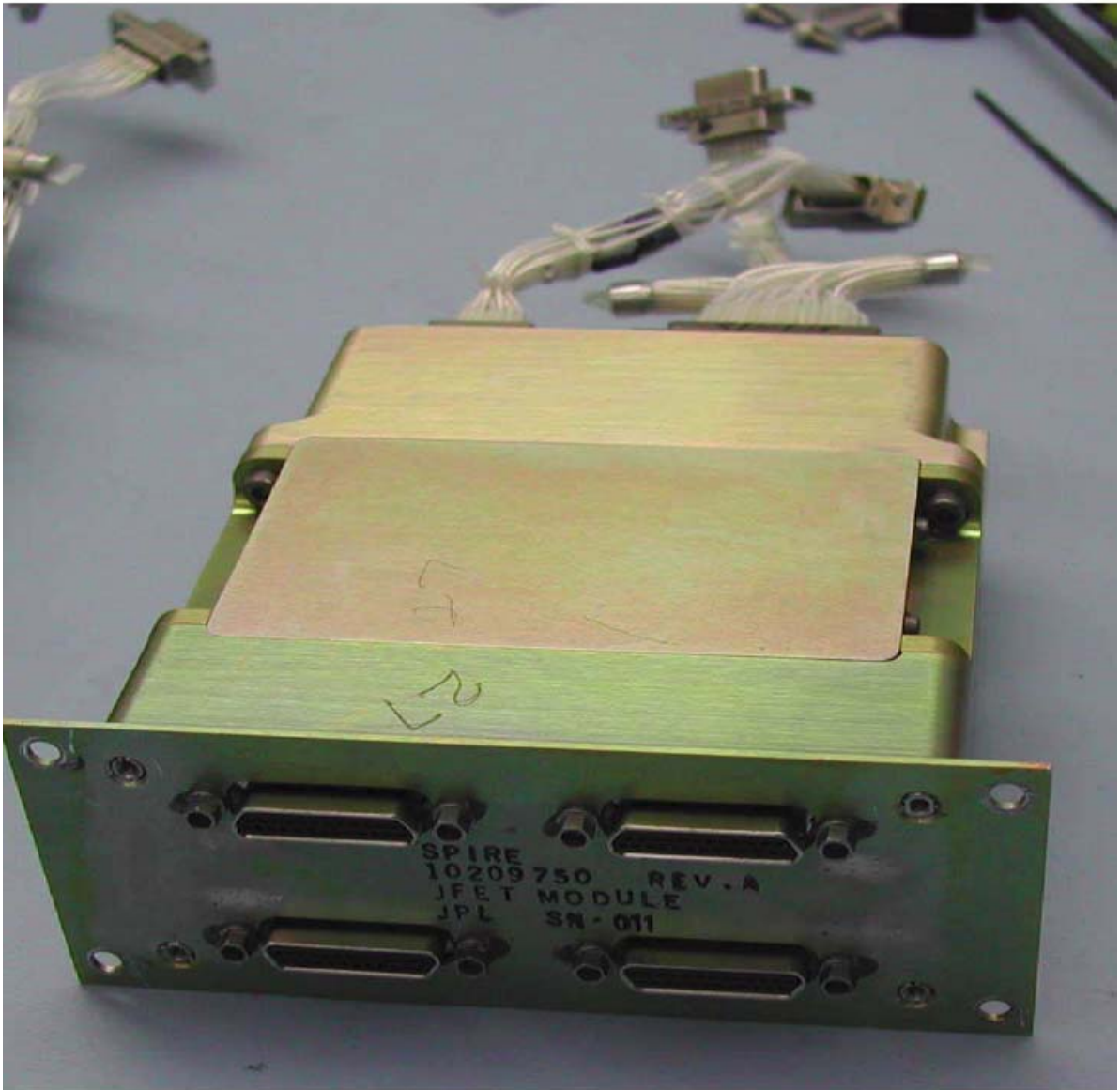


Signed HRCR 1st Page

JPL Hardware Requirements Certification Review – SPIRE Element No. D-30472

Assembly / Subsystem		PEM			Phone		Section		Date
SPIRE		Martin Herman			(818) 354-8541		386		1 November, 2004
Drawing/ Part No.	Dwg. Rev.	Nomenclature			Serial No.	Model	Type	Final IR No.	Mass (Meas. / Req.)
10209750-1	A	JFET Module			011	FLIGHT	N/A	923844	269 gm / 305 gm
Check applicable answer and provide explanation in remarks column		Y	E	N	Remarks		Data Attachments		Signature & Date
1. Are all drawings and specifications complete, approved, released and frozen?		X					14. Latest Top Assembly drawings <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None		Cognizant Engineer Stew Tsey 11/1/04
2. Do the released drawings and specifications reflect all approved changes?		X					15. List of open ECRs <input type="checkbox"/> Attached <input checked="" type="checkbox"/> None		PEM Martin 11/1/04
3. Is hardware identical to other hardware delivered? If no, provide difference list.		X					16. Waivers (RFW request for waiver) <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None		QA Engineer 11/30/04 Jana Valopala
4. Does the hardware meet its functional requirements, specifications, waivers, ICDs?		X			EIDP attached. Also see item # 8 attachments.		17. Open MRB <input type="checkbox"/> Attached <input checked="" type="checkbox"/> None		Environments/Reliability J - 122 11/1/04
5. Are all IR and MRB dispositioned and concurred by QA?		X					18. Open PFR on this H/W <input type="checkbox"/> Attached <input checked="" type="checkbox"/> None		Mission Assurance Mgr. J - 122 11/1/04
6. Is complete as-built list information included in the build book?		X					19. Open PFR on similar H/W <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None		Project Office J - 122 11/1/04
7. Have all required environmental tests & analyses been completed?		X			ETAS attached		20. Handling Document → See Item 11 <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None		PI Martin 11/1/04 JB
8. Is all required assembly and/or subsystem level functional testing complete?		X			Performance Test Data Attached. Also see EIDP in item # 4.		21. Shortage List <input type="checkbox"/> Attached <input checked="" type="checkbox"/> None		
9. Have all piece parts, processes and materials been approved by JPL?		X					22. Requirements Verification Matrix <input checked="" type="checkbox"/> Attached (See #4, #7, #8) <input type="checkbox"/> None		
10. Does this hardware meet all contamination control requirements?		X			Parts, processes and MIUL met all contamination control and out-gassing requirements.		23. Qualification Status <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None		
11. Are all shipping containers, shipping and special handling procedures ready?		X			See Attached Document D-26790		24. Mate / Demate Record <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None		
12. Is additional work required to bring this hardware to flight readiness?			X				25. Operating Log <input checked="" type="checkbox"/> Attached (See Item # 24) <input type="checkbox"/> None		
13. Is this hardware acceptable for flight?		X					26. MICD <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None		

SPIRE JFET Module S/N 011



**RAL EIDP Table of Contents Versus JPL HRCR Check List Item Numbers**

RAL EIDP Section Number	RAL EIDP Title	JPL HRCR Check List Item Number	Notes
1	Shipping Documents		Shipper and Final IR
2	Transportation, Packing, Handling & Integration Procedures	11	Special Handling Document D-26790
3	Certificate of Conformance / Delivery Review Board MOM		HRCR book is the C of C
4	As Built Configuration Status List	1 & 2	Drawing List & Status
5	List of Waivers	4	RFW (request for waiver) Attached
6	Copies of Waivers	4 & 7	RFW (request for waiver) Attached
7	List of Non-Conformance Reports		See RFW in 4 & 7
8	Copies of Non-Conformance Reports		See RFW in 4 & 7
9	Cleanliness Statement		Final IR QA Inspection
10	Operational Manual		NA
11	Top Level Drawings (inc. Family Tree)	14	Top Assembly Drawing
12	Interface Drawings	26	MICD Drawing
13	Functional, Block & Mechanical Drawings		NA
14	Electrical Circuit Drawings		NA
15	Serialized Components List		In build books – not shipped
16	Mass Properties/ Power Budget	HRCR Check List Page 1	Mass listed in HRCR check list
17	Qualification Status List / Test Matrix	23	Qualification Unit Test Matrix
18	Test Reports	4, 7, 8, 23	
19	Open Work / Deferred Work / Open Tests		NA
20	Calibration Data		NA
21	Historical Record	23	Qualification Unit Test Matrix
22	Manufacturing Logbook(s)		In build books – not shipped
23	Operating Time / Cycle Record	25	
24	Connector Mating Record	24	
25	Age Sensitive Items Record		NA
26	Pressure Vessels – History/Test Record		NA
27	Temporary Installation Record		NA
28	Reference List of EIDPs (Lower level)		NA
29	Other Useful Information		NA

JPL Hardware Requirements  
Certification Review (HRCR)

Junction Field Effect Transistor (JFET)  
Flight Module

10209750-1 S/N 011

SPIRE Element  
Herschel Space Observatory Project

November 1, 2004

### Configuration of Modules, Boards & Membranes

Module 10209750-1	S/N 10	S/N 10	S/N 11	S/N 11
PWB 10209760-1	S/N 19	S/N 26	S/N 21	S/N 27
Membrane 10209758-1	J5.5.3	J6.7.5	J5.6.1	J6.7.6

## **Attachment of HRCR Items #1 Drawing Release Status**

### ***ALL ASSEMBLY & PARTS DRAWINGS ARE RELEASED IN PDMS***

#### Released Drawings:

- 10209719-1 assembly built per released Rev. A drawing (studlock)**
- 10209722-1 assembly built per released Rev. B drawing (interface drawing)**
- 10209750-1 assembly built per released Rev. B drawing (module assy)**
- 10209751-1 assembly built per released Rev. B drawing (chassis 1)**
- 10209752-1 assembly built per released Rev. A drawing (chassis 2)**
- 10209753-1 assembly built per released Rev. A drawing (chassis 3)**
- 10209754-1 assembly built per released Rev. C drawing (mount)**
- 10209756-1 assembly built per released Rev. B drawing (chassis lid)**
- 10209757-1 assembly built per released Rev. A drawing (membrane)**
- 10209758-1 assembly built per released Rev. A drawing (membrane assy)**
- 10209759-1,-2,-4 redlined Rev. B drawing (gasket)**
- 10209760-1 assembly built per released Rev. C drawing (board assembly)**
- 10209761-1 assembly built per released Rev. B drawing (solder connector)**
- 10209769-1 assembly built per released Rev. A drawing (stiffener)**
- 10209777-1 assembly built per released Rev. B drawing (board)**
- 10209858-2 assembly built per released Rev. A drawing (special fastener)**
- 10217636-1 assembly built per released Rev. A drawing (clip)**

## Attachment of HRCR Item #4: EIDP

### EIDP Coverage For JFET Testing

Unit Identification							
Name	:	JFET PFM Module					
Part #	:	10209750-1					
S/N	:	#011					
Environmental Testing							
		Axes Tested	Temp	Duration/# of Cycle	Requirement	Source	Waiver
Random Vibration Test		X, Y, Z	Rm T	1 min/axis	X, Y, Z	SSSD, JFET-DES-07	
High Level Sine Vibe Test		None	NA	NA	X, Y, Z	SSSD, JFET-DES-07	HR-SP-JPL-RFW-005
Bakeout		NA	80 C	25.25 hrs	> 24 HRS		
Thermal Cycles		NA	RmT to 80 K	2	Minimum 1	D-20549	
Performance Characteristics							
			<b>Specification</b>		<b>Source</b>		<b>Waiver</b>
Power needed for <11 bad channels (Min Perf.)		8.20 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02		HR-SP-JPL-RFW-004
Power needed for <4 bad channels (Design Value)		8.98 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02		
Power needed for 100 % Yield per unit		9.60 mW	NA		NA		
Median Noise at < 11 bad chs.		8.20 nV/rtHz	<15 nV/rtHz Min Performance	<7 nV/rtHz Design Value	SSSD, JFET-PER-01		
Median Noise at < 4 bad chs.		7.83 nV/rtHz			SSSD, JFET-PER-01		
Median Noise at 100 % Yield.		7.22 nV/rtHz			SSSD, JFET-PER-01		
# of Channels over the max. offset voltage		0	< 15 mV		SSSD, BDA-DRCU-27		
Common Mode Rejection Ratio		< -80 dB by design, as measured in EM4 unit				SSSD, BDA-DRCU-11	
Board Level Details							
		Board SN 021 (JAA'-JDD')		Board SN 027 (JAA'-JDD')		Source	
# Channels Tested	:	24		24			
Median Noise at 3.5 mW	:	22.40 nV/rtHz		13.42 nV/rtHz		SSSD, JFET-PER-01	
# of good channels at 3.5 mW	:	9	37.5% Yield	13	54.2% Yield	SSSD, JFET-PER-02	
Power Needed for 100 % Yield	:	4.78 mW		4.83 mW		SSSD, JFET-PER-02	
Median Noise at High Power (w/ 100 % Yield)		7.77 nV/rtHz		7.09 nV/rtHz		SSSD, JFET-PER-01	
Median Gain at High Power		0.98		0.97		NA	
Heater Resistance, 4K Reference value		3.582 kΩ		2.555 kΩ		NA	
Definitions							
Good Channels	:	Noise less than a min. performance value of 15 nV/rtHz					
Yield	:	# of Good Channels / 24					
Filenames							
Noise Measurements	:	JFET_Module_SN011_Noise_data.pdf					
Source Voltages (RmT, 4K)	:	JFET Module SN010,SN011 source voltage data.pdf					
Notes							
1) The Base temperature for all performance characterization was 4K							
2) All Noise Measurements were made with the inputs shorted to ground							
3) Type of membranes:		SN021: 33% Overetched		SN027: 47% Overetched			

### Attachment of HRCR Item # 4: RFW (request for waiver)

		<b>RFW/RFD Number:</b>	<b>HR-SP-JPL-RFW-TBD</b>	
<b>Spacecraft / Project</b>	Herschel	<b>Originator's Name</b>	Steve Tseng	
<b>System / Experiment / Model</b>	1.1 SPIRE	<b>Signature / Date</b>		
<b>Sub-System</b>	detectors	<b>Request Type</b> (Highlight applicable request)	Waiver (RFW)	Deviation (RFD)
<b>Assembly</b>	JFET modules	1.1.1.1 <u>Organisation</u>	Jet Propulsion Laboratory	
<b>Sub-Assembly</b>		<b>Ref. Doc. / Drwg No.</b>	SPIRE-JPL-PRJ-000456	
<b>Item</b>		<b>References</b>		
<b>Serial No.</b>				
<b>RFW/RFD Title</b>	JFET Power Dissipation s/n 011			

End Item(s) Affected (Hardware, Software)				
Name	CI-Number	Model(s)		
JFET Module p/n 10209750 s/n 011		PFM		
Requirement / Interface Documents Affected				
Specification/Drawing Title	Number	Issue	Date	App. Paragraph
BDA-SSSD	SPIRE-JPL-PRJ-0004456	3.2	7/1/03	JFET-PER-01 JFET-PER-02 JFET-TEC-05
Description of Deviation / Discrepancy / Non-Conformance				
<p>Requirement states that dissipation of photometer JFETs is to be less than 7 mW average, while supplying 90% of channels with voltage noise &lt; 15 nV/rtHz according to BDA-SSSD JFET-PER-01, JFET-PER-02, JFET-TEC-05. Measured JFET performance of the JFETs indicates that 9.60 mW of power dissipation will be required to meet the specified yield and noise performance specifications.</p>				
Other Items or Requirements (Potentially) Affected				
<p>Overall sensitivity of the bolometer sub-system is affected by JFET noise performance. JFET power dissipation impacts the heat sink temperature of the 3He refrigerator and may in turn increase the base detector temperature. Dissipation of JFETs affects power dissipation on cryostat.</p>				
Need for RFW/RFD and Rationale for Acceptance				
<p>Measured JFET performance of JFETs indicates that 9.60 mW of power dissipation will be required to meet the specified yield and noise performance specifications. JPL is unable to significantly alter the JFET fabrication process in order to meet the power specification without undue risk to the stated PFM/FS delivery dates. Furthermore, JPL requests a full system optimisation to revisit the noise and power requirements on the JFETs. The JFET modules can meet the noise design value with 100 % yield at higher dissipation.</p>				
	Approved	Rejected	Name	Date
Engineering:				
Product Assurance:				
CCB-Chairman:				
Principal Investigator				
Product Assurance:				
Co-Investigator				
Prime Contractor				
ESA Project Office				



**Attachment of HRCR Item #7: RFW (request for waiver)**

<b>RFW/RFD Number:</b>	<b>HR-SP-JPL-RFW-005</b>
------------------------	--------------------------

<b>Spacecraft / Project</b>	Herschel	<b>Originator's Name</b>	Kalyani Sukhatme	
<b>System / Experiment / Model</b>	SPIRE	<b>Signature / Date</b>		
<b>Sub-System</b>	detectors	<b>Request Type</b> (Highlight applicable request)	Waiver (RFW)	Deviation (RFD)
<b>Assembly</b>		<b>Organisation</b>	Jet Propulsion Laboratory	
<b>Sub-Assembly</b>		<b>Ref. Doc. / Drwg No.</b>	SPIRE-JPL-PRJ-000456	
<b>Item</b>		<b>References</b>		
<b>Serial No.</b>				
<b>RFW/RFD Title</b>	BDA and JFET module sine test deletion			

End Items(s) Affected (Hardware, Software)		
Name	CI-Number	Model(s)
Bolometric Detector Assemblies JFET Modules		CQM, PFM, FS CQM, PFM, FS

Requirement / Interface Documents Affected				
Specification/Drawing Title	Number	Issue	Date	App. Paragraph
BDA-SSSD (SPIRE-JPL-PRJ-000456)		3.2	Jan 7, 2003	BDA-DES-10, JFET-DES-07

**Description of Deviation / Discrepancy / Non-Conformance**  
 High Level Sine- Vibe Test is not performed on these units

**Other Items or Requirements (Potentially) Affected**

**Need for RFW/RFD and Rationale for Acceptance**  
 The hardware has to be qualified under a cold vibration test and is installed in the cold vibration facility for the purpose of the test. The high level sine vibration test configuration will put the hardware and the personnel at risk since the cold vibration facility is not structurally capable of withstanding the high levels. Obtaining additional resources (cost and schedule) for developing a new set-up is not feasible at this time.

	Approved	Rejected	Name	Date
JPL Engineering:				
JPL Product Assurance:				
CCB-Chairman:				
Principal Investigator				
Product Assurance:				
Co-Investigator				
Prime Contractor				
ESA Project Office				

Attachment of HRCR Item #7: ETAS (environmental test summary)

<b>ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)</b>			
AUTHORIZATION SECTION			
PROJECT Herschel		LOG NO. HS029	
S TEM/ASSEMBLY TITLE S JFET Modules S/N010,011		DATE ISSUED 8/31/04	
REFERENCE DESIGNATION NUMBER	PART NO. (IF MULTIPLE, ATTACH LIST) 10209750-1	REV.	SERIAL NO. 010, 011
HARDWARE TYPE <input type="checkbox"/> EM QUAL <input checked="" type="checkbox"/> FLIGHT <input type="checkbox"/> FLIGHT SPARE <input type="checkbox"/> OTHER		PRE-ENVIRONMENTAL INSPECTION REPORT NUMBER (ATTACH IIR)	
WIRING HARNESS <input type="checkbox"/> EM QUAL <input type="checkbox"/> FLIGHT <input type="checkbox"/> EM <input type="checkbox"/> SE		PART NO.	REV.
TEST DESCRIPTION (CHECK ALL APPLICABLE) <input type="checkbox"/> SINE VIBRATION <input type="checkbox"/> PYROSHOCK <input type="checkbox"/> ACOUSTIC <input type="checkbox"/> EMC <input type="checkbox"/> OTHER _____ <input checked="" type="checkbox"/> RANDOM VIBRATION <input checked="" type="checkbox"/> THERMAL VAC. <input type="checkbox"/> THERMAL ATMOSPHERE		TYPE OF TEST <input type="checkbox"/> QUALIFICATION <input type="checkbox"/> FLIGHT ACCEPTANCE <input checked="" type="checkbox"/> PROTO FLIGHT <input type="checkbox"/> RETEST	
WILL ALL TESTS/LEVELS/DURATIONS REQUIRED BY THE PROJECT DOCUMENTS BE PERFORMED ON THIS UNIT? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST)    ENTER PROJ. DOC. NO. AND REV. _____			
HAS THE UNIT PASSED ALL PRE-ENVIRONMENTAL FUNCTIONAL TESTS? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST)    BRIEF EXPLANATION _____			
HAVE ALL DESIGN ANALYSES BEEN COMPLETED AND REQUIRED CHANGES BEEN IMPLEMENTED? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST)    BRIEF EXPLANATION _____			
IS THE TEST ARTICLE IDENTICAL TO OTHER FLIGHT UNITS? <input type="checkbox"/> YES <input checked="" type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST)    BRIEF EXPLANATION Siffeners have been added to the design and included on this unit			
ARE ALL PFRs AGAINST THIS UNIT CLOSED? <input type="checkbox"/> YES <input checked="" type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST)    BRIEF EXPLANATION PFR's in process of closure. All issues have been addressed and qualified.			
HAVE ALL WAIVERS AND ECRs BEEN APPROVED AND ARE THEY INCORPORATED? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST)    BRIEF EXPLANATION _____			
TEST AUTHORIZED BY			
COGNIZANT ENGINEER <i>R. Sukhrie</i>	DATE 2/3/04	TECHNICAL MGR./INSTR MRG./PI PREP REP <i>Martin H</i>	ENVIRONMENTAL REQUIREMENTS ENG. <i>J-1 ell</i>
SUMMARY SECTION			
TEST AGENCY (IF MULTIPLE, ATTACH SUMMARY AND TEST DATES) JPL Building 144	TEST INITIATION DATE 8/31/04	ACCUMULATED OPERATING HOURS PRIOR TO FIRST ENVIRONMENTAL TEST	
SERIAL NUMBERS ACTUALLY TESTED S/N 010, 011	TEST TERMINATION DATE 10/26/04	OPERATING HOURS DURING ENVIRONMENTAL EXPOSURE	
TEST DESCRIPTION			
VIBRATION AXES: X Y Z SINE VIBRATION <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> RANDOM VIBRATION <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/>	ACOUSTIC <input type="checkbox"/>	PYROSHOCK SHOCK AXES: X Y Z SHOCKS/AXIS: <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	<input checked="" type="checkbox"/> THERMAL VACUUM PRESSURE: <10E-5 <77K NO OF CYCLES: 2 → ← 3 <input type="checkbox"/> TEMPERATURE ATMOSPHERE <input type="checkbox"/> OTHER
EMC <input type="checkbox"/> ESD <input type="checkbox"/> COND. SUSC. <input type="checkbox"/> RAD. SUSC. <input type="checkbox"/> COND. EMIS. <input type="checkbox"/> RAD. EMIS.	<input type="checkbox"/> ISOLATION <input type="checkbox"/> MAGNETICS	TEMP. LEVEL (°C) AND ACCUMULATED DURATION (HRS.) HOT: 37 °C, _____ h    COLD: 4K _____ h HOT: _____ °C, _____ h    COLD: _____ °C, _____ h	
WERE THERE ANY PFRs GENERATED DURING ENVIRONMENTAL TESTS? <input type="checkbox"/> YES <input checked="" type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST)		LIST PFR NOS. / BRIEF EXPLANATION	
ARE THE POST ENVIRONMENTAL DAMAGE INSPECTIONS COMPLETE? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF YES, ATTACH A COPY OF THE INSPECTION REPORTS. IF NO, ATTACH EXPLANATION)		LIST PFR NOS. / BRIEF EXPLANATION	
WERE ALL PLANNED TESTS/LEVELS/DURATIONS ACHIEVED? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST)		LIST PFR NOS. / BRIEF EXPLANATION	
<input type="checkbox"/> TESTS HAVE NOT BEEN SUCCESSFULLY COMPLETED. SEE THE ATTACHED SUMMARY FOR ACTIONS THAT NEED TO BE TAKEN.			
COGNIZANT ENGINEER	DATE	TECHNICAL MGR./INSTR MRG./PI PREP REP	ENVIRONMENTAL REQUIREMENTS ENG.
HARDWARE HAS SUCCESSFULLY COMPLETED THE ENVIRONMENTAL TESTS LISTED ON THIS FORM OR REMAINING ACTIONS HAVE BEEN TAKEN, INCLUDING RETEST.			
COGNIZANT ENGINEER <i>RLW</i>	DATE 10/27/04	TECHNICAL MGR./INSTR MRG./PI PREP REP <i>Martin H</i>	ENVIRONMENTAL REQUIREMENTS ENG. <i>R. J. Penner</i>

**Attachment of HRCR Item #7: ETAS (environmental test summary)**



**ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)**

**OTHER AUTHORIZATION PROVISIONS AND EXPLANATIONS**

1 is a 3-axis warm vibration test (room temp) done on the JFET flight modules SN010 and 011. The test will be done with the JFET unit mounted inside a mock-up JFET rack. The unit will be assessed both before and after the test with visual inspections and electrical checkouts. 3 response accelerometers will be mounted onto the JFET rack in order to give response data.

2 to 3 vacuum thermal cycles will also be completed.

Attachment of HRCR Item #7: ETAS (environmental test summary)

ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)		ENVIRONMENTAL TEST SUMMARY				PASS/ FAIL	COMMENTS													
HARDWARE	S/N	ETAS	TEST ENVIRONMENT LEVELS & DURATION	DATE TEST PERFORMED	TEST AGENCY															
SPIRE JFET (10209750-1)	010, 011	HSO29	<p>X, Y, and Z 1 minute Random Vibe</p> <table border="1"> <thead> <tr> <th>Frequency [Hz]</th> <th>Spec [g<sup>2</sup>.Hz]</th> </tr> </thead> <tbody> <tr> <td>20</td> <td>0.01</td> </tr> <tr> <td>100</td> <td>0.05</td> </tr> <tr> <td>300</td> <td>0.05</td> </tr> <tr> <td>499</td> <td>0.0214</td> </tr> <tr> <td>500</td> <td>0.0214</td> </tr> <tr> <td>2000</td> <td>0.00214</td> </tr> </tbody> </table> <p>Each axis 1/4 g sine sweep 20-2000 Hz each axis</p> <p>2-3 vacuum thermal cycles. &lt;10E-5 mbar, &lt;70K</p>	Frequency [Hz]	Spec [g <sup>2</sup> .Hz]	20	0.01	100	0.05	300	0.05	499	0.0214	500	0.0214	2000	0.00214			
Frequency [Hz]	Spec [g <sup>2</sup> .Hz]																			
20	0.01																			
100	0.05																			
300	0.05																			
499	0.0214																			
500	0.0214																			
2000	0.00214																			

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## Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise For Module 10 & 11

### JFET SOURCE VOLTAGE MEASUREMENT

Post Vibe, post bake, SN10,11 module, Post Perf test, Thermal Cycle to 4K grn dewar.

power cable		pwr1	pwr2	pwr4 (this was flipped		pwr3	
Date		10/8/2004	10/8/2004	10/8/2004	10/8/2004	10/8/2004	10/8/2004
T. plate		4K	4K	4K	4K	4K	4K
Vdd		3	3	3	3	3	3
Vss		-1.5	1.5	-1.5	-1.5	-1.5	-1.5
Vdd		1.4238	1.5263	1.0078	1.0078	1.51	1.51
Vss		1.4221	1.5244	1.0059	1.0059	1.5082	1.5082
SN		19	28	21	21	27	27
Channel #			DELTA		DELTA		DELTA
1	a	0.751	0.005	0.687	0.004	0.677	0.001
	b	0.756		0.691		0.676	0.001
2	a	0.284	0.01	0.893	0.004	0.658	0.001
	b	0.254		0.897		0.657	0.001
3	a	0.894	0.009	0.729	0.005	1.216	0.009
	b	0.903		0.734		1.225	0.009
4	a	0.716	0.003	0.702	0	0.910	0.002
	b	0.719		0.702		0.908	0.002
5	a	1.171	0.008	0.504	0.004	0.671	0.004
	b	1.179		0.500		0.675	0.004
6	a	0.546	0.002	0.728	0.002	0.651	0.003
	b	0.548		0.728		0.654	0.003
7	a	0.578	0.003	0.716	0	1.000	0.006
	b	0.581		0.716		0.994	0.006
8	a	0.708	0.002	0.554	0.0016	0.750	0.003
	b	0.708		0.558		0.753	0.003
9	a	0.954	0.009	0.780	0	0.924	0.007
	b	0.963		0.780		0.917	0.007
10	a	0.372	0.003	0.656	0.002	0.675	0.003
	b	0.369		0.654		0.678	0.003
11	a	0.300	0.006	0.756	0.001	0.959	0.014
	b	0.306		0.756		0.945	0.014
12	a	0.431	0.003	0.705	0.001	1.028	0.002
	b	0.434		0.704		1.030	0.002
13	a	0.485	0.003	0.983	0.009	0.683	0.004
	b	0.488		0.992		0.687	0.004
14	a	0.577	0.005	0.923	0	1.197	0.002
	b	0.582		0.923		1.195	0.002
15	a	0.891	0.004	0.587	0.003	0.679	0.002
	b	0.895		0.590		0.677	0.002
16	a	0.692	0.001	0.785	0.005	0.653	0
	b	0.691		0.780		0.653	0
17	a	0.732	0	0.683	0.002	0.682	0.004
	b	0.732		0.681		0.678	0.004
18	a	1.316	0.01	0.880	0.002	1.053	0.007
	b	1.326		0.882		1.080	0.007
19	a	0.554	0.006	0.946	0.004	1.182	0.009
	b	0.549		0.942		1.191	0.009
20	a	0.603	0.001	0.600	0.001	0.969	0.001
	b	0.602		0.601		0.968	0.001
21	a	0.962	0	0.927	0.001	0.993	0.002
	b	0.962		0.926		0.991	0.002
22	a	1.244	0.009	0.913	0	1.303	0.01
	b	1.253		0.913		1.293	0.01
23	a	1.343	0.01	0.738	0.004	1.329	0.004
	b	1.333		0.742		1.333	0.004
24	a	1.312	0.014	0.704	0.01	1.607	0.012
	b	1.298		0.694		1.595	0.012

## Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise

### Board S/N 021 in Module S/N 011

	Pwr1	Pwr2	Pwr3	Pwr4	Pwr5	Pwr6	Pwr7	Pwr8
Vdd (V)	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5
Vss (V)	-1.85	-1.9	-1.8	-1.7	-1.6	-1.65	-1.75	-1.3
Vdd' (V)	2.429	2.428	2.43	2.43	2.435	2.435	2.431	2.443
Vss' (V)	-1.777	-1.826	-1.729	-1.631	-1.535	-1.583	-1.68	-1.242
Idd (mA)	1.1924	1.2137	1.1713	1.1289	1.0863	1.1075	1.15	0.9558
Iss (mA)	1.1473	1.1685	1.1262	1.084	1.0415	1.0627	1.1051	0.9119
I (mA)	1.16985	1.1911	1.14875	1.10645	1.0639	1.0851	1.12755	0.93385
P (mW)	4.9203891	5.0669394	4.77765125	4.49329345	4.223683	4.3599318	4.63535805	3.44123725

Channel Num			Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz
Channel: 1	14.55	8.04	8.33	11.08	13.74	13.61	8.68	25.38
Channel: 2	11.25	7.39	5.93	6.17	9.03	6.69	6.15	13.19
Channel: 3	12.15	12.27	13.91	12.40	15.67	12.19	13.34	17.75
Channel: 4	7.51	6.02	5.95	5.88	6.88	4.84	6.39	22.90
Channel: 5	8.64	6.96	6.68	6.68	6.63	5.60	6.89	21.89
Channel: 6	10.12	5.95	7.88	11.66	15.85	13.71	9.34	25.19
Channel: 7	6.92	8.35	8.19	7.77	7.81	7.70	8.75	9.19
Channel: 8	8.75	7.10	6.94	6.57	8.08	8.29	7.69	14.19
Channel: 9	7.69	6.88	6.80	9.10	10.63	9.51	7.09	10.63
Channel: 10	8.20	5.49	6.57	8.49	13.63	10.16	7.75	30.66
Channel: 11	11.92	12.78	12.44	8.70	9.17	10.00	8.33	31.37
Channel: 12	10.52	9.88	9.05	17.97	26.00	23.22	14.30	23.49
Channel: 13	16.59	14.36	12.45	9.73	10.12	10.67	13.52	17.90
Channel: 14	11.99	10.33	12.46	17.71	17.47	16.32	16.43	23.60
Channel: 15	11.67	7.20	7.67	7.51	11.68	9.61	10.15	73.18
Channel: 16	9.78	5.92	6.72	8.41	8.20	7.67	8.08	11.80
Channel: 17	10.86	5.91	5.87	6.23	6.60	6.75	5.16	8.22
Channel: 18	10.65	7.13	7.27	8.44	7.32	8.61	7.45	11.16
Channel: 19	9.85	8.24	9.47	19.02	32.05	24.72	15.27	40.58
Channel: 20	7.85	8.26	8.72	15.95	28.38	23.31	10.64	69.65
Channel: 21	7.06	7.73	7.89	10.51	18.85	15.78	9.00	42.23
Channel: 22	8.31	9.02	8.72	10.15	7.86	7.68	8.16	13.88
Channel: 23	6.85	4.95	6.26	6.65	5.69	7.41	7.16	11.25
Channel: 24	7.97	7.77	6.38	8.75	8.38	7.12	6.25	44.20
<b>Median</b>	9.81	7.56	7.77	8.72	9.65	9.56	8.25	22.40
<b>Overall Mean</b>	9.90	8.08	8.27	10.06	12.74	11.30	9.25	25.56
<b>Good Mean</b>	9.61	8.08	8.27	8.54	8.91	8.83	8.65	11.50
MP Req'd					15			
Yield	0.96	1.00	1.00	0.83	0.71	0.79	0.92	0.38
# Good Ch.	23	24	24	20	17	19	22	9
# Bad Ch.	1	0	0	4	7	5	2	15

JFET\_Mod11\_brd21\_Noise\_perf.xls

## Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise

### Board S/N 027 in Module S/N 011

	Pwr10	Pwr11	Pwr12	Pwr13	Pwr14	Pwr15	Pwr16	Pwr17	Pwr18	Pwr19	Pwr20	Pwr20
Vdd (V)	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5
Vss (V)	-1.39	-1.37	-1.35	-1.3	-1.25	-1.1	-1.07	-1	-1.15	-0.9	-0.97	-1.2
Vdd' (V)	2.413	2.414	2.414	2.417	2.418	2.424	2.426	2.429	2.422	2.433	2.43	2.42
Vss' (V)	-1.302	-1.283	-1.263	-1.215	-1.167	-1.023	-0.994	-0.927	-1.072	-0.831	-0.899	-1.119
Idd (mA)	1.4617	1.4483	1.4344	1.4006	1.3666	1.2638	1.2432	1.1949	1.2986	1.1253	1.1744	1.3326
Iss (mA)	1.4204	1.4071	1.3931	1.3594	1.3257	1.2233	1.2027	1.1547	1.2579	1.0852	1.1342	1.2918
I (mA)	1.44105	1.4277	1.41375	1.38	1.34615	1.24355	1.22295	1.1748	1.27825	1.10525	1.1543	1.3122
P (mW)	5.35350075	5.2782069	5.19835875	5.01216	4.82594775	4.28651685	4.182489	3.9426288	4.4662055	3.607536	3.8426647	4.6438758

Channel Num	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz
Channel: 1	7.40	9.32	9.54	7.86	7.90	5.91	7.02	7.10	7.35	9.22	7.05	7.96
Channel: 2	5.94	6.24	7.87	5.28	6.35	8.29	6.93	7.94	6.56	7.06	6.63	6.17
Channel: 3	8.99	9.21	10.39	11.28	11.83	9.67	10.29	7.99	10.84	7.77	7.09	11.55
Channel: 4	6.10	6.80	6.54	6.09	5.69	7.61	5.97	6.14	6.42	9.61	8.87	4.44
Channel: 5	8.53	8.10	8.86	11.13	12.59	34.03	41.59	62.16	24.00	64.70	80.07	17.56
Channel: 6	9.33	7.37	8.86	8.69	4.84	7.04	6.66	6.05	8.01	8.19	6.28	6.46
Channel: 7	7.17	7.73	7.49	7.37	9.00	33.25	42.37	68.85	21.22	110.04	82.81	14.80
Channel: 8	9.50	8.78	8.47	7.49	7.82	6.81	7.21	6.44	7.21	6.86	6.50	8.80
Channel: 9	5.57	6.72	6.34	6.52	8.16	16.00	20.60	37.92	10.93	41.64	39.67	8.17
Channel: 10	5.40	6.60	7.00	6.01	5.16	5.45	5.23	5.93	6.89	6.77	7.05	5.67
Channel: 11	7.76	8.51	9.30	6.05	6.73	6.94	6.75	6.92	7.66	10.74	9.36	7.52
Channel: 12	6.63	7.43	6.55	7.56	7.46	8.00	7.80	12.05	7.72	29.18	11.83	7.75
Channel: 13	4.84	6.13	6.55	6.09	6.11	8.40	8.12	12.01	6.80	37.53	15.72	6.06
Channel: 14	7.50	5.59	6.25	7.60	6.04	9.39	8.83	15.17	8.82	33.64	17.57	6.69
Channel: 15	8.69	7.48	8.32	7.83	7.17	8.28	8.07	10.25	7.92	17.73	13.61	6.57
Channel: 16	6.78	6.54	7.17	8.57	7.02	6.53	7.86	9.93	7.40	24.35	12.83	6.88
Channel: 17	7.98	6.70	6.80	6.76	6.16	7.27	6.57	7.34	7.28	15.95	9.31	8.22
Channel: 18	6.34	7.70	7.25	6.80	6.47	7.65	6.84	7.11	6.41	14.20	8.99	6.30
Channel: 19	8.95	8.73	6.28	6.76	7.50	7.07	8.27	7.69	5.87	11.98	9.16	7.68
Channel: 20	7.15	5.45	6.68	6.25	6.74	7.03	6.91	11.20	4.91	28.15	14.67	5.91
Channel: 21	8.65	7.64	7.17	9.46	8.59	16.99	17.95	20.70	11.81	12.64	19.65	10.58
Channel: 22	6.98	6.09	5.02	7.14	6.34	4.90	6.57	6.62	5.59	10.10	6.86	6.00
Channel: 23	9.99	7.91	9.49	9.06	8.01	7.46	8.33	7.12	6.23	9.28	7.03	7.47
Channel: 24	7.49	6.93	6.16	8.24	7.17	9.75	8.09	12.35	7.75	16.83	14.58	8.50
Median	7.45	7.40	7.17	7.43	7.09	7.63	7.83	7.96	7.38	13.42	9.34	7.49
Overall Mean	7.49	7.32	7.51	7.58	7.37	10.41	11.28	15.12	8.82	22.67	17.63	8.07
Good Mean	7.49	7.32	7.51	7.58	7.37	7.47	7.41	8.32	7.56	9.57	9.32	7.66
MP Reqd												
Yield	1.00	1.00	1.00	1.00	1.00	0.83	0.83	0.79	0.92	0.54	0.75	0.96
# Good Ch.	24	24	24	24	24	20	20	19	22	13	18	23
# Bad Ch.	0	0	0	0	0	4	4	5	2	11	6	1

JFET\_Mod11\_brd27\_Noise\_perf.xls

## Attachment of HRCR Item # 9: SPIRE MIUL Cover Page

MIUL = Material Identification & Utilization List

### Materials and Processes List

SPIRE

JPL D-25725

REV B  
1/05/04

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Reviewed by:

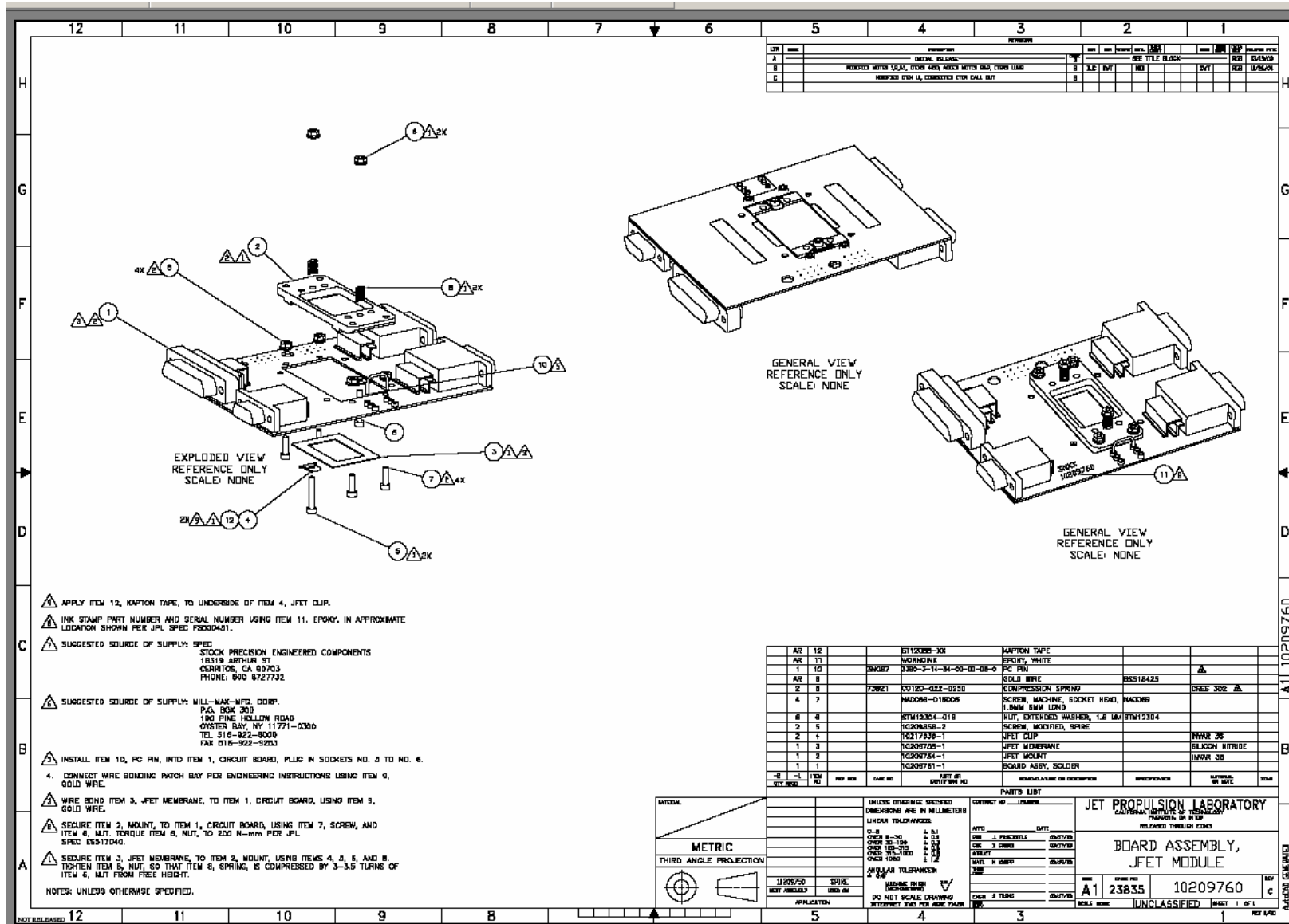
  
M. Knopp M&P Engineer



**Attachment of HRCR Item # 11:**

**See End of This HRCR Package for  
“JFET Module Handling Document”**

### Attachment of HRCR Item # 14: JFET Module Top Assembly Drawing 10209750-1



**Attachment of HRCR Item # 19:**

**Open PFR on Similar Hardware**

<b>PFR</b>	<b>Z82995</b>
<b>PFR</b>	<b>Z82997</b>
<b>PFR</b>	<b>Z82999</b>
<b>PFR</b>	<b>Z83353</b>
<b>PFR</b>	<b>Z83666</b>
<b>PFR</b>	<b>Z83673</b>
<b>PFR</b>	<b>Z84063</b>
<b>PFR</b>	<b>Z84064</b>

## Attachment of HRCR Item # 23: Qualification Compliance Test

### Qualification Model JFET Module

EIDP Coveragepage For JFET Testing						
<b>Unit Identification</b>						
Name	:	JFET QM Module				
Part #	:	10209750-1				
S/N	:	#001				
<b>Environmental Testing</b>						
		<b>Axes Tested</b>	<b>Temperature</b>	<b>Duration/# of Cycle</b>	<b>Requirement</b>	<b>Source</b> Waiver
Random Vibration Test		X, Y, Z	100 K	2 min/axis	X, Y, Z	SSSD, JFET-DES-07
High Level Sine Vibe Test		None	NA	NA	X, Y, Z	SSSD, JFET-DES-07 HR-SP-JPL- RFW_005
Bakeout		NA	80 C	72 Hours	80C, 72 Hrs	D-20549
Thermal Cycles		NA	RmT to 80 K	27	Minimum 15	D-20549
<b>Performance Characteristics</b>						
			<b>Specification</b>		<b>Source</b>	<b>Waiver</b>
Power needed for <11 bad channels (Min Perf.)	9.1 mW		11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	RFW in process
Power needed for <4 bad channels (Design Value)	10.8 mW		11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	
Power needed for 100 % Yield per unit	13.5 mW		NA		NA	
Median Noise at < 11 bad chs.	7.13 nV/rtHz	<15 nV/rtHz			SSSD, JFET-PER-01	
Median Noise at < 4 bad chs.	6.1 nV/rtHz	Min		<7 nV/rtHz	SSSD, JFET-PER-01	
Median Noise at 100 % Yield.	6.97 nV/rtHz	Performance		Design Value	SSSD, JFET-PER-01	
# of Channels over the max. offset voltage	0	< 15 mV for CQM < 15 mV for PFM/FS			SSSD, BDA-DRCU-27	
Common Mode Rejection Ratio	< -80 dB by design, as measured in EM4 unit				SSSD, BDA-DRCU-11	
<b>Board Level Detail</b>						
		<b>Board SN 001</b>			<b>Source</b>	
# Channels Tested	:	24				
Median Noise at 3.5 mW	:	18 nV/rtHz			SSSD, JFET-PER-01	
# of good channels at 3.5 mW	:	7	29% Yield		SSSD, JFET-PER-02	
Power Needed for 100 % Yield	:	6.75 mW			SSSD, JFET-PER-02	
Median Noise at High Power (w/ 100 % Yield)	:	6.97 nV/rtHz			SSSD, JFET-PER-01	
Median Gain at High Power	:	0.98			NA	
<b>Definitions</b>						
Good Channels	:	Noise less than a min. performance value of 15 nV/rtHz				
Yield	:	# of Good Channels / 24				
<b>Filenames</b>						
Noise Measurements	:	QualJFETPostVibeNoise_Summary.pdf				
<b>Notes</b>						
1) The Base temperature for all performance characterization was 4K						
2) All Noise Measurements were made with the inputs shorted to ground						

Attachment of HRCR Item # 24 & #25: Mate/Demate & Operation Logs

Hardware ID	JFET	Module	S/N	10,11	SHT 1			
Date	Time	AIDS	Power	Mate	Demate	Transport	Notes	
9/7/04	3P	243694				x	103 → 158	
9/8	10A	"					run out, thermal cycle	
9/10	730A	"				x	158 → 183	
9/10	12P	"	x	x			.5 hr each brd, warm s.v.	
9/16	9A	243695				x	183 → 144 shake	
9/16	3P	"				x	144 → 183	
9/21	8A		x				8 hrs, brd 19, noise	
9/22	"		x				" " "	
9/23	"		x				1 hr, brd 19, noise	
9/23	"		x				7 hr, brd 26, noise	
9/26	"		x				8 hr, " "	
9/27	"		x				4 hr, " "	
10/31	"		x				8 hr, brd 21	
9/28	"		x				8 hr, brd 27, noise	
9/29	"		x				" " "	
9/30	"		x				" " "	
10/1	"		x				1 hr, brd 27, noise	
10/4	"		x				2 hr, each board, gain, CMER	
10/5	8A						Warm to RM T	

**Attachment of HRCR Item # 24 & #25: Mate/Demate & Operation Logs (continued)**

Hardware ID	JFET		Modules		S/N 10, 11		SKT 1	
Date	Time	AIDS	Power	Mate	Demate	Transport	Notes	
10/6	8A	243696					<del>cool</del> .5 hr each brd, rmt. S.V.	
10/6	10A	"					cool to LN2.	
10/6	6P	"					cool to LHe.	
10/8	12P	"	x				.5 hr each brd, LHe S.V.	
10/8	1P	"					warm to rmt.	
10/11	10A	"	x				.5 hr each brd, rmt S.V.	
10/13	10A	"			x		move modules from demor into flight cabinet.	
10/27	1P	"				x	183 → 103	

Attachment of HRCR Items # 24 & # 25: Mate/Demate & Operation Logs (PWB S/N 021)

DEVICE/BRD S/N: 021 (34)

USE THE "NOTE" COLUMN TO DESCRIBE ACTIONS  
 PROJECT: SPIRE/JFET BOARD

DATE	TIME	TECH	PWR ON	PWR OFF	MATE				DEMATE				TRANSFORT	NOTE
					JAA	JBB	JCC	JDD	JAA	JBB	JCC	JDD		
1/23/04		NAN			1	1	1	1	1	1	1	1		INITIAL GND 9 CHASSIS
2/12/04		NAN			1	1	1	1	1	1	1	1		GND 9 CHASSIS TEST
3/2/04		NAN												"
3/5/04		NAN												GND 9 CHASSIS TEST
3/5/04		NAN	1	1										SOURCE TEST
5/19/04		NAN	1	1					1	1				ALL TEST DEMATE
8/30/04		NAN			1	1			1	1				GND 9 CHASSIS TEST
8/30/04		NAN	✓	✓										(GND) SOURCE TEST
9/3/04		ST	1	1	1	1	2	2	1	1	2	2		Module Test 1
9/7/04		ST	1	1	1	1	2	2	1	1	2	2		Module Test 2

SERVER

SERVER

Attachment of HRCR Items # 24 & # 25: Mate/Demate & Operation Logs (PWB S/N 027)

DEVICE/BRD S/N: 027 (42)

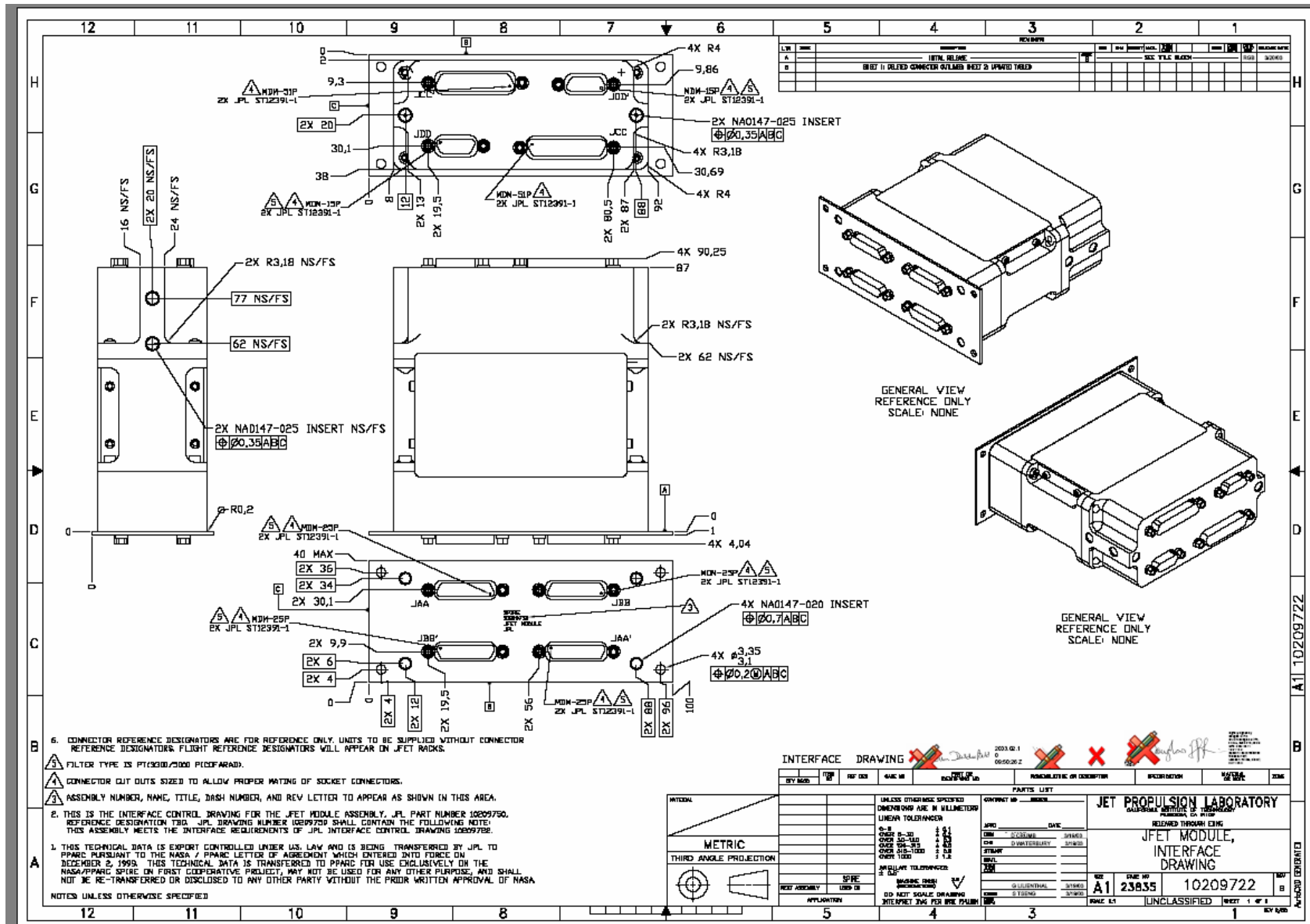
USE THE "NOTE" COLUMN TO DESCRIBE ACTIONS

PROJECT: SPIRE/JFET BOARD

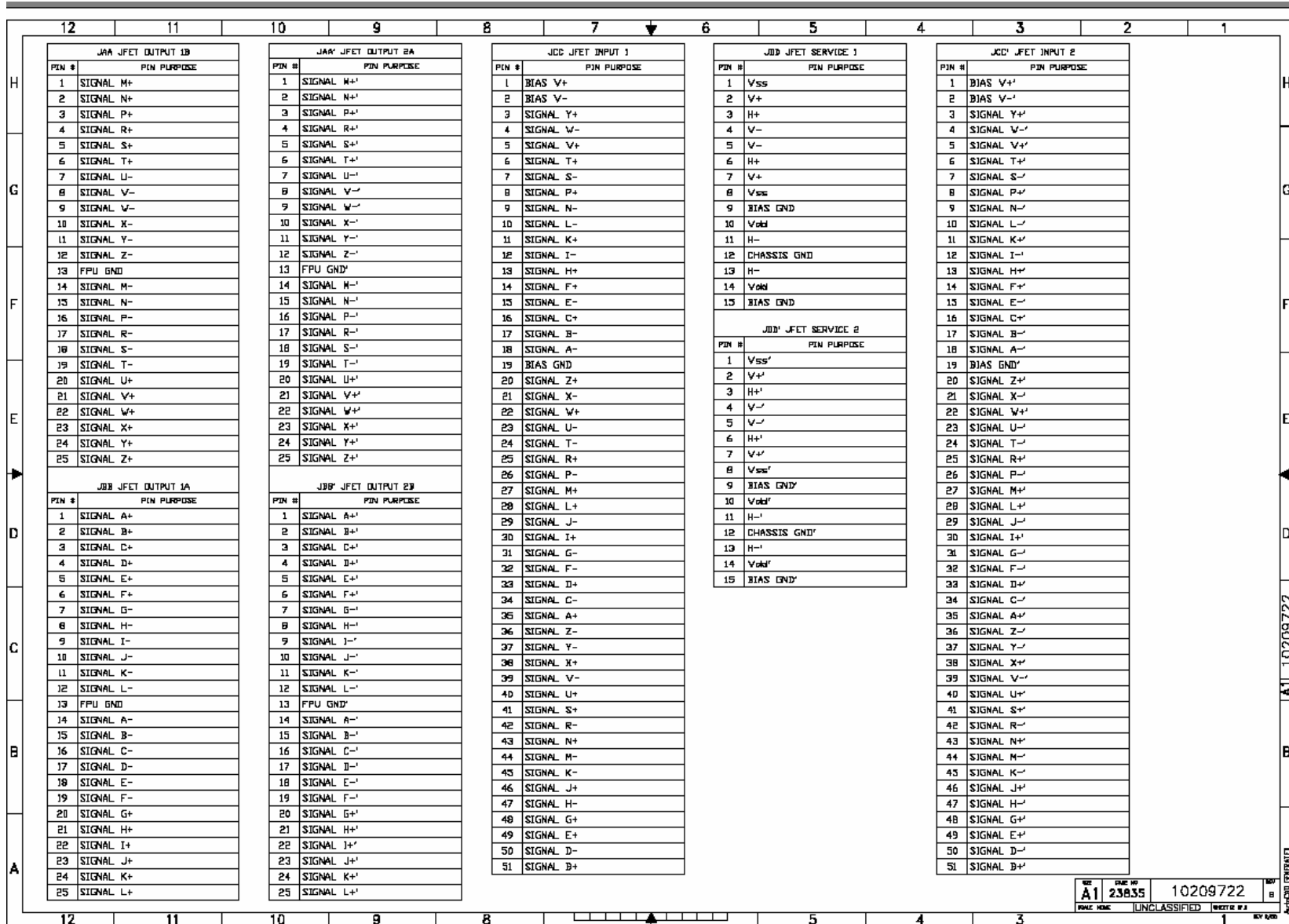
DATE	TIME	TECH	PWR ON	PWR OFF	MATE				DEMATE				TRANSFORT	NOTE
					JAA	JBB	JCC	JDD	JAA	JBB	JCC	JDD		
3/18/04	1:00 PM	NAN			✓	✓	✓	✓						GND of CHASSIS / SKIVER'S ON
4/7/04		NAN												GND of CHASSIS "
6/7/04		NAN												GND of CHASSIS "
6/7/04		NAN	✓	✓										SOURCE "
7/16/04		NAN												GND of CHASSIS "
7/16/04		NAN	✓	✓										SOURCE "
8-6-04		NAN							✓	✓	✓	✓		DEMATE SAVERS, MATE
8-26-04		ST.					✓	✓						MATE JCC, JDD.
8-30-04		NAN			✓	✓								GND of CHASSIS TEST
8-30-4		NAN	✓	✓					✓	✓				SOURCE TEST
9-3-04		ST	1	1	1	1	2	3	1	1	2	3		Module Test 1
9-7-04		ST	1	1	1	1	2	3	1	1	2	3		Module Test 2



Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 1 of 2)



Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 2 of 2)



**Attachment of HRCR Item # 11:**

**SPIRE**

**Handling Document**

**Field Effect Transistor (JFET) Module**

**10209750-1**

**Prepared by: Kalyani Sukhatme**

**10 September, 2003**

# Hardware Handling Guidelines

**Contamination:** Open shipment suitcase in a FED-STD-209 Class 10,000 clean room (ISO 14644-1 class 7) or better. Handle hardware with gloves.

**ESD:** Handle with grounding straps, ESD-safe gloves and ESD smocks at an ESD-safe workstation. Maintain shorting plugs on the unit whenever ESD is a concern. Refer to attached electrical handling document for other important safety precautions.

**Fragile:** Do not drop or otherwise shock the hardware including the shipping suitcase and container.

**Humidity Sensitive:** Place hardware in a humidity controlled Class 10,000 clean room. Maintain humidity level at 35%-50% RH typical, for ESD safety.

# SPIRE JFET Electrical Handling Document

1	Introduction .....	1
1.1	Hardware Description .....	1
2	Handling.....	2
3	Power ON Procedure.....	2
4	Electrical Check-out Test: Characteristic Offset Voltage Measurement.....	3

# 1. Introduction

This document provides guidelines for electrical handling for the SPIRE JFET Module.

## 1.1 Hardware Description

Each JFET module has two sets of 24 JFET channels. The JFET channels are populated on 1.0 micron thick Silicon Nitride membranes which provides thermal isolation. The operating temperature for these JFETs is ~120 K. The process of powering up the JFETs dissipates heat into the membrane resulting in a temperature increase with respect to the base temperature (4K to 10 K). Higher the power dissipation, higher is the temperature of the JFETs.

Each JFET channel consists of a matched pair of FETs (Figure 1.1-1) with a requirement for the offset voltage of less than **15 mV** between the matched pair. [The characteristic offset voltage is the difference between the source voltages ( $V_{sa}$  and  $V_{sb}$  with respect to ground) of the two FETs.]

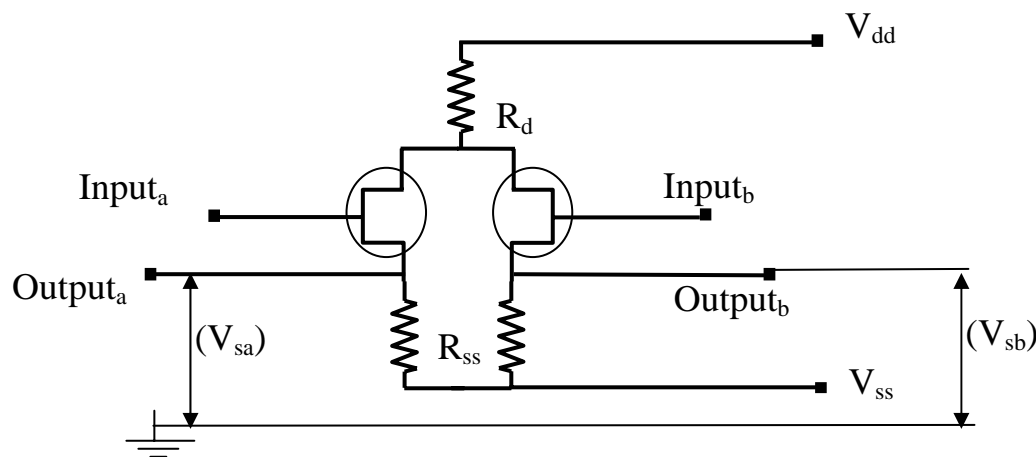


Figure 1.1-1

The Gates of the JFETs are the 'Inputs' of the circuit and the Sources ( $V_{sa}$  and  $V_{sb}$ ) of the JFETs are the outputs, as marked in Figure 1.1-1.  $V_{dd}$  and  $V_{ss}$  are the power lines for the circuit.

### Handling

1. **The JFET Module is Contamination Sensitive:** Handle the unit with Gloves only in a FED-STD-209 Class 100000 clean room (ISO 14644-1 class 7) or better.
2. **The JFET Module is ESD Sensitive:** Please handle with appropriate ESD hardware handling procedures. Handle with grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.
3. **The JFET Module is Fragile:** Please do not drop or otherwise shock the unit. Please DO NOT remove the cover of the JFET Module.

### Power ON Procedure

1. The JFET Module should be powered on **WITH the shorting plugs** (JPL Supplied Protection connectors) in place and with the **inputs shorted to ground**. Pins #9 and #15 on the 15-pin MDM connectors on the JFET Module are the bias grounds on the module. These pins should also be shorted to the power supply ground. The unit may be powered up without the shorting plug only when the inputs are connected to the detector system.

Under no circumstances the unit should be powered up without the inputs shorted to ground either via the shorting plug (JPL Supplied) or via the detector system.

2. Do not exceed a voltage of +5 V for the Vdd line and -5 V for the Vss line of the JFET Module.
3. When removing the shorting plugs from the unit for installation into the instrument, please use standard ESD precautions including grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.

**Electrical Check-out Test: Characteristic Offset Voltage Measurement**

- 1) Verify that the gates of the JFET channels (Inputs) are shorted together and grounded.
- 2) Apply the power supply ground to the bias ground pins on the unit (Pins 9 and 15 on the 15-pin MDM connectors)
- 3) Power on the JFET modules with Vdd = +3 V and Vss = -1.5 V
- 4) Verify that the handheld multimeter is in calibration.
- 5) Connect one side of the handheld multimeter to ground (Power supply ground).
- 6) And measure the voltage with respect to ground of each side (V<sub>sa</sub> and V<sub>sb</sub>) of each channel.
- 7) Calculate the characteristic offset voltage (V<sub>offset</sub>) for each channel (V<sub>offset</sub>= V<sub>sa</sub>-V<sub>sb</sub>)
- 8) Compare the values for each of the channels with the specific datasheet provided with the unit.  
The datasheets accompanying the unit also provides the values for the drain and source currents for a similar test performed at JPL.

**REFER TO MEASURED SOURCE VOLTAGE DATA FOR ACTUAL HARDWARE.** Here is an example of the source voltage values and the drain and the source currents obtained for such a test at room temperature are given in the Table 4-1

T, JFET	rm T	
Vdd	3 V	
Vss	-1.5 V	
Idd	1.564 mA	
Iss	1.5686 mA	
<b>Channel #</b>	<b>(V)</b>	<b>DELTA (V)</b>
1	1.130	0
	1.130	
2	1.075	0.001
	1.074	
3	0.781	0.001
	0.780	
4	1.088	0.005
	1.093	
5	0.834	0.001
	0.833	
6	1.012	0.003
	1.015	
7	0.785	0.002
	0.787	
8	1.148	0.004
	1.144	
9	0.753	0
	0.753	

10	0.693	0.008
	0.701	
11	1.110	0.004
	1.114	
12	0.758	0.001
	0.759	
13	0.832	0.002
	0.830	
14	1.264	0.001
	1.265	
15	1.206	0
	1.206	
16	0.818	0.001
	0.819	
17	0.526	0.005
	0.521	
18	1.423	0
	1.423	
19	0.773	0.002
	0.775	
20	0.873	0.004
	0.877	
21	1.387	0.006
	1.393	
22	1.417	0.003
	1.420	
23	0.887	0.002
	0.889	
24	0.888	0.003
	0.891	

**- END OF -**  
**Attachment of HRCR Item # 11:**  
**JFET Module Handling Document**



**Attachment of HRCR Item # 19:**

**Open PFR on Similar Hardware**

<b>PFR</b>	<b>Z82995</b>
<b>PFR</b>	<b>Z82997</b>
<b>PFR</b>	<b>Z82999</b>
<b>PFR</b>	<b>Z83353</b>
<b>PFR</b>	<b>Z83666</b>
<b>PFR</b>	<b>Z83673</b>
<b>PFR</b>	<b>Z84063</b>
<b>PFR</b>	<b>Z84064</b>

END OF  
HRCR PACKAGE