

SPIRE-LAM-PRJ-002974

HERSCHEL - SPIRE

LPU: Interface Control Document

Prepared by:	Signature
Dominique Pouliquen Date: 2 August 2007	
Checked by:	Signature
Date:	

Change record

Date	Issue	Revision	Modification	Pages affected
5 July 2007	1	0	Creation of the document (LAM.PJT.SPI.NOT.070705_01)	All
19 July 2007	1	0	Change of reference to officialise the document Suppression of the electrical scheme <u>LPU direct electrical interfaces unchanged</u> Proposed modification of the MCU harness included (DG's section) Addition of the mechanical interfaces	All
24 July 2007	1	1	Note added in DG's section where an error has been detected: bad type of connectors for FCU P43 and FPU P44. <u>LPU direct electrical interfaces unchanged</u>	§3.3
2 August 2007	1	2	Reference of the SPIRE Harness Definition Document updated (1.4) Now that the SPIRE HDD is updated, <ul style="list-style-type: none"> ➤ Pinout concerning the SPIRE harness deleted ➤ DG's section deleted Paragraph title corrected <u>LPU electrical interfaces unchanged</u>	§2.1 §3.2 §3.3 §3.2

Distribution list

Institute	Name	Issue/Revision						
		1/0	1/1	1/2	1/3	1/4	1/5	
CNES	Blanc Y.							
CNES	Casteras C.							
CNES	Condé E.							
CNES	Mercier K.	X	X	X				
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RAL	Griffin D.	X	X	X				
RAL	Griffin M.J.							
RAL	King K.J.							
RAL	Sawyer E.	X	X	X				
RAL	Swinyard B.M.							
CEA	Auguères J.L.							
CEA	Cara C.	X	X	X				
CEA	Fontignie J.	X	X	X				
CEA	Tourrette T.	X	X					
LAM	Baluteau J.P.							
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LAM	Origné A.							
LAM	Pouliquen D.							
LAM	Repetti B.	X	X	X				
LAM	Roman F.							
LAM	Rousset G.	X	X	X				
	LPU FM ADP							

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Aucune entrée de table d'illustration n'a été trouvée.

1 Scope of the document

This document describes the electrical and mechanical interfaces of the Latch Power Unit (LPU).

2 Documents

2.1 Applicable Documents

	Title	Author	Reference	Date
1	SPIRE Harness Definition	D.K. Griffin	SPIRE-RAL-PRJ-000608 Iss 1.4	01/08/2007

2.2 Reference Documents

#	Title	Author	Reference	Date

3 Electrical interface

For each circuit (prime and redundant), 2 connectors are mounted for a total of 4 on the LPU:

- ✓ LPU J41/J42: power (28V) supply and command lines from satellite, DEMA 9P
- ✓ LPU J43/J44: harness from MCU and to SMECm latch, DEMA 9S.

LPU J41 and LPU J43 are for the prime coil circuit.

LPU J42 and LPU J44 are for the redundant coil circuit.

3.1 LPU J41/J42 pin allocation:

LPU J41/J42	
Type : DEMA 9 P	
Pin number	Function
1	Hold Command Power
2	Hold Command return
4	Satellite power
5	Satellite power return
7	Release Command Power
8	Release Command Return
3, 6, 9	Not connected

3.2 LPU J43/J44 pin allocation:

LPU J431/J44	
Type : DEMA 9 S	
Pin number	Function
2	SMEC LL power supply (from MCU)
7	SMEC LL power return (from MCU)
3	SMEC LL power shield
4	SMEC LL power supply (To SMECm)
8	SMEC LL power return (To SMECm)
1, 5, 6, 9	Not connected

4 Mechanical interface

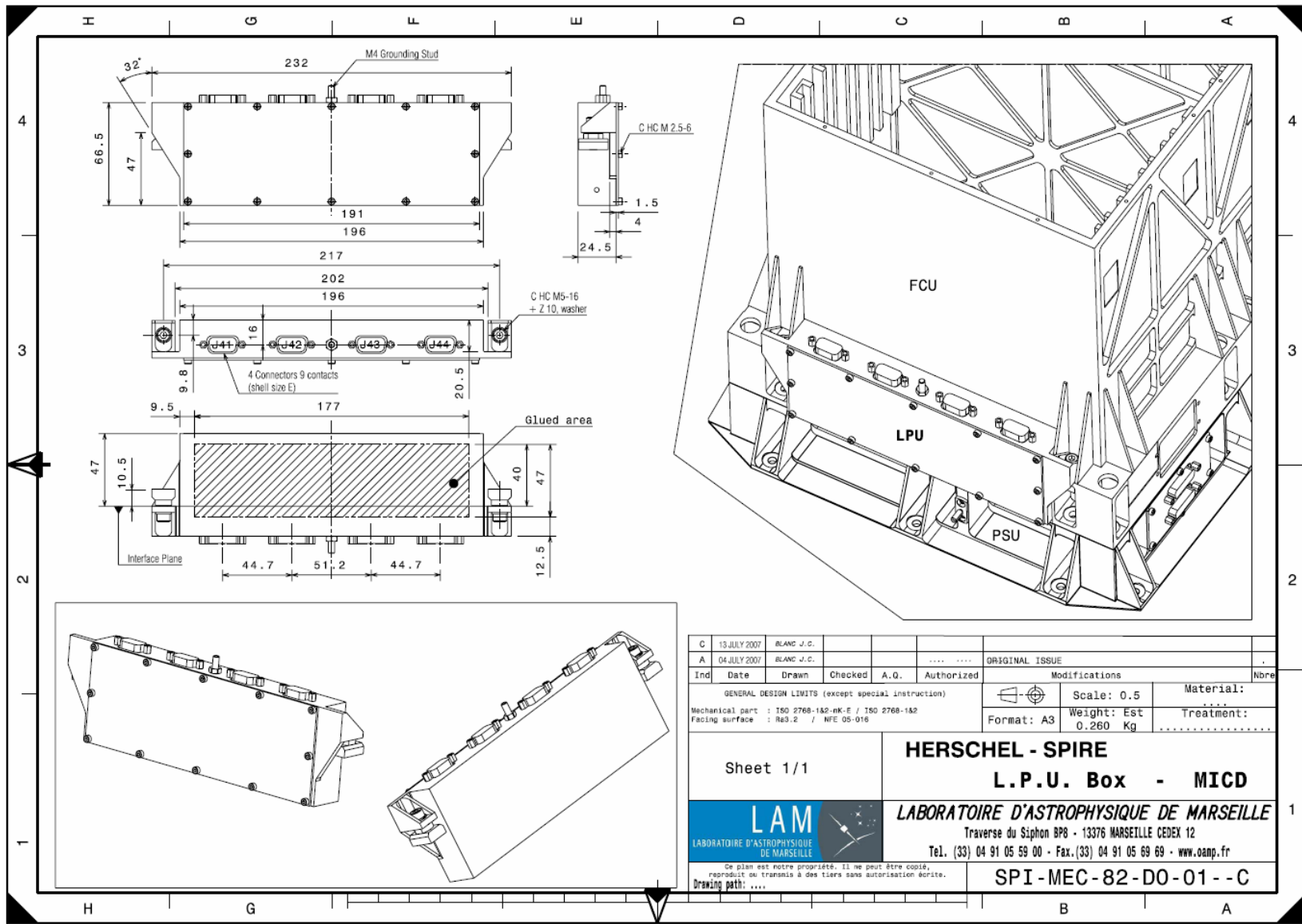
The following drawings give:

SPI-MEC-82-DO-01- -C: The overall LPU MICD

SPI-MEC-82-DO-02- -A: the gluing area on the FCU +Xsat face

SPI-MEC-82-DS-01- -A: the surface treatment of the LPU box

SPI-MEC-82-DS-02- -A: the surface treatment of the LPU lid



C	13 JULY 2007	BLANC J.C.									
A	04 JULY 2007	BLANC J.C.				ORIGINAL ISSUE			
Ind	Date	Drawn	Checked	A.O.	Authorized	Modifications					Nbre
GENERAL DESIGN LIMITS (except special instruction)										Scale: 0.5	
Mechanical part : ISO 2768-1&2-mK-E / ISO 2768-1&2										Material:	
Facing surface : Ra3.2 / NFE 05-016										Weight: Est	
										Format: A3	
										0.260 Kg	
										Treatment:	

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L.P.U. Box - MICD



LABORATOIRE D'ASTROPHYSIQUE DE MARSEILLE
Traverse du Siphon BP8 - 13376 MARSEILLE CEDEX 12
Tel. (33) 04 91 05 59 00 - Fax. (33) 04 91 05 69 69 - www.oamp.fr

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Drawing path:

SPI-MEC-82-DO-01--C

