SPIRE DCU FM ACCEPTANCE

Thermal Vacuum (VTC) Tests Report

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Abreviations list

AIV	Acceptance, Integration and Validation
CEA	Commissariat à l'Energie Atomique
DCU	Detector Control Unit
DPU	Digital Processing Unit
DRCU	Detector Readout and Control Unit
EM	Engineering Model
FCU	Focal Plane Control Unit
FM	Flight Model
FPU	Focal Plane Unit
FS	Flight Spare model
GSE	Ground Support Equipment
H/K	HouseKeeping
I&T	Integration and Test
I/F	Interface
ICD	Interface Control Document
IID	Instrument Interface Document
IRD	Instrument Requirements Document
LAM	Laboratoire d'Astrophysique de Marseille
LETI	Laboratoire d'Electronique, de Technologie et d'Instrumentation
LTU	Local Test Unit
MCU	Mechanism Control Unit
PB	Power Bench
PFM	Proto Flight Model
PSU	Power Supply Unit
QM	Qualification Model
RAL	Rutherford Appleton Laboratory
SAp	Service d'Astrophysique (CEA/DAPNIA)
S/C	SpaceCraft
SCU	Subsystem Control Unit
SEDI	Service d'Electronique et d'Informatique (CEA/DAPNIA)
STB	Simplified Test Board
SPIRE	Spectral and Photometric Imaging REceiver
STM	Structural and Thermal Model
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
TC	TeleCommand
TM	TeleMetry

2 Applicable documents

[AD1] HERSCHEL/SPIRE DRCU Interface Control Document	SAP-SPIRE-CCa-075-02
[AD2] HERSCHEL/SPIRE DRCU/DPU Interface Control Document	SAP-SPIRE-CCa-076-02
[AD3] Herschel/SPIRE DRCU AIV PLAN	SAp-SPIRE-HT-0082-02
[AD4] HERSCHEL/SPIRE DRCU Subsystem specification	Sap-SPIRE-CCa-0025-00
[AD5] Herschel/Planck Instrument Interface Document IID Part A "	SCI-PT-IIDA/SPIRE-04624
[AD6] Herschel/Planck Instrument Interface Document Part B Instrument "SPIRE"	SCI-PT-IIDB/SPIRE-02124
[AD7]	
[AD8] SPIRE HS DCU FM Functional test procedure	SAp-SPIRE-TT-0387-06
[AD9] SPIRE HS DCU FM Procédure de vide thermique	SAp-SPIRE-HT-0389-06

3 Reference documents

[RD1] HERSCHEL/SPIRE DCU EM/QM1 Test Report	Sap-SPIRE-CCa-0129-03 Issue 1.0
[RD2] DS-SPIRE development tree	Sap-SPIRE-DS - Version 07/03/2002
[RD3] FIRST/SPIRE DRCU and WIH Development Plan	SAP-SPIRE-JLA-0047-01
[RD 4] Rapport d'essais	Référence Intespace E5831 HSDQMTHER
[RD 5] HS-DCU FM TRR Report	SAp-SPIRE- QA-0418-06

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Introduction

This technical report applies to the Vibration tests performed on the DCU QM2 equipment for the HERSCHEL SPIRE Project.

These tests have been performed at Intespace between July 4th 2006 and July 10th 2006.

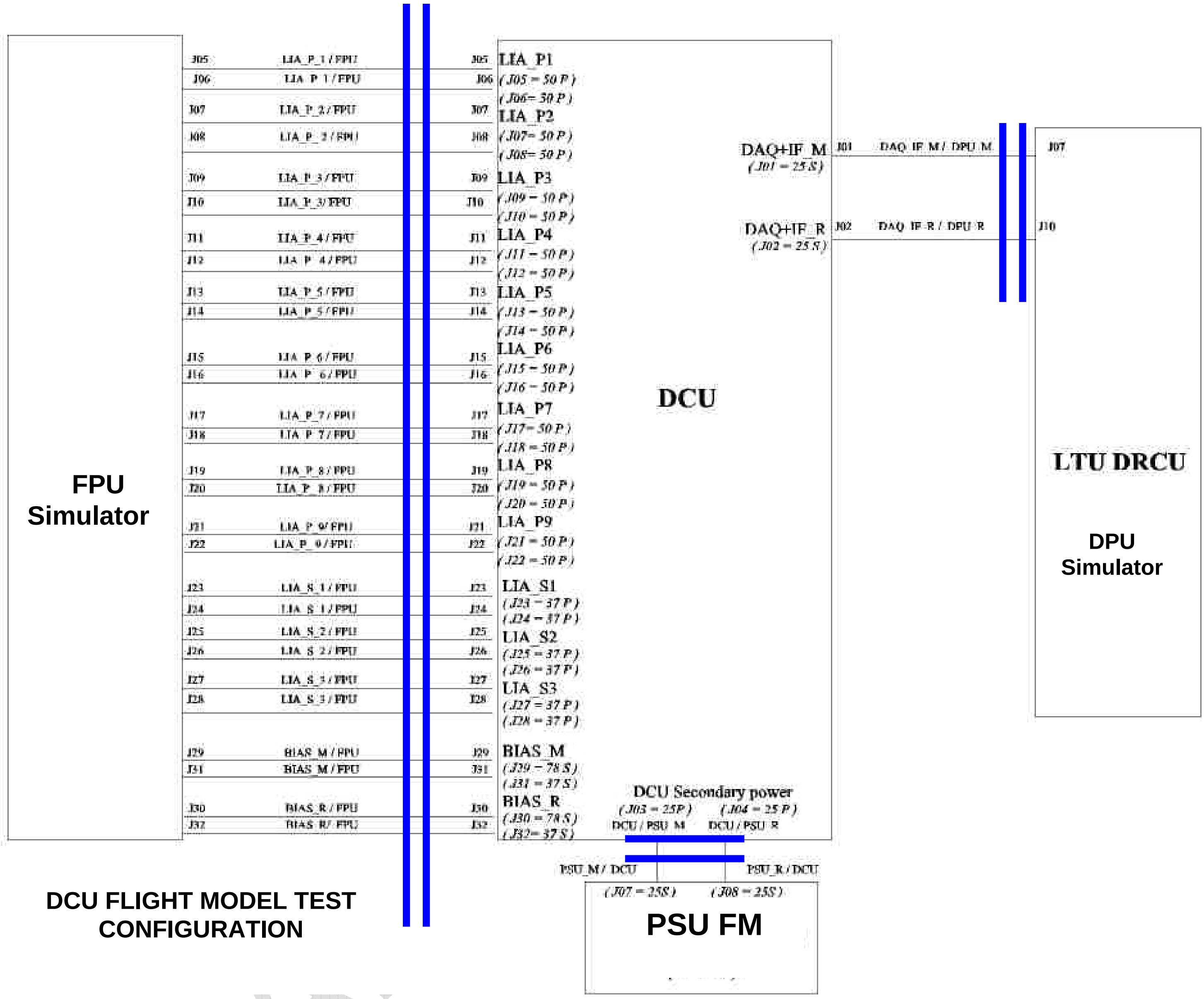
5 Test Configuration

We use the LTU in its latest software configuration, the fully assembled DCU and FCU, the FPU and the PSU Flight Model (PSU FM).

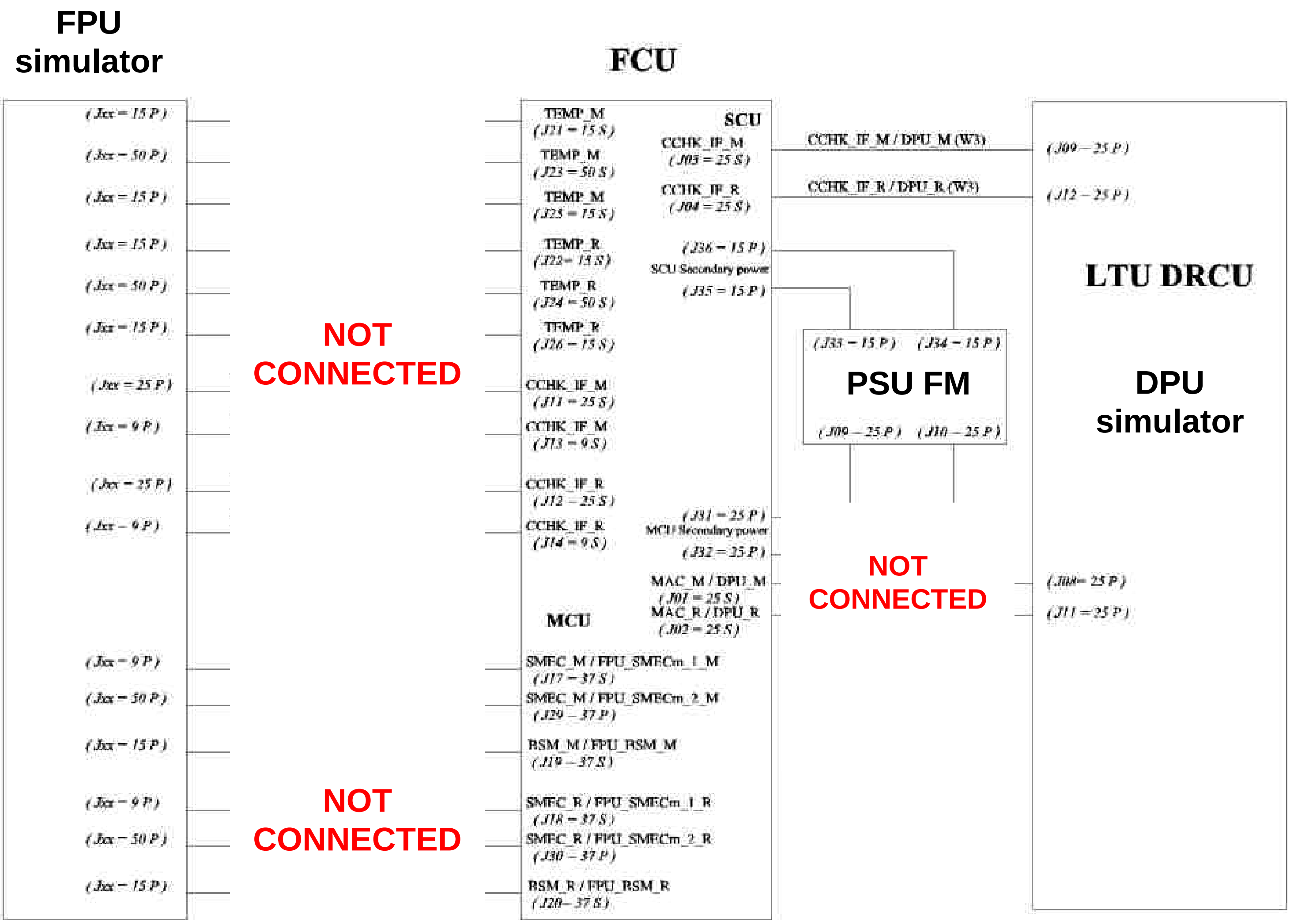
Before to connect any harness, we place savers on all connectors

Connect all harnesses as described below :

- Between DCU and FPU
- Between DCU and LTU
- Between SCU and LTU
- Between DCU and PSU FM
- Between SCU and PSU FM



DCU FM VTC test configuration

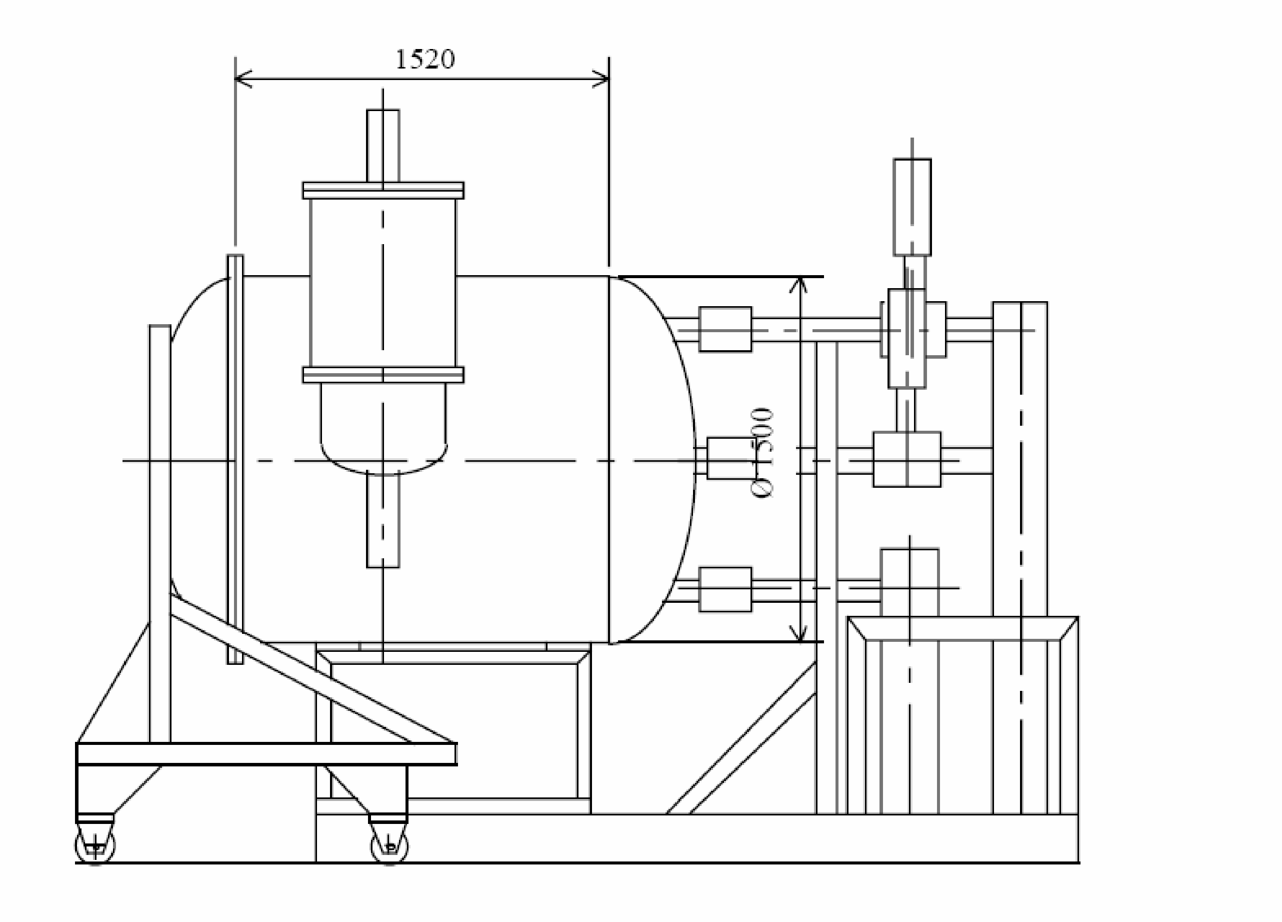


DCU FM VTC test configuration

6 Test Program

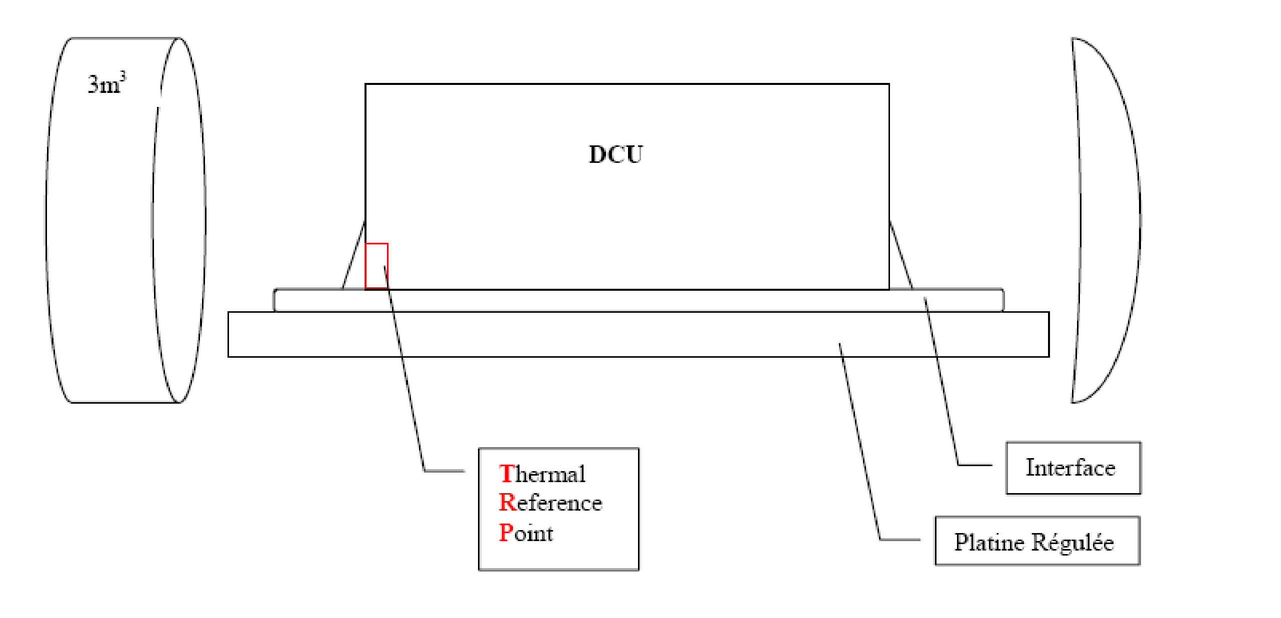
The description of the VTC test is given in the vibration tests procedure [AD9].

The thermal cycling has been performed in a dedicated thermal vacuum chamber « SEAVOM 3m^3 » from INTESPACE.

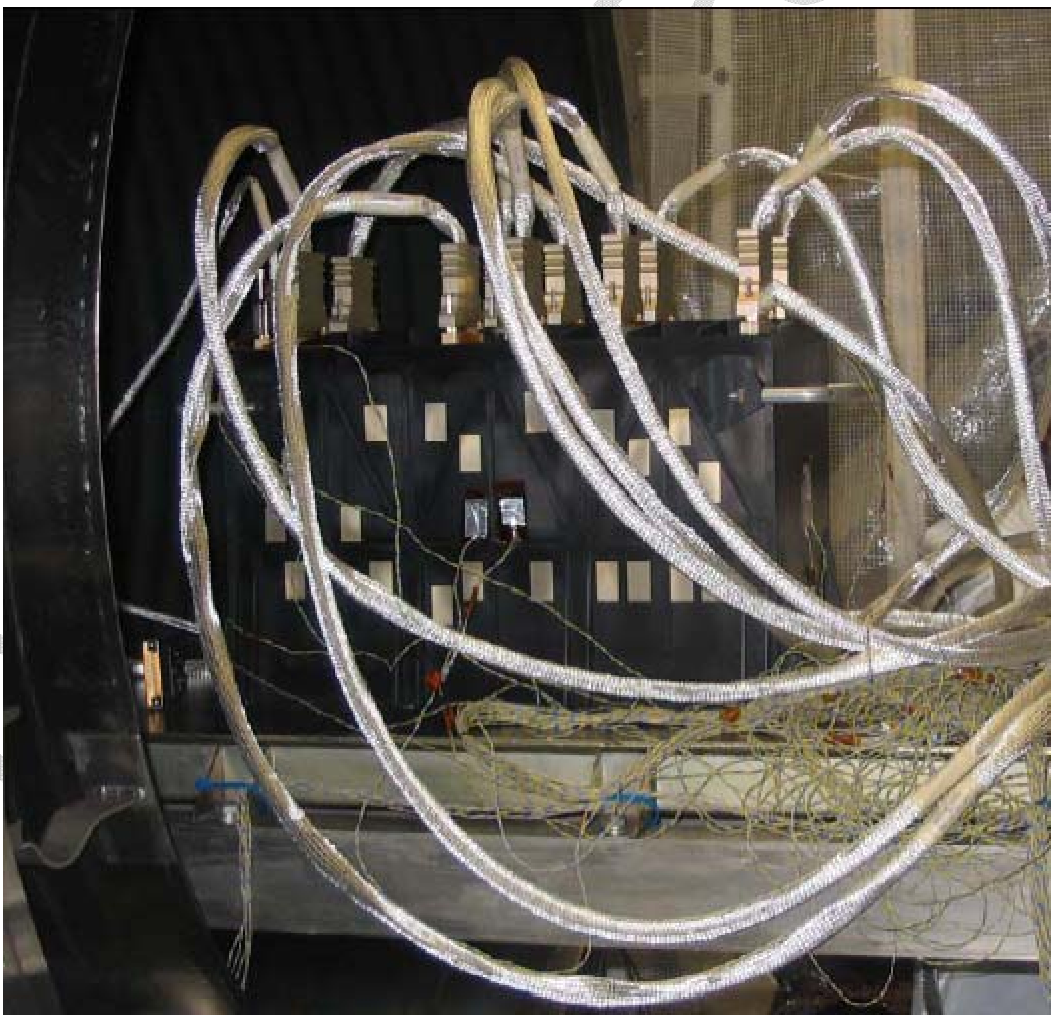


The electronic box DCU is screwed on an interface plate following interface specifications.

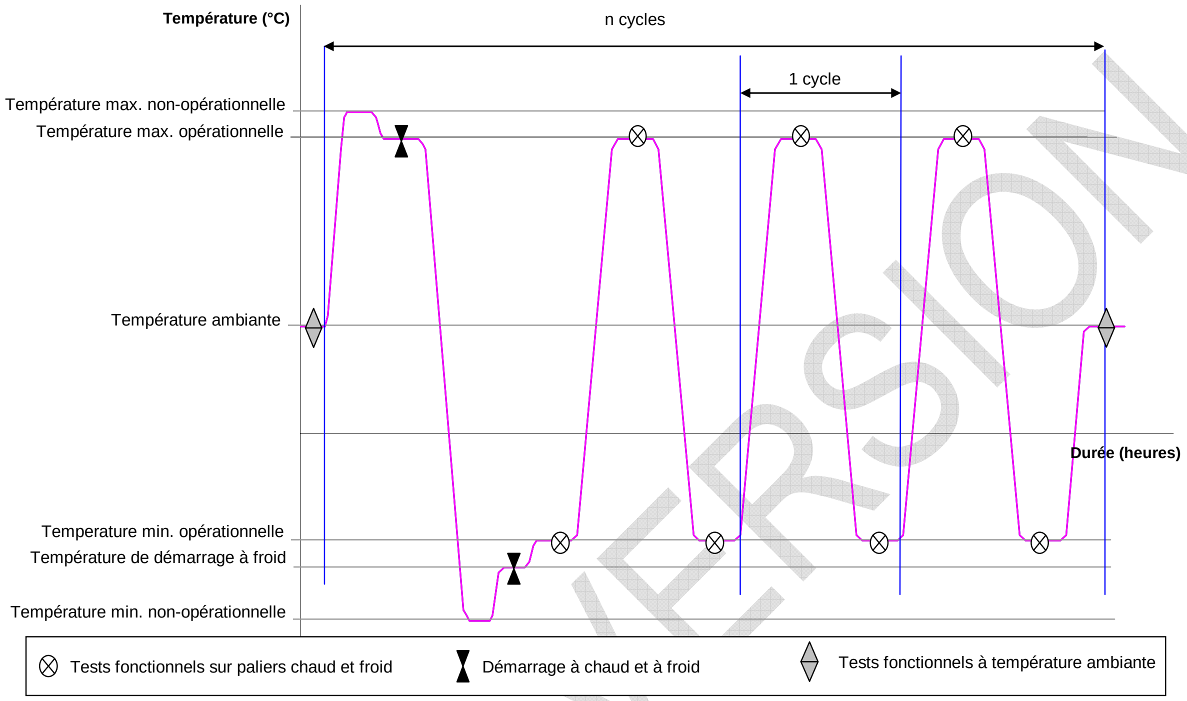
The test is monitored with the temperature measured at TRP (Thermal Reference Point) level on the box.



3m3
DCU
Thermal
Reference
Point
Interface
Platine Régulée



The test sequence is represented thereafter :



The test sequence has 4 cycles.

The temperatures applied for qualification are :

Modes de fonctionnement de HS DCU	Température Max (°C)	Température Min
Opérationnel	50	-20
Non opérationnel	60	-35
Démarrage	50	-30

The actual evolution of the temperature is given thereafter. It shows that the specification of the cycling described in [AD9] is fulfilled.

The results of the functional tests are given in the next chapter.

Functional tests have been performed on plateau levels. The detailed description of the cycle is given thereafter.

7 Report of the functional tests

The results of all the functional tests (on many plateau levels) are given in [RD4] to [RD16].

The list of the performed test, with reference to [AD8] is :

DCU QM2 tests	Test -1 : Before VTC	Test 0 : After installation in VTC cmaber	Test 1 : Warm start (cycle 1)	Test 2 : Cold start (cycle 1)	Test 3 : Cold plateau (cycle 1)	Test 4 : Warm plateau (cycle 2)	Test 5 : Cold plateau (cycle 2)	Test 6 : Warm start (cycle 3)	Test 7 : Cold start (cycle 3)	Test 8 : Warm plateau (cycle 4)	Test 9 : Cold plateau (cycle 4)	Test 10 : Ambient final
Consumption (redundant)	x	x	x	x	x	x	x	x	x	x	x	x
Consumption (main)	x	x	x	x	x	x	x	x	x	x	x	x
Frame generation	x											
HK acquisition	x	x	x	x	x	x	x	x	x	x	x	x
BIAS half level	x	x	x	x	x	x	x	x	x	x	x	x
Optimum phase	x											
Gains	x	x	x	x	x	x	x	x	x	x	x	x
Cross talk	x											
Noise	x											
Offset (TBC)	x	x	x	x	x	x	x	x	x	x	x	x
Bandwidth	x											

In this document, only the main results are given.

7.1 Visual inspection

A visual inspection was performed before and after the VTC tests. It revealed no specific problem.

7.2 Consumption tests

The consumption measured at PSU FM level on DCU main side are :

Before VTC

Conso 28 V	DCU main		DCU redundant	
ON	400	mA	400	mA
MCU On	810	mA	810	mA
MCU On booté	880	mA	870	mA
MCU On & LIAP ON	2100	mA	2090	mA
MCU On & LIAS ON	1230	mA	1220	mA

First warm plateau at 50°C

Conso 28 V	DCU main		DCU redundant	
ON	400	mA	400	mA
MCU On	810	mA	810	mA
MCU On booté	880	mA	870	mA
MCU On & LIAP ON	2100	mA	2080	mA
MCU On & LIAS ON	1230	mA	1220	mA
MCU Off & LIAP ON	1580	mA	1590	mA
MCU Off & LIAS ON	750	mA	740	mA

Cold start at -30°C

Conso 28 V	DCU main		DCU redundant	
ON	400	mA	400	mA
MCU On	810	mA	810	mA
MCU On booté	870	mA	870	mA
MCU On & LIAP ON	2080	mA	2070	mA
MCU On & LIAS ON	1220	mA	1220	mA
MCU Off & LIAP ON	1570	mA	1570	mA
MCU Off & LIAS ON	740	mA	760	mA

First cold plateau at -20°C

Conso 28 V	DCU main		DCU redundant	
ON	400	mA	400	mA
MCU On	810	mA	810	mA
MCU On booté	880	mA	870	mA
MCU On & LIAP ON	2080	mA	2070	mA
MCU On & LIAS ON	1220	mA	1220	mA
MCU Off & LIAP ON	1580	mA	1580	mA
MCU Off & LIAS ON	750	mA	740	mA

Second warm plateau at 50°C

Conso 28 V	DCU main		DCU redundant	
ON	400	mA	400	mA
MCU Off & LIAP ON	1570	mA	1570	mA
MCU Off & LIAS ON	740	mA	740	mA

Second cold plateau at -20°C

Conso 28 V	DCU main		DCU redundant	
ON	400	mA	400	mA
MCU Off & LIAP ON	1600	mA	1600	mA
MCU Off & LIAS ON	750	mA	750	mA

Third warm plateau at 50°C

Conso 28 V	DCU main		DCU redundant	
ON	400	mA	400	mA
MCU Off & LIAP ON	1570	mA	1570	mA
MCU Off & LIAS ON	740	mA	740	mA

Third cold plateau at -20°C

Conso 28 V	DCU main		DCU redundant	
ON	400	mA	400	mA
MCU Off & LIAP ON	1600	mA	1600	mA
MCU Off & LIAS ON	750	mA	750	mA

Fourth warm plateau at 50°C

Conso 28 V	DCU main		DCU redundant	
ON	400	mA	400	mA
MCU Off & LIAP ON	1600	mA	1600	mA
MCU Off & LIAS ON	750	mA	750	mA

Fourth cold plateau at -20°C

Conso 28 V	DCU main	DCU redundant
ON	400 mA	400 mA
MCU Off & LIAP ON	1600 mA	1600 mA
MCU Off & LIAS ON	750 mA	740 mA

Ambient final 20°C

Conso 28 V	DCU main	DCU redundant
ON	400 mA	400 mA
MCU Off & LIAP ON	1610 mA	1610 mA
MCU Off & LIAS ON	750 mA	740 mA

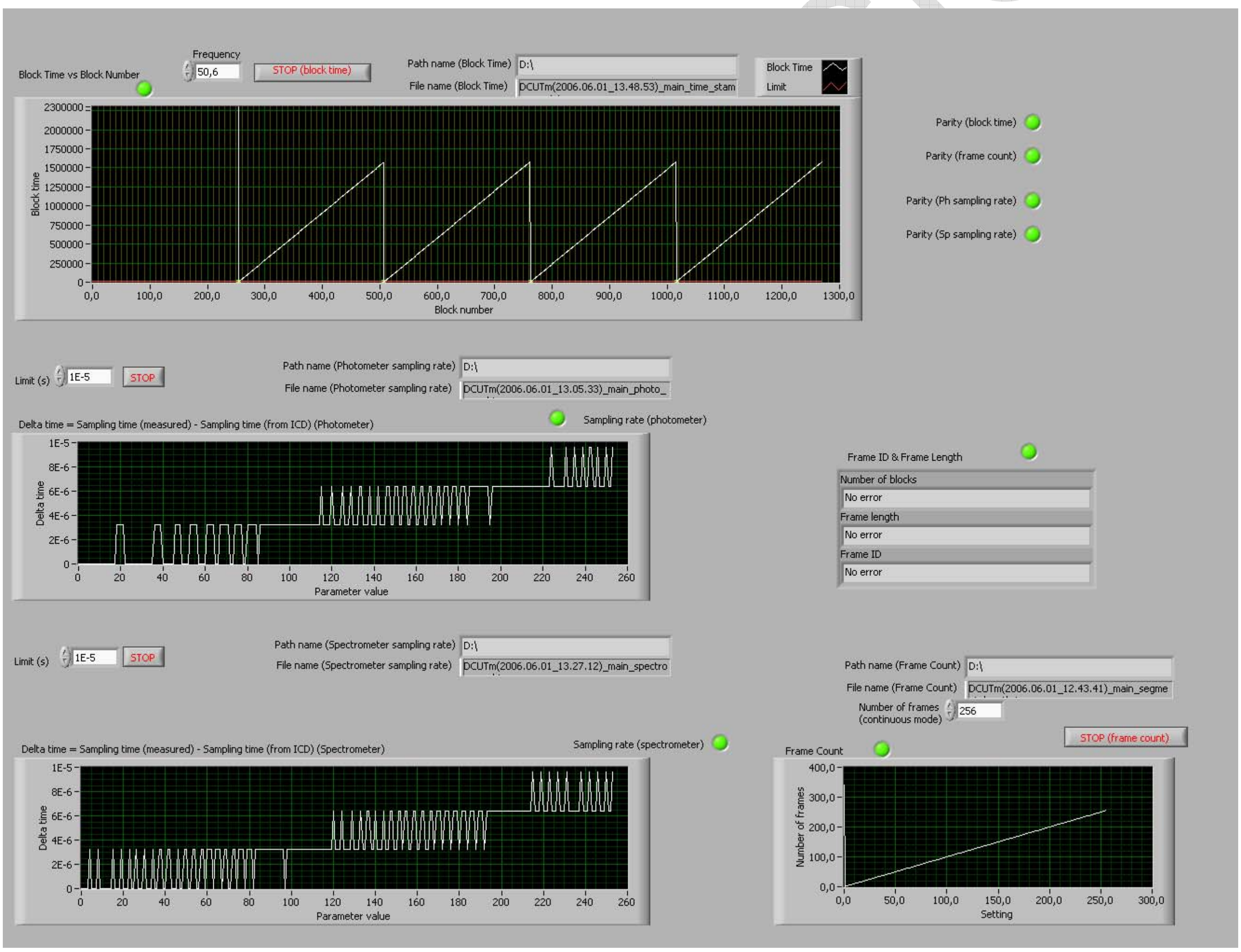
The consumptions did not move during the VTC cycling.

7.3 Frame generation Tests

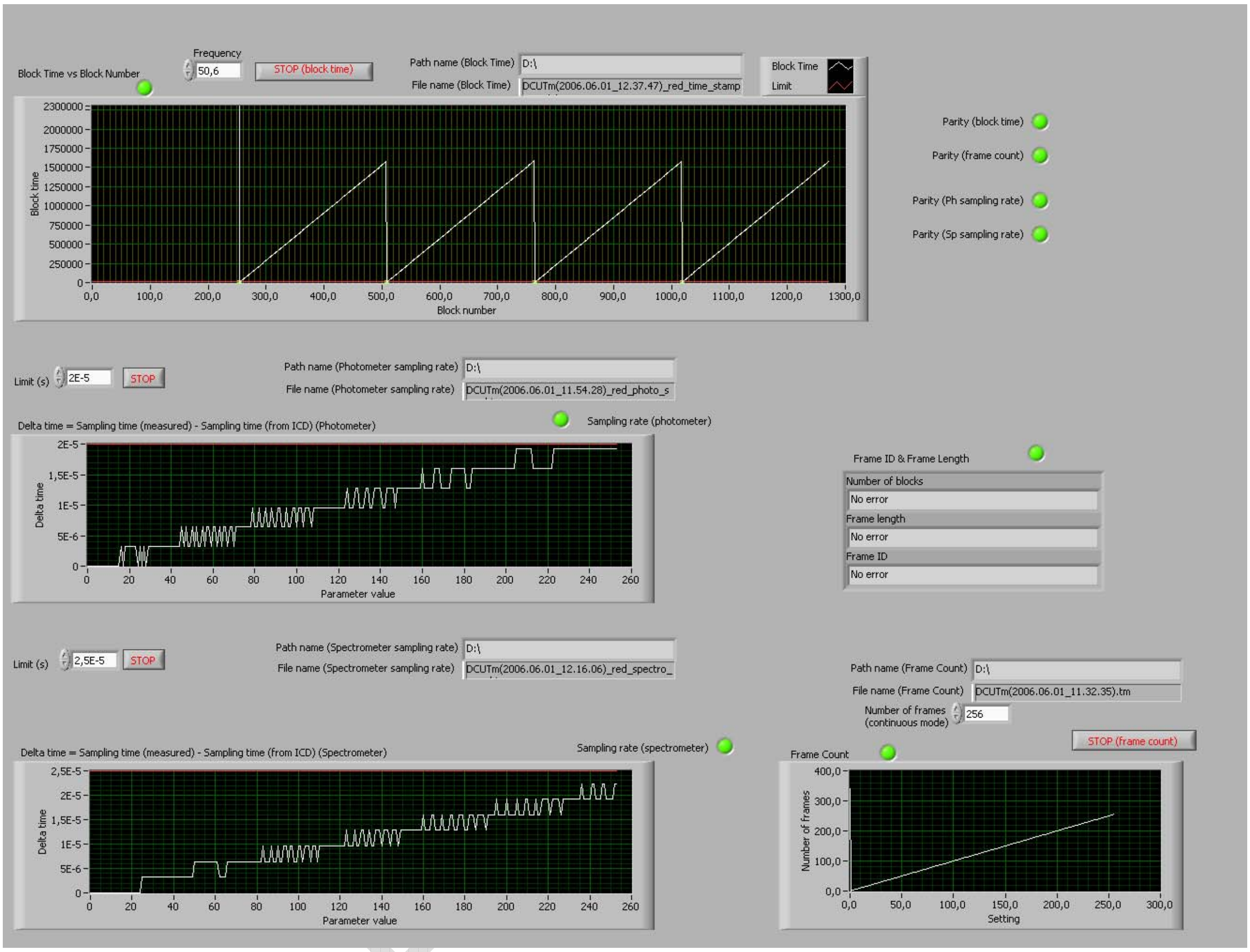
The test consist in testing the frame generation (frame length, frame modes, frames content and ID), It also tests the reset of the time stamp within the frames, the frame generation frequencies (photo and spectro) as well as the number of frames commanded during telemetry acquisitions.

The results obtained are the same after VTC than before. These are summarized in the following screenshot relative to the tests performed before the VTC.

Main side



Redundant side



8 HouseKeepings

We have started the DCU Monitoring Mode from LTU (1 Hz frequency) during the whole VTC test and the results were consistent with the expected values.

Note that we observe the results over a sufficient time (1 minute).

We thereafter show the results relative the H/K acquisitions performed after the VTC tests at 25°C :

When LIAP ON, Main side

MONITORING

DCU

Nom Parametre	Description	Valeur C...	Min	Max	Unite
BIAS_TEMP	BIAS board Temp	21.59	-31.01	70.01	°C
LIA_S1_TEMP	LIAS board 1 Temp	21.45	-31.01	70.01	°C
LIA_S2_TEMP	LIAS board 2 Temp	21.08	-31.01	70.01	°C
LIA_S3_TEMP	LIAS board 3 Temp	20.72	-31.01	70.01	°C
LIA_P9_TEMP	LIAP board 9 Temp	21.18	-31.01	70.01	°C
LIA_P8_TEMP	LIAP board 8 Temp	21.50	-31.01	70.01	°C
LIA_P7_TEMP	LIAP board 7 Temp	21.18	-31.01	70.01	°C
LIA_P6_TEMP	LIAP board 6 Temp	21.25	-31.01	70.01	°C
LIA_P5_TEMP	LIAP board 5 Temp	21.22	-31.01	70.01	°C
LIA_P4_TEMP	LIAP board 4 Temp	21.45	-31.01	70.01	°C
LIA_P3_TEMP	LIAP board 3 Temp	21.04	-31.01	70.01	°C
LIA_P2_TEMP	LIAP board 2 Temp	21.21	-31.01	70.01	°C
LIA_P1_TEMP	LIAP board 1 Temp	21.57	-31.01	70.01	°C
DAQ_IF_TEMP	DAQ_IF board Temp	21.56	-31.01	70.01	°C
BDAQ_P5	BIAS/DAQ_IF +5V(before post regu...	5.08	4.90	5.26	V
BDAQ_P9	BIAS/DAQ_IF +9V(before post regu...	8.96	8.50	9.10	V
BDAQ_N9	BIAS/DAQ_IF -9V(before post regul...	-9.04	-9.10	-8.50	V
LIAP_P5	LIAP +5V(before post regulator)	5.14	4.90	5.27	V
LIAP_P9	LIAP +9V(before post regulator)	11.48	11.20	11.60	V
LIAP_N9	LIAP -9V(before post regulator)	-11.51	-11.60	-11.20	V
LIAS_P5	LIAS +5V(before post regulator)	0.09	4.90	5.26	V
LIAS_P9	LIAS +9V(before post regulator)	0.01	11.20	11.60	V
LIAS_N9	LIAS -9V(before post regulator)	0.01	-11.60	-11.20	V
PWR_STATUS	LIA1 to LIA12 12 +5V/+9V/-9V status	0000	0.00	0.00	hexa
T/C_1	16 bits ADC (Offset=0) 1	2207			Decimal
T/C_2	16 bits ADC (Offset=0) 2	4351			Decimal
T/C_3	16 bits ADC (Offset=0) 3	255			Decimal

When LIAS ON, Main side

MONITORING

DCU

Nom Parametre	Description	Valeur C...	Min	Max	Unite
BIAS_TEMP	BIAS board Temp	21.76	-31.01	70.01	°C
LIA_S1_TEMP	LIAS board 1 Temp	21.45	-31.01	70.01	°C
LIA_S2_TEMP	LIAS board 2 Temp	21.10	-31.01	70.01	°C
LIA_S3_TEMP	LIAS board 3 Temp	20.73	-31.01	70.01	°C
LIA_P9_TEMP	LIAP board 9 Temp	21.44	-31.01	70.01	°C
LIA_P8_TEMP	LIAP board 8 Temp	21.80	-31.01	70.01	°C
LIA_P7_TEMP	LIAP board 7 Temp	21.47	-31.01	70.01	°C
LIA_P6_TEMP	LIAP board 6 Temp	21.59	-31.01	70.01	°C
LIA_P5_TEMP	LIAP board 5 Temp	21.57	-31.01	70.01	°C
LIA_P4_TEMP	LIAP board 4 Temp	21.77	-31.01	70.01	°C
LIA_P3_TEMP	LIAP board 3 Temp	21.45	-31.01	70.01	°C
LIA_P2_TEMP	LIAP board 2 Temp	21.53	-31.01	70.01	°C
LIA_P1_TEMP	LIAP board 1 Temp	21.89	-31.01	70.01	°C
DAQ_IF_TEMP	DAQ_IF board Temp	22.23	-31.01	70.01	°C
BDAQ_P5	BIAS/DAQ_IF +5V(before post regu...	5.08	4.90	5.26	V
BDAQ_P9	BIAS/DAQ_IF +9V(before post regu...	8.96	8.50	9.10	V
BDAQ_N9	BIAS/DAQ_IF -9V(before post regul...	-9.04	-9.10	-8.50	V
LIAP_P5	LIAP +5V(before post regulator)	0.22	4.90	5.27	V
LIAP_P9	LIAP +9V(before post regulator)	0.01	11.20	11.60	V
LIAP_N9	LIAP -9V(before post regulator)	0.00	-11.60	-11.20	V
LIAS_P5	LIAS +5V(before post regulator)	5.21	4.90	5.26	V
LIAS_P9	LIAS +9V(before post regulator)	11.54	11.20	11.60	V
LIAS_N9	LIAS -9V(before post regulator)	-11.54	-11.60	-11.20	V
PWR_STATUS	LIA1 to LIA12 12 +5V/+9V/-9V status	0000	0.00	0.00	hexa
T/C_1	16 bits ADC (Offset=0) 1	2207			Decimal
T/C_2	16 bits ADC (Offset=0) 2	4351			Decimal
T/C_3	16 bits ADC (Offset=0) 3	255			Decimal

When LIAP ON, Redundant side

MONITORING

DCU

Nom Parametre	Description	Valeur C...	Min	Max	Unite
BIAS_TEMP	BIAS board Temp	21.41	-31.01	70.01	°C
LIA_S1_TEMP	LIAS board 1 Temp	21.04	-31.01	70.01	°C
LIA_S2_TEMP	LIAS board 2 Temp	21.07	-31.01	70.01	°C
LIA_S3_TEMP	LIAS board 3 Temp	20.84	-31.01	70.01	°C
LIA_P9_TEMP	LIAP board 9 Temp	21.56	-31.01	70.01	°C
LIA_P8_TEMP	LIAP board 8 Temp	21.19	-31.01	70.01	°C
LIA_P7_TEMP	LIAP board 7 Temp	21.21	-31.01	70.01	°C
LIA_P6_TEMP	LIAP board 6 Temp	21.57	-31.01	70.01	°C
LIA_P5_TEMP	LIAP board 5 Temp	21.28	-31.01	70.01	°C
LIA_P4_TEMP	LIAP board 4 Temp	21.50	-31.01	70.01	°C
LIA_P3_TEMP	LIAP board 3 Temp	21.45	-31.01	70.01	°C
LIA_P2_TEMP	LIAP board 2 Temp	21.73	-31.01	70.01	°C
LIA_P1_TEMP	LIAP board 1 Temp	21.48	-31.01	70.01	°C
DAQ_IF_TEMP	DAQ_IF board Temp	21.08	-31.01	70.01	°C
BDAQ_P5	BIAS/DAQ_IF +5V(before post regu...	5.07	4.90	5.26	V
BDAQ_P9	BIAS/DAQ_IF +9V(before post regu...	8.98	8.50	9.10	V
BDAQ_N9	BIAS/DAQ_IF -9V(before post regul...	-9.06	-9.10	-8.50	V
LIAP_P5	LIAP +5V(before post regulator)	5.15	4.90	5.27	V
LIAP_P9	LIAP +9V(before post regulator)	11.50	11.20	11.60	V
LIAP_N9	LIAP -9V(before post regulator)	-11.51	-11.60	-11.20	V
LIAS_P5	LIAS +5V(before post regulator)	0.00	4.90	5.26	V
LIAS_P9	LIAS +9V(before post regulator)	0.00	11.20	11.60	V
LIAS_N9	LIAS -9V(before post regulator)	-0.00	-11.60	-11.20	V
PWR_STATUS	LIA1 to LIA12 12 +5V/+9V/-9V status	0000	0.00	0.00	hexa
T/C_1	16 bits ADC (Offset=0) 1	2175			Decimal
T/C_2	16 bits ADC (Offset=0) 2	255			Decimal
T/C_3	16 bits ADC (Offset=0) 3	250			Decimal

When LIAS ON, Redundant side

MONITORING

DCU

Nom Parametre	Description	Valeur C...	Min	Max	Unite
BIAS_TEMP	BIAS board Temp	21.47	-31.01	70.01	°C
LIA_S1_TEMP	LIAS board 1 Temp	20.99	-31.01	70.01	°C
LIA_S2_TEMP	LIAS board 2 Temp	21.07	-31.01	70.01	°C
LIA_S3_TEMP	LIAS board 3 Temp	20.89	-31.01	70.01	°C
LIA_P9_TEMP	LIAP board 9 Temp	21.65	-31.01	70.01	°C
LIA_P8_TEMP	LIAP board 8 Temp	21.31	-31.01	70.01	°C
LIA_P7_TEMP	LIAP board 7 Temp	21.31	-31.01	70.01	°C
LIA_P6_TEMP	LIAP board 6 Temp	21.63	-31.01	70.01	°C
LIA_P5_TEMP	LIAP board 5 Temp	21.39	-31.01	70.01	°C
LIA_P4_TEMP	LIAP board 4 Temp	21.59	-31.01	70.01	°C
LIA_P3_TEMP	LIAP board 3 Temp	21.56	-31.01	70.01	°C
LIA_P2_TEMP	LIAP board 2 Temp	21.82	-31.01	70.01	°C
LIA_P1_TEMP	LIAP board 1 Temp	21.57	-31.01	70.01	°C
DAQ_IF_TEMP	DAQ_IF board Temp	21.41	-31.01	70.01	°C
BDAQ_P5	BIAS/DAQ_IF +5V(before post regu...	5.07	4.90	5.26	V
BDAQ_P9	BIAS/DAQ_IF +9V(before post regu...	8.98	8.50	9.10	V
BDAQ_N9	BIAS/DAQ_IF -9V(before post regul...	-9.06	-9.10	-8.50	V
LIAP_P5	LIAP +5V(before post regulator)	0.01	4.90	5.27	V
LIAP_P9	LIAP +9V(before post regulator)	0.01	11.20	11.60	V
LIAP_N9	LIAP -9V(before post regulator)	-0.00	-11.60	-11.20	V
LIAS_P5	LIAS +5V(before post regulator)	5.21	4.90	5.26	V
LIAS_P9	LIAS +9V(before post regulator)	11.54	11.20	11.60	V
LIAS_N9	LIAS -9V(before post regulator)	-11.55	-11.60	-11.20	V
PWR_STATUS	LIA1 to LIA12 12 +5V/+9V/-9V status	0000	0.00	0.00	hexa
T/C_1	16 bits ADC (Offset=0) 1	2175			Decimal
T/C_2	16 bits ADC (Offset=0) 2	255			Decimal
T/C_3	16 bits ADC (Offset=0) 3	250			Decimal

All the H/K observed after the VTC were consistent.

Thereafter, are reported the H/K as measured at the stabilized temperature levels.

Source H/K Channel	Test 0 20°C	Test 1 50°C	Test 2 -30°C	Test 3 -20°C	Test 4 50°C	Test 5 -20°C	Test 6 50°C	Test 7 -20°C	Test 8 50°C	Test 9 -20°C	Test 10 20°C
DAQ-IF TEMP (°C)	24,12	55,57	-31,64	-11,68	57,05	-10,89	57,8	-8,43	54,64	-15,17	21,56
BIAS TEMP (°C)	23,57	56,08	-31,24	-14,97	55,89	-12,98	55,63	-10,41	54,76	-12,7	21,59
LIAS 1 TEMP (°C)	22,81	56,08	-29,85	-16,87	55,53	-11,43	53,57	-7,86	54,64	-6,87	21,45
LIAS 2 TEMP (°C)	22,56	55,8	-30,22	-18,21	54,09	-11,11	52,08	-7,6	54,28	-6,26	21,08
LIAS 3 TEMP (°C)	22,53	55,56	-31,29	-19,06	53,54	-12,38	51,68	-9,19	54,24	-6,99	20,72
LIAP 9 TEMP (°C)	22,56	55,71	-29,99	-13,83	57,1	-14,81	55,82	-11,05	54,53	-10,14	21,18
LIAP 8 TEMP (°C)	22,99	55,89	-29,56	-12,29	58,56	-15,69	57,36	-11,88	55,01	-11,01	21,5
LIAP 7 TEMP (°C)	22,63	55,51	-29,61	-11,94	58,88	-16,44	57,59	-12,55	54,67	-11,62	21,18
LIAP 6 TEMP (°C)	22,75	55,45	-29,36	-11,56	59,11	-16,7	58,01	-12,82	54,64	-11,94	21,25
LIAP 5 TEMP (°C)	22,78	55,59	-29,53	-11,72	59,25	-17,08	58,03	-13,2	54,73	-12,29	21,22
LIAP 4 TEMP (°C)	22,92	55,76	-11,72	-11,5	59,43	-17,17	58,27	-13,4	54,78	-12,58	21,45
LIAP 3 TEMP (°C)	22,5	55,25	-29,93	-11,63	58,91	-17,81	57,97	-14,23	54,12	-13,57	21,04
LIAP 2 TEMP (°C)	22,55	55,51	-30,07	-12,04	58,67	-18,01	57,77	-14,56	54,12	-13,94	21,21
LIAP 1 TEMP (°C)	22,75	55,6	-30,33	-12,85	57,85	-18,33	57,08	-15,3	53,85	-14,81	21,57

Table 8 LIA boards temperatures

The voltages remained nominal during the whole VTC cycle, that is :

BDAQ 5V = 5,1 V +/- 0,05 V
BDAQ 9V = 9,0 V +/- 0,05 V
BDAQ -9V = -9,0 V +/- 0,05 V

When LIAP ON,
LIAP 5V = 5,15 V +/- 0,05 V
LIAP 11V = 11,5 V +/- 0,05 V
LIAP -11V = -11,50 V +/- 0,05 V

When LIAS ON,
LIAS 5V = 5,2 V +/- 0,05 V
LIAS 11V = 11,5 V +/- 0,05 V

```
LIASP -11V = -11,5 V              +/- 0,05 V
```

9

BIAS generation tests

In this test, performed at each stabilized temperature level, we have set all the JFET BIAS (JFET Vdd, Vss and Heater BIAS) to their maximum and the BIAS amplitudes levels (PLW, PMW, PSW, PTC, SSW, SLW) to half maximum.

The results, as measured by the FPU simulator, are given in the thereafter table :

Parameter	Before VTC	At 50°C, last cycle	At -20°C, last cycle
P250 ampli (V)	64.341E-3	64.341E-3	64.341E-3
P250 freq (Hz)	201.348E+0	201.348E+0	201.348E+0
P350 ampli (V)	64.736E-3	64.656E-3	64.736E-3
P350 freq (Hz)	201.348E+0	201.348E+0	201.348E+0
PTC ampli (V)	128,069E-3	127.857E-3	127.857E-3
PTC freq (Hz)	201.357E+0	201.357E+0	201.357E+0
P500 ampli (V)	65.139E-3	65.139E-3	65.139E-3
P500 freq (Hz)	201.357E+0	201.357E+0	201.357E+0
SSW ampli (V)	89.234E-3	89.154E-3	89.154E-3
SSW freq (Hz)	201.368E+0	201.368E+0	201.368E+0
SLW ampli (V)	89.081E-3	89.001E-3	89.001E-3
SLW freq (Hz)	201.359E+0	201.359E+0	201.359E+0
Vdd1_P (V)	2.476E+0	2.476E+0	2.478E+0
Vss1_P (V)	-4.938E+0	-4.933E+0	-4.938E+0
Vdd2_P (V)	2.478E+0	2.478E+0	2.478E+0
Vss2_P (V)	-4.934E+0	-4.932E+0	-4.934E+0
Vdd3_P (V)	2.478E+0	2.478E+0	2.479E+0
Vss3_P (V)	-4.9356E+0	-4.935E+0	-4.935E+0
Vdd4_P (V)	2.477E+0	2.477E+0	2.477E+0
Vss4_P (V)	-4.935E+0	-4.933E+0	-4.935E+0
Vdd5_P (V)	2.477E+0	2.477E+0	2.477E+0
Vss5_P (V)	-4.936E+0	-4.935E+0	-4.936E+0
Vdd6_P (V)	2.479E+0	2.476E+0	2.478E+0
Vss6_P (V)	-4.935E+0	-4.936E+0	-4.933E+0
Vdd7_P (V)	2.478E+0	2.476E+0	2.476E+0
Vss7_P (V)	-4.938E+0	-4.933E+0	-4.934E+0
Vdd8_P (V)	2.476E+0	2.477E+0	2.479E+0
Vss8_P (V)	-4.931E+0	-4.928E+0	-4.935E+0
Vdd9_P (V)	2.477E+0	2.478E+0	2.478E+0
Vss9_P (V)	-4.935E+0	-4.930E+0	-4.935E+0
Vdd10_P (V)	2.478E+0	2.476E+0	2.478E+0
Vss10_P (V)	-4.933E+0	-4.933E+0	-4.935E+0
Vdd11_P (V)	2.476E+0	2.476E+0	2.476E+0
Vss11_P (V)	-4.934E+0	-4.934E+0	-4.934E+0
Vdd12_P (V)	2.477E+0	2.475E+0	2.477E+0
Vss12_P (V)	-4.935E+0	-4.933E+0	-4.932E+0
Vdd1_S (V)	2.475E+0	2.474E+0	2.473E+0
Vss1_S (V)	-4.931E+0	-4.926E+0	-4.928E+0
Vdd2_S (V)	2.474E+0	2.474E+0	2.474E+0
Vss2_S (V)	-4.924E+0	-4.929E+0	-4.927E+0
Vdd3_S (V)	2.475E+0	2.473E+0	2.473E+0
Vss3_S (V)	-4.929E+0	-4.926E+0	-4.925E+0
Vdd_TC (V)	2.478E+0	2.478E+0	2.478E+0
Vss_TC (V)	-4.938E+0	-4.933E+0	-4.939E+0
Nheater_P SW1(V)	-4.736E+0	-4.800E+0	-4.641E+0
Nheater_P SW2(V)	-4.703E+0	-4.770E+0	-4.612E+0
Nheater_P SW3(V)	-4.730E+0	-4.796E+0	-4.639E+0
Nheater_P MW1(V)	-4.731E+0	-4.792E+0	-4.642E+0
Nheater_P MW2(V)	-4.719E+0	-4.779E+0	-4.631E+0
Nheater_P LW1(V)	-4.723E+0	-4.783E+0	-4.634E+0
Nheater_S SW(V)	-4.948E+0	-4.950E+0	-4.948E+0
Nheater_S LW(V)	-4.947E+0	-4.948E+0	-4.947E+0
Nheater_TC (V)	-4.956E+0	-4.958E+0	-4.955E+0

We then check that the BIAS amplitudes, the BIAS frequencies, the Vdd level, the VSS levels and the Heater BIAS levels are consistent with the expected values and do not vary with the temperature.

10

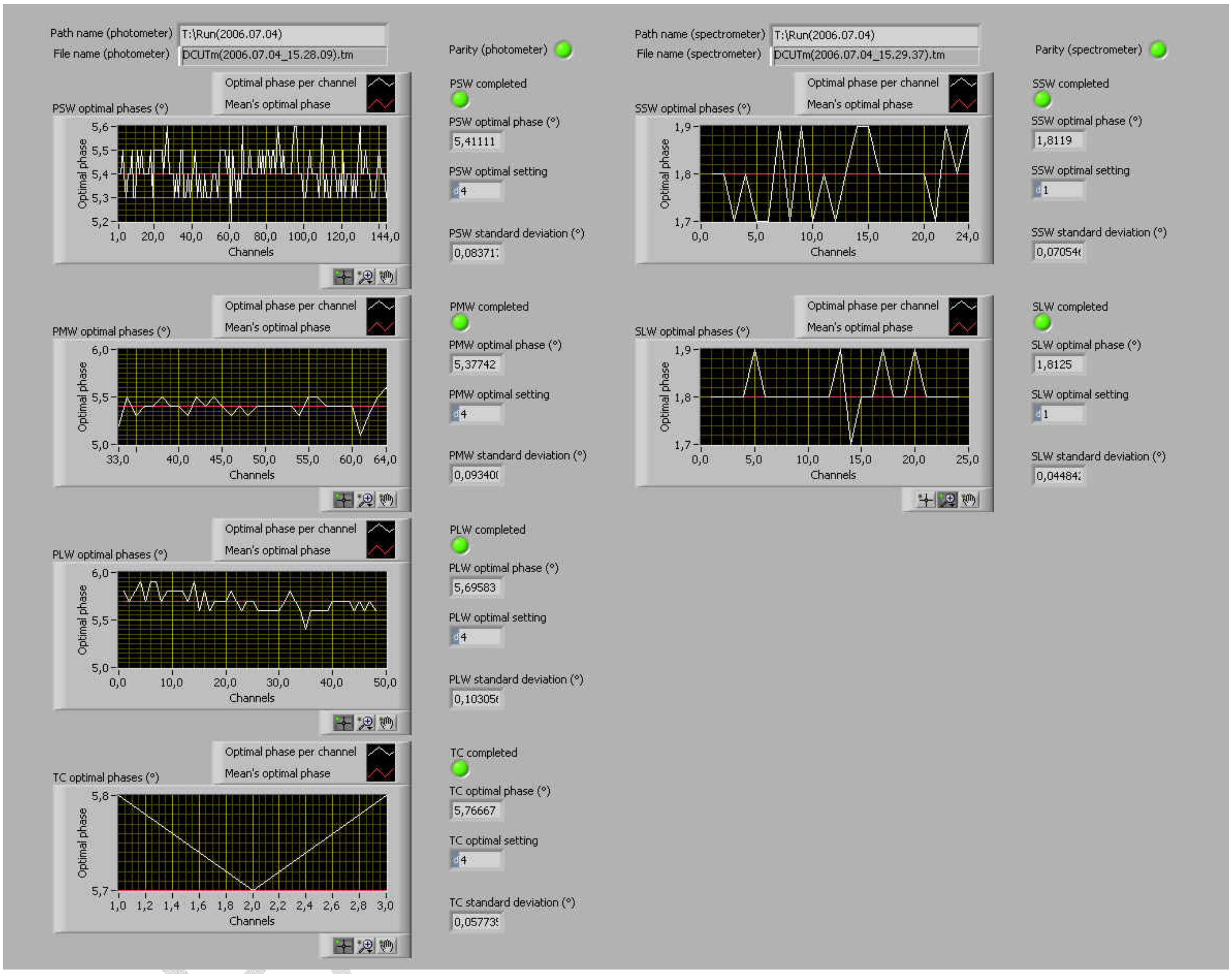
Demodulation Tests

We tested the optimal demodulation several times during the VTC cycling and observed no significant influence of the temperature on the optimal phase.

We thereafter represent the optimal phase as measured before the VTC cycling.

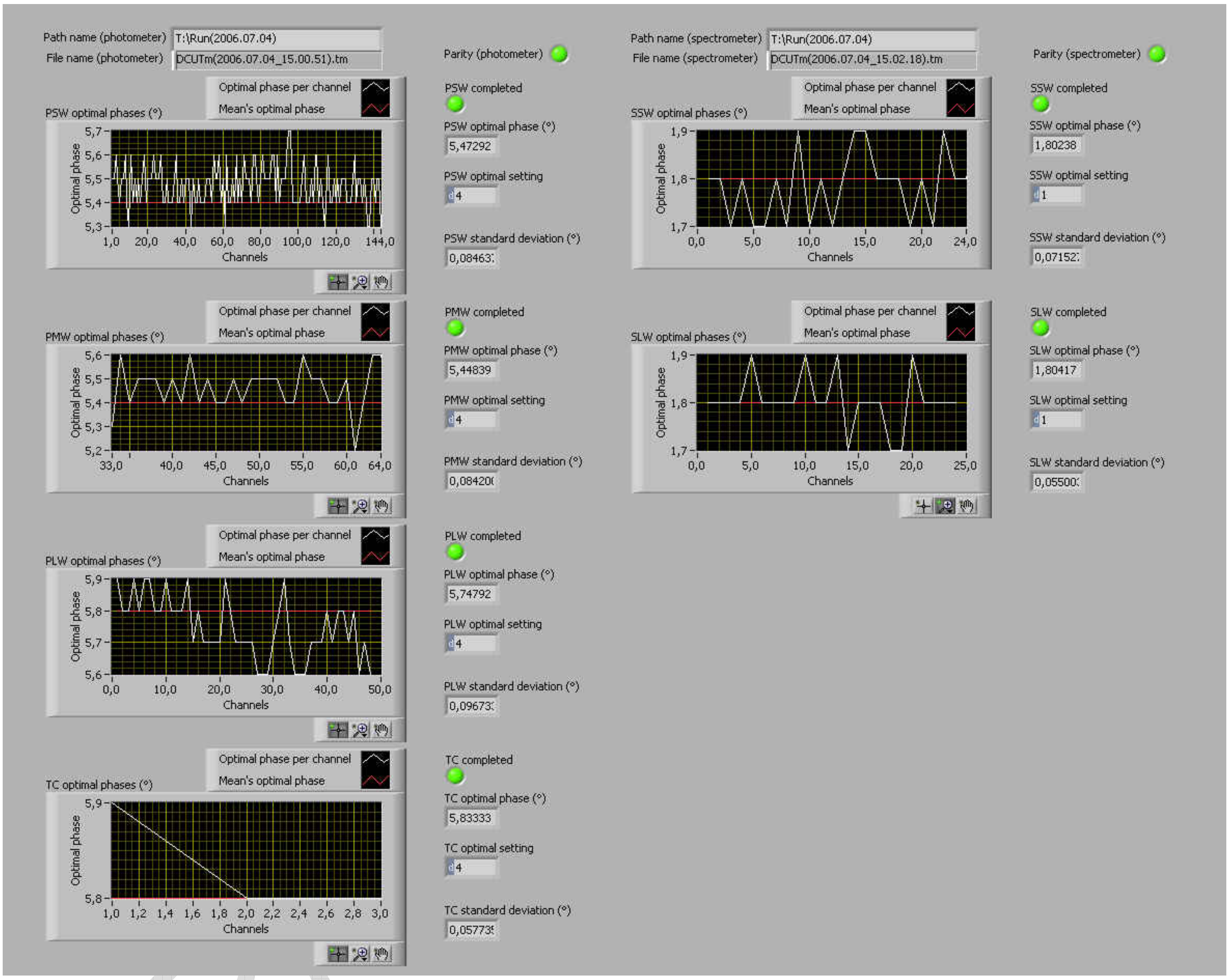
Optimal phase

Main side, before VTC



Optimal phase

Redundant side, before VTC



11 Gain Tests

The FPU simulator sends on all channels a sinusoïdal signal with a magnitude of 0,5 mV pic pic a and a frequency of 0,1 Hz modulated at 100 % (Offset = 0).

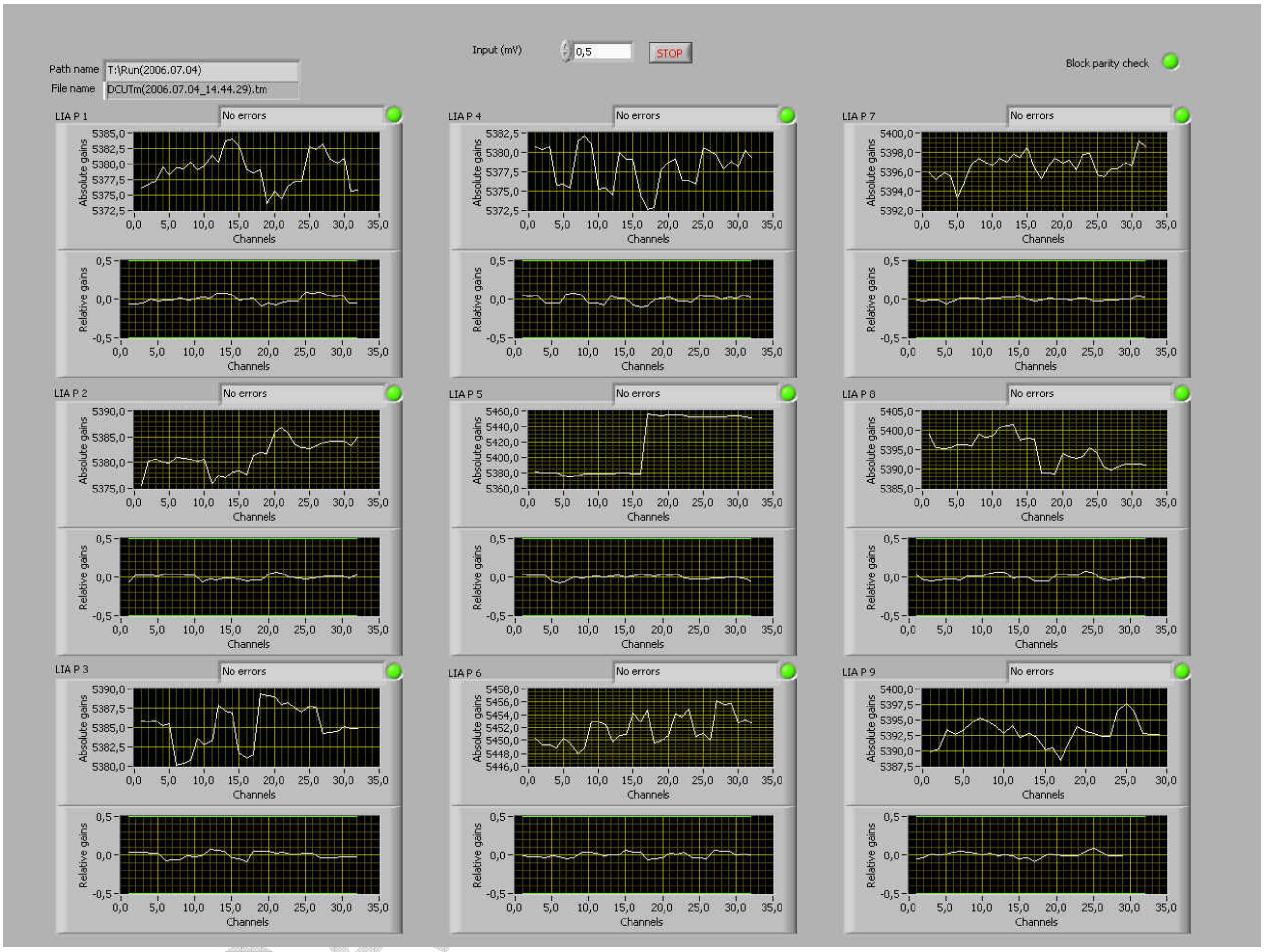
We show thereafter the graphics representing the gains obtained after the VTC tests, for each channel and per board.

We notice that the gains remain within the +/- 0,5% specified margin for all channels within a half board.

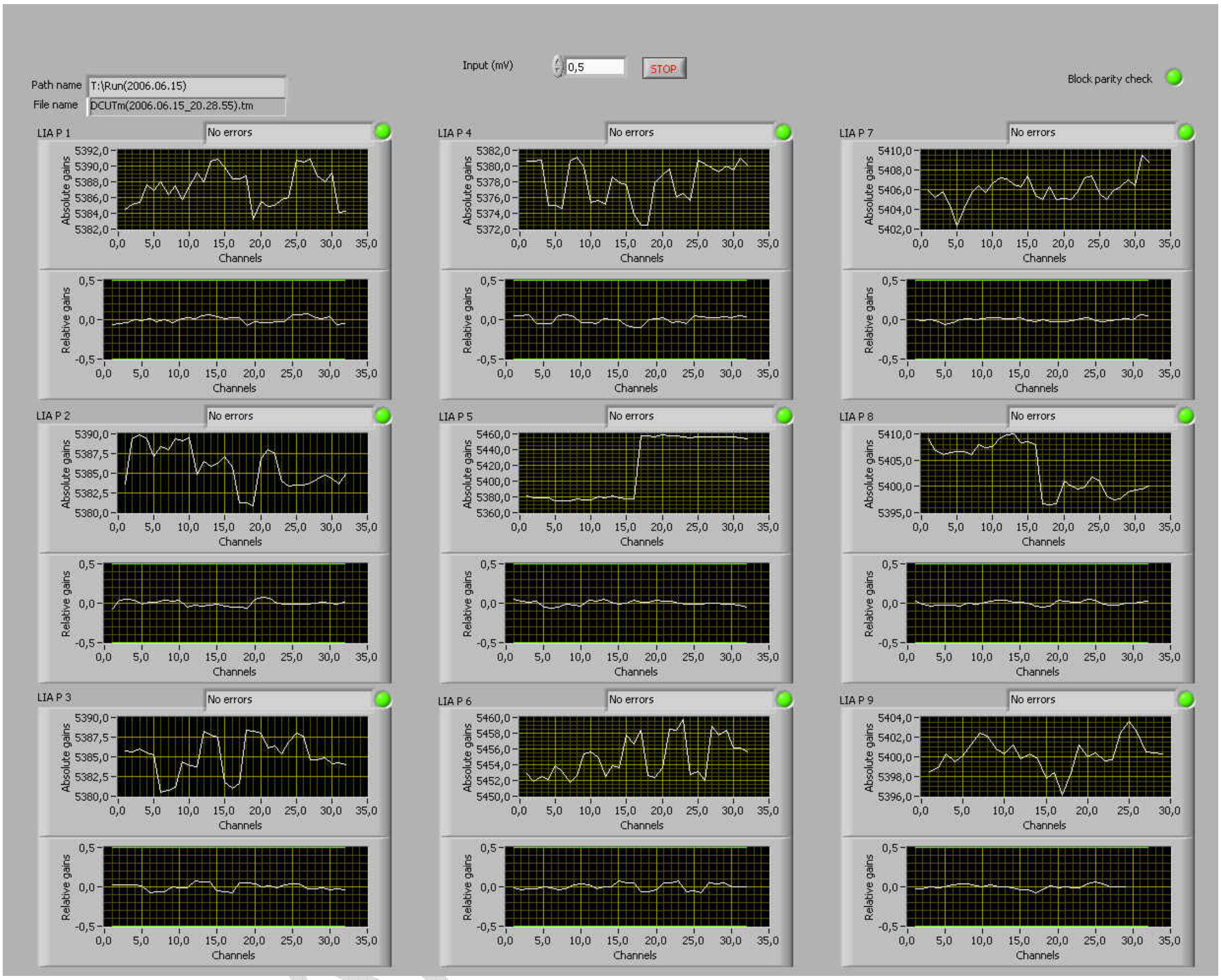
The gains of all the LIAP boards appear to be slightly different, which is probably due to the difference between the signals sent by the FPU simulator on the corresponding boards.

11.1 Photometer gains

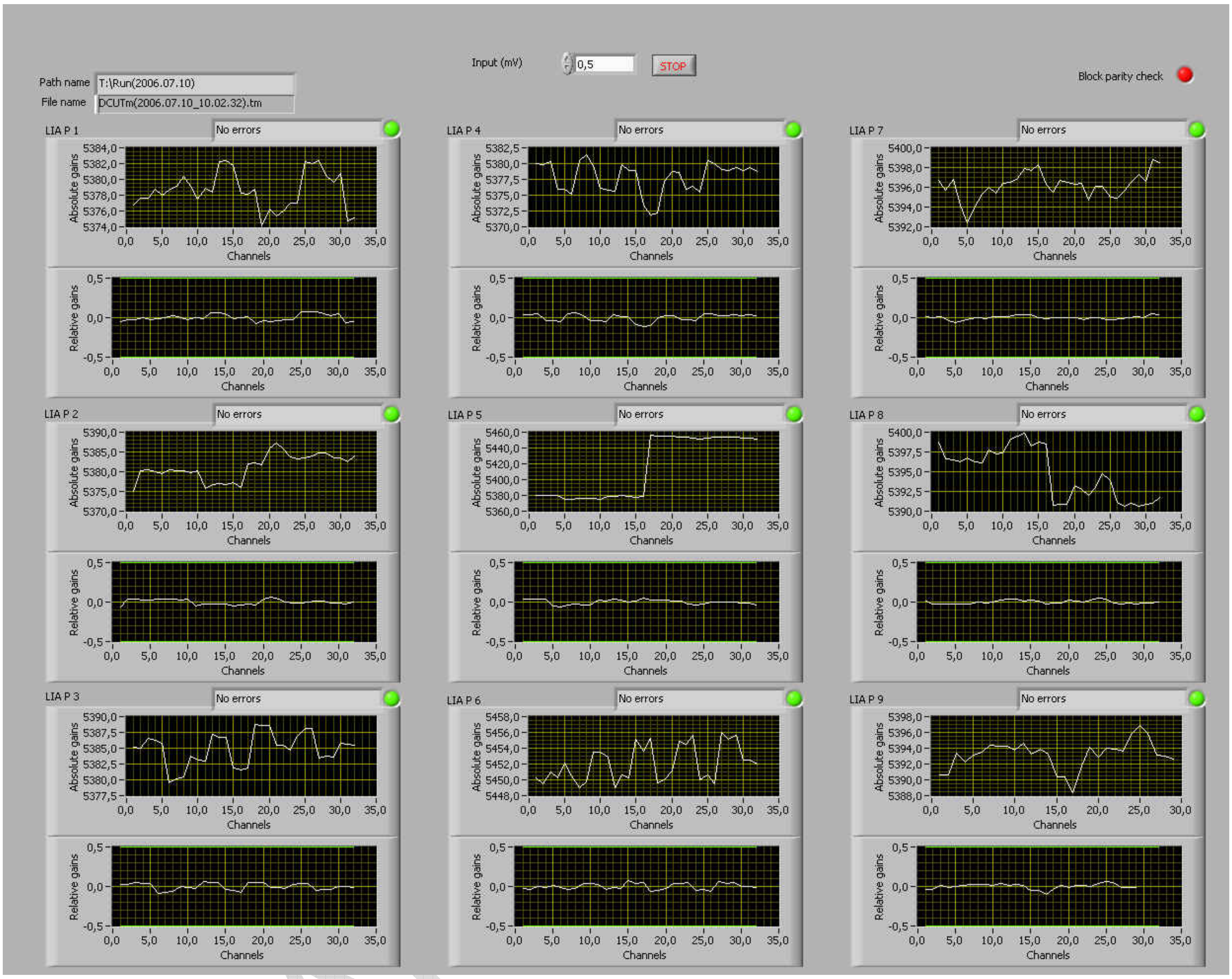
Before VTC, main side



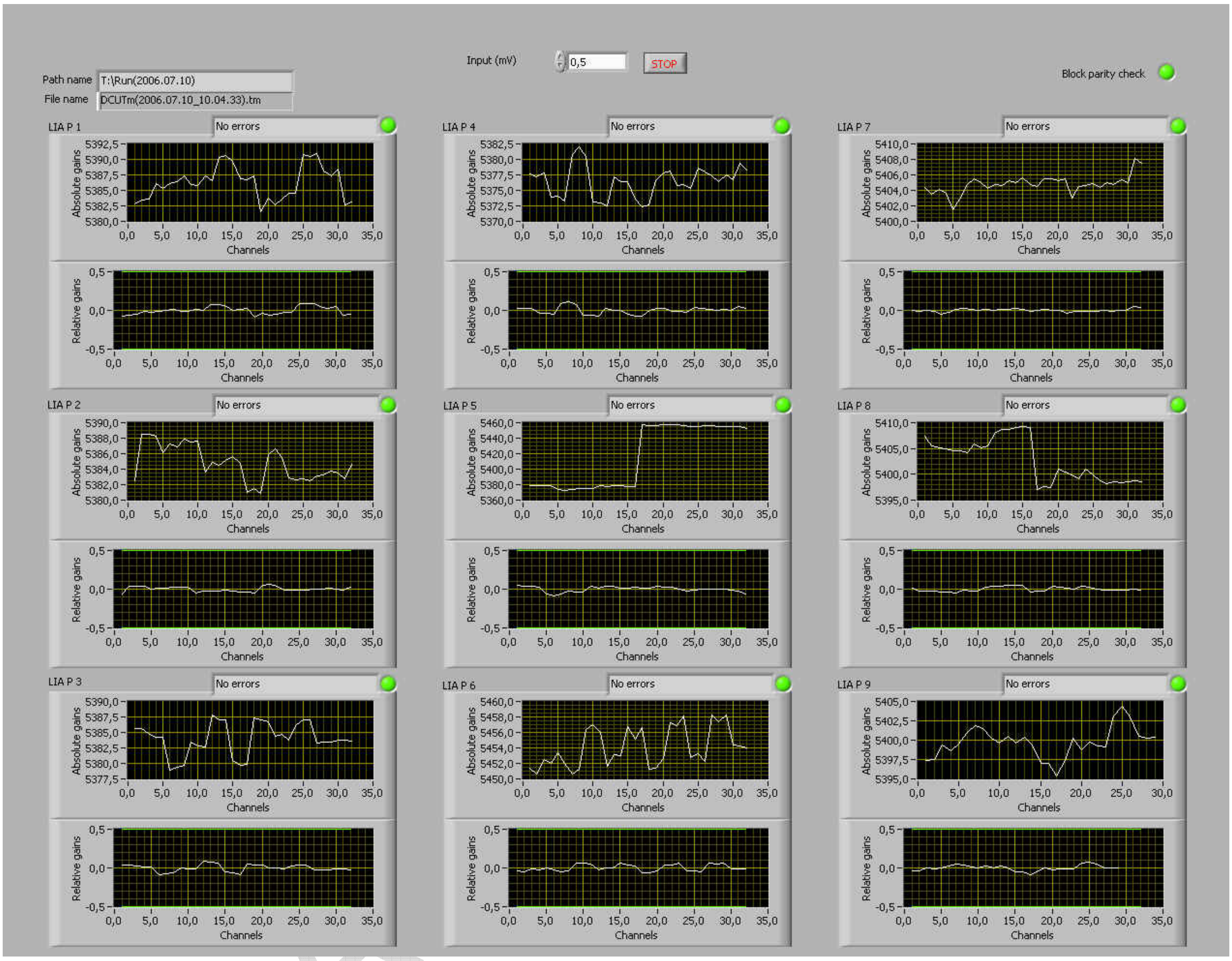
Before VTC, redundant side



After VTC, Main side



After VTC, Redundant side

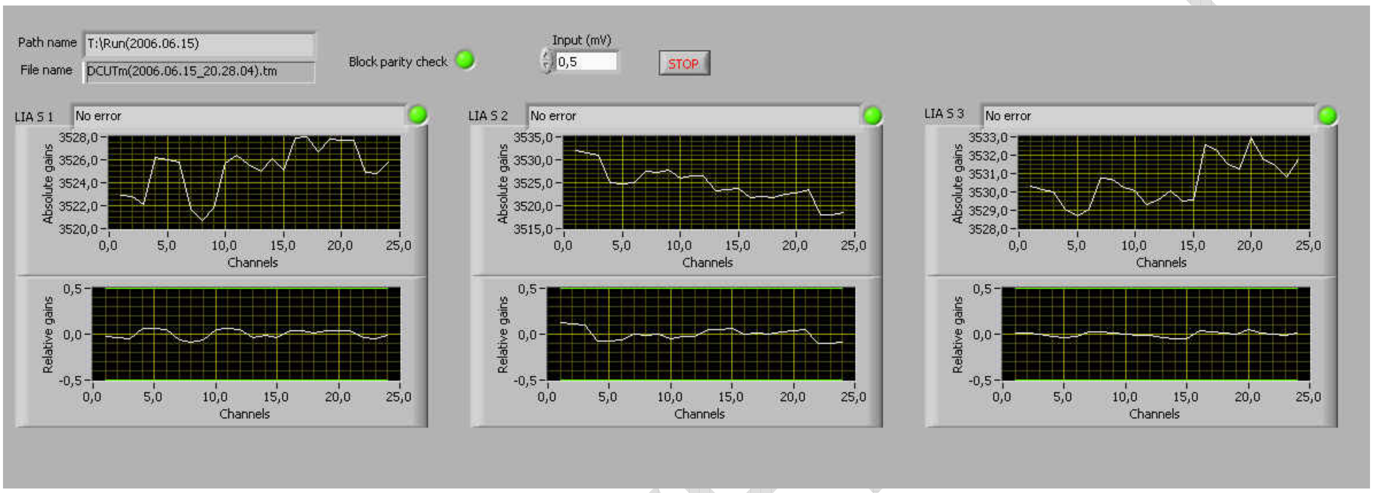


We notice no change in the photometer gain values due to the VTC tests

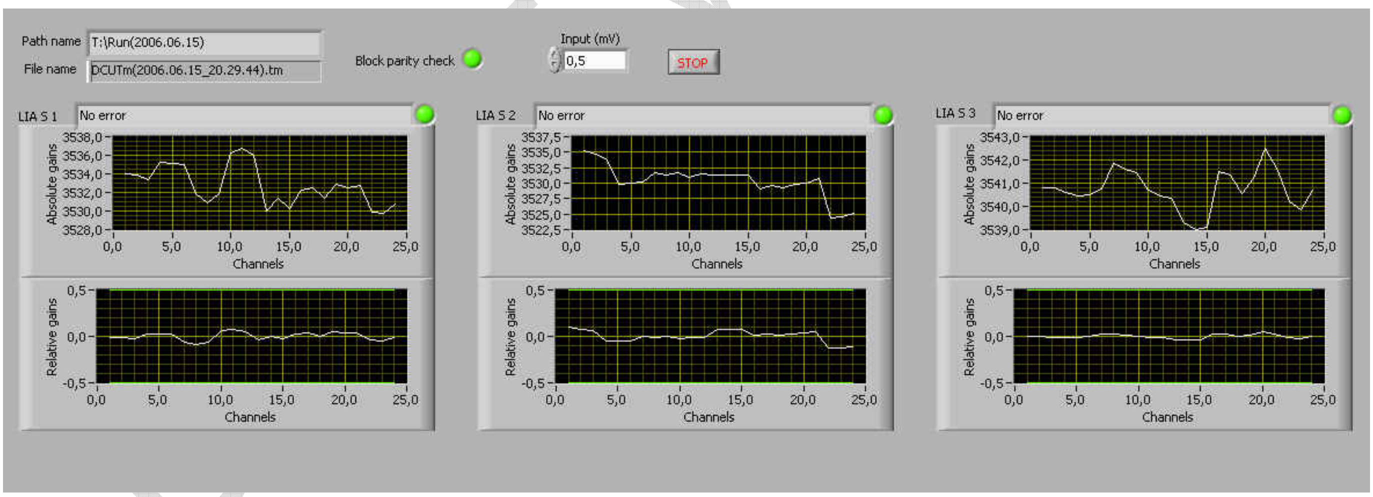
11.2 Spectrometer gains

Before VTC

Main side

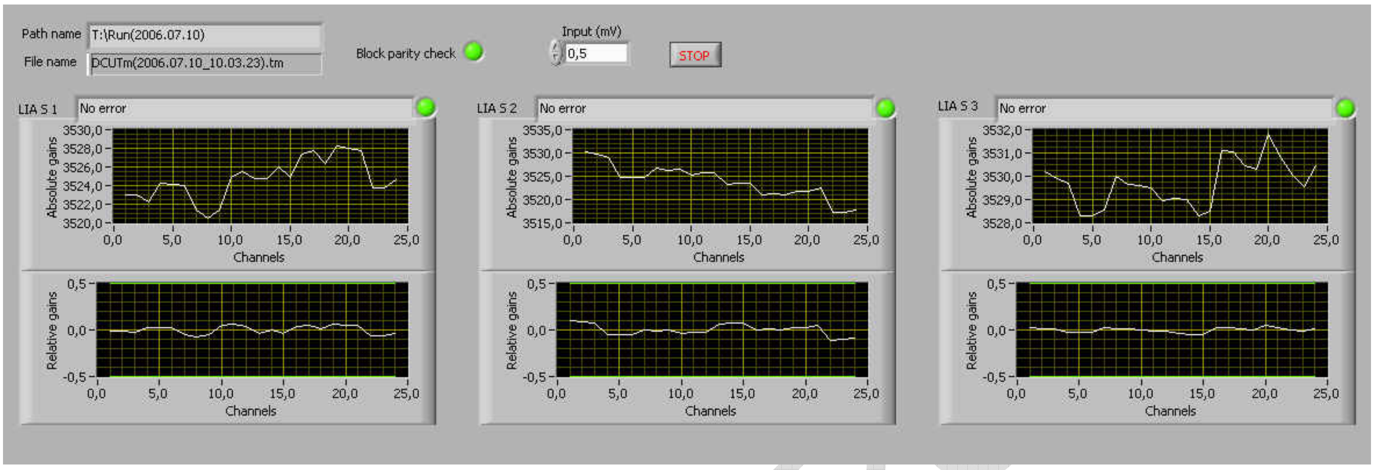


Redundant side

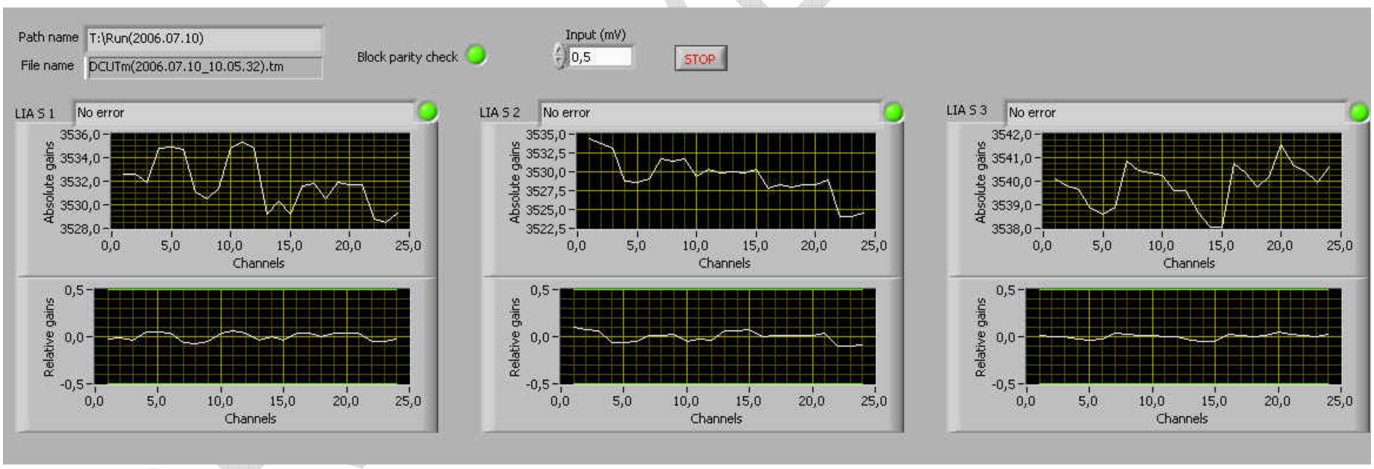


After VTC

Main side



Redundant side



We notice no change in the spectrometer gain values due to the VTC tests

11.3 Evolution of the gains with respect to the temperature

The thereafter table summarizes the gains as measured on DCU LIA boards (main side) during the VTC cycling.

Source / LIA Board	Test 0 20°C	Test 1 50°C	Test 2 -30°C	Test 3 -20°C	Test 4 50°C	Test 5 -20°C	Test 6 50°C	Test 7 -20°C	Test 8 50°C	Test 9 -20°C	Test 10 20°C
LIAS 1 GAIN	**3535**	3528	-	3520,8	3528	3521,2	3528,2	3523,5	3527,5	3521	3524
LIAS 2 GAIN	**3529,5**	3530	-	3519	3530	3519,5	3530	3520,5	3529	3520	3525
LIAS 3 GAIN	**3539,8**	3533,2	-	3523	3532	3522,8	3532,8	3521,3	3533,2	3523,2	3528,25
LIAP 9 GAIN	5393,5	5398,5	-	5384,5	5400	5384	5400	5384,5	5400	5383,8	5393
LIAP 8 GAIN	5396	5401	-	5389	5402	5388,8	5402,5	5389,5	5402,6	5388,5	5397
LIAP 7 GAIN	5393,5	5400	-	5384	5401	5384	5401	5384	5400	5384,5	5392,5
LIAP 6 GAIN	5450	5455,5	-	5443	5456	5442,5	5456,5	5443,5	5457	5444,5	5452
LIAP 5 GAIN channels 1 -16	5455	5456	-	5446	5461	5445	5462	5446	5460	5446	5455
LIAP 5 GAIN channels 17 -32	5375	5382	-	5365	5385	5365	5385	5365	5385	5365	5375
LIAP 4 GAIN	5375,5	5382	-	5365,5	5383	5364,3	5383,8	5366	5382,6	5365	5376
LIAP 3 GAIN	5385,5	5390,5	-	5377	5391	5377	5391	5377	5391	5377,5	5386
LIAP 2 GAIN	5380	5384	-	5372	5385	5370	5385	5372,5	5384,3	5372	5379,7
LIAP 1 GAIN	5378,5	5382,5	-	5371	5383	5369	5383,5	5371,5	5383,6	5370	5378

Table 11.3 LIA boards gains

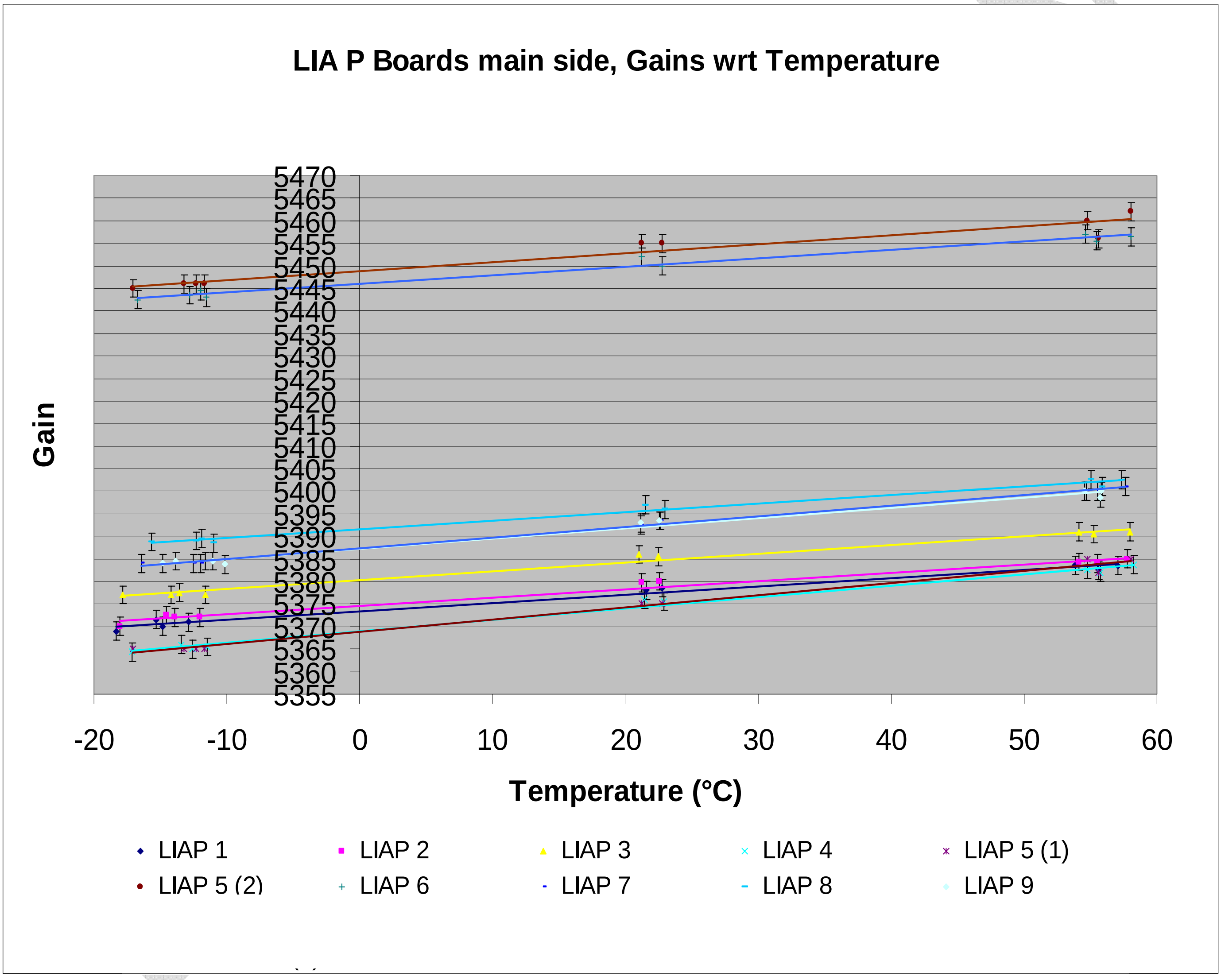
We notice that the gains slightly decreases at low temperatures and increase at high temperatures.

When we correlate this table with the table 8 (in chapter 8) that reports the boards temperatures, we can study the evolution of the boards gains with respect to their temperature.

For the photometer channels, the gain slope wrt temperature, as shown on the thereafter graphics is varies approximately as follows :

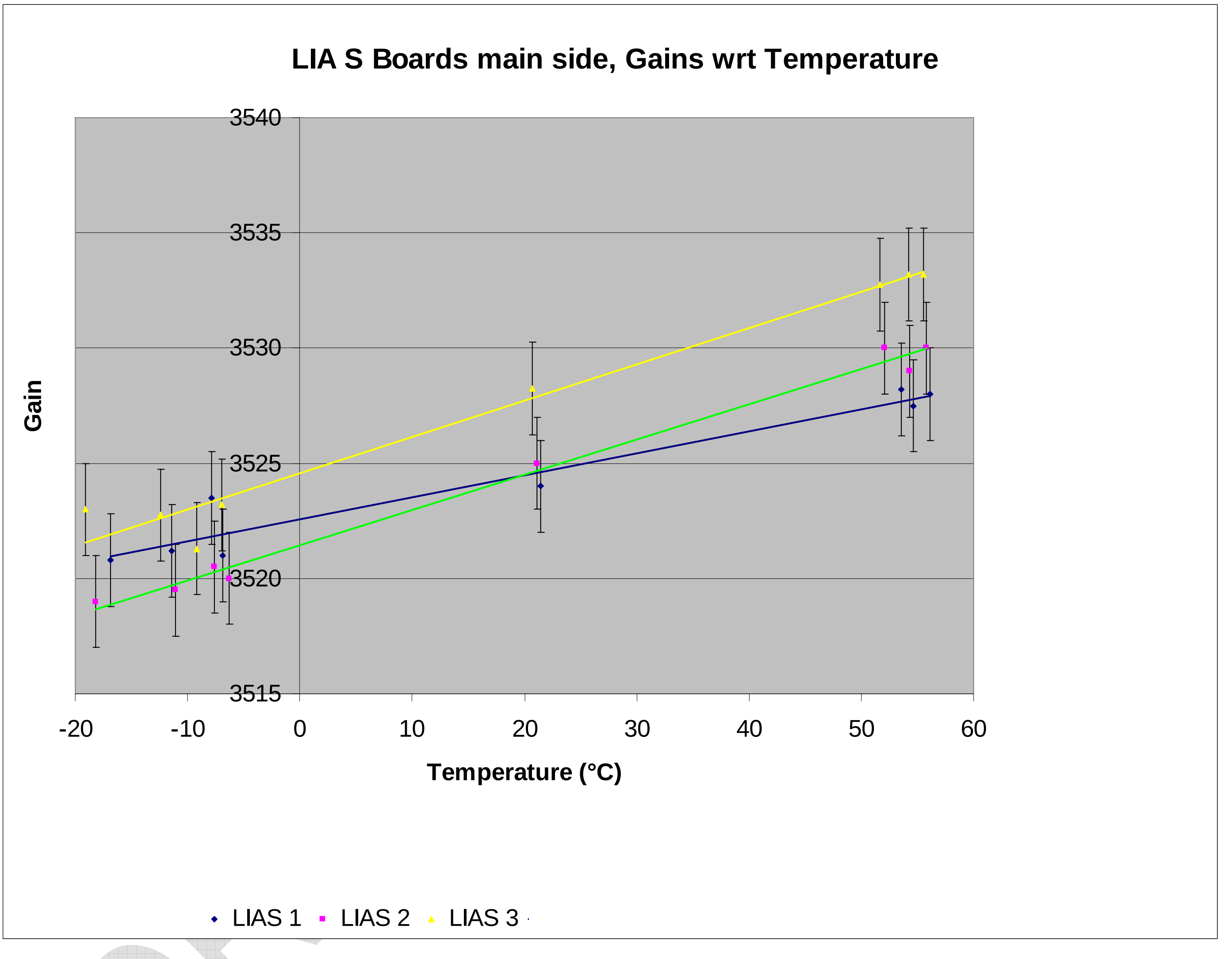
ΔG/G varies between 0,0037 % /°C and 0,0046 % /°C depending on the board.

The thereafter graphic is applicable to the photometer main side.



For the spectrometer channels, we measure the following gain evolution : $\Delta G/G$ = 0,0045 % /°C.

The thereafter graphic is applicable to the spectrometer main side.



The same behaviour has been observed on redundant side, the only difference is that the measured gain values are slightly different as we can see in the following table :

Gain Values at ambient temperature (20°C) [1,2, 3]	Main side	Redundant side
LIAP 1	5377,5	5387
LIAP 2	5379,5	5387,5
LIAP 2	5385	5385
LIAP 4	5375,5	5375
LIAP 5 (1 : channels 1:16/2 : channels 17:32)	5375/**5455**	5375/**5455**
LIAP 6	**5451**	**5455**
LIAP 7	5393	5403
LIAP 8	5397	5406
LIAP 9	5392,6	5401,5
LIAS 1	3525,5	3535,75
LIAS 2	3524,5	3530
LIAS 3	3528,75	3540,6

1 We measure the gain on each board (with reference value on channel 5 of each board, except for LIAP 5 where we take as reference the channels 5 and 20 that belong to the two half boards)

2 The gains difference between boards (or between two half boards as for LIAP 5) is due to the difference of signals sent by the FPU simulator to the DCU boards. This has been checked by inverting connectors.

3 We notice a slight gain difference of gains between main and redundant sides.

12 Offets

In this test, we use a simulator input file that consist in sinus signal with the same peak to peak level of 0,2 mV on all channels but at different magnitude levels (id est with different offsets) within the specified range. The purpose is then to check that the automatic offset function allows reading the signal within its specified magnitude range.

We perform signal acquisition using the FPU simulator script : Script_Spire_ScieNiveaux.spt
Simulator freq = 0.32 (0,08 Hz)

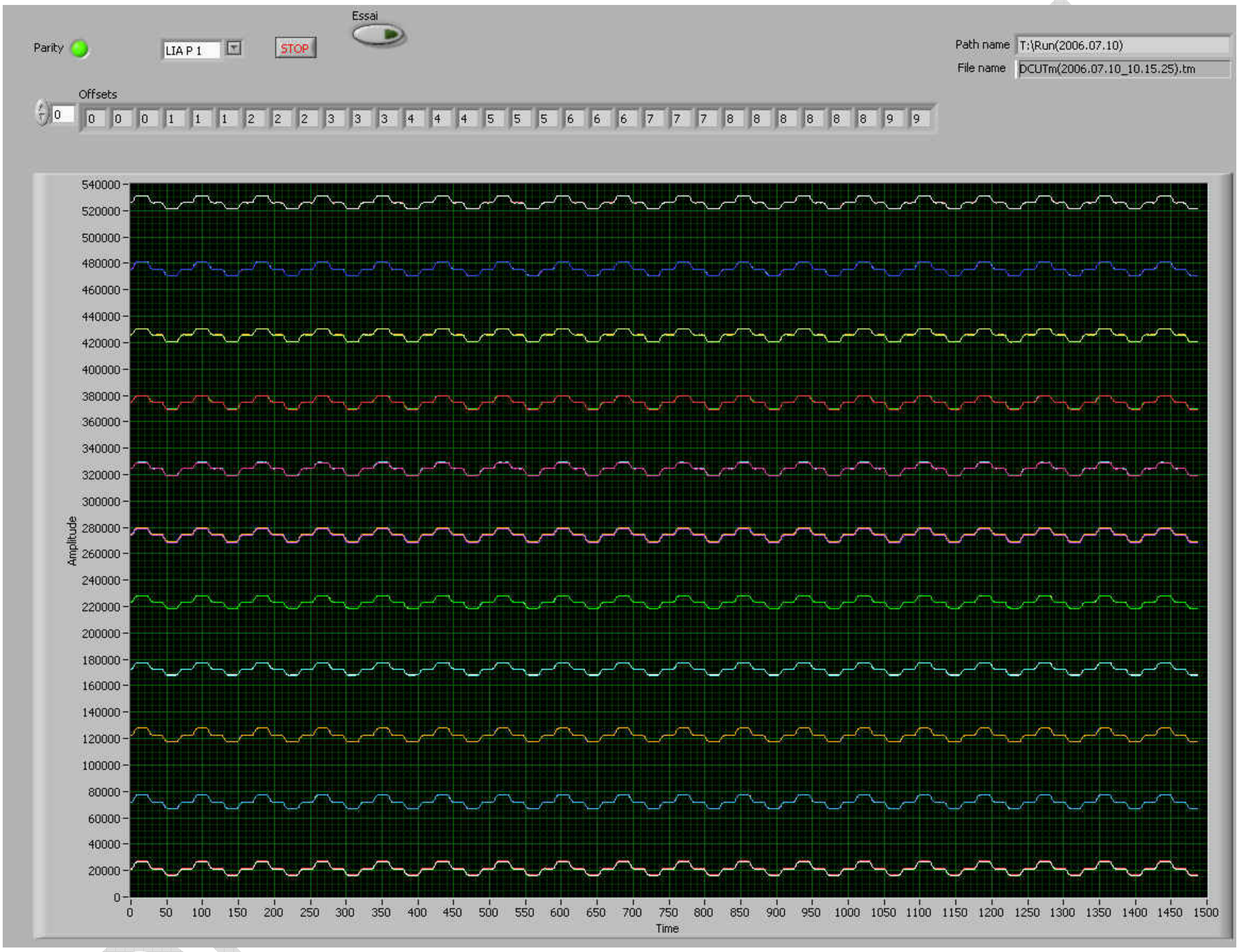
On LIA P boards as well as on LIAS boards, the same signal is sent on a group of 3 channels.

Offsets have been tested on each stabilized level during VTC cycling. We thereafter represent the results some significant obtained at the end of the VTC cycling on the DCU main side.

We thereafter represent the signal as read from TM files. The value of the offset has been added to the signal so as to differentiate the channels and to re create the signal.

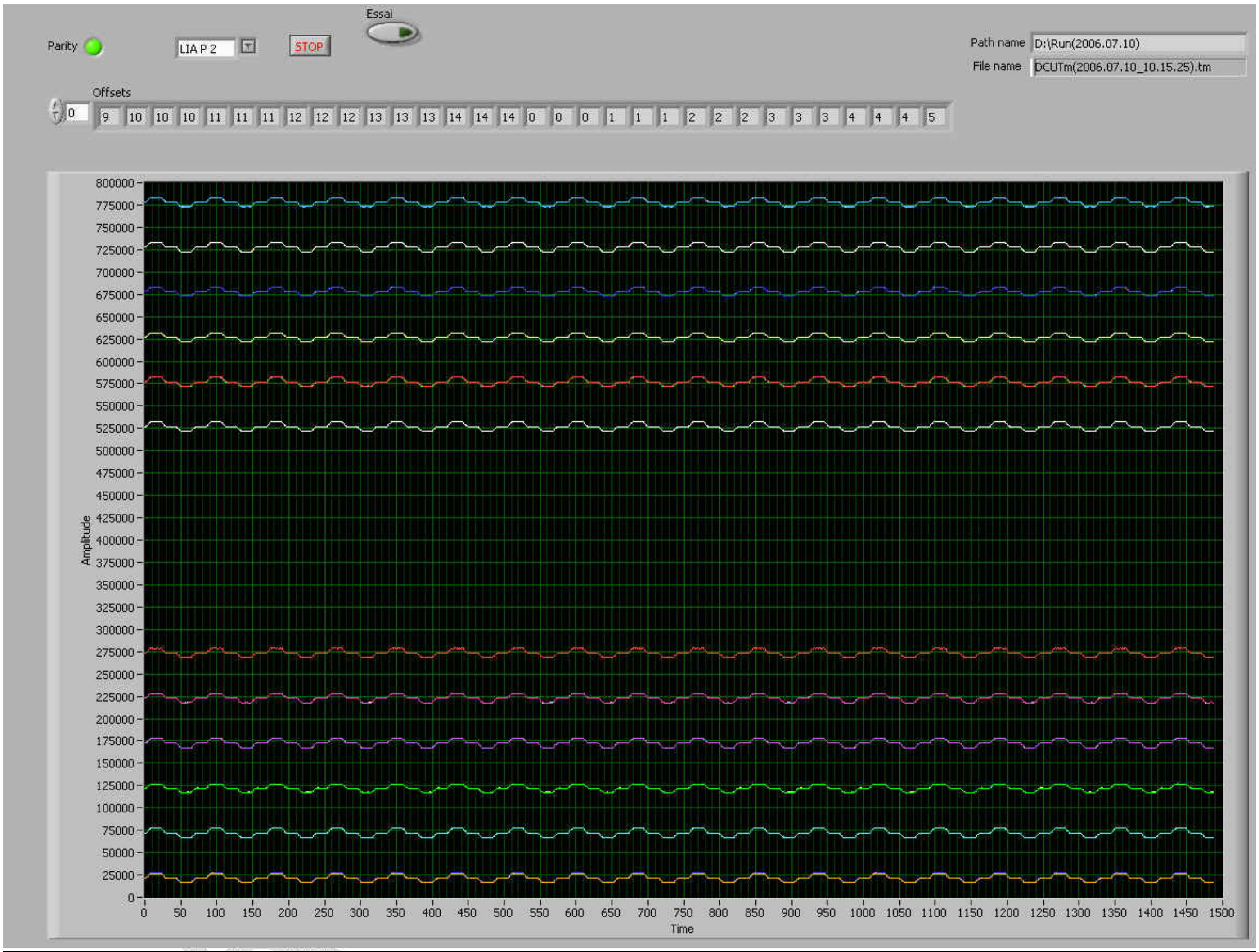
Offsets for LIAP 1 board.

The input signal here has an offset from 0 mV to 10 mV depending on the channels; the offset is automatically computed then added to the output signal in the thereafter representation. The value of the offset computed by DCU appears on the first line in the above graphics.



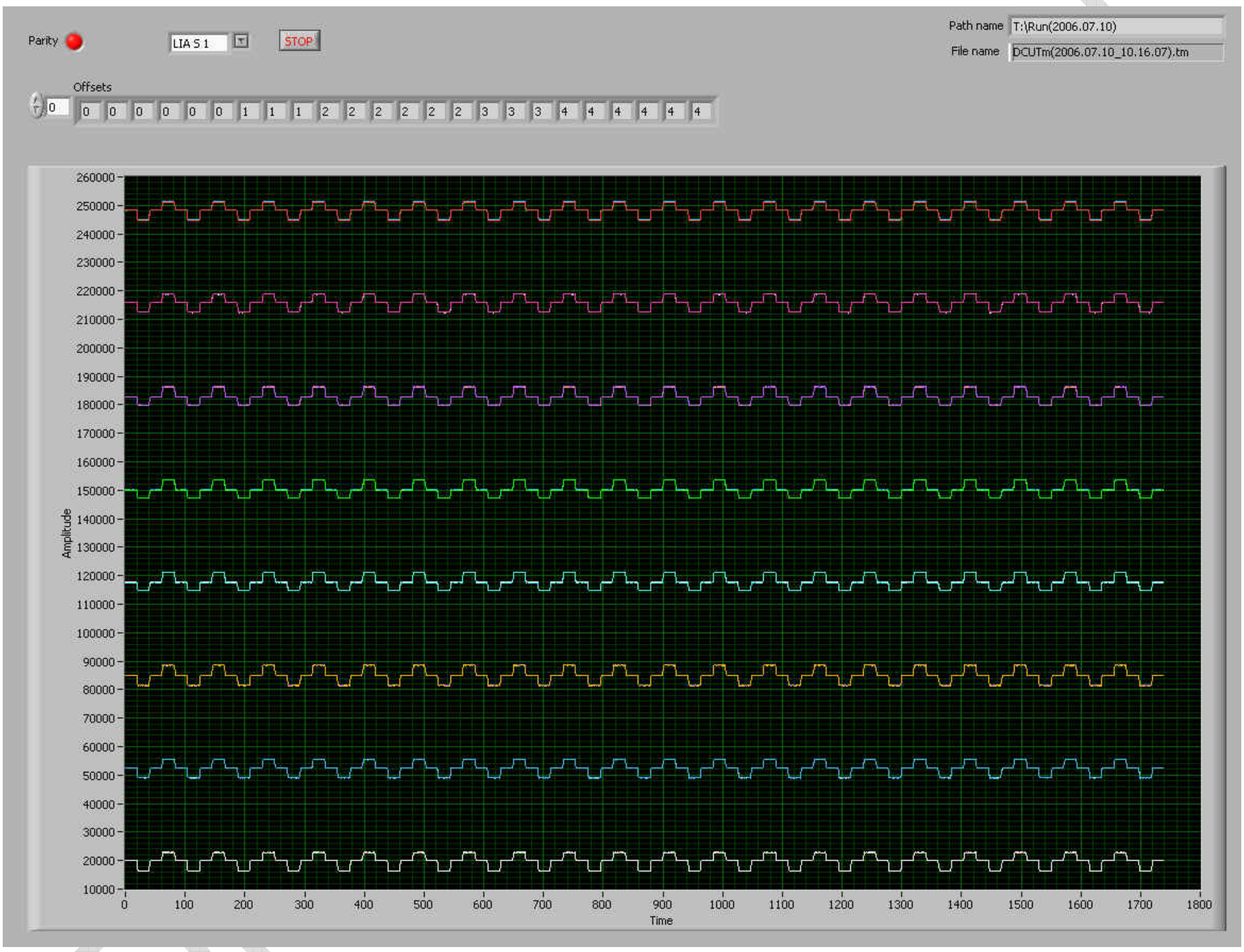
Offsets for LIAP 2 board.

The input signal here has an offset from 10 mV to 15 mV depending on the channels; the offset is automatically computed then added to the output signal in the thereafter representation. The value of the offset computed by DCU appears on the first line in the above graphics.



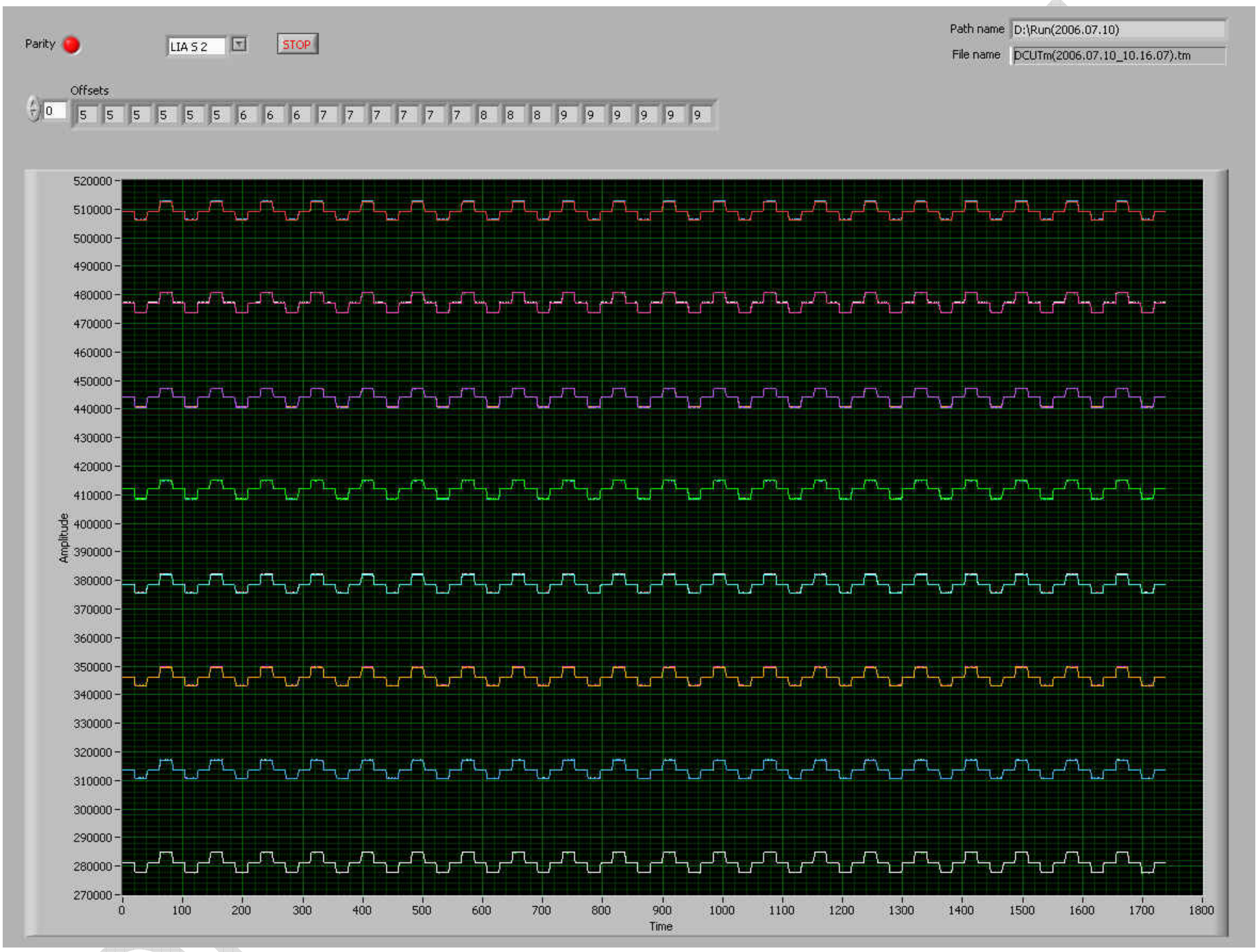
Offsets for LIAS 1 board.

The input signal here has an offset from 0 mV to 7 mV depending on the channels; the offset is automatically computed then added to the output signal in the thereafter representation. The value of the offset computed by DCU appears on the first line in the above graphics.



Offsets for LIAS 2 board.

The input signal here has an offset from 8 mV to 15 mV depending on the channels; the offset is automatically computed then added to the output signal in the thereafter representation. The value of the offset computed by DCU appears on the first line in the above graphics.



We notice that the offset function worked correctly within the acceptance temperature range and within the specified signal magnitude levels during the whole VTC tests.

13 Conclusion

The VTC tests on the HS DCU FM showed that :

- The gain vary slightly with the temperature : $\Delta G/G$ = 0,0045 % /°C for both photometer and photometer channels, which is acceptable.
- The power consumption remains stable with temperature
- The DCU remains fully functional at acceptance temperature levels
- No NCR has been issued from these tests