



SPIRE DCU FM ACCEPTANCE

Vibration Tests Report

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1 Abreviations list





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2 Applicable documents

[AD1] HERSCHEL/SPIRE DRCU Interface Control Document	SAP-SPIRE-CCa-075-02
[AD2] HERSCHEL/SPIRE DRCU/DPU Interface Control Document	SAP-SPIRE-CCa-076-02
[AD3] Herschel/SPIRE DRCU AIV PLAN	SAp-SPIRE-HT-0082-02
[AD4] HERSCHEL/SPIRE DRCU Subsystem specification	Sap-SPIRE-CCa-0025-00
[AD5] Herschel/Planck Instrument Interface Document IID Part A "	SCI-PT-IIDA/SPIRE-04624
[AD6] Herschel/Planck Instrument Interface Document Part B Instrument "SPIRE"	SCI-PT-IIDB/SPIRE-02124
[AD7] Herschel SPIRE Detector Subsystem Specification Document	SPIRE –JPL-PRJ-000456
[AD8] HS_DCU FLIGHT MODEL (FM) functional tests procedure	SAp-SPIRE-HT-0387-06
[AD9] HSDCU FM Procédure de vibration	SAp-SPIRE-TT-0400-06

3 <u>Reference documents</u>

[RD1] HERSCHEL/SPIRE DCU EM/QM1 Test Report	Sap-SPIRE-CCa-0129-03 Issue 1.0
[RD2] DS-SPIRE development tree	Sap-SPIRE-DS - Version 07/03/2002
[RD3] FIRST/SPIRE DRCU and WIH Development	SAP-SPIRE-JLA-0047-01
Plan	
[RD4] HSDCU FM Mechanical Tests report	Intespace Reference E5831
[RD5] HS-DCU FM TRR Report	SAp-SPIRE- QA-0418-06





4 Introduction

This technical report applies to the Vibration tests performed on the DCU FM equipment for the HERSCHEL SPIRE Project.

These tests have been performed at Intespace between June 12th 2006 and June 15th 2006.

5 Test Configuration

We use the LTU in its latest software configuration, the fully assembled DCU and FCU, the FPU and the PSU Flight Model (PSU FM).

Before to connect any harness, we place savers on all connectors

Connect all harnesses as described below :

- Between DCU and FPU
- Between DCU and LTU
- Between SCU and LTU
- Between DCU and PSU FM
- Between SCU and PSU FM

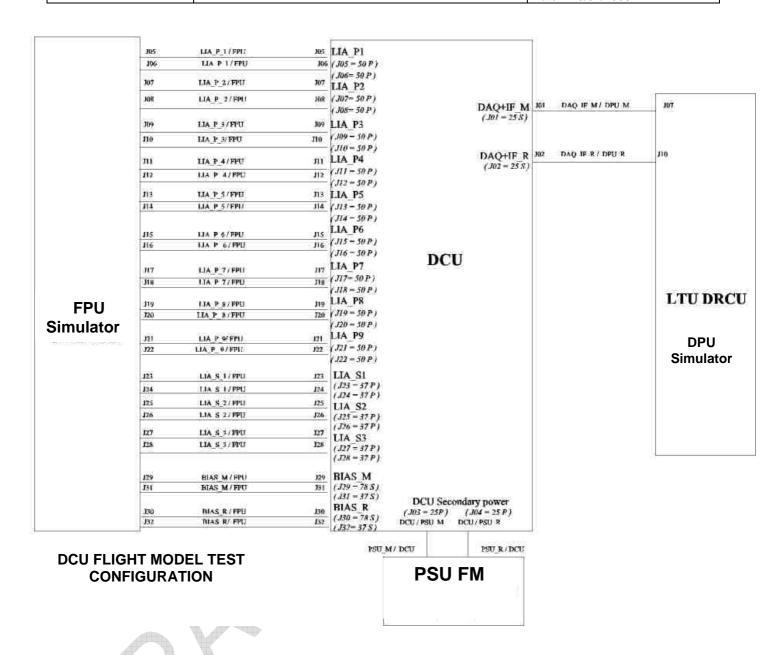


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DCU FM vibrations test configuration

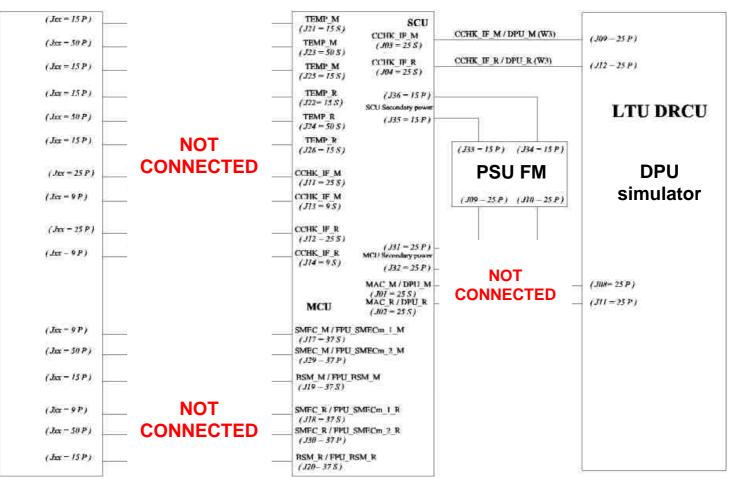


FCU



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FPU simulator





DCU FM vibrations test configuration





6 Test Program

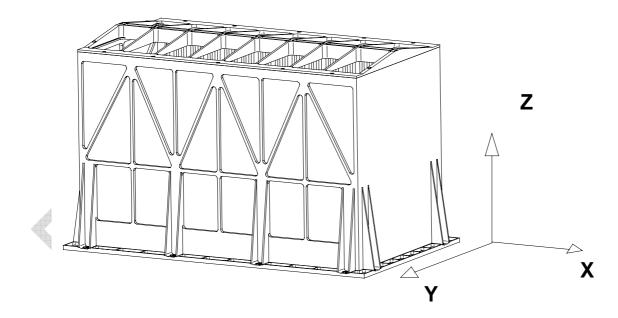
The description of the vibration test is given in the vibration tests procedure [AD9].

The DCU is mounted on the shaker through a rigid interface (f >2 kHz). We apply on this interface the specified vibration levels.

Before and after applying these levels, we apply acceptance sinus and random levels that show the DCU eigen frequencies of the structure. By comparison of the dynamic signatures (low level sinus) of the DCU before and after the tests, we check its structural integrity.

The tests are performed on **Z**,**X**,**Y** axes successively in the reference frame given in [AD9].

An additional vibration on X axis has also been performed at protoflight level.







Preliminary tests have been performed on the interface plate of the shaker before mounting the DCU on it.

Before to start the vibration procedure and after the vibrations applied on each axis, we perform a full functional test following the functional test procedure [AD8].

The sequence, which is the same on each axis, is as follows :

Test	
Functional test	Refer to [AD8]
Low level Sinus	Described in § 6.1 of [AD9]
Acceptance level Sinus	Described in § 6.2 of [AD9]
Random low level	Described in § 6.3 of [AD9]
Random qualification level	Described in § 6.4 of [AD9]
Low level Sinus	Described in § 6.1 of [AD9]
Functional test	Refer to [AD8]

For representativity reasons (with respect to DCU QM2 qualification model), a complementary test has been performed on X axis at "protoflight" level.

The results of the mechanical tests are given in the next chapter.

The results of the functional tests are given in the chapter 8.





7 Report of the mechanical tests

It consists in the analysis of the response of the structure to the applied vibration levels. All the data relative to these tests are given in the test report from Intespace referenced as [RD4].

The comparison of the low level sinus response before and after the vibration applied on each axis is being analyzed thereafter.

We look for eigen frequencies and associated magnitudes and check their shift following the test (frequency shift should be lower than 5%). We also test that all eigen frequencies are above 150 Hz.

Vibration on Z axis







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Vibration on X axis









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Vibration on Y axis







The data given in the test report [RD4] show that :

Considering the magnitude of the response levels, the safety margins, with respect to qualification model are :

- on X axis : 0,9 at acceptance levels
- on Y axis : 1,10 at acceptance levels
- on Z axis : 1,42 at acceptance levels

This results, which shows that the levels measured during acceptance vibrations tests were above these measured at qualifications one. For representativity reasons, it has then been decided to make an additional vibration tet on X axis at protoflight level.

We then obtain a safety margin on X axis of 1,16 at protoflight levels

The signatures remain the same as for qualification level (frequency shift lower than 5% as specified) on X and Z axis.

The frequency shift on Y axis is of about 10% which remains acceptable. This frequency shift might be due to the rearrangement of the racks that sustain the boards. As a matter of facts there is a shearing constraint, located where the racks are tightened, on this axis.

For all the graphics showing the responses to the vibration levels, refer to [RD4].





Report of the functional tests 8

The purpose of the tests performed between vibrations on eaxch axis is to check that the DCU FM remains functionsl. Therefore, no performance tests have been performed at during these tests.

The list of the performed test, with reference to [AD8] is :

the performed test, with reference to [AD8] is :					
DCU QM2 tests	Preliminary : before vibrations	After Z and X axis	Final (after Y axis)	After protoflight levels on X axis	
Consumption (redundant)	x	X	x	x	
Consumption (main)	X	X	X	X	
Frame generation					
HK acquisition	x	X	x	X	
BIAS					
BIAS stand alone				x	
Optimum phase	X				
Batch edition	x				
Gains	x	x	х	x	
Cross talk					
Noise			x	x	
Offset			x	x	
Bandwidth					

In this document, only the main results are given.





8.1 Visual inspection

A visual inspection was performed after each axis. It revealed no specific problem.

8.2 Consumption tests

The consumption measured at PSU FM level on DCU main side are :

Before vibrations

Conso 28 V	DCU mair	ı,	DCU r	edundant
ON	100		400	
ON	400 mA	A	400	mA
MCU On	810 mA	A	810	mA
MCU On booté	870 mA	A	870	mA
MCU Off & LIAP ON	1610 mA	4	1610	mA
MCU Off & LIAS ON	1160 mA	A	1160	mA

After Z axis vibrations

Conso 28 V	DCU	main,	DCU	redundant
ON	400	mA	400	mA
MCU On	810	mA	810	mA
MCU On booté	870	mA	870	mA
MCU Off & LIAP ON	1610	mA	1610	mA
MCU Off & LIAS ON 🥒	1160	mA	1160	mA

After	Х	axis	vibrations	
				4

ON	400	mA	400	mA
MCU On	810	mA	810	mA
MCU On booté	870	mA	870	mA
MCU Off & LIAP ON	1610	mA	1610	mA
MCU Off & LIAS ON	1160	mA	1160	mA

After Y axis vibrations

ON	400	mA	400	mA
MCU On	810	mA	810	mA
MCU On booté	870	mA	870	mA
MCU Off & LIAP ON	1590	mA	1590	mA



1160 mA



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MCU Off & LIAS ON 1160 mA

After X axis vibrations (protoflight level)

Conso 28 V	Main	Redundant	4
ON	400 mA	400 mA	
MCU On	810 mA	810 mA	
MCU On booté	870 mA	870 mA	
LIAP ON	2100 mA	2090 mA	
LIAS ON	1190 mA	1220 mA	

The consumptions did not move following the vibrations.

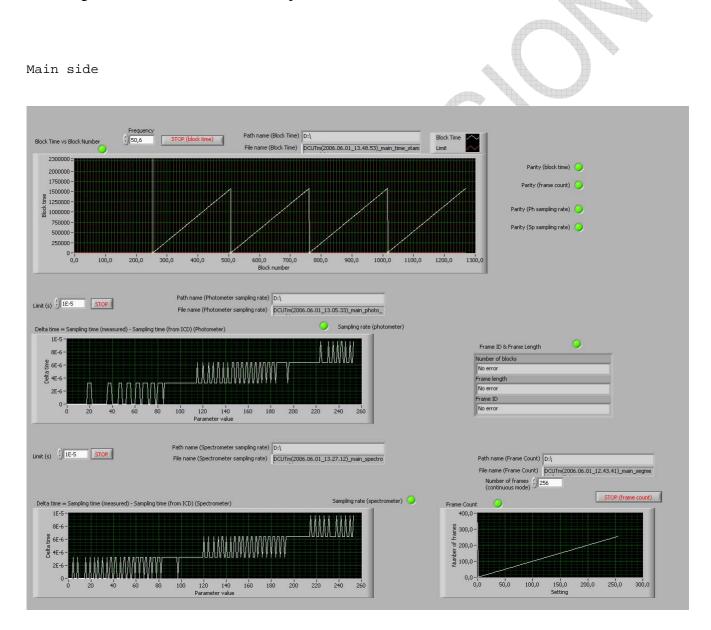




8.3 Frame generation Tests

The test consist in testing the frame generation (frame length, frame modes, frames content and ID), It also tests the reset of the time stamp within the frames, the frame generation frequencies (photo and spectro) as well as the number of frames commanded during telemetry acquisitions.

The results obtained are the same after vibrations than before. These are summarized in the following screenshot relative to the tests performed before the vibrations.

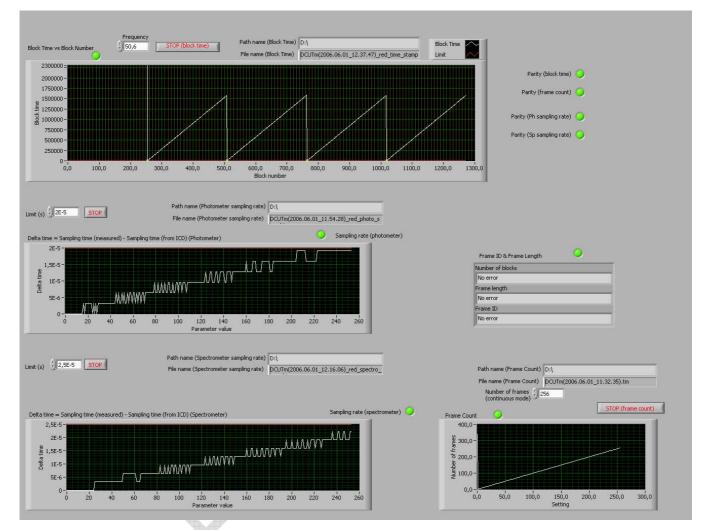






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Redundant side









8.4 HouseKeepings

We have started the DCU Monitoring Mode from LTU (1 Hz frequency) after each vibration test (each axis) and the results were consistent with the expected values. Note that we observe the results over a sufficient time (1 minute).

We thereafter show the results relative the H/K acquisitions performed after the vibrations :

When LIAP ON,

Main

Nom Parametre	Description	Valeur C	Min	Max	Unite
BIAS_TEMP	BIAS board Temp	22.87	-31.01	70.01	C
LIA_S1_TEMP	LIAS board 1 Temp	22.78	-31.01	70.01	°C
LIA_S2_TEMP	LIAS board 2 Temp	22.37	-31.01	70.01	°C
LIA_S3_TEMP	LIAS board 3 Temp	21.98	-31.01	70.01	°C
LIA_P9_TEMP	LIAP board 9 Temp	22.55	-31.01	70.01	°C
LIA_P8_TEMP	LIAP board 8 Temp	22.92	-31.01	70.01	ດໍດໍດໍດໍດໍດໍດໍດໍດໍດໍດໍ
LIA_P7_TEMP	LIAP board 7 Temp	22.60	-31.01	70.01	°C
LIA_P6_TEMP	LIAP board 6 Temp	22.75	-31.01	70.01	°C
LIA_P5_TEMP	LIAP board 5 Temp	22.63	-31.01	70.01	°C
LIA_P4_TEMP	LIAP board 4 Temp	22.81	-31.01	70.01	°C
LIA_P3_TEMP	LIAP board 3 Temp	22.41	-31.01	70.01	°C
LIA_P2_TEMP	LIAP board 2 Temp	22.55	-31.01	70.01	°C
LIA_P1_TEMP	LIAP board 1 Temp	22.79	-31.01	70.01	°C
DAQ_IF_TEMP	DAQ_IF board Temp	23.10	-31.01	70.01	
BDAQ_P5	BIAS/DAQ_IF +5V(before post regu	5.11	4.90	5.26	V
BDAQ_P9	BIAS/DAQ_IF +9V(before post regu	8.96	8.50	9.10	V
BDAQ_N9	BIAS/DAQ_IF -9V(before post regul	-9.04	-9.10	-8.50	V
LIAP_P5	LIAP +5V(before post regulator)	5.16	4.90	5.27	V
LIAP_P9	LIAP +9V(before post regulator)	11.51	11.20	11.60	V
LIAP_N9	LIAP -9V(before post regulator)	-11.53	-11.60	-11.20	V
LIAS_P5	LIAS +5V(before post regulator)	0.09	4.90	5.26	V
LIAS_P9	LIAS +9V(before post regulator)	0.12	11.20	11.60	V
LIAS_N9	LIAS -9V(before post regulator)	0.01	-11.60	-11.20	V
PWR_STATUS	LIA1 to LIA12 12 +5V/+9V/-9V status	0000	0.00	0.00	hexa
T/C_1	16 bits ADC (Offset=0) 1	2207			Decimal
T/C_2	16 bits ADC (Offset=0) 2	4159			Decimal
T/C_3	16 bits ADC (Offset=0) 3	251			Decimal



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Redundant

Nom Parametre	Description	Valeur C	Min	Max	Unite
BIAS_TEMP	BIAS board Temp	22.63	-31.01	70.01	°C
LIA_S1_TEMP	LIAS board 1 Temp	22.29	-31.01	70.01	°C
LIA_S2_TEMP	LIAS board 2 Temp	22.35	-31.01	70.01	°C
LIA_S3_TEMP	LIAS board 3 Temp	22.18	-31.01	70.01	°C
LIA_P9_TEMP	LIAP board 9 Temp	22.84	-31.01	70.01	°C
LIA_P8_TEMP	LIAP board 8 Temp	22.56	-31.01	70.01	°C
LIA_P7_TEMP	LIAP board 7 Temp	22.53	-31.01	70.01	°C
LIA_P6_TEMP	LIAP board 6 Temp	22.82	-31.01	70.01	°C
LIA_P5_TEMP	LIAP board 5 Temp	22.55	-31.01	70.01	បំ បំ បំបំបំបំបំបំបំបំ
LIA_P4_TEMP	LIAP board 4 Temp	22.73	-31.01	70.01	°C
LIA_P3_TEMP	LIAP board 3 Temp	22.69	-31.01	70.01	°C
LIA_P2_TEMP	LIAP board 2 Temp	22.87	-31.01	70.01	°C
LIA_P1_TEMP	LIAP board 1 Temp	22.60	-31.01	70.01	°C
DAQ_IF_TEMP	DAQ_IF board Temp	22.55	-31.01	70.01	°C
BDAQ_P5	BIAS/DAQ_IF +5V(before post regu	5.10	4.90	5.26	V
BDAQ_P9	BIAS/DAQ_IF +9V(before post regu	8.99	8.50	9.10	V
BDAQ_N9	BIAS/DAQ_IF -9V(before post regul	-9.06	-9.10	-8.50	V
LIAP_P5	LIAP +5V(before post regulator)	5.17	4.90	5.27	V
LIAP_P9	LIAP +9V(before post regulator)	11.52	11.20	11.60	V
LIAP_N9	LIAP -9V(before post regulator)	-11.53	-11.60	-11.20	V
LIAS_P5	LIAS +5V(before post regulator)	0.00	4.90	5.26	V
LIAS_P9	LIAS +9V(before post regulator)	0.12	11.20	11.60	V
LIAS_N9	LIAS -9V(before post regulator)	0.00	-11.60	-11.20	V
PWR_STATUS	LIA1 to LIA12 12 +5V/+9V/-9V status	0000	0.00	0.00	hexa
T/C_1	16 bits ADC (Offset=0) 1	2173			Decimal
T/C_2	16 bits ADC (Offset=0) 2	255			Decimal
T/C_3	16 bits ADC (Offset=0) 3	250			Decimal





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When LIAS ON

Main

MONTOHING					
-DCU					
Nom Parametre	Description	Valeur C	Min	Max	Unite
BIAS_TEMP	BIAS board Temp	22.98	-31.01	70.01	°C
LIA_S1_TEMP	LIAS board 1 Temp	22.72	-31.01	70.01	°C
LIA_S2_TEMP	LIAS board 2 Temp	22.38	-31.01	70.01	י ס נ
LIA_S3_TEMP	LIAS board 3 Temp	22.00	-31.01	70.01	°C
LIA_P9_TEMP	LIAP board 9 Temp	22.70	-31.01	70.01	°C
LIA_P8_TEMP	LIAP board 8 Temp	23.07	-31.01	70.01	°C
LIA_P7_TEMP	LIAP board 7 Temp	22.82	-31.01	70.01	°C
LIA_P6_TEMP	LIAP board 6 Temp	22.92	-31.01	70.01	°C
LIA_P5_TEMP	LIAP board 5 Temp	22.89	-31.01	70.01	°C
LIA_P4_TEMP	LIAP board 4 Temp	23.11	-31.01	70.01	ດໍ ດໍ ດໍ ດໍ ດໍ ດໍ
LIA_P3_TEMP	LIAP board 3 Temp	22.70	-31.01	70.01	°C
LIA_P2_TEMP	LIAP board 2 Temp	22.75	-31.01	70.01	°C
LIA_P1_TEMP	LIAP board 1 Temp	23.04	-31.01	70.01	0° 0°
DAQ_IF_TEMP	DAQ_IF board Temp	23.53	-31.01	70.01	°C
BDAQ_P5	BIAS/DAQ_IF +5V(before post regu	5.11	4.90	5.26	V
BDAQ_P9	BIAS/DAQ_IF +9V(before post regu	8.96	8.50	9.10	V
BDAQ_N9	BIAS/DAQ_IF -9V(before post regul	-9.04	-9.10	-8.50	V
LIAP_P5	LIAP +5V(before post regulator)	0.22	4.90	5.27	V
LIAP_P9	LIAP +9V(before post regulator)	0.17	11.20	11.60	V
LIAP_N9	LIAP -9V(before post regulator)	0.00	-11.60	-11.20	V
LIAS_P5	LIAS +5V(before post regulator)	5.21	4.90	5.26	V
LIAS_P9	LIAS +9V(before post regulator)	11.55	11.20	11.60	V
LIAS_N9	LIAS -9V(before post regulator)	-11.55	-11.60	-11.20	V
PWR_STATUS	LIA1 to LIA12 12 +5V/+9V/-9V status	0000	0.00	0.00	hexa
T/C_1	16 bits ADC (Offset=0) 1	2207			Decimal
T/C_2	16 bits ADC (Offset=0) 2	4159			Decimal
T/C_3	16 bits ADC (Offset=0) 3	251			Decimal



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Redundant

Nom Parametre	Description	Valeur C	Min	Max	Unite
BIAS_TEMP	BIAS board Temp	22.72	-31.01	70.01	°C
LIA_S1_TEMP	LIAS board 1 Temp	22.29	-31.01	70.01	°C
LIA_S2_TEMP	LIAS board 2 Temp	22.35	-31.01	70.01	°C
LIA_S3_TEMP	LIAS board 3 Temp	22.11	-31.01	70.01	°C
LIA_P9_TEMP	LIAP board 9 Temp	22.95	-31.01	70.01	°C
LIA_P8_TEMP	LIAP board 8 Temp	22.67	-31.01	70.01	°C
LIA_P7_TEMP	LIAP board 7 Temp	22.64	-31.01	70.01	°C
LIA_P6_TEMP	LIAP board 6 Temp	22.95	-31.01	70.01	°C
LIA_P5_TEMP	LIAP board 5 Temp	22.72	-31.01	70.01	°C
LIA_P4_TEMP	LIAP board 4 Temp	22.87	-31.01	70.01	°C
LIA_P3_TEMP	LIAP board 3 Temp	22.84	-31.01	70.01	 Addadadadadada
LIA_P2_TEMP	LIAP board 2 Temp	23.05	-31.01	70.01	°C
LIA_P1_TEMP	LIAP board 1 Temp	22.67	-31.01	70.01	°C
DAQ_IF_TEMP	DAQ_IF board Temp	22.92	-31.01	70.01	°C
BDAQ_P5	BIAS/DAQ_IF +5V(before post regu	5.10	4.90	5.26	V
BDAQ_P9	BIAS/DAQ_IF +9V(before post regu	8.98	8.50	9.10	V
BDAQ_N9	BIAS/DAQ_IF -9V(before post regul	-9.06	-9.10	-8.50	V
LIAP_P5	LIAP +5V(before post regulator)	0.00	4.90	5.27	V
LIAP_P9	LIAP +9V(before post regulator)	0.16	11.20	11.60	V
LIAP_N9	LIAP -9V(before post regulator)	-0.00	-11.60	-11.20	V
LIAS_P5	LIAS +5V(before post regulator)	5.22	4.90	5.26	V
LIAS_P9	LIAS +9V(before post regulator)	11.55	11.20	11.60	V
LIAS_N9	LIAS -9V(before post regulator)	-11.56	-11.60	-11.20	V
PWR_STATUS	LIA1 to LIA12 12 +5V/+9V/-9V status	0000	0.00	0.00	hexa
T/C_1	16 bits ADC (Offset=0) 1	2173			Decimal
T/C_2	16 bits ADC (Offset=0) 2	255			Decimal
T/C_3	16 bits ADC (Offset=0) 3	250			Decimal

All the H/K observed after the vibrations were consistent.





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8.5 BIAS generation tests

In this test, performed at each stabilized temperature level, we have set all the JFET BIAS (JFET Vdd, Vss and Heater BIAS) to their maximum and the BIAS amplitudes levels (PLW, PMW, PSW, PTC, SSW, SLW) to half maximum.

Measurements have been performed after each axis. We check that the BIAS amplitudes, the BIAS frequencies, the Vdd level, the VSS levels and the Heater BIAS levels are consistent with the expected values and do not vary following the vibrations.

No significant change has been observed and the values measures remained nominal. The results obtained after all vibrations, as measured by the FPU simulator, are given in the thereafter table :





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Parameter BIAS After vibrations P250 ampli (V) 64.341E-3 P250 freq (Hz) 201.348E+0 P350 ampli (V) 64.736E-3 P350 freq (Hz) 201.348E+0 PTC ampli (V) 128,069E-3 PTC freq (Hz) 201.357E+0 P500 ampli (V) 65.139E-3 P500 freq (Hz) 201.357E+0 SSW ampli (V) 89.234E-3 SSW freq (Hz) 201.368E+0 SLW ampli (V) 89.081E-3 SLW freq (Hz) 201.359E+0 Vdd1_P (V) 2.476E+0 Vss1_P (V) -4.938E+0 Vds2_P (V) -4.934E+0	
P250 ampli (V)64.341E-3P250 freq (Hz)201.348E+0P350 ampli (V)64.736E-3P350 freq (Hz)201.348E+0PTC ampli (V)128,069E-3PTC freq (Hz)201.357E+0P500 ampli (V)65.139E-3P500 freq (Hz)201.357E+0SSW ampli (V)89.234E-3SSW freq (Hz)201.368E+0SLW ampli (V)89.081E-3SLW freq (Hz)201.359E+0Vdd1_P (V)2.476E+0Vss1_P (V)2.478E+0	
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VSS3_P V -4.9330E+0 Vdd4_P (V) 2.477E+0	
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	_
	_
Vdd6_P (V) 2.479E+0	_
$Vss6_P(V) -4.935E+0$	_
Vdd7_P (V) 2.478E+0	_
Vss7_P (V) -4.938E+0	
Vdd8_P (V) 2.476E+0	
Vss8_P (V) -4.931E+0	_
Vdd9_P (V) 2.477E+0	
Vss9_P (V) -4.935E+0	_
Vdd10_P (V) 2.478E+0	
Vss10_P (V) -4.933E+0	_
Vdd11_P (V) 2.476E+0	
Vss11_P (V) -4.934E+0	
Vdd12_P (V) 2.477E+0	
Vss12_P (V) -4.935E+0	
Vdd1_S (V) 2.475E+0	
Vss1_S (V) -4.931E+0	
Vdd2_S (V) 2.474E+0	
Vss2_S (V) -4.924E+0	
Vdd3_S (V) 2.475E+0	
Vss3_S (V) -4.929E+0	
Vdd_TC (V) 2.478E+0	
Vss_TC (V) -4.938E+0	
Nheater_P SW1(V) -4.736E+0	
Nheater_P SW2(V) -4.703E+0	
Nheater_P SW3(V) -4.730E+0	
Nheater_P MW1(V) -4.731E+0	
Nheater_P MW2(V) -4.719E+0	
Nheater_P LW1(V) -4.723E+0	
Nheater_S SW(V) -4.948E+0	
Nheater_S LW(V) -4.947E+0	1
Nheater_TC (V) -4.956E+0	



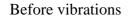


8.6 Gain Tests

The FPU simulator sends on all channels a sinusoïdal signal with a magnitude of 0,5 mV pic pic a and a frequency of 0,1 Hz modulated at 100 % (Offset = 0).

We measure the DCU output levels on all available photometer and spectrometer channels.

8.6.1 Photometer Main side



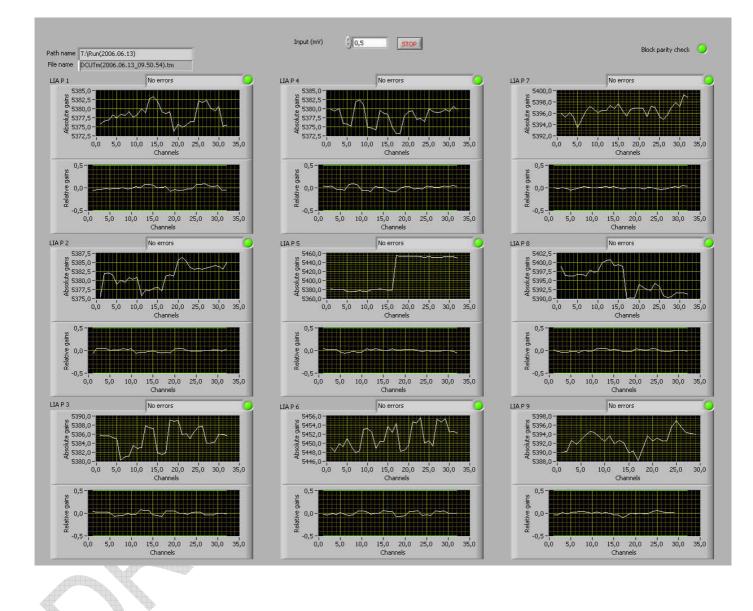






SAp-SPIRE- HT-0391-06 V1.0 Issue : 1.0 Date : 25/07/2006

After Z axis vibrations





DSM - DAPNIA

SAp-SPIRE- HT-0391-06 V1.0 Issue : 1.0 Date : 25/07/2006

After X axis vibrations

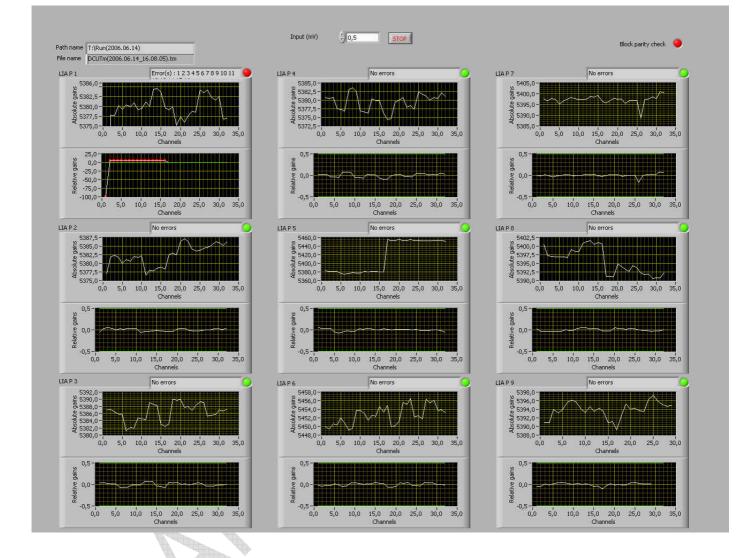






SAp-SPIRE- HT-0391-06 V1.0 Issue : 1.0 Date : 25/07/2006

After Y axis vibrations

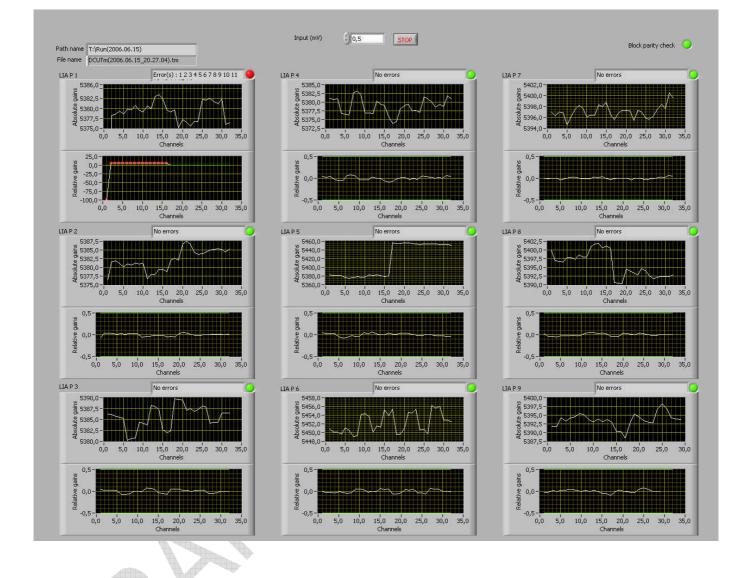






SAp-SPIRE- HT-0391-06 V1.0 Issue : 1.0 Date : 25/07/2006

After X axis vibrations at protoflight level







SAp-SPIRE- HT-0391-06 V1.0 Issue : 1.0 Date : 25/07/2006

8.6.2 Photometer Redundant side

Before vibrations







SAp-SPIRE- HT-0391-06 V1.0 Issue : 1.0 Date : 25/07/2006

After Z axis vibrations

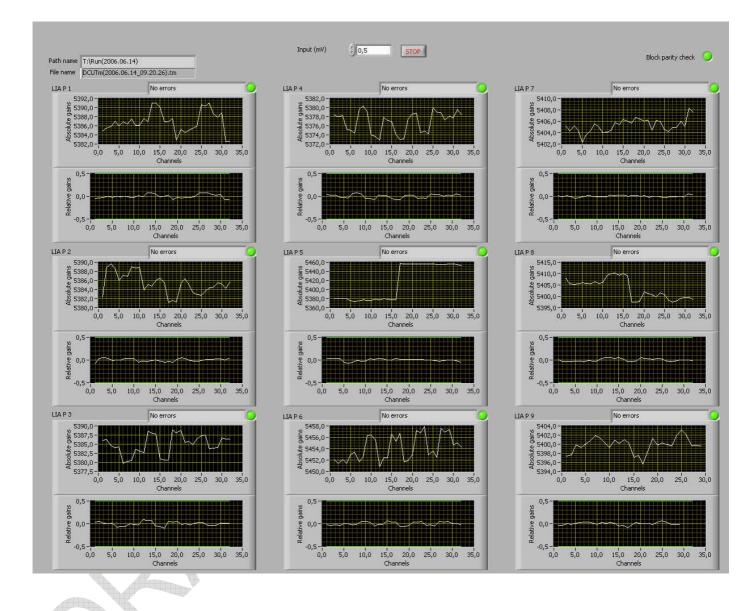




DSM - DAPNIA

SAp-SPIRE- HT-0391-06 V1.0 Issue : 1.0 Date : 25/07/2006

After X axis vibrations

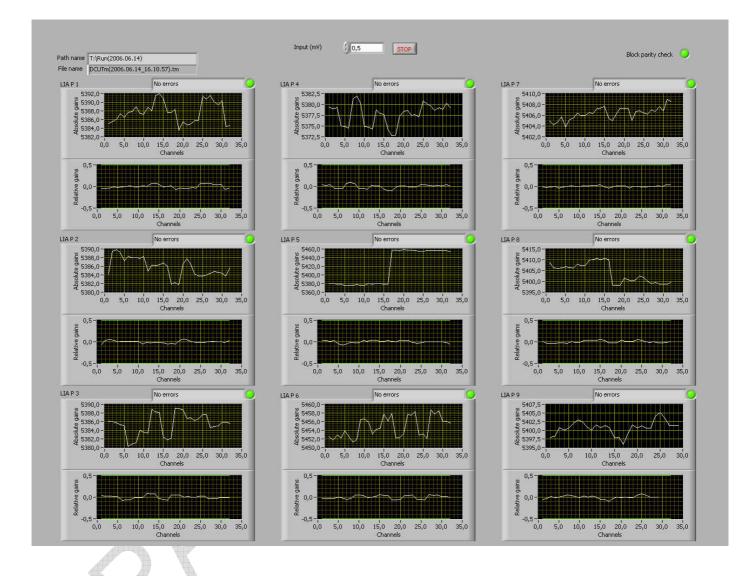






SAp-SPIRE- HT-0391-06 V1.0 Issue : 1.0 Date : 25/07/2006

After Y axis vibrations

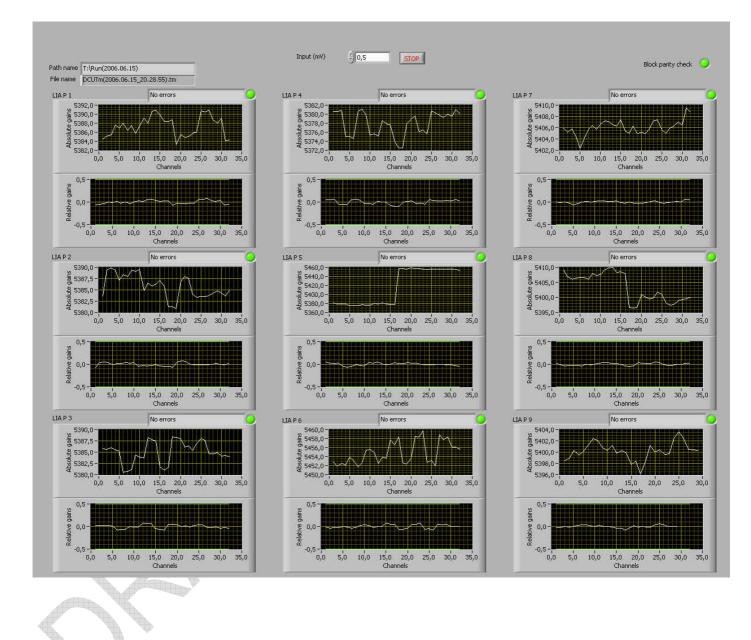






SAp-SPIRE- HT-0391-06 V1.0 Issue : 1.0 Date : 25/07/2006

After X axis vibrations at protoflight level



We notice no change in the gain values after the vibration tests





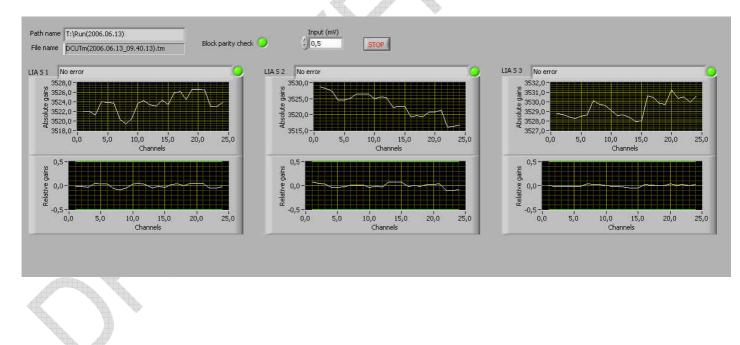
SAp-SPIRE- HT-0391-06 V1.0 Issue : 1.0 Date : 25/07/2006

8.6.3 Spectrometer main side

Before vibrations



After Z axis vibrations





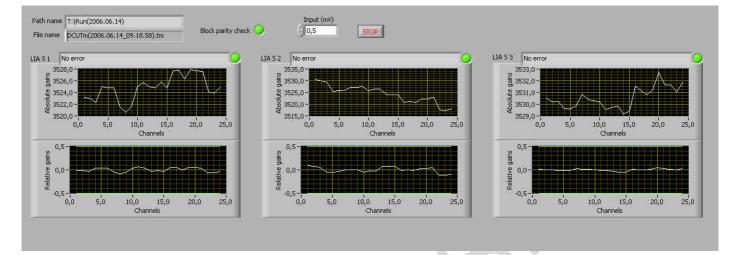
SPIRE DCU FM ACCEPTANCE

Vibration Tests Report



SAp-SPIRE- HT-0391-06 V1.0 Issue : 1.0 Date : 25/07/2006

After X axis vibrations



After Y axis vibrations

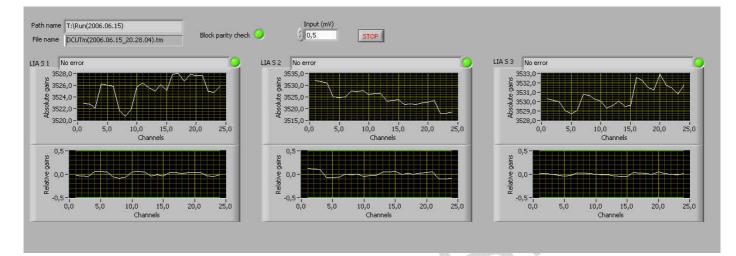






SAp-SPIRE- HT-0391-06 V1.0 Issue : 1.0 Date : 25/07/2006

After X axis vibrations at protoflight level



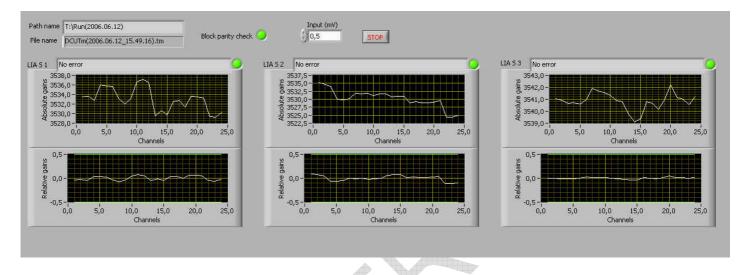
We notice no change in the gain values after the vibration tests



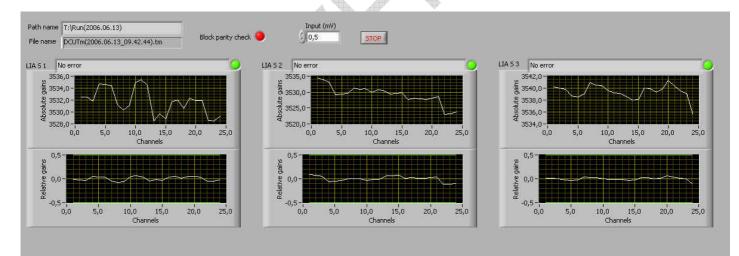


8.6.4 Spectrometer redundant side

Before vibrations



After Z axis vibrations





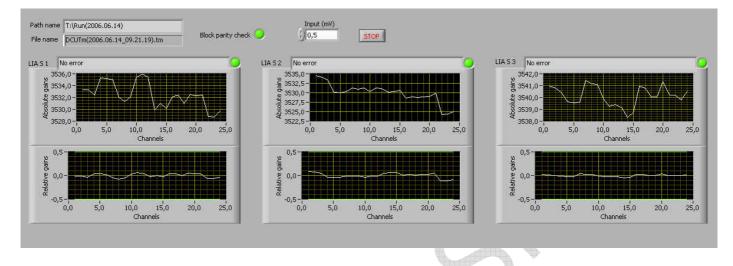
SPIRE DCU FM ACCEPTANCE

Vibration Tests Report

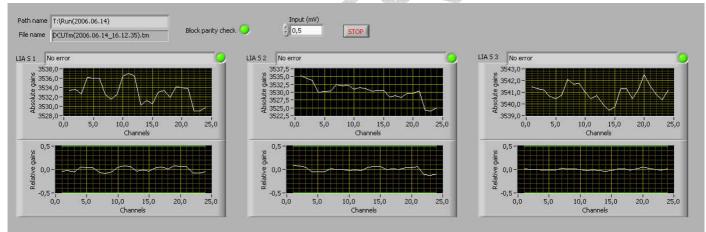


SAp-SPIRE- HT-0391-06 V1.0 Issue : 1.0 Date : 25/07/2006

After X axis vibrations



After Y axis vibrations



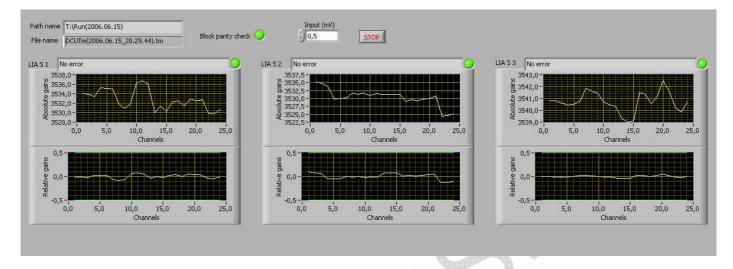








After X axis vibrations at protoflight level



We notice no change in the gain values after the vibration tests

8.6.5 Summary

Gain measurements

We measure the gain on each board (with reference value on channel 5 of each board, except for LIAP5 where we take as reference the channels 5 and 20 that belong to the two half boards)

	Main side	Main side	Redundant side	Redundant side
,	Before vibrations	After vibrations	Before vibrations	After vibrations
LIAP1	5377,5	5378,5	5387	5387
LIAP2	5379,5	5380	5387,5	5387,5
LIAP2	5385	5385	5385	5385
LIAP4	5375,5	5376	5375	5375
LIAP5	5375/5455	5375/5455	5375/5455	5375/5455
LIAP6	5451	5451	5455	5455
LIAP7	5393	5394,5	5403	5402,3
LIAP8	5397	5397,5	5406	5406
LIPA9	5392,6	5394	5401,5	5400
LIAS1	3525,5	3526	3535,75	3535
LIAS2	3524,5	3525	3530	3530
LIAS3	3528,75	3528,75	3540,6	3540,5





We see that the gains do not move following vibrations (the gain value is assumed to have an accuracy range of +/-1).

The gains difference between boards (or between two half boards as for LIAP 5) is due to the difference of signals sent by the FPU simulator to the DCU boards. This has been checked by inverting connectors.

We notice a slight gain difference of gains between main and redundant sides.





9 Conclusion

The tests reveal no susceptibility of the DCU FM box (mechanical and functional aspects) to the acceptance vibrations levels.