

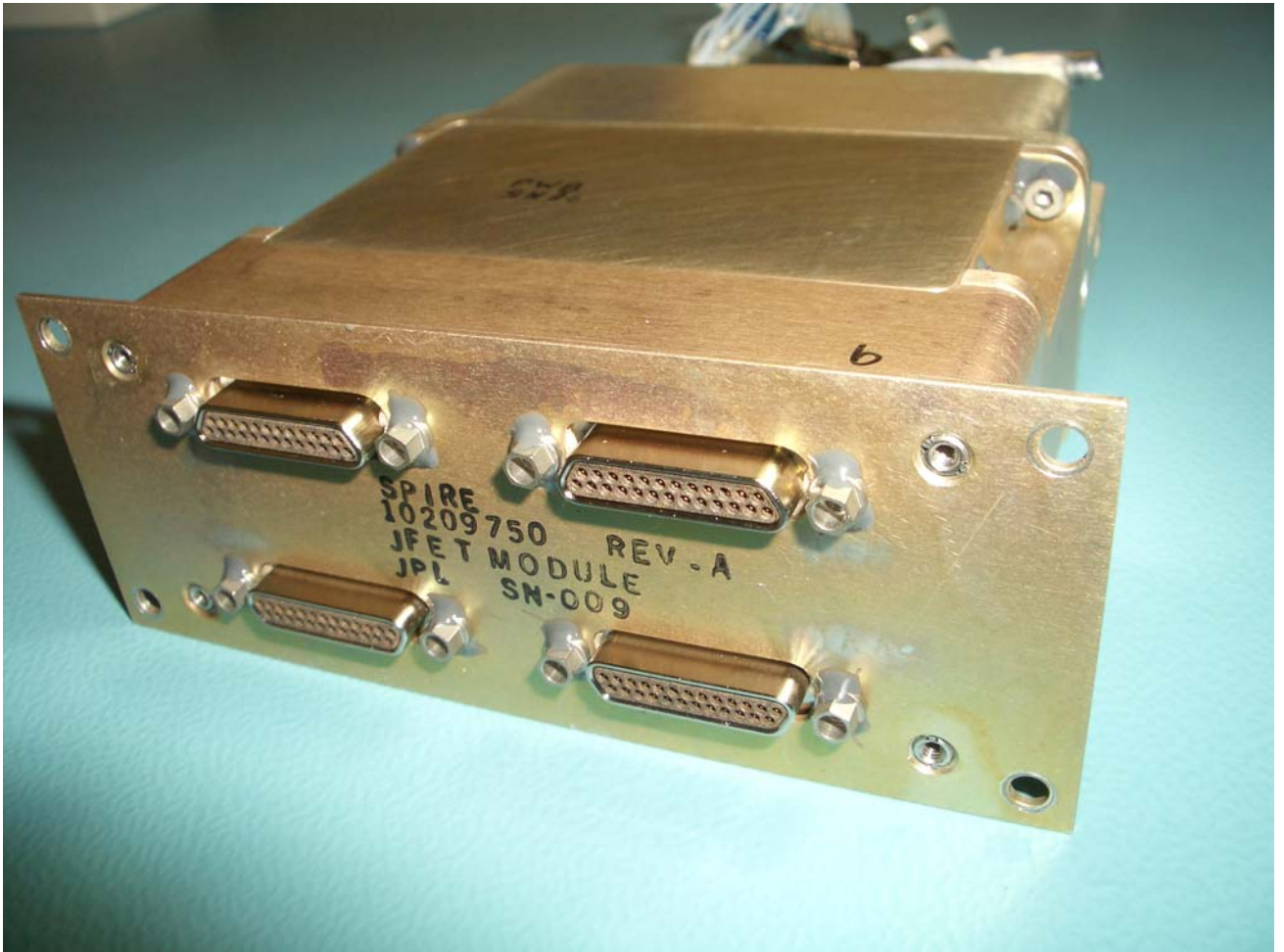
JPL Hardware Requirements Certification Review – SPIRE Element No. D-30420

Signed HRCR 1st Page

JPL Hardware Requirements Certification Review – SPIRE Element No. D-30420

Assembly / Subsystem		PEM	Phone	Section		Date	
SPIRE		Martin Herman	(818) 354-8541	386		11 October, 2004	
Drawing/ Part No.	Dwg. Rev.	Nomenclature	Serial No.	Model	Type	Final IR No.	Mass (Meas. / Req.)
10209750-1	A	JFET Module	009	FLIGHT	N/A	922703	272 gm / 305 gm
Check applicable answer and provide explanation in remarks column		Y E S	N O	N A	Remarks	Data Attachments	Signature & Date
1. Are all drawings and specifications complete, approved, released and frozen?			X		See Attached	14. Latest Top Assembly drawings <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None	Cognizant Engineer <i>Slev Tracy</i> 10/11/04
2. Do the released drawings and specifications reflect all approved changes?		X	X		See Attached	15. List of open ECRs <input type="checkbox"/> Attached <input checked="" type="checkbox"/> None	PEM, For MTH <i>Richard P. Vargay</i> 10/11/04
3. Is hardware identical to other hardware delivered? If no, provide difference list.		X				16. Waivers (RFW request for waiver) <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None	QA Engineer <i>Suzanne Valenzuela</i> 11/30/04
4. Does the hardware meet its functional requirements, specifications, waivers, ICDs?		X			EIDP attached. Also see item #8 attachments.	17. Open MRB <input type="checkbox"/> Attached <input checked="" type="checkbox"/> None	Environments/Reliability <i>[Signature]</i>
5. Are all IR and MRB's dispositioned and concurred by QA?		X				18. Open PFR on this H/W <input type="checkbox"/> Attached <input checked="" type="checkbox"/> None	Mission Assurance Mgr. <i>J - Lee</i>
6. Is complete as-built list information included in the build book?		X				19. Open PFR on similar H/W <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None	Project Office <i>Mangal Arking</i> 10/11/04
7. Have all required environmental tests & analyses been completed?		X			ETAS attached	20. Handling Document → See Item 11 <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None	PJ <i>Martin # for JB</i> 10/11/04
8. Is all required assembly and/or subsystem level functional testing complete?		X			Test Results Attached. Also see EDIP EIDP	21. Shortage List <input type="checkbox"/> Attached <input checked="" type="checkbox"/> None	
9. Have all piece parts, processes and materials been approved by JPL?		X				22. Requirements Verification Matrix <input checked="" type="checkbox"/> Attached (See #4, #7, #8) <input type="checkbox"/> None	
10. Does this hardware meet all contamination control requirements?		X			Parts, processes and MIUL met all contamination control and out-gassing requirements.	23. Qualification Status <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None	
11. Are all shipping containers, shipping and special handling procedures ready?		X			See Attached Document D-26790	24. Mate / Demate Record <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None	
12. Is additional work required to bring this hardware to flight readiness?			X			25. Operating Log <input checked="" type="checkbox"/> Attached (See Item # 24) <input type="checkbox"/> None	
13. Is this hardware acceptable for flight?		X				26. MICD <input checked="" type="checkbox"/> Attached <input type="checkbox"/> None	

SPIRE JFET Module S/N 009



RAL EIDP Table of Contents Versus JPL HRCR Check List Item Numbers

RAL EIDP Section Number	RAL EIDP Title	JPL HRCR Check List Item Number	Notes
1	Shipping Documents		Shipper and Final IR
2	Transportation, Packing, Handling & Integration Procedures	11	Special Handling Document D-26790
3	Certificate of Conformance / Delivery Review Board MOM		HRCR book is the C of C
4	As Built Configuration Status List	1 & 2	Drawing List & Status
5	List of Waivers	4	RFW (request for waiver) Attached
6	Copies of Waivers	4 & 7	RFW (request for waiver) Attached
7	List of Non-Conformance Reports		See RFW in 4 & 7
8	Copies of Non-Conformance Reports		See RFW in 4 & 7
9	Cleanliness Statement		Final IR QA Inspection
10	Operational Manual		NA
11	Top Level Drawings (inc. Family Tree)	14	Top Assembly Drawing
12	Interface Drawings	26	MICD Drawing
13	Functional, Block & Mechanical Drawings		NA
14	Electrical Circuit Drawings		NA
15	Serialized Components List		In build books – not shipped
16	Mass Properties/ Power Budget	HRCR Check List Page 1	Mass listed in HRCR check list
17	Qualification Status List / Test Matrix	23	Qualification Unit Test Matrix
18	Test Reports	4, 7, 8, 23	
19	Open Work / Deferred Work / Open Tests		NA
20	Calibration Data		NA
21	Historical Record	23	Qualification Unit Test Matrix
22	Manufacturing Logbook(s)		In build books – not shipped
23	Operating Time / Cycle Record	25	
24	Connector Mating Record	24	
25	Age Sensitive Items Record		NA
26	Pressure Vessels – History/Test Record		NA
27	Temporary Installation Record		NA
28	Reference List of EIDPs (Lower level)		NA
29	Other Useful Information		NA

JPL Hardware Requirements
Certification Review (HRCR)

Junction Field Effect Transistor (JFET)
Flight Module

10209750-1 S/N 009

SPIRE Element
Herschel Space Observatory Project

October 11, 2004

Module 10209750-1	S/N 8	S/N 8	S/N 9	S/N 9
PWB 10209760-1	S/N 18	S/N 29	S/N 20	S/N 24
Membrane 10209758-1	J5.5.1	J6.8.5	J5.5.4	J5.6.4

Attachment of HRCR Items #1 & #2

Drawing Release Status

All redlined drawings to be updated and placed in JPL PDMS for approval by the end of calendar year 2004

Redlined / Unreleased Drawings:

10209750-1 redlined Rev. A drawing (module assy)
10209751-1 redlined Rev. A drawing (chassis 1)
10209754-1 redlined Rev. B drawing (mount)
10209757-1 unreleased Rev. A drawing (membrane)
10209759-1,-2,-4 redlined Rev. A drawing (gasket)
10209760-1 redlined Rev. A drawing (board assy)
10209761-1 redlined Rev. A drawing (soldering board)
10209769-1 unreleased Rev. X2 drawing (stiffener)
10209777-1 redlined Rev. A drawing (board)
10217636-1 unreleased Rev. A drawing (clip)

Released Drawings:

10209722-1 assembly built per released Rev.B drawing (interface drawing)
10209758-1 assembly built per released Rev.A drawing (membrane assy)
10209858-2 assembly built per released Rev.A drawing (special fastener)
10209752-1 assembly built per released Rev.A drawing (chassis 2)
10209753-1 assembly built per released Rev.A drawing (chassis 3)
10209756-1 assembly built per released Rev.B drawing (chassis lid)
10209719-1 assembly built per released Rev.A drawing (studlock)

Attachment of HRCR Item #4: EIDP

EIDP Coveragepage For JFET Testing

Unit Identification							
Name	:	JFET PFM Module					
Part #	:	10209750-1					
S/N	:	#009					
Environmental Testing							
		Axes Tested	Temp	Duration/# of Cycle	Requirement	Source	
Random Vibration Test		X, Y, Z	Rm T	1 min/axis	X, Y, Z	SSSD, JFET-DES-07	
High Level Sine Vibe Test		None	NA	NA	X, Y, Z	SSSD, JFET-DES-07	
Bakeout		NA	80 C	25.5 hrs	> 24 HRS		
Thermal Cycles		NA	RmT to 80 K	2	Minimum 1	D-20549	
Performance Characteristics							
				Specification		Source	
Power needed for <11 bad channels (Min Perf.)		8.70 mW		11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	
Power needed for <4 bad channels (Design Value)		9.45 mW		11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	
Power needed for 100 % Yield per unit		10.54 mW		NA		NA	
Median Noise at < 11 bad chs.		8.09 nV/rHz	<15 nV/rHz Min Performance	<7 nV/rHz Design Value		SSSD, JFET-PER-01	
Median Noise at < 4 bad chs.		7.35 nV/rHz				SSSD, JFET-PER-01	
Median Noise at 100 % Yield.		6.78 nV/rHz				SSSD, JFET-PER-01	
# of Channels over the max. offset voltage		0	< 15 mV			SSSD, BDA-DRCU-27	
Common Mode Rejection Ratio		< -60 dB by design, as measured in EM4 unit					SSSD, BDA-DRCU-11
Board Level Details							
		Board SN 020 (JAA'-JDD')		Board SN 024 (JAA'-JDD)		Source	
# Channels Tested	:	24		24			
Median Noise at 3.5 mW	:	30.4 nV/rHz		14.01 nV/rHz		SSSD, JFET-PER-01	
# of good channels at 3.5 mW	:	2	8% Yield	13	54% Yield	SSSD, JFET-PER-02	
Power Needed for 100 % Yield	:	5.49 mW		5.04 mW		SSSD, JFET-PER-02	
Median Noise at High Power (w/ 100 % Yield)		6.07 nV/rHz		7.18 nV/rHz		SSSD, JFET-PER-01	
Median Gain at High Power		0.98		0.98		NA	
Heater Resistance, 4K Reference value		2.320 kΩ		3.232 kΩ		NA	
Definitions							
Good Channels	:	Noise less than a min. performance value of 15 nV/rHz					
Yield	:	# of Good Channels / 24					
Filenames							
Noise Measurements	:	JFET_Module_SN09_Noise_data.pdf					
Source Voltages (RmT, 4K)	:	JFET Module SN08,SN09 source voltage data.pdf					
Notes							
1) The Base temperature for all performance characterization was 4K							
2) All Noise Measurements were made with the inputs shorted to ground							
3) Type of membranes: SN020: 29% Overetched SN024: 32% Overetched							

Attachment of HRCR Item # 4: RFW (request for waiver)

		RFW/RFD Number:	HR-SP-JPL-RFW-TBD
Spacecraft / Project	Herschel	Originator's Name	Steve Tseng
System / Experiment / Model	1.1 SPIRE	Signature / Date	
Sub-System	detectors	Request Type (Highlight applicable request)	Waiver (RFW) Deviation (RFD)
Assembly	JFET modules	1.1.1.1 <u>Organisation</u>	Jet Propulsion Laboratory
Sub-Assembly		Ref. Doc. / Drwg No.	SPIRE-JPL-PRJ-000456
Item		References	
Serial No.			
RFW/RFD Title	JFET Power Dissipation s/n 009		

End Items(s) Affected (Hardware, Software)				
Name	CI-Number	Model(s)		
JFET Module p/n 10209750 s/n 009		PFM		
Requirement / Interface Documents Affected				
Specification/Drawing Title	Number	Issue	Date	App. Paragraph
BDA-SSSD	SPIRE-JPL-PRJ-0004456	3.2	7/1/03	JFET-PER-01 JFET-PER-02 JFET-TEC-05
Description of Deviation / Discrepancy / Non-Conformance				
<p>Requirement states that dissipation of photometer JFETs is to be less than 7 mW average, while supplying 90% of channels with voltage noise < 15 nV/rHz according to BDA-SSSD JFET-PER-01, JFET-PER-02, JFET-TEC-05. Measured JFET performance of the JFETs indicates that 10.54 mW of power dissipation will be required to meet the specified yield and noise performance specifications.</p>				
Other Items or Requirements (Potentially) Affected				
<p>Overall sensitivity of the bolometer sub-system is affected by JFET noise performance. JFET power dissipation impacts the heat sink temperature of the 3He refrigerator and may in turn increase the base detector temperature. Dissipation of JFETs affects power dissipation on cryostat.</p>				
Need for RFW/RFD and Rationale for Acceptance				
<p>Measured JFET performance of JFETs indicates that 10.54 mW of power dissipation will be required to meet the specified yield and noise performance specifications. JPL is unable to significantly alter the JFET fabrication process in order to meet the power specification without undue risk to the stated PFM/FS delivery dates. Furthermore, JPL requests a full system optimisation to revisit the noise and power requirements on the JFETs. The JFET modules can meet the noise design value with 100 % yield at higher dissipation.</p>				
	Approved	Rejected	Name	Date
Engineering:				
Product Assurance:				
CCB-Chairman:				
Principal Investigator				
Product Assurance:				
Co-Investigator				
Prime Contractor				
ESA Project Office				

Attachment of HRCR Item #7: RFW (request for waiver)

RFW/RFD Number:	HR-SP-JPL-RFW-005
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Spacecraft / Project	Herschel	Originator's Name	Kalyani Sukhatme	
System / Experiment / Model	SPIRE	Signature / Date		
Sub-System	detectors	Request Type (Highlight applicable request)	Waiver (RFW)	Deviation (RFD)
Assembly		Organisation	Jet Propulsion Laboratory	
Sub-Assembly		Ref. Doc. / Drwg No.	SPIRE-JPL-PRJ-000456	
Item		References		
Serial No.				
RFW/RFD Title	BDA and JFET module sine test deletion			

End Items(s) Affected (Hardware, Software)		
Name	CI-Number	Model(s)
Bolometric Detector Assemblies JFET Modules		CQM, PFM, FS CQM, PFM, FS

Requirement / Interface Documents Affected				
Specification/Drawing Title	Number	Issue	Date	App. Paragraph
BDA-SSSD (SPIRE-JPL-PRJ-000456)		3.2	Jan 7, 2003	BDA-DES-10, JFET-DES-07

Description of Deviation / Discrepancy / Non-Conformance
 High Level Sine- Vibe Test is not performed on these units

Other Items or Requirements (Potentially) Affected

Need for RFW/RFD and Rationale for Acceptance
 The hardware has to be qualified under a cold vibration test and is installed in the cold vibration facility for the purpose of the test. The high level sine vibration test configuration will put the hardware and the personnel at risk since the cold vibration facility is not structurally capable of withstanding the high levels. Obtaining additional resources (cost and schedule) for developing a new set-up is not feasible at this time.

	Approved	Rejected	Name	Date
JPL Engineering:				
JPL Product Assurance:				
CCB-Chairman:				
Principal Investigator				
Product Assurance:				
Co-Investigator				
Prime Contractor				
ESA Project Office				

**Attachment of HRCR Item #7: ETAS (environmental test summary)
For Module 8 & 9**



ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)

AUTHORIZATION SECTION					
PROJECT Mantel			LOG NO. HS028		
SYSTEM/ASSEMBLY TITLE SPIRE JFET Modules S/N008,009				DATE ISSUED 8/16/04	
REFERENCE DESIGNATION NUMBER		PART NO. (IF MULTIPLE, ATTACH LIST) 10209750-1		REV. SERIAL NO. 008, 009	
HARDWARE TYPE <input type="checkbox"/> EM QUAL <input checked="" type="checkbox"/> FLIGHT <input type="checkbox"/> FLIGHT SPARE <input type="checkbox"/> OTHER			PRE-ENVIRONMENTAL INSPECTION REPORT NUMBER (ATTACH IF)		
WIRING HARNESS <input type="checkbox"/> EM QUAL <input type="checkbox"/> FLIGHT <input checked="" type="checkbox"/> EM <input checked="" type="checkbox"/> SE			PART NO.		SERIAL NO.
TEST DESCRIPTION (CHECK ALL APPLICABLE) <input type="checkbox"/> SINE VIBRATION <input type="checkbox"/> PYROSHOCK <input type="checkbox"/> ACOUSTIC <input type="checkbox"/> EMC <input type="checkbox"/> OTHER _____ <input checked="" type="checkbox"/> RANDOM VIBRATION <input checked="" type="checkbox"/> THERMAL VAC. <input type="checkbox"/> THERMAL ATMOSPHERE				TYPE OF TEST <input type="checkbox"/> QUALIFICATION <input type="checkbox"/> FLIGHT ACCEPTANCE <input checked="" type="checkbox"/> PROTO FLIGHT <input type="checkbox"/> RETEST	
WILL ALL TESTS/LEVELS/DURATIONS REQUIRED BY THE PROJECT DOCUMENTS BE PERFORMED ON THIS UNIT? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) ENTER PROJ. DOC. NO. AND REV. _____					
HAS THE UNIT PASSED ALL PRE-ENVIRONMENTAL FUNCTIONAL TESTS? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION					
HAVE ALL DESIGN ANALYSES BEEN COMPLETED AND REQUIRED CHANGES BEEN IMPLEMENTED? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION					
IS THE TEST ARTICLE IDENTICAL TO OTHER FLIGHT UNITS? <input type="checkbox"/> YES <input checked="" type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION Stiffeners have been added to the design and included on this unit (Brd SN31 in Mod001rc)					
ARE ALL PFRs AGAINST THIS UNIT CLOSED? <input type="checkbox"/> YES <input checked="" type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION PFR's in process of closure. All issues have been addressed and qualified.					
HAVE ALL WAIVERS AND ECRs BEEN APPROVED AND ARE THEY INCORPORATED? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION					
TEST AUTHORIZED BY					
COGNIZANT ENGINEER <i>[Signature]</i>		DATE 9/15/04		TECHNICAL MGR./INSTR MRG./PI PREP REP <i>[Signature]</i>	
				ENVIRONMENTAL REQUIREMENTS ENG. DATE 9/15/04	
SUMMARY SECTION					
TEST AGENCY (IF MULTIPLE, ATTACH SUMMARY AND TEST DATES) JPL Building 144		TEST INITIATION DATE 8/18/04		ACCUMULATED OPERATING HOURS PRIOR TO FIRST ENVIRONMENTAL TEST	
SERIAL NUMBERS ACTUALLY TESTED		TEST TERMINATION DATE 9/16/04		OPERATING HOURS DURING ENVIRONMENTAL EXPOSURE	
TEST DESCRIPTION					
VIBRATION AXES: X Y Z SINE VIBRATION <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> RANDOM VIBRATION <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/>		ACOUSTIC <input type="checkbox"/>		PYROSHOCK SHOCK AXES: X Y Z <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> SHOCKS/AXIS:	
EMC <input type="checkbox"/> ESD <input type="checkbox"/> COND. SUSC. <input type="checkbox"/> RAD. SUSC. <input type="checkbox"/> COND. EMIS. <input type="checkbox"/> RAD. EMIS. <input type="checkbox"/> ISOLATION <input type="checkbox"/> MAGNETICS		THERMAL VACUUM PRESSURE: <10E-5 298 to 70K NO OF CYCLES: 2<-#<-3		TEMPERATURE ATMOSPHERE <input type="checkbox"/> OTHER NO OF CYCLES:	
TEMP. LEVEL (°C) AND ACCUMULATED DURATION (HRS.) HOT: _____°C, _____h COLD: _____°C, _____h HOT: _____°C, _____h COLD: _____°C, _____h					
WERE THERE ANY PFRs GENERATED DURING ENVIRONMENTAL TESTS? <input type="checkbox"/> YES <input checked="" type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST)			LIST PFR NOS. / BRIEF EXPLANATION		
ARE THE POST ENVIRONMENTAL DAMAGE INSPECTIONS COMPLETE? <input type="checkbox"/> YES <input checked="" type="checkbox"/> NO (IF YES, ATTACH A COPY OF THE INSPECTION REPORTS. IF NO, ATTACH EXPLANATION)			LIST PFR NOS. / BRIEF EXPLANATION		
WERE ALL PLANNED TESTS/LEVELS/DURATIONS ACHIEVED? <input checked="" type="checkbox"/> YES <input type="checkbox"/> NO (IF NO, ATTACH EXCEPTIONS LIST)			LIST PFR NOS. / BRIEF EXPLANATION		
TESTS HAVE NOT BEEN SUCCESSFULLY COMPLETED. SEE THE ATTACHED SUMMARY FOR ACTIONS THAT NEED TO BE TAKEN.					
COGNIZANT ENGINEER		DATE		TECHNICAL MGR./INSTR MRG./PI PREP REP DATE ENVIRONMENTAL REQUIREMENTS ENG. DATE	
<input checked="" type="checkbox"/> HARDWARE HAS SUCCESSFULLY COMPLETED THE ENVIRONMENTAL TESTS LISTED ON THIS FORM OR REMAINING ACTIONS HAVE BEEN TAKEN, INCLUDING RETEST.					
COGNIZANT ENGINEER <i>[Signature]</i>		DATE 9/15/04		TECHNICAL MGR./INSTR MRG./PI PREP REP DATE ENVIRONMENTAL REQUIREMENTS ENG. DATE <i>[Signature]</i>	

**Attachment of HRCR Item #7: ETAS (environmental test summary)
For Module 8 & 9**

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ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)

OTHER AUTHORIZATION PROVISIONS AND EXPLANATIONS

This is a 3-axis warm vibration test (room temp) done on the JFET flight modules SN008 and 009. The test will be done with the JFET unit mounted inside a mock-up JFET rack. The unit will be assessed both before and after the test with visual inspections and electrical checkouts. 3 response accelerometers will be mounted onto the JFET rack in order to give response data.

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**Attachment of HRCR Item #7: ETAS (environmental test summary)
For Module 8 & 9**

ENVIRONMENTAL TEST HORIZONTAL AND SUMMARY (ETAS)		ENVIRONMENTAL TEST SUMMARY				COMMENTS															
HARDWARE	S/N	ETAS	TEST ENVIRONMENT LEVELS & DURATION	DATE TEST PERFORMED	TEST AGENCY		PASS/ FAIL														
SPIRE JFET (10209750-1)	008, 009	HSO28	<p>X, Y, and Z 1 minute Random Vibe</p> <table border="1"> <thead> <tr> <th>Frequency [Hz]</th> <th>Spec [g².Hz]</th> </tr> </thead> <tbody> <tr> <td>20</td> <td>0.01</td> </tr> <tr> <td>100</td> <td>0.05</td> </tr> <tr> <td>300</td> <td>0.05</td> </tr> <tr> <td>499</td> <td>0.0214</td> </tr> <tr> <td>500</td> <td>0.0214</td> </tr> <tr> <td>2000</td> <td>0.00214</td> </tr> </tbody> </table> <p>Each axis 1/4 g sine sweep 20-2000 Hz each axis</p>	Frequency [Hz]	Spec [g ² .Hz]	20	0.01	100	0.05	300	0.05	499	0.0214	500	0.0214	2000	0.00214				
Frequency [Hz]	Spec [g ² .Hz]																				
20	0.01																				
100	0.05																				
300	0.05																				
499	0.0214																				
500	0.0214																				
2000	0.00214																				

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Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise For Module 8 & 9

JFET SOURCE VOLTAGE MEASUREMENT

Post vibe, post bake, SN8,9 module, Perf Test (4K T) in green dewar.

Date			9/2/2004		9/2/2004		9/2/2004		9/2/2004	
T, plate			He		He		He		He	
T, JFET			He		He		He		He	
Vdd			3		3		3		3	
Vss			-1.5		-1.5		-1.5		-1.5	
Idd			1.3449		1.0852		1.379		1.082	
Iss			1.3426		1.0834		1.3769		1.0803	
SN			18		29		20		24	
Channel #				DELTA		DELTA		DELTA		DELTA
1	a		0.528		1.277		0.543		0.664	
	b		0.528	0	1.268	0.009	0.538	0.005	0.664	0
2	a		0.399		1.209		0.714		1.340	
	b		0.402	0.003	1.205	0.004	0.712	0.002	1.348	0.008
3	a		1.228		0.705		0.493		0.668	
	b		1.217	0.011	0.707	0.002	0.497	0.004	0.668	0
4	a		0.180		1.255		0.549		0.673	
	b		0.173	0.007	1.247	0.008	0.547	0.002	0.671	0.002
5	a		1.015		0.740		0.519		1.269	
	b		1.005	0.01	0.737	0.003	0.524	0.005	1.278	0.007
6	a		0.559		0.861		1.064		0.660	
	b		0.565	0.006	0.859	0.002	1.059	0.005	0.661	0.001
7	a		1.243		0.990		0.263		0.593	
	b		1.257	0.014	0.991	0.001	0.260	0.003	0.593	0
8	a		1.181		0.716		1.490		0.656	
	b		1.193	0.012	0.711	0.005	1.486	0.004	0.658	0.002
9	a		0.366		0.850		0.474		0.928	
	b		0.362	0.004	0.849	0.001	0.472	0.002	0.933	0.005
10	a		0.548		0.857		0.358		0.654	
	b		0.549	0.001	0.855	0.002	0.361	0.003	0.651	0.003
11	a		0.473		0.934		0.882		0.651	
	b		0.468	0.005	0.932	0.002	0.881	0.001	0.652	0.001
12	a		0.870		1.184		0.924		0.941	
	b		0.869	0.001	1.182	0.002	0.912	0.012	0.940	0.001
13	a		1.354		0.915		0.550		0.708	
	b		1.347	0.007	0.913	0.002	0.548	0.002	0.711	0.003
14	a		0.507		1.129		0.536		1.230	
	b		0.511	0.004	1.137	0.008	0.536	0.001	1.223	0.007
15	a		0.594		0.829		0.842		0.667	
	b		0.596	0.002	0.827	0.002	0.841	0.001	0.668	0.001
16	a		0.678		0.980		0.546		0.659	
	b		0.675	0.003	0.988	0.008	0.552	0.006	0.662	0.003
17	a		0.699		0.388		0.833		1.046	
	b		0.697	0.002	0.399	0.011	0.828	0.005	1.051	0.005
18	a		0.479		0.812		1.324		1.086	
	b		0.480	0.001	0.815	0.003	1.336	0.012	1.094	0.008
19	a		0.504		0.737		0.635		0.674	
	b		0.507	0.003	0.739	0.002	0.634	0.001	0.671	0.003
20	a		0.676		0.806		0.804		0.899	
	b		0.678	0.002	0.809	0.003	0.810	0.006	0.892	0.007
21	a		1.198		0.650		0.426		0.661	
	b		1.187	0.011	0.649	0.001	0.426	0	0.661	0
22	a		0.456		0.867		0.669		0.665	
	b		0.455	0.001	0.871	0.004	0.688	0.001	0.669	0.004
23	a		0.797		0.740		0.536		0.669	
	b		0.789	0.008	0.742	0.002	0.540	0.004	0.670	0.001
24	a		0.873		1.479		0.487		1.487	
	b		0.869	0.004	1.472	0.007	0.489	0.002	1.478	0.009

Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise

Board S/N 020 in Module S/N 009

	Pwr1	Pwr2	Pwr3	Pwr4	Pwr5	Pwr6
Vdd (V)	3	2.5	2.5	2.5	2.5	2.5
Vss (V)	-1.5	-1.5	-1.4	-1.3	-1.55	-1.45
Vdd' (V)	2.915	2.416	2.42	2.424	2.414	2.418
Vss' (V)	-1.414	-1.409	-1.319	-1.223	-1.463	-1.367
Idd (mA)	1.4123	1.3992	1.3316	1.263	1.4331	1.3653
Iss (mA)	1.3787	1.367	1.2997	1.2313	1.4008	1.3333
I (mA)	1.3955	1.3831	1.31565	1.24715	1.41695	1.3493
P (mW)	6.0411195	5.2903575	4.91921535	4.54835605	5.49351515	5.1071005

Channel Num			Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz
Channel: 1	7.05	5.82	7.20	7.40	5.13	5.31
Channel: 2	5.91	5.94	8.58	15.93	5.18	6.64
Channel: 3	6.24	6.84	9.30	21.22	5.82	8.18
Channel: 4	6.29	5.80	7.10	8.83	4.48	6.46
Channel: 5	6.42	5.46	8.70	11.06	6.13	7.13
Channel: 6	5.53	6.12	7.19	5.89	5.30	6.01
Channel: 7	6.27	6.59	6.16	6.13	6.12	6.69
Channel: 8	5.98	13.89	28.15	66.24	10.26	19.99
Channel: 9	4.78	5.68	6.13	5.48	5.19	6.07
Channel: 10	6.60	8.47	6.28	11.72	6.27	6.75
Channel: 11	6.88	7.22	7.26	7.84	5.82	6.93
Channel: 12	5.74	8.34	7.72	11.12	8.05	7.46
Channel: 13	5.86	6.22	5.76	9.04	5.08	5.23
Channel: 14	5.52	6.44	7.66	11.28	5.37	7.66
Channel: 15	6.45	7.34	6.28	7.01	6.43	6.25
Channel: 16	7.35	7.21	6.95	7.81	6.08	7.49
Channel: 17	6.95	6.63	6.86	7.19	5.99	7.07
Channel: 18	5.64	5.47	7.44	7.04	6.06	7.30
Channel: 19	7.61	16.70	35.38	76.49	11.66	28.04
Channel: 20	5.80	9.33	15.99	23.41	8.25	9.47
Channel: 21	9.11	11.48	11.12	8.33	12.34	12.40
Channel: 22	7.01	5.76	5.54	5.58	4.61	4.60
Channel: 23	6.23	8.08	7.71	9.15	7.88	7.47
Channel: 24	10.78	7.91	6.09	6.97	6.82	6.28
Median	6.28	6.73	7.23	8.58	6.07	7.00
Overall Mean	6.58	7.70	9.69	14.92	6.68	8.45
Good Mean	6.58	7.30	7.29	8.15	6.68	7.04
MP Reqd					15	
Yield	1.00	0.96	0.88	0.79	1.00	0.92
# Good Ch.	24	23	21	19	24	22
# Bad Ch.	0	1	3	5	0	2

JFET_Mod9_brd20_Noise_perf.xls

Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise

Board S/N 024 in Module S/N 009

	Pwr1	Pwr2	Pwr3	Pwr4	Pwr5	Pwr6	Pwr7	Pwr8
Vdd (V)	3	2.5	2.5	2.5	2.5	2.5	2.5	2.5
Vss (V)	-1.5	-1.5	-1.6	-1.7	-1.8	-1.63	-1.3	-1.55
Vdd' (V)	2.933	2.435	2.431	2.429	2.426	2.431	2.44	2.433
Vss' (V)	-1.433	-1.433	-1.531	-1.628	-1.725	-1.56	-1.239	-1.482
Idd (mA)	1.103	1.0942	1.139	1.1888	1.2355	1.1561	0.9986	1.118
Iss (mA)	1.061	1.054	1.1016	1.1481	1.1946	1.1157	0.9589	1.0776
I (mA)	1.082	1.0741	1.1203	1.16845	1.21505	1.1359	0.97875	1.0978
P (mW)	4.724012	4.1546188	4.4386286	4.74040165	5.04367255	4.5333769	3.60082125	4.297887

Channel Num			Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz
Channel: 1	4.89	7.49	5.59	6.88	5.63	6.31	9.52	5.27
Channel: 2	6.26	7.77	6.54	7.37	6.70	6.80	9.18	6.34
Channel: 3	10.73	18.74	22.53	13.97	7.03	12.00	18.66	18.43
Channel: 4	6.39	20.00	11.57	7.47	7.61	9.12	30.45	13.73
Channel: 5	6.75	6.56	6.85	9.47	7.76	6.77	13.25	5.28
Channel: 6	10.67	9.27	10.84	15.19	10.75	9.29	12.10	8.99
Channel: 7	6.72	7.18	6.48	5.59	5.68	6.46	22.78	6.71
Channel: 8	6.39	6.88	6.03	5.89	6.16	6.38	13.48	5.40
Channel: 9	5.43	6.66	6.07	5.86	7.16	5.78	28.84	6.43
Channel: 10	9.09	10.72	10.23	9.55	12.39	10.94	49.38	10.94
Channel: 11	9.45	29.07	18.04	10.33	7.28	15.23	22.08	21.22
Channel: 12	8.79	11.48	10.91	8.24	9.73	8.51	12.78	11.47
Channel: 13	7.01	8.73	7.54	6.52	6.55	6.43	22.69	5.99
Channel: 14	8.19	16.24	10.58	6.94	8.29	10.47	46.99	14.49
Channel: 15	15.54	10.15	12.47	16.22	13.47	14.02	13.23	10.84
Channel: 16	7.40	7.30	7.17	7.01	7.18	6.57	10.54	8.60
Channel: 17	6.69	7.30	6.17	5.33	6.99	8.94	11.39	7.16
Channel: 18	6.25	6.14	8.05	6.28	6.48	7.10	8.33	6.65
Channel: 19	6.75	6.85	5.35	7.46	6.61	9.78	14.53	6.24
Channel: 20	7.73	16.06	9.46	7.55	7.45	8.55	21.20	13.10
Channel: 21	10.48	25.58	18.12	10.01	7.18	11.69	19.83	18.55
Channel: 22	7.56	6.21	5.15	6.89	8.07	6.18	5.52	5.61
Channel: 23	6.43	5.99	6.17	6.75	7.09	6.73	18.56	5.98
Channel: 24	9.17	7.07	11.99	8.88	7.86	9.75	10.97	13.45
Median	7.21	7.63	7.79	7.41	7.18	8.53	14.01	7.88
Overall Mean	7.95	11.06	9.58	8.40	7.80	8.74	18.59	9.87
Good Mean	7.62	7.76	8.15	7.74	7.80	8.46	11.14	8.51
MP Req'd					15			
Yield	0.96	0.75	0.88	0.92	1.00	0.96	0.54	0.88
# Good Ch.	23	18	21	22	24	23	13	21
# Bad Ch.	1	6	3	2	0	1	11	3

JFET_Mod9_brd24_Noise_perf.xls

Attachment of HRCR Item # 9: SPIRE MIUL Cover Page

MIUL = Material Identification & Utilization List

Materials and Processes List

SPIRE

JPL D-25725

REV B
1/05/04

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Reviewed by:


M. Knopp M&P Engineer

Attachment of HRCR Item # 11:

**See End of This HRCR Package for
“JFET Module Handling Document”**

Attachment of HRCR Item # 14: JFET Module Top Assembly Drawing 10209750-1

EXPLODED VIEW
REFERENCE ONLY
SCALE: NONE
-1 CONFIGURATION

EXPLODED VIEW
REFERENCE ONLY
SCALE: NONE
-2 CONFIGURATION

GENERAL VIEW
REFERENCE ONLY
SCALE: NONE
ALL CONFIGURATIONS

ITEM	QTY	DESCRIPTION	REV	DATE	BY	CHKD	APP'D
AR 17	1	2218A/B					
AR 16	1	WORNINX					
4	15	NA0069-020006					
16	16	10209719-1					
4	5	13					
8	12	NA0069-016005					
16	16	11					
2	2	10					
2	2	8					
2	2	7					
4	4	6					
2	2	5					
2	2	4					
1	1	3					
1	1	2					
1	1	1					
-2	-1	1					

PARTS LIST

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN MILLIMETERS
LINEAR TOLERANCES:
0-6 ±0.1
6-25 ±0.2
25-100 ±0.3
100-150 ±0.4
150-500 ±0.5
500-1000 ±0.75
ANGULAR TOLERANCES:
M ±0.5

CONTRACT NO. 124886
DATE: 3/15/03
REV. 11/20/03
RELEASED THROUGH EDMS
JFET MODULE ASSEMBLY
CASE NO. 10209750
REV. A
SCALE NONE UNCLASSIFIED SHEET 1 OF 1
REV. 5/06

NOTES: UNLESS OTHERWISE SPECIFIED:
1. THIS ASSEMBLY MEETS INTERFACE REQUIREMENTS OF JPL INTERFACE DRAWING 10209722.
2. TORQUE ITEM 11 AND 12, SCREWS, TO 200 NMM PLUS RUNNING TORQUE PER JPL SPEC E5517040.
3. TORQUE ITEM 13, SCREW, TO 470 NMM PLUS RUNNING TORQUE PER JPL SPEC E5517040.
4. FOR LIST OF MATERIALS ON ITEM 8, BOARD ASSEMBLY, SEE DRAWING 10209780.
5. FOR LIST OF MATERIALS ON ITEM 9, BOARD ASSEMBLY SIMULATOR, SEE DRAWING 10209761.
6. TORQUE ITEM 14, STUDLOCK, TO 2.3-2.9 N*MS PER JPL SPEC E5504255.
7. TORQUE ITEM 15, SCREW, TO 100 NMM PLUS RUNNING TORQUE PER JPL SPEC E5517040.
8. INK STAMP PROJECT, PART NUMBER, REVISION LETTER, SERIAL NUMBER, TITLE, AND JPL, USING ITEM 16 AT APPROXIMATE LOCATION SHOWN, PER JPL SPEC F5500451.
9. SPOT BOND ALL FASTENERS EXCEPT FOR SCREWS USED TO STUDLOCK ITEM 16 USING ITEM 17, EPOXY.
10. Bond Stiffener 10209769-1 (item 18) to board using epoxy HYSOL 9309-3 A/B (item 21). Attach board with stiffeners including locking nut on spring to chassis 2 (10209752-1, item 2) using flat-spring-flat 3-washer set and torque fasteners (NA0069-016008, item 22) to set and torque fasteners (NA0069-016008, item 22) to 220 NMM (111-in-lb) per JPL Spec E5517040, ST 7-6-04.

Handwritten notes:
- (OPTIONAL) INK Stamp Board SW on lid for identification of PWB using item 16 at approximate location shown per JPL spec F550451.
- Bond Stiffener 10209769-1 (item 18) to board using epoxy HYSOL 9309-3 A/B (item 21). Attach board with stiffeners including locking nut on spring to chassis 2 (10209752-1, item 2) using flat-spring-flat 3-washer set and torque fasteners (NA0069-016008, item 22) to 220 NMM (111-in-lb) per JPL Spec E5517040, ST 7-6-04.
- ST 3-19-03
- ST 7-6-04

Signature: Greg Chapman 10-1-2004

Attachment of HRCR Item # 19:

Open PFR on Similar Hardware

PFR	Z82995
PFR	Z82997
PFR	Z82999
PFR	Z83353
PFR	Z83666
PFR	Z83673
PFR	Z84063
PFR	Z84064

Attachment of HRCR Item # 23: Qualification Compliance Test

Qualification Model JFET Module

EIDP Coveragepage For JFET Testing

Unit Identification						
Name	:	JFET QM Module				
Part #	:	10209750-1				
S/N	:	#001				
Environmental Testing						
		Axes Tested	Temperature	Duration/# of Cycle	Requirement	Source
Random Vibration Test		X, Y, Z	100 K	2 min/axis	X, Y, Z	SSSD, JFET-DES-07
High Level Sine Vibe Test		None	NA	NA	X, Y, Z	SSSD, JFET-DES-07
Bakeout		NA	80 C	72 Hours	80C, 72 Hrs	D-20549
Thermal Cycles		NA	RmT to 80 K	27	Minimum 15	D-20549
Performance Characteristics						
			Specification		Source	Waiver
Power needed for <11 bad channels (Min Perf.)	9.1 mW			11 mW for CQM, 7 mW for PFM/FS	SSSD, JFET-TEC-05, JFET-PER-02	RFW in process
Power needed for <4 bad channels (Design Value)	10.8 mW			11 mW for CQM, 7 mW for PFM/FS	SSSD, JFET-TEC-05, JFET-PER-02	
Power needed for 100 % Yield per unit	13.5 mW	NA		NA		
Median Noise at < 11 bad chs.	7.13 nV/rtHz	<15 nV/rtHz		SSSD, JFET-PER-01		
Median Noise at < 4 bad chs.	6.1 nV/rtHz	Min	<7 nV/rtHz	SSSD, JFET-PER-01		
Median Noise at 100 % Yield.	6.97 nV/rtHz	Performance	Design Value	SSSD, JFET-PER-01		
# of Channels over the max. offset voltage	0	< 15 mV for CQM < 15 mV for PFM/FS			SSSD, BDA-DRCU-27	
Common Mode Rejection Ratio	< -80 dB by design, as measured in EM4 unit				SSSD, BDA-DRCU-11	
Board Level Detail						
		Board SN 001			Source	
# Channels Tested	:	24				
Median Noise at 3.5 mW	:	18 nV/rtHz			SSSD, JFET-PER-01	
# of good channels at 3.5 mW	:	7	29% Yield		SSSD, JFET-PER-02	
Power Needed for 100 % Yield	:	6.75 mW				SSSD, JFET-PER-02
Median Noise at High Power (w/ 100 % Yield)		6.97 nV/rtHz			SSSD, JFET-PER-01	
Median Gain at High Power		0.98			NA	
Definitions						
Good Channels	:	Noise less than a min. performance value of 15 nV/rtHz				
Yield	:	# of Good Channels / 24				
Filenames						
Noise Measurements	:	QualJFETPostVibeNoise_Summary.pdf				
Notes						
1) The Base temperature for all performance characterization was 4K						
2) All Noise Measurements were made with the inputs shorted to ground						

Attachment of HRCR Item # 24 & #25: Mate/Demate & Operation Logs

Hardware ID JFET module S/N 8.9							
Date	Time	AIDS	Power	Mate	Demate	Transport	Notes
8/19	9 A	243576				x	103 → 158
8/19	1 P	"					begin pump out (LE-Star)
8/20	6:30 P	"					temp stabilize @ 80°C
8/21	8:00 P	"					begin 80°C → rmt
8/23	7 A	"				x	158 → 183
8/23			x				S.V. all boards (1.5 hr each board)
8/23							assemble into shake facility
8/25						x	183 → 144
8/25							shake 60 sec/axis, 3 axes
8/25						x	144 → 183
8/26							out of shake facility, install in arm dewar
8/26			x				S.V. warm post shake measurements
8/26							pump out
8/27			x				Noise, board 18, 8 hrs
8/28			x				Noise, board 29, 8 hrs
8/28			x				Noise, board 20, 1 hrs
8/30			x				Noise, board 20, 8 hrs
8/31			x				Noise, board 24, 8 hrs
9/1			x				gain, each board 2 hrs
9/2			x				S.V., 4K, 1.5 hr each board
9/13			x				S.V., rmt, 1.5 hr each board
9/13			x				S.V., LN2, 1.5 hr each board
9/15			x				S.V., rmt, 1.5 hr each board
9/15					x	x	out of dewar, over to 103,

Attachment of HRCR Items # 24 & # 25: Mate/Demate & Operation Logs (PWB S/N 020)

USE THE "NOTE" COLUMN TO DESCRIBE ACTIONS

DEVICE (BRD) S/N: 020 (33) PROJECT: SPIRE/JFET BOARD

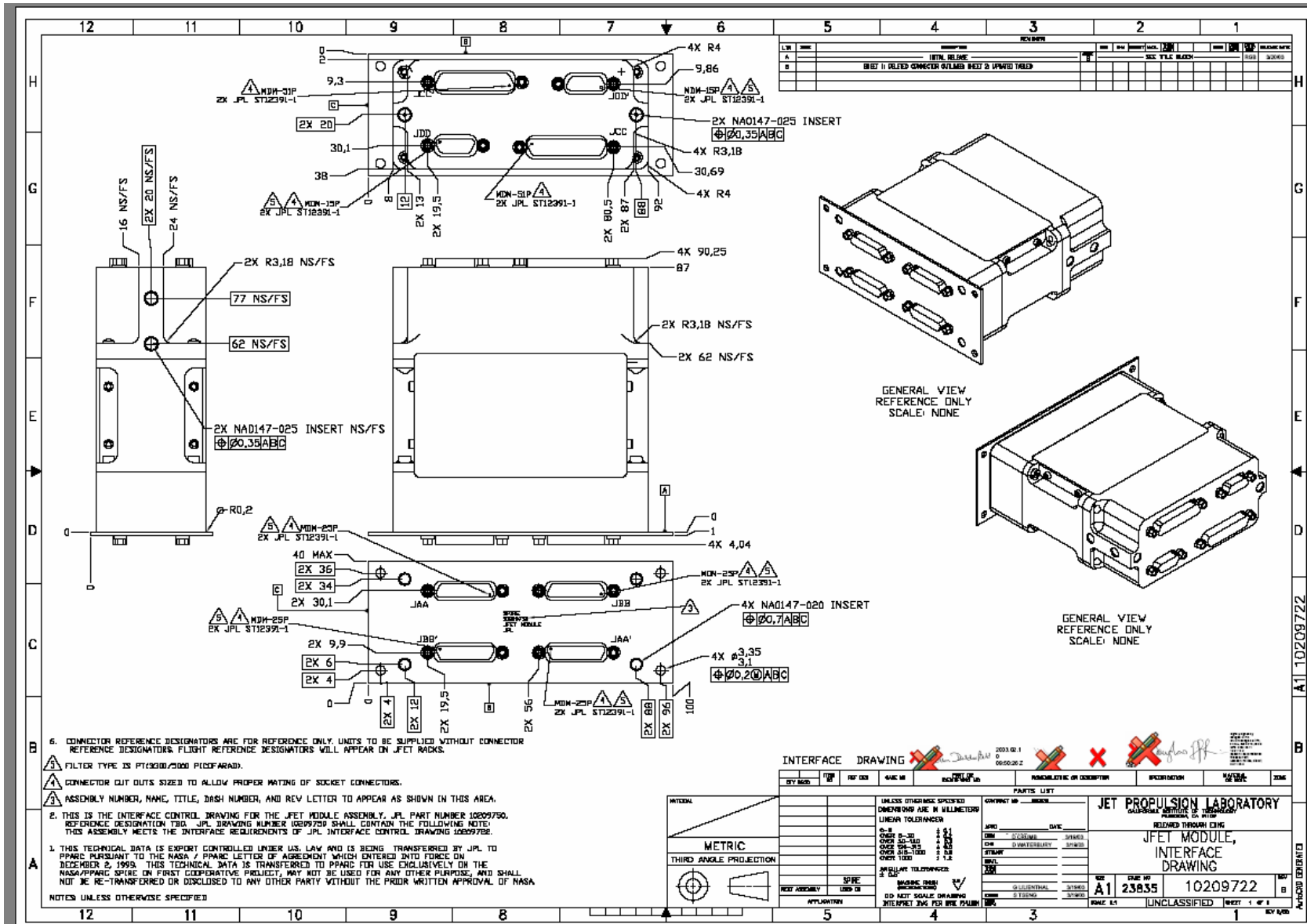
DATE	TIME	TECH	PWR ON	PWR OFF	MATE				DEMATE				TRANSFORT	NOTE
					JAA	JBB	JCC	JDD	JAA	JBB	JCC	JDD		
1-23-4		NAN			/	/	/	/	/	/	/	/		INITIAL GND'S CHASSIS
2-12-4		NAN			/	/	/	/	/	/	/	/		GND'S CHASSIS TEST
2-27-4		NAN												GND'S CHASSIS TEST
3-4-4		NAN												GND "
3-4-4		NAN	/	/										SOURCE TEST
5-18-4		NAN												GND'S CHASSIS
5-18-4		NAN	/	/										SOURCE TEST
5-20-4		NAN												GND'S CHASSIS
5-20-4		NAN	/	/										SOURCE TEST
8-5-4		NAN							/	/	/	/		DEMATE SAVER
8-6-4		NAN			/	/	/	/			/	/		GND'S CHASSIS
8-6-4		NAN	/	/			/	/	/	/				SOURCE TEST
8-12-04		NAN			/	/	/	/	/	/	/	/		GND'S CHASSIS
8/12-04		NAN	/	/			/	/	/	/	/	/		SOURCE TEST
8/13/04		NAN			/	/	/	/			/	/		GND'S CHASSIS
8/14/04		NAN			/	/	/	/			/	/		GND'S CHASSIS
8/14/04		NAN	/	/			/	/						SOURCE TEST

Attachment of HRCR Items # 24 & # 25: Mate/Demate & Operation Logs (PWB S/N 024)

DEVICE/BRD S/N: 24 (38) PROJECT: SPIRE/JFET BOARD USE THE "NOTE" COLUMN TO DESCRIBE ACTIONS

DATE	TIME	TECH	PWR ON	PWR OFF	MATE				DEMATE				TRANSFORT	NOTE
					JAA	JBB	JCC	JDD	JAA	JBB	JCC	JDD		
3-3-4	3:00 P	NW			1	1	1	1						GND & CHASSIS TEST
3-4-4	7:00 A	NW			1	1	1	1						GND & CHASSIS TEST
3-4-4	7:30	NW			1	1	1	1						SAVER ON
3/19/04		NW												GND & CHASSIS w/ SAVER ON
4-5-04		NW												GND & CHASSIS
4-5-04		NW	✓	✓										SOURCE
7-16-4		NW												GND & CHASSIS
7-16-4		NW	✓	✓										SOURCE
8-5-4		NW							1	1	1	1		DEMATE SAVERS
8-6-4		NW			1	1	1	1			1	1		GND & CHASSIS
8-6-4		NW	✓	✓	1	1	1	1						SOURCE TEST
8-9-4		NW			1	1	1	1			1	1		GND & CHASSIS
8-9-4		NW	✓	✓			1	1	1	1				SOURCE TEST
8-12-4		NW			1	1	1	1			1	1		GND & CHASSIS
8-12-4		NW	✓	✓			1	1	1	1				SOURCE TEST
8-14-4		NW			1	1	1	1			1	1		GND & CHASSIS
8-14-4		NW	✓	✓			1	1	1	1				SOURCE

Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 1 of 2)



Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 2 of 2)

	12	11	10	9	8	7	6	5	4	3	2	1																																																															
H	JAA JFET OUTPUT 1B					JAB JFET OUTPUT 2A					JCC JFET INPUT 1					JDD JFET SERVICE 1					JCD' JFET INPUT 2																																																						
	PIN #	PIN PURPOSE											PIN #	PIN PURPOSE											PIN #	PIN PURPOSE											PIN #	PIN PURPOSE											PIN #	PIN PURPOSE																									
	1	SIGNAL M+											1	SIGNAL M+											1	BIAS V+											1	VSS											1	BIAS V+																									
	2	SIGNAL N+											2	SIGNAL N+											2	BIAS V-											2	V+											2	BIAS V-																									
	3	SIGNAL P+											3	SIGNAL P+											3	SIGNAL Y+											3	H+											3	SIGNAL Y+																									
	4	SIGNAL R+											4	SIGNAL R+											4	SIGNAL W-											4	V-											4	SIGNAL W-																									
	5	SIGNAL S+											5	SIGNAL S+											5	SIGNAL V+											5	V-											5	SIGNAL V+																									
	6	SIGNAL T+											6	SIGNAL T+											6	SIGNAL T+											6	H+											6	SIGNAL T+																									
	7	SIGNAL U-											7	SIGNAL U-											7	SIGNAL S-											7	V+											7	SIGNAL S-																									
	8	SIGNAL V-											8	SIGNAL V-											8	SIGNAL P+											8	VSS											8	SIGNAL P+																									
	9	SIGNAL W-											9	SIGNAL W-											9	SIGNAL N-											9	BIAS GND											9	SIGNAL N-																									
	10	SIGNAL X-											10	SIGNAL X-											10	SIGNAL L-											10	Vdd											10	SIGNAL L-																									
	11	SIGNAL Y-											11	SIGNAL Y-											11	SIGNAL K+											11	H-											11	SIGNAL K+																									
	12	SIGNAL Z-											12	SIGNAL Z-											12	SIGNAL I-											12	CHASSIS GND											12	SIGNAL I-																									
	13	FPU GND											13	FPU GND											13	SIGNAL H+											13	H-											13	SIGNAL H+																									
	14	SIGNAL M-											14	SIGNAL M-											14	SIGNAL F+											14	Vdd											14	SIGNAL F+																									
	15	SIGNAL N-											15	SIGNAL N-											15	SIGNAL E-											15	BIAS GND											15	SIGNAL E-																									
	16	SIGNAL P-											16	SIGNAL P-											16	SIGNAL C+											JDD' JFET SERVICE 2					16	SIGNAL C+																																
	17	SIGNAL R-											17	SIGNAL R-											17	SIGNAL B-											PIN #	PIN PURPOSE											17	SIGNAL B-																									
	18	SIGNAL S-											18	SIGNAL S-											18	SIGNAL A-											1	VSS'											18	SIGNAL A-																									
	19	SIGNAL T-											19	SIGNAL T-											19	BIAS GND											2	V+											19	BIAS GND'																									
	20	SIGNAL U+											20	SIGNAL U+											20	SIGNAL Z+											3	H+											20	SIGNAL Z+																									
	21	SIGNAL V+											21	SIGNAL V+											21	SIGNAL X-											4	V-											21	SIGNAL X-																									
	22	SIGNAL W+											22	SIGNAL W+											22	SIGNAL W+											5	V-											22	SIGNAL W+																									
	23	SIGNAL X+											23	SIGNAL X+											23	SIGNAL U-											6	H+											23	SIGNAL U-																									
24	SIGNAL Y+											24	SIGNAL Y+											24	SIGNAL T-											7	V+											24	SIGNAL T-																										
25	SIGNAL Z+											25	SIGNAL Z+											25	SIGNAL R+											8	VSS'											25	SIGNAL R+																										
JBB JFET OUTPUT 1A													JBB' JFET OUTPUT 2B																																																														
PIN #	PIN PURPOSE											PIN #	PIN PURPOSE																																																														
1	SIGNAL A+											1	SIGNAL A+																																																														
2	SIGNAL B+											2	SIGNAL B+																																																														
3	SIGNAL C+											3	SIGNAL C+																																																														
4	SIGNAL D+											4	SIGNAL D+																																																														
5	SIGNAL E+											5	SIGNAL E+																																																														
6	SIGNAL F+											6	SIGNAL F+																																																														
7	SIGNAL G-											7	SIGNAL G-																																																														
8	SIGNAL H-											8	SIGNAL H-																																																														
9	SIGNAL I-											9	SIGNAL I-																																																														
10	SIGNAL J-											10	SIGNAL J-																																																														
11	SIGNAL K-											11	SIGNAL K-																																																														
12	SIGNAL L-											12	SIGNAL L-																																																														
13	FPU GND											13	FPU GND																																																														
14	SIGNAL A-											14	SIGNAL A-																																																														
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23	SIGNAL J+											23	SIGNAL J+																																																														
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25	SIGNAL L+											25	SIGNAL L+																																																														
12	11	10	9	8	7	6	5	4	3	2	1																																																																

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Attachment of HRCR Item # 11:

SPIRE

Handling Document

Field Effect Transistor (JFET) Module

10209750-1

Prepared by: Kalyani Sukhatme

10 September, 2003

Hardware Handling Guidelines

Contamination: Open shipment suitcase in a FED-STD-209 Class 10,000 clean room (ISO 14644-1 class 7) or better. Handle hardware with gloves.

ESD: Handle with grounding straps, ESD-safe gloves and ESD smocks at an ESD-safe workstation. Maintain shorting plugs on the unit whenever ESD is a concern. Refer to attached electrical handling document for other important safety precautions.

Fragile: Do not drop or otherwise shock the hardware including the shipping suitcase and container.

Humidity Sensitive: Place hardware in a humidity controlled Class 10,000 clean room. Maintain humidity level at 35%-50% RH typical, for ESD safety.

SPIRE JFET Electrical Handling Document

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1. Introduction

This document provides guidelines for electrical handling for the SPIRE JFET Module.

1.1 Hardware Description

Each JFET module has two sets of 24 JFET channels. The JFET channels are populated on 1.0 micron thick Silicon Nitride membranes which provides thermal isolation. The operating temperature for these JFETs is ~120 K. The process of powering up the JFETs dissipates heat into the membrane resulting in a temperature increase with respect to the base temperature (4K to 10 K). Higher the power dissipation, higher is the temperature of the JFETs.

Each JFET channel consists of a matched pair of FETs (Figure 1.1-1) with a requirement for the offset voltage of less than **15 mV** between the matched pair. [The characteristic offset voltage is the difference between the source voltages (V_{sa} and V_{sb} with respect to ground) of the two FETs.]

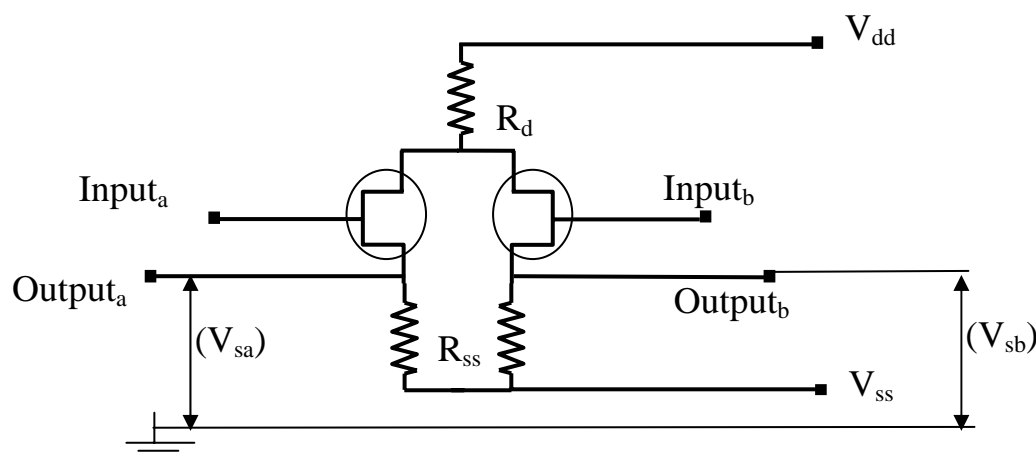


Figure 1.1-1

The Gates of the JFETs are the 'Inputs' of the circuit and the Sources (V_{sa} and V_{sb}) of the JFETs are the outputs, as marked in Figure 1.1-1. V_{dd} and V_{ss} are the power lines for the circuit.

Handling

1. **The JFET Module is Contamination Sensitive:** Handle the unit with Gloves only in a FED-STD-209 Class 100000 clean room (ISO 14644-1 class 7) or better.
2. **The JFET Module is ESD Sensitive:** Please handle with appropriate ESD hardware handling procedures. Handle with grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.
3. **The JFET Module is Fragile:** Please do not drop or otherwise shock the unit. Please DO NOT remove the cover of the JFET Module.

Power ON Procedure

1. The JFET Module should be powered on **WITH the shorting plugs** (JPL Supplied Protection connectors) in place and with the **inputs shorted to ground**. Pins #9 and #15 on the 15-pin MDM connectors on the JFET Module are the bias grounds on the module. These pins should also be shorted to the power supply ground. The unit may be powered up without the shorting plug only when the inputs are connected to the detector system.

Under no circumstances the unit should be powered up without the inputs shorted to ground either via the shorting plug (JPL Supplied) or via the detector system.

2. Do not exceed a voltage of +5 V for the Vdd line and -5 V for the Vss line of the JFET Module.
3. When removing the shorting plugs from the unit for installation into the instrument, please use standard ESD precautions including grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.

Electrical Check-out Test: Characteristic Offset Voltage Measurement

- 1) Verify that the gates of the JFET channels (Inputs) are shorted together and grounded.
- 2) Apply the power supply ground to the bias ground pins on the unit (Pins 9 and 15 on the 15-pin MDM connectors)
- 3) Power on the JFET modules with Vdd = +3 V and Vss = -1.5 V
- 4) Verify that the handheld multimeter is in calibration.
- 5) Connect one side of the handheld multimeter to ground (Power supply ground).
- 6) And measure the voltage with respect to ground of each side (V_{sa} and V_{sb}) of each channel.
- 7) Calculate the characteristic offset voltage (V_{offset}) for each channel (V_{offset}= V_{sa}-V_{sb})
- 8) Compare the values for each of the channels with the specific datasheet provided with the unit.
The datasheets accompanying the unit also provides the values for the drain and source currents for a similar test performed at JPL.

REFER TO MEASURED SOURCE VOLTAGE DATA FOR ACTUAL HARDWARE. Here is an example of the source voltage values and the drain and the source currents obtained for such a test at room temperature are given in the Table 4-1

T, JFET	rm T	
Vdd	3 V	
Vss	-1.5 V	
Idd	1.564 mA	
Iss	1.5686 mA	
Channel #	(V)	DELTA (V)
1	1.130	0
	1.130	
2	1.075	0.001
	1.074	
3	0.781	0.001
	0.780	
4	1.088	0.005
	1.093	
5	0.834	0.001
	0.833	
6	1.012	0.003
	1.015	
7	0.785	0.002
	0.787	
8	1.148	0.004
	1.144	
9	0.753	0
	0.753	

10	0.693	0.008
	0.701	
11	1.110	0.004
	1.114	
12	0.758	0.001
	0.759	
13	0.832	0.002
	0.830	
14	1.264	0.001
	1.265	
15	1.206	0
	1.206	
16	0.818	0.001
	0.819	
17	0.526	0.005
	0.521	
18	1.423	0
	1.423	
19	0.773	0.002
	0.775	
20	0.873	0.004
	0.877	
21	1.387	0.006
	1.393	
22	1.417	0.003
	1.420	
23	0.887	0.002
	0.889	
24	0.888	0.003
	0.891	

- END OF -
Attachment of HRCR Item # 11:
JFET Module Handling Document

Attachment of HRCR Item # 19:

Open PFR on Similar Hardware

PFR	Z82995
PFR	Z82997
PFR	Z82999
PFR	Z83353
PFR	Z83666
PFR	Z83673
PFR	Z84063
PFR	Z84064

END OF
HRCR PACKAGE