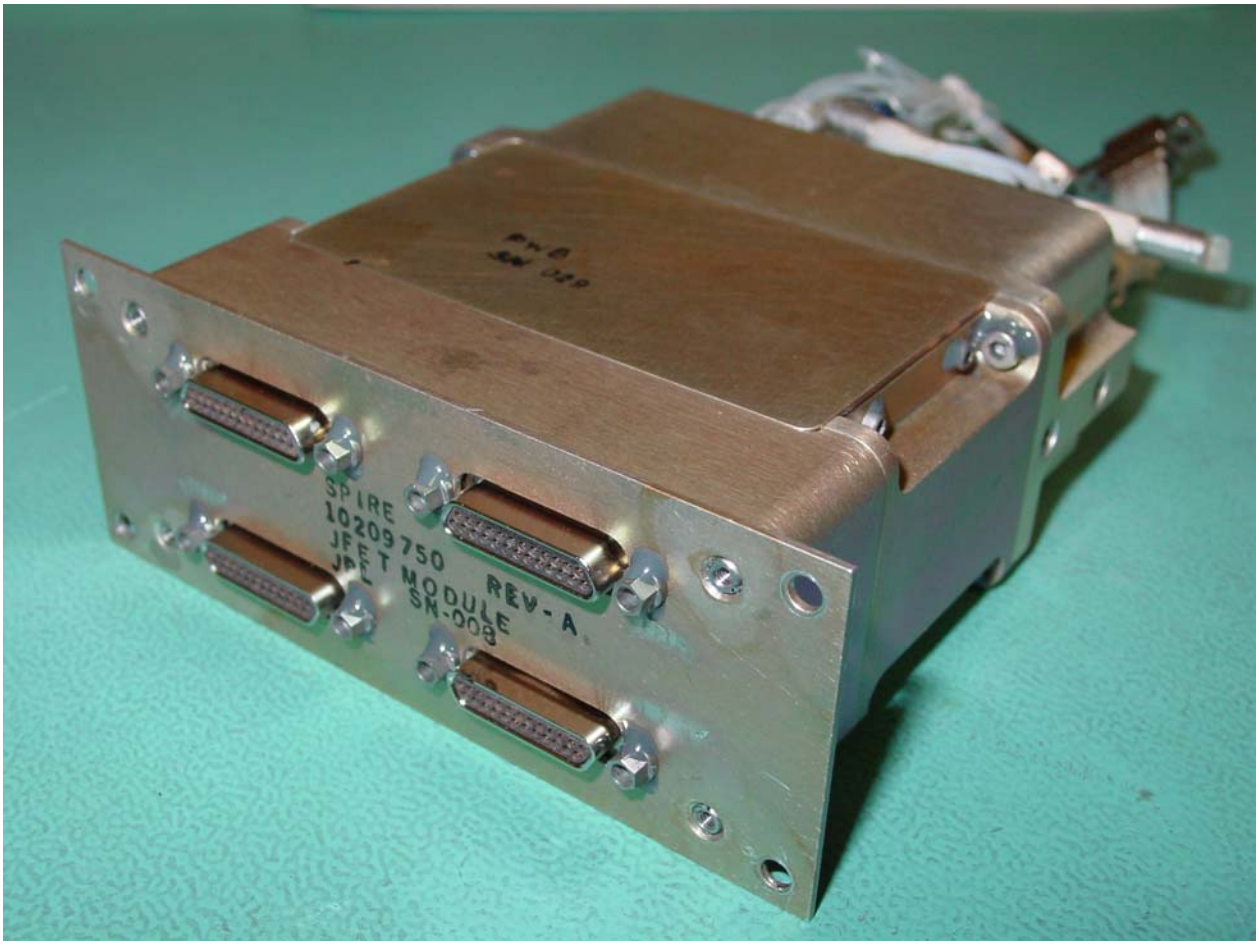
Signed HRCR 1st page

JPL Hardware Requirements Certification Review – SPIRE Element No. D-30419

Assembly / Subsystem		PEM		Phone		Section		Date
SPIRE		Martin Herman		(818) 354-8541		386		11 October, 2004
Drawing/ Part No.	Dwg. Rev.	Nomenclature		Serial No.	Model	Type	Final IR No.	Mass (Meas. / Req.)
10209750-1	A	JFET Module		008	FLIGHT	N/A	922703	271 gm / 305 gm

Check applicable answer and provide explanation in remarks column	YES	NO	NA	Remarks	Data Attachments	Signature & Date
1. Are all drawings and specifications complete, approved, released and frozen?		X		See Attached	14. Latest Top Assembly drawings ☒ Attached ☐ None	Cognizant Engineer Steve Tsey 10/11/04
2. Do the released drawings and specifications reflect all approved changes?	X	~~X~~		See Attached	15. List of open ECRs ☐ Attached ☒ None	PEM For MIH Richard P. Vaguine 10/11/04
3. Is hardware identical to other hardware delivered? If no, provide difference list.	~~X~~		X		16. Waivers (RFW request for waiver) ☒ Attached ☐ None	QA Engineer 11/29/04 Lorraine Valenzuela
4. Does the hardware meet its functional requirements, specifications, waivers, ICDs?	X			EIDP attached. Also see item #8 attachments.	17. Open MRB ☐ Attached ☒ None	Environments/Reliability
5. Are all IR and MRB's dispositioned and concurred by QA?	X				18. Open PFR on this H/W ☐ Attached ☒ None	Mission Assurance Mgr.
6. Is complete as-built list information included in the build book?	X				19. Open PFR on similar H/W ☒ Attached ☐ None	Project Office 10/11/04 Margaret C. Frerichs
7. Have all required environmental tests & analyses been completed?	X			ETAS attached	20. Handling Document → See Item 11 ☒ Attached ☐ None	PI 10/8/04 Martin Herman for JB
8. Is all required assembly and/or subsystem level functional testing complete?	X			Test Results Attached. Also see ~~EDIP~~ EIDP in item #4.	21. Shortage List ☐ Attached ☒ None	
9. Have all piece parts, processes and materials been approved by JPL?	X				22. Requirements Verification Matrix ☒ Attached (See #4, #7, #8) ☐ None	
10. Does this hardware meet all contamination control requirements?	X			Parts, processes and MIUL met all contamination control and out-gassing requirements.	23. Qualification Status ☒ Attached ☐ None	
11. Are all shipping containers, shipping and special handling procedures ready?	X			See Attached Document D-26790	24. Mate / Demate Record ☒ Attached ☐ None	
12. Is additional work required to bring this hardware to flight readiness?		X			25. Operating Log ☒ Attached (See Item # 24) ☐ None	
13. Is this hardware acceptable for flight?	X				26. MICD ☒ Attached ☐ None	

SPIRE JFET Moudle S/N 008



RAL EIDP Table of Contents Versus JPL HRCR Check List Item Numbers

RAL EIDP Section Number	RAL EIDP Title	JPL HRCR Check List Item Number	Notes
1	Shipping Documents		Shipper and Final IR
2	Transportation, Packing, Handling & Integration Procedures	11	Special Handling Document D-26790
3	Certificate of Conformance / Delivery Review Board MOM		HRCR book is the C of C
4	As Built Configuration Status List	1 & 2	Drawing List & Status
5	List of Waivers	4	RFW (request for waiver) Attached
6	Copies of Waivers	4 & 7	RFW (request for waiver) Attached
7	List of Non-Conformance Reports		See RFW in 4 & 7
8	Copies of Non-Conformance Reports		See RFW in 4 & 7
9	Cleanliness Statement		Final IR QA Inspection
10	Operational Manual		NA
11	Top Level Drawings (inc. Family Tree)	14	Top Assembly Drawing
12	Interface Drawings	26	MICD Drawing
13	Functional, Block & Mechanical Drawings		NA
14	Electrical Circuit Drawings		NA
15	Serialized Components List		In build books – not shipped
16	Mass Properties/ Power Budget	HRCR Check List Page 1	Mass listed in HRCR check list
17	Qualification Status List / Test Matrix	23	Qualification Unit Test Matrix
18	Test Reports	4, 7, 8, 23	
19	Open Work / Deferred Work / Open Tests		NA
20	Calibration Data		NA
21	Historical Record	23	Qualification Unit Test Matrix
22	Manufacturing Logbook(s)		In build books – not shipped
23	Operating Time / Cycle Record	25	
24	Connector Mating Record	24	
25	Age Sensitive Items Record		NA
26	Pressure Vessels – History/Test Record		NA
27	Temporary Installation Record		NA
28	Reference List of EIDPs (Lower level)		NA
29	Other Useful Information		NA

JPL Hardware Requirements Certification Review (HRCR)

Junction Field Effect Transistor (JFET) Flight Module

10209750-1 S/N 008

SPIRE Element
Herschel Space Observatory Project

October 11, 2004

Module 10209750-1	S/N 8	S/N 8	S/N 9	S/N 9
PWB 10209760-1	S/N 18	S/N 29	S/N 20	S/N 24
Membrane 10209758-1	J5.5.1	J6.8.5	J5.5.4	J5.6.4

Attachment of HRCR Items #1

Drawing Release Status

All redlined drawings to be updated and placed in JPL PDMS for approval by the end of calendar year 2004

Redlined / Unreleased Drawings:

10209750-1 redlined Rev. A drawing (module assy)
10209751-1 redlined Rev. A drawing (chassis 1)
10209754-1 redlined Rev. B drawing (mount)
10209757-1 unreleased Rev. A drawing (membrane)
10209759-1,-2,-4 redlined Rev. A drawing (gasket)
10209760-1 redlined Rev. A drawing (board assy)
10209761-1 redlined Rev. A drawing (soldering board)
10209769-1 unreleased Rev. X2 drawing (stiffener)
10209777-1 redlined Rev. A drawing (board)
10217636-1 unreleased Rev. A drawing (clip)

Released Drawings:

10209722-1 assembly built per released Rev.B drawing (interface drawing)
10209758-1 assembly built per released Rev.A drawing (membrane assy)
10209858-2 assembly built per released Rev.A drawing (special fastener)
10209752-1 assembly built per released Rev.A drawing (chassis 2)
10209753-1 assembly built per released Rev.A drawing (chassis 3)
10209756-1 assembly built per released Rev.B drawing (chassis lid)
10209719-1 assembly built per released Rev.A drawing (studlock)

Attachment of HRCR Item #4: EIDP

EIDP Coverpage For JFET Testing

Unit Identfication							
Name	:	JFET PFM Module					
Part #	:	10209750-1					
S/N	:	#008					

Environmemtal Testing	Axes Tested	Temp	Duration/# of Cycle	Requirement	Source	Waiver
Random Vibration Test	X, Y, Z	Rm T	1 min/axis	X, Y, Z	SSSD, JFET-DES-07	
High Level Sine Vibe Test	None	NA	NA	X, Y, Z	SSSD, JFET-DES-07	HR-SP-JPL-RFW-005
Bakeout	NA	80 C	25.5 hrs	> 24 HRS		
Thermal Cycles	NA	RmT to 80 K	2	Minimum 1	D-20549	

Performance Characteristics		Specification		Source	Waiver
Power needed for <11 bad channels (Min Perf.)	8.71 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	HR-SP-JPL-RFW-004
Power needed for <4 bad channels (Design Value)	10.00 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	
Power needed for 100 % Yield per unit	10.84 mW	NA		NA	
Median Noise at < 11 bad chs.	8.11 nV/rtHz	<15 nV/rtHz Min Performance	<7 nV/rtHz Design Value	SSSD, JFET-PER-01	
Median Noise at < 4 bad chs.	7.06 nV/rtHz			SSSD, JFET-PER-01	
Median Noise at 100 % Yield.	6.94 nV/rtHz			SSSD, JFET-PER-01	
# of Channels over the max. offset voltage	0	< 15 mV		SSSD, BDA-DRCU-27	
Common Mode Rejection Ratio	< -60 dB by design, as measured in EM4 unit			SSSD, BDA-DRCU-11	

Board Level Details		Board SN 018 (JAA'-JDD')		Board SN 029 (JAA-JDD)		Source
# Channels Tested	:	24		24		
Median Noise at 3.5 mW	:	36.34 nV/rtHz		14.54 nV/rtHz		SSSD, JFET-PER-01
# of good channels at 3.5 mW	:	2	8% Yield	12	50% Yield	SSSD, JFET-PER-02
Power Needed for 100 % Yield	:	5.54 mW		5.31 mW		SSSD, JFET-PER-02
Median Noise at High Power (w/ 100 % Yield)		6.53 nV/rtHz		7.17 nV/rtHz		SSSD, JFET-PER-01
Median Gain at High Power		0.98		0.98		NA
Heater Resistance, 4K Reference value		2.499 kΩ		3.350 kΩ		NA

Definitions		
Good Channels	:	Noise less than a min. performance value of 15 nV/rtHz
Yield	:	# of Good Channels / 24
Filenames		
Noise Measurements	:	JFET_Module_SN08_Noise_data.pdf
Source Voltages (RmT, 4K)	:	JFET Module SN08,SN09 source voltage data.pdf
Notes		
1) The Base temperature for all performance characterization was 4K		
2) All Noise Measurements were made with the inputs shorted to ground		
3) Type of membranes:		SN018: 24% Overetched / SN029: 64% Overetched

Attachment of HRCR Item # 4: RFW (request for waiver)

RFW/RFD Number:	HR-SP-JPL-RFW-**TBD**

Spacecraft / Project	Herschel	**Originator's Name**	Steve Tseng	
System / Experiment / Model	**1.1 SPIRE**	**Signature / Date**		
Sub-System	detectors	**Request Type** **(Highlight applicable request)**	Waiver (RFW)	Deviation (RFD)
Assembly	JFET modules	1.1.1.1 Organisation	Jet Propulsion Laboratory	
Sub-Assembly		**Ref. Doc. / Drwg No.**	SPIRE-JPL-PRJ-000456	
Item		**References**		
Serial No.				
RFW/RFD Title	**JFET Power Dissipation s/n 008**			

End Items(s) Affected (Hardware, Software)		
Name	**CI-Number**	**Model(s)**
JFET Module p/n 10209750 s/n 008		PFM

Requirement / Interface Documents Affected				
Specification/Drawing Title	**Number**	**Issue**	**Date**	**App. Paragraph**
BDA-SSSD	SPIRE-JPL-PRJ-0004456	3.2	7/1/03	JFET-PER-01 JFET-PER-02 JFET-TEC-05

Description of Deviation / Discrepancy / Non-Conformance

Requirement states that dissipation of photometer JFETs is to be less than 7 mW average, while supplying 90% of channels with voltage noise < 15 nV/rtHz according to BDA-SSSD JFET-PER-01, JFET-PER-02, JFET-TEC-05. Measured JFET performance of the JFETs indicates that 10.84 mW of power dissipation will be required to meet the specified yield and noise performance specifications.

Other Items or Requirements (Potentially) Affected

Overall sensitivity of the bolometer sub-system is affected by JFET noise performance. JFET power dissipation impacts the heat sink temperature of the 3He refrigerator and may in turn increase the base detector temperature. Dissipation of JFETs affects power dissipation on cryostat.

Need for RFW/RFD and Rationale for Acceptance

Measured JFET performance of JFETs indicates that 10.84 mW of power dissipation will be required to meet the specified yield and noise performance specifications. JPL is unable to significantly alter the JFET fabrication process in order to meet the power specification without undue risk to the stated PFM/FS delivery dates. Furthermore, JPL requests a full system optimisation to revisit the noise and power requirements on the JFETs. The JFET modules can meet the noise design value with 100 % yield at higher dissipation.

	Approved	**Rejected**	**Name**	**Date**
Engineering:				
Product Assurance:				
CCB-Chairman:				
Principal Investigator				
Product Assurance:				
Co-Investigator				
Prime Contractor				
ESA Project Office				

Attachment of HRCR Item #7: RFW (request for waiver)

RFW/RFD Number:	HR-SP-JPL-RFW-005

Spacecraft / Project	Herschel	**Originator's Name**	Kalyani Sukhatme	
System / Experiment / Model	**SPIRE**	**Signature / Date**		
Sub-System	detectors	**Request Type** **(Highlight applicable request)**	Waiver (RFW)	Deviation (RFD)
Assembly		Organisation	Jet Propulsion Laboratory	
Sub-Assembly		**Ref. Doc. / Drwg No.**	SPIRE-JPL-PRJ-000456	
Item		**References**		
Serial No.				
RFW/RFD Title	**BDA and JFET module sine test deletion**			

End Items(s) Affected (Hardware, Software)		
Name	**CI-Number**	**Model(s)**
Bolometric Detector Assemblies JFET Modules		CQM, PFM, FS CQM, PFM, FS

Requirement / Interface Documents Affected				
Specification/Drawing Title	**Number**	**Issue**	**Date**	**App. Paragraph**
BDA-SSSD (SPIRE-JPL-PRJ-000456)		3.2	Jan 7, 2003	BDA-DES-10, JFET-DES-07

Description of Deviation / Discrepancy / Non-Conformance

High Level Sine- Vibe Test is not performed on these units

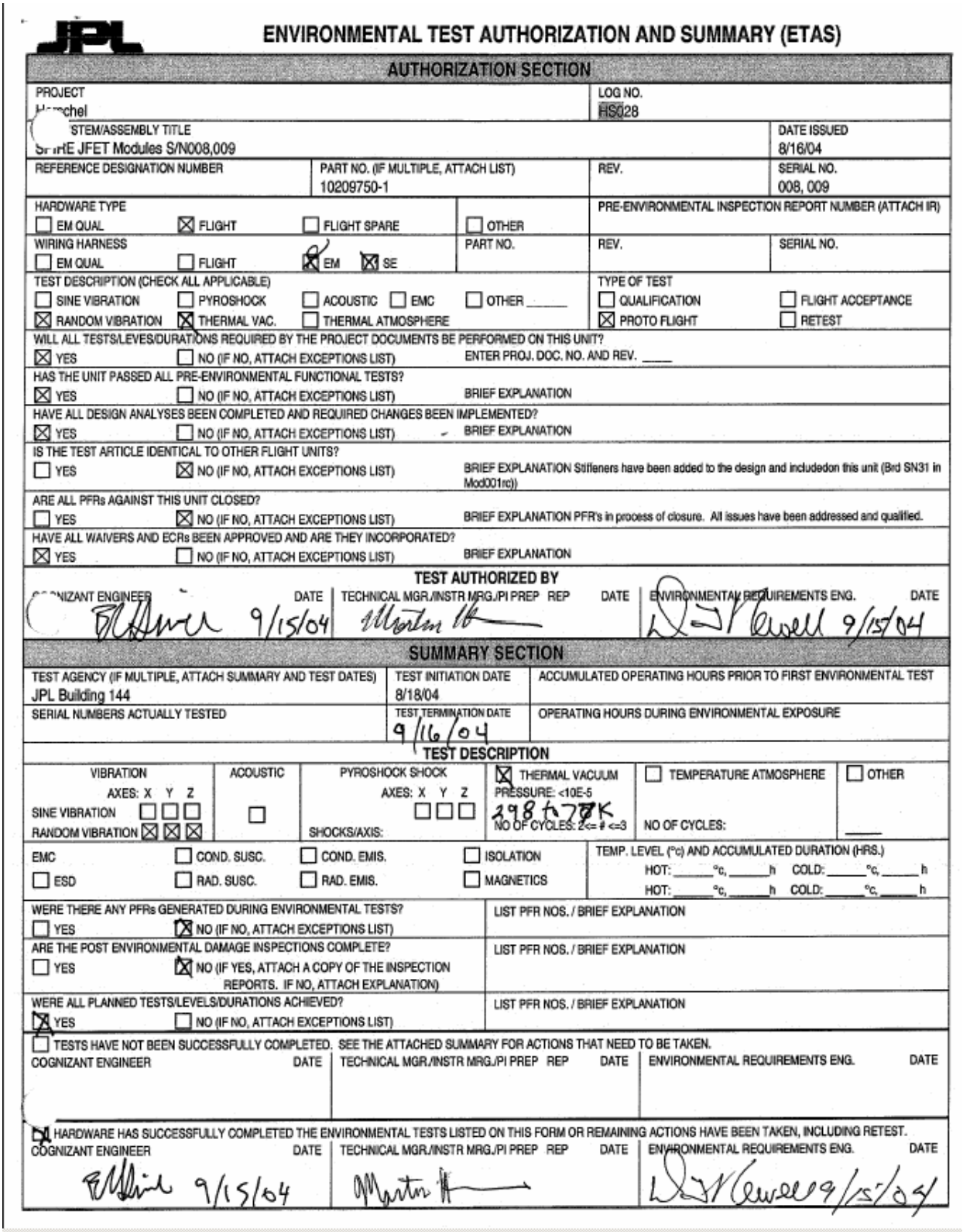
Other Items or Requirements (Potentially) Affected

Need for RFW/RFD and Rationale for Acceptance

The hardware has to be qualified under a cold vibration test and is installed in the cold vibration facility for the purpose of the test. The high level sine vibration test configuration will put the hardware and the personnel at risk since the cold vibration facility is not structurally capable of withstanding the high levels. Obtaining additional resources (cost and schedule) for developing a new set-up is not feasible at this time.

	Approved	**Rejected**	**Name**	**Date**
JPL Engineering:				
JPL Product Assurance:				
CCB-Chairman:				
Principal Investigator				
Product Assurance:				
Co-Investigator				
Prime Contractor				
ESA Project Office				

Attachment of HRCR Item #7: ETAS (environmental test summary)
For Module 8 & 9



ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)

AUTHORIZATION SECTION

PROJECT: Herschel		LOG NO.: HS028	
SYSTEM/ASSEMBLY TITLE: SPIRE JFET Modules S/N008,009			DATE ISSUED: 8/16/04
REFERENCE DESIGNATION NUMBER	PART NO. (IF MULTIPLE, ATTACH LIST): 10209750-1	REV.	SERIAL NO.: 008, 009

HARDWARE TYPE: ☐ EM QUAL ☒ FLIGHT ☐ FLIGHT SPARE ☐ OTHER — PRE-ENVIRONMENTAL INSPECTION REPORT NUMBER (ATTACH IR)

WIRING HARNESS: ☐ EM QUAL ☐ FLIGHT ☒ EM ☒ SE — PART NO. — REV. — SERIAL NO.

TEST DESCRIPTION (CHECK ALL APPLICABLE): ☐ SINE VIBRATION ☐ PYROSHOCK ☐ ACOUSTIC ☐ EMC ☐ OTHER ____ ☒ RANDOM VIBRATION ☒ THERMAL VAC. ☐ THERMAL ATMOSPHERE

TYPE OF TEST: ☐ QUALIFICATION ☐ FLIGHT ACCEPTANCE ☒ PROTO FLIGHT ☐ RETEST

WILL ALL TESTS/LEVES/DURATIONS REQUIRED BY THE PROJECT DOCUMENTS BE PERFORMED ON THIS UNIT?
☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) ENTER PROJ. DOC. NO. AND REV. ____

HAS THE UNIT PASSED ALL PRE-ENVIRONMENTAL FUNCTIONAL TESTS?
☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION

HAVE ALL DESIGN ANALYSES BEEN COMPLETED AND REQUIRED CHANGES BEEN IMPLEMENTED?
☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION

IS THE TEST ARTICLE IDENTICAL TO OTHER FLIGHT UNITS?
☐ YES ☒ NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION Stiffeners have been added to the design and includedon this unit (Brd SN31 in Mod001rc))

ARE ALL PFRs AGAINST THIS UNIT CLOSED?
☐ YES ☒ NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION PFR's in process of closure. All issues have been addressed and qualified.

HAVE ALL WAIVERS AND ECRs BEEN APPROVED AND ARE THEY INCORPORATED?
☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION

TEST AUTHORIZED BY

COGNIZANT ENGINEER	DATE	TECHNICAL MGR./INSTR MRG./PI PREP REP	DATE	ENVIRONMENTAL REQUIREMENTS ENG.	DATE
[signature]	9/15/04	[signature]		[signature]	9/15/04

SUMMARY SECTION

TEST AGENCY (IF MULTIPLE, ATTACH SUMMARY AND TEST DATES)	TEST INITIATION DATE	ACCUMULATED OPERATING HOURS PRIOR TO FIRST ENVIRONMENTAL TEST
JPL Building 144	8/18/04	
SERIAL NUMBERS ACTUALLY TESTED	TEST TERMINATION DATE: 9/16/04	OPERATING HOURS DURING ENVIRONMENTAL EXPOSURE

TEST DESCRIPTION

VIBRATION	ACOUSTIC	PYROSHOCK SHOCK	THERMAL VACUUM	TEMPERATURE ATMOSPHERE	OTHER
AXES: X Y Z		AXES: X Y Z	☒ PRESSURE: <10E-5	☐	☐
SINE VIBRATION ☐☐☐	☐	☐☐☐	298 to 78K		
RANDOM VIBRATION ☒☒☒		SHOCKS/AXIS:	NO OF CYCLES: 2<= # <=3	NO OF CYCLES:	____

EMC	☐ COND. SUSC.	☐ COND. EMIS.	☐ ISOLATION	TEMP. LEVEL (°c) AND ACCUMULATED DURATION (HRS.)
☐ ESD	☐ RAD. SUSC.	☐ RAD. EMIS.	☐ MAGNETICS	HOT: ____°c, ____h COLD: ____°c, ____h
				HOT: ____°c, ____h COLD: ____°c, ____h

WERE THERE ANY PFRs GENERATED DURING ENVIRONMENTAL TESTS?
☐ YES ☒ NO (IF NO, ATTACH EXCEPTIONS LIST) — LIST PFR NOS. / BRIEF EXPLANATION

ARE THE POST ENVIRONMENTAL DAMAGE INSPECTIONS COMPLETE?
☐ YES ☒ NO (IF YES, ATTACH A COPY OF THE INSPECTION REPORTS. IF NO, ATTACH EXPLANATION) — LIST PFR NOS. / BRIEF EXPLANATION

WERE ALL PLANNED TESTS/LEVELS/DURATIONS ACHIEVED?
☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) — LIST PFR NOS. / BRIEF EXPLANATION

☐ TESTS HAVE NOT BEEN SUCCESSFULLY COMPLETED. SEE THE ATTACHED SUMMARY FOR ACTIONS THAT NEED TO BE TAKEN.

COGNIZANT ENGINEER	DATE	TECHNICAL MGR./INSTR MRG./PI PREP REP	DATE	ENVIRONMENTAL REQUIREMENTS ENG.	DATE

☒ HARDWARE HAS SUCCESSFULLY COMPLETED THE ENVIRONMENTAL TESTS LISTED ON THIS FORM OR REMAINING ACTIONS HAVE BEEN TAKEN, INCLUDING RETEST.

COGNIZANT ENGINEER	DATE	TECHNICAL MGR./INSTR MRG./PI PREP REP	DATE	ENVIRONMENTAL REQUIREMENTS ENG.	DATE
[signature]	9/15/04	[signature]		[signature]	9/15/04

Attachment of HRCR Item #7: ETAS (environmental test summary)
For Module 8 & 9

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JPL

ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)

OTHER AUTHORIZATION PROVISIONS AND EXPLANATIONS

This is a 3-axis warm vibration test (room temp) done on the JFET flight modules SN008 and 009. The test will be done with the JFET unit mounted inside a mock-up JFET rack. The unit will be assessed both before and after the test with visual inspections and electrical checkouts. 3 response accelerometers will be mounted onto the JFET rack in order to give response data.

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Attachment of HRCR Item #7: ETAS (environmental test summary)
For Module 8 & 9

ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)
ENVIRONMENTAL TEST SUMMARY

HARDWARE	S/N	ETAS	TEST ENVIRONMENT LEVELS & DURATION	DATE TEST PERFORMED	TEST AGENCY	PASS/ FAIL	COMMENTS
SPIRE JFET (10209750-1)	008, 009	HSO28	**X, Y, and Z** 1 minute Random Vibe Frequency [Hz] / Spec [g^2.Hz] 20 / 0.01 100 / 0.05 300 / 0.05 499 / 0.0214 500 / 0.0214 2000 / 0.00214 Each axis1/4 g sine sweep 20-2000 Hz each axis				

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Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise
For Module 8 & 9

JFET SOURCE VOLTAGE MEASUREMENT

Post vibe, post bake, SN8,9 module, Perf Test (4K T) in green dewar.

Date			9/2/2004		9/2/2004		9/2/2004		9/2/2004	
T, plate			He		He		He		He	
T, JFET			He		He		He		He	
Vdd			3		3		3		3	
Vss			-1.5		-1.5		-1.5		-1.5	
Idd			1.3449		1.0852		1.379		1.062	
Iss			1.3426		1.0834		1.3769		1.0603	
SN			18		29		20		24	
Channel #				DELTA		DELTA		DELTA		DELTA
1	a		0.528	0	1.277	0.009	0.543	0.005	0.664	0
	b		0.528		1.268		0.538		0.664	
2	a		0.399	0.003	1.209	0.004	0.714	0.002	1.340	0.008
	b		0.402		1.205		0.712		1.348	
3	a		1.228	0.011	0.705	0.002	0.493	0.004	0.668	0
	b		1.217		0.707		0.497		0.668	
4	a		0.180	0.007	1.255	0.008	0.549	0.002	0.673	0.002
	b		0.173		1.247		0.547		0.671	
5	a		1.015	0.01	0.740	0.003	0.519	0.005	1.269	0.007
	b		1.005		0.737		0.524		1.276	
6	a		0.559	0.006	0.661	0.002	1.064	0.005	0.660	0.001
	b		0.565		0.659		1.059		0.661	
7	a		1.243	0.014	0.990	0.001	0.263	0.003	0.593	0
	b		1.257		0.991		0.260		0.593	
8	a		1.181	0.012	0.716	0.005	1.490	0.004	0.656	0.002
	b		1.193		0.711		1.486		0.658	
9	a		0.366	0.004	0.650	0.001	0.474	0.002	0.928	0.005
	b		0.362		0.649		0.472		0.933	
10	a		0.548	0.001	0.657	0.002	0.358	0.003	0.654	0.003
	b		0.549		0.655		0.361		0.651	
11	a		0.473	0.005	0.934	0.002	0.682	0.001	0.651	0.001
	b		0.468		0.932		0.681		0.652	
12	a		0.870	0.001	1.184	0.002	0.924	0.012	0.941	0.001
	b		0.869		1.182		0.912		0.940	
13	a		1.354	0.007	0.915	0.002	0.550	0.002	0.708	0.003
	b		1.347		0.913		0.548		0.711	
14	a		0.507	0.004	1.129	0.008	0.536	0.001	1.230	0.007
	b		0.511		1.137		0.535		1.223	
15	a		0.594	0.002	0.829	0.002	0.642	0.001	0.667	0.001
	b		0.596		0.827		0.641		0.668	
16	a		0.678	0.003	0.980	0.008	0.546	0.006	0.659	0.003
	b		0.675		0.988		0.552		0.662	
17	a		0.699	0.002	0.388	0.011	0.833	0.005	1.046	0.005
	b		0.697		0.399		0.828		1.051	
18	a		0.479	0.001	0.812	0.003	1.324	0.012	1.086	0.008
	b		0.480		0.815		1.336		1.094	
19	a		0.504	0.003	0.737	0.002	0.635	0.001	0.674	0.003
	b		0.507		0.739		0.634		0.671	
20	a		0.676	0.002	0.696	0.003	0.804	0.006	0.899	0.007
	b		0.678		0.699		0.810		0.892	
21	a		1.198	0.011	0.650	0.001	0.426	0	0.661	0
	b		1.187		0.649		0.426		0.661	
22	a		0.456	0.001	0.867	0.004	0.689	0.001	0.665	0.004
	b		0.455		0.871		0.688		0.669	
23	a		0.797	0.008	0.740	0.002	0.536	0.004	0.669	0.001
	b		0.789		0.742		0.540		0.670	
24	a		0.873	0.004	1.479	0.007	0.487	0.002	1.487	0.009
	b		0.869		1.472		0.489		1.478	

Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise

Board S/N 018 in Module S/N 008

	Pwr1	Pwr2	Pwr3	Pwr4	Pwr5	Pwr6
Vdd (V)	3	2.5	2.5	2.5	2.5	2.5
Vss (V)	-1.5	-1.5	-1.4	-1.3	-1	-1.6
Vdd' (V)	2.916	2.417	2.421	2.425	2.436	2.413
Vss' (V)	-1.416	-1.416	-1.321	-1.224	-0.935	-1.513
Idd (mA)	1.3804	1.3683	1.3061	1.2429	1.0509	1.431
Iss (mA)	1.3444	1.3338	1.2717	1.2088	1.0178	1.3962
I (mA)	1.3624	1.35105	1.2889	1.22585	1.03435	1.4136
P (mW)	5.9019168	5.17857465	4.8230638	4.47312665	3.48679385	5.5497936

Channel Num			Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz
Channel: 1	6.36	6.78	5.80	6.05	39.26	5.67
Channel: 2	8.90	6.22	6.06	5.65	41.56	6.68
Channel: 3	7.23	7.10	5.75	6.68	27.97	5.99
Channel: 4	11.55	6.97	8.30	8.19	34.96	7.09
Channel: 5	11.68	14.52	19.14	32.18	52.22	12.73
Channel: 6	7.79	14.50	26.64	39.68	60.29	7.10
Channel: 7	6.79	6.44	8.03	12.91	95.10	6.46
Channel: 8	5.64	5.76	7.43	6.76	27.53	5.28
Channel: 9	6.03	6.51	5.73	10.99	29.93	4.31
Channel: 10	6.30	5.77	5.49	5.96	13.86	6.33
Channel: 11	8.45	19.95	26.57	27.50	59.91	12.22
Channel: 12	5.82	8.87	10.99	15.01	37.72	6.05
Channel: 13	6.85	7.78	9.41	7.36	24.11	7.00
Channel: 14	7.68	11.50	12.53	8.03	34.62	10.49
Channel: 15	7.85	19.48	27.35	30.61	55.02	9.40
Channel: 16	6.47	6.55	7.06	5.90	7.61	6.41
Channel: 17	6.23	7.15	5.95	7.25	43.34	6.60
Channel: 18	7.19	7.07	6.46	6.68	46.28	5.90
Channel: 19	6.07	6.41	6.62	5.42	24.09	6.37
Channel: 20	7.21	7.51	7.78	7.97	31.24	7.21
Channel: 21	6.73	6.56	8.47	12.45	45.88	5.68
Channel: 22	6.80	5.35	5.66	6.13	21.45	5.07
Channel: 23	8.19	8.70	7.54	6.97	22.02	8.23
Channel: 24	6.96	7.30	13.47	26.72	43.21	7.36
Median	6.91	7.08	7.66	7.67	36.34	6.53
Overall Mean	7.37	8.78	10.59	12.88	38.30	7.15
Good Mean	7.37	7.79	7.73	7.63	10.74	7.15
MP Reqd					15	
Yield	**1.00**	**0.92**	**0.83**	**0.75**	**0.08**	**1.00**
# Good Ch.	24	22	20	18	2	24
# Bad Ch.	0	2	4	6	22	0

Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise

Board S/N 029 in Module S/N 008

	Pwr1	Pwr2	Pwr3	Pwr4	Pwr5	Pwr6
Vdd (V)	3	2.5	2.5	2.5	2.5	2.6
Vss (V)	-1.5	-1.8	-1.85	-1.5	-1.25	-1.8
Vdd' (V)	2.932	2.424	2.423	2.433	2.44	2.524
Vss' (V)	-1.432	-1.723	-1.772	-1.432	-1.189	-1.723
Idd (mA)	1.1283	1.2647	1.2891	1.1177	0.9938	1.2667
Iss (mA)	1.0847	1.2218	1.2462	1.0755	0.9522	1.2236
I (mA)	1.1065	1.24325	1.26765	1.0966	0.973	1.24515
P (mW)	4.828766	5.15575775	5.31779175	4.238359	3.531017	5.28815205

Channel Num			Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz
Channel: 1	6.58	7.49	8.12	7.52	12.81	8.96
Channel: 2	15.06	11.05	12.27	15.24	9.94	12.30
Channel: 3	8.88	8.35	7.32	8.58	10.58	7.42
Channel: 4	6.03	6.72	5.74	6.81	9.93	5.33
Channel: 5	11.54	10.79	9.15	13.53	9.57	10.11
Channel: 6	6.57	6.05	7.09	10.68	41.71	6.60
Channel: 7	6.22	5.23	5.91	6.59	8.05	6.46
Channel: 8	7.43	6.09	6.68	19.37	70.83	7.32
Channel: 9	13.95	10.49	9.63	45.22	105.71	10.28
Channel: 10	6.96	6.76	6.55	6.16	7.04	6.19
Channel: 11	5.85	7.92	5.38	7.54	8.39	6.14
Channel: 12	7.02	6.91	6.05	8.31	32.23	6.50
Channel: 13	28.12	17.81	12.66	64.56	60.75	14.55
Channel: 14	7.70	7.63	7.65	13.83	30.40	7.20
Channel: 15	8.43	7.07	6.56	19.26	40.25	6.77
Channel: 16	10.18	8.81	9.22	10.21	17.40	8.32
Channel: 17	7.64	7.24	9.76	6.84	8.09	6.88
Channel: 18	6.98	6.80	7.25	8.76	27.25	6.01
Channel: 19	6.45	7.38	6.44	6.91	16.27	7.79
Channel: 20	6.60	6.11	6.67	5.03	11.91	6.26
Channel: 21	6.86	6.52	6.94	6.87	7.06	6.72
Channel: 22	6.09	6.61	7.31	10.12	31.66	8.14
Channel: 23	7.05	7.85	6.84	6.46	11.28	6.21
Channel: 24	7.44	7.96	7.50	9.82	16.66	7.80
Median	7.04	7.31	7.17	8.67	14.54	7.04
Overall Mean	8.82	7.98	7.69	13.51	25.24	7.76
Good Mean	7.66	7.56	7.69	8.45	9.56	7.76
MP Reqd					15	
Yield	**0.92**	**0.96**	**1.00**	**0.79**	**0.50**	**1.00**
# Good Ch.	22	23	24	19	12	24
# Bad Ch.	2	1	0	5	12	0

Attachment of HRCR Item # 9: SPIRE MIUL Cover Page

MIUL = Material Identification & Utilization List

Materials and Processes List

SPIRE

JPL D-25725

REV B
1/05/04

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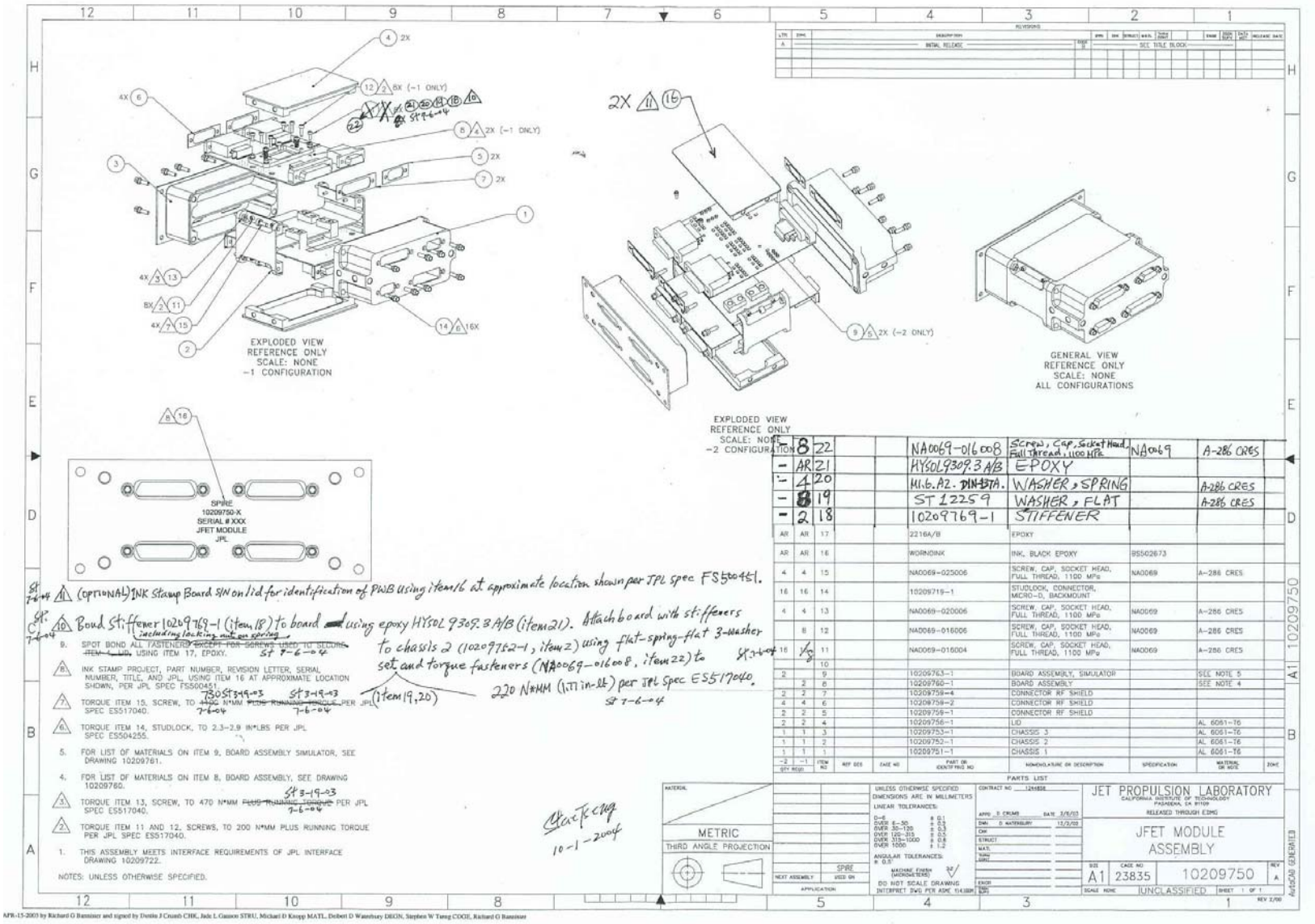
Reviewed by: _____
M. Knopp M&P Engineer

Attachment of HRCR Item # 11:

See End of This HRCR Package for "JFET Module Handling Document"

Attachment of HRCR Item # 14: JFET Module Top Assembly Drawing 10209750-1



Attachment of HRCR Item # 19:

Open PFR on Similar Hardware

PFR	Z82995
PFR	Z82997
PFR	Z82999
PFR	Z83353
PFR	Z83666
PFR	Z83673
PFR	Z84063
PFR	Z84064

Attachment of HRCR Item # 23: Qualification Compliance Test

Qualification Model JFET Module

EIDP Coverpage For JFET Testing

Unit Identfication		
Name	:	JFET QM Module
Part #	:	10209750-1
S/N	:	#001

Environmemtal Testing	Axes Tested	Temperature	Duration/# of Cycle	Requirement	Source	Waiver
Random Vibration Test	X, Y, Z	100 K	2 min/axis	X, Y, Z	SSSD, JFET-DES-07	
High Level Sine Vibe Test	None	NA	NA	X, Y, Z	SSSD, JFET-DES-07	HR-SP-JPL-RFW_005
Bakeout	NA	80 C	72 Hours	80C, 72 Hrs	D-20549	
Thermal Cycles	NA	RmT to 80 K	27	Minimum 15	D-20549	

Performance Characteristics		Specification		Source	Waiver
Power needed for <11 bad channels (Min Perf.)	9.1 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	RFW in process
Power needed for <4 bad channels (Design Value)	10.8 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	
Power needed for 100 % Yield per unit	13.5 mW	NA		NA	
Median Noise at < 11 bad chs.	7.13 nV/rtHz	<15 nV/rtHz Min Performance		SSSD, JFET-PER-01	
Median Noise at < 4 bad chs.	6.1 nV/rtHz		<7 nV/rtHz Design Value	SSSD, JFET-PER-01	
Median Noise at 100 % Yield.	6.97 nV/rtHz			SSSD, JFET-PER-01	
# of Channels over the max. offset voltage	0	< 15 mV for CQM < 15 mV for PFM/FS		SSSD, BDA-DRCU-27	
Common Mode Rejection Ratio	< -60 dB by design, as measured in EM4 unit			SSSD, BDA-DRCU-11	

Board Level Detail		Board SN 001		Source
# Channels Tested	:	24		
Median Noise at 3.5 mW	:	18 nV/rtHz		SSSD, JFET-PER-01
# of good channels at 3.5 mW	:	7	29% Yield	SSSD, JFET-PER-02
Power Needed for 100 % Yield	:	6.75 mW		SSSD, JFET-PER-02
Median Noise at High Power (w/ 100 % Yield)		6.97 nV/rtHz		SSSD, JFET-PER-01
Median Gain at High Power		0.98		NA

Definitions		
Good Channels	:	Noise less than a min. performance value of 15 nV/rtHz
Yield	:	# of Good Channels / 24
Filenames		
Noise Measurements	:	QualJFETPostVibeNoise_Summary.pdf

Notes	
1)	The Base temperature for all performance characterization was 4K
2)	All Noise Measurements were made with the inputs shorted to ground

Attachment of HRCR Item # 24 & #25: Mate/Demate & Operation Logs

Hardware ID: JFET module S/N 8, 9

Date	Time	AIDS	Power	Mate	Demate	Transport	Notes
8/19	9 A	243576				×	103 → 158
8/19	1 P	"					begin pump out (< 1E-5 torr)
8/20	6:30 P	"					temp stabilized @ 80°C
8/21	8:00 P M	"					begin 80°C → rm T
8/23	7 A	"				×	158 → 183
8/23			×				S.V. all boards (.5 hr each brd)
8/23							assemble into shake facility
8/25						×	183 → 144
8/25							shake 60 sec/axis, 3 axes
8/25						×	144 → 183
8/26							out of shake facility, install in grn dewar
8/26			×				S.V. warm post shake measurements
8/26							pump out
8/27			×				Noise, brd 18, 8 hrs
8/28			×				Noise, brd 29, 8 hrs
8/28			×				noise, brd 20, 1 hrs
8/30			×				noise, brd 20, 8 hrs
8/31			×				noise, brd 24, 8 hrs
9/1			×				gain, each brd 2 hrs
9/2			×				S.V., 4K, .5 hr each brd
9/13			×				S.V., rm T, .5 hr each brd
9/13			×				S.V., LN2, .5 hr each brd
9/15			×				S.V., rm T .5 hr each brd
9/15					×	×	out of dewar, over to 103,

Attachment of HRCR Items # 24 & # 25: Mate/Demate & Operation Logs (PWB S/N 018)

USE THE "NOTE" COLUMN TO DESCRIBE ACTIONS

DEVICE (BRD) S/N: 018 (32) PROJECT: SPIRE/ JFET BOARD

DATE	TIME	TECH	PWR ON	PWR OFF	MATE				DEMATE				TRANSFORT	NOTE
					JAA	JBB	JCC	JDD	JAA	JBB	JCC	JDD		
1/23/04		NAW			1	1	1	1	1	1	1	1		GND & CHASSIS TEST SAVER
2/18/04		NAW			1	1	1	1	1	1	1	1		GND & CHASSIS TEST
3/4/04		NAW			1	1	1	1			1	1		GND & CHASSI TEST
3/4/04		NAW	1	1			1	1	1	1				SOURCE TEST
5/19/04		NAW	1	1										ALL TEST
8-6-04		NAW			1	1	1	1			1	1		GND & CHASSI TEST
8-6-04		NAW	1	1			1	1			1	1		~~GND~~ SOURCE TEST NAW
8-6-04		NAW							1	1	1	1		SAVER DEMATE
8-9-04		NAW			1	1	1	1			1	1		GND & CHASSI
8-9-04		NAW	1	1			1	1	1	1				SOURCE TEST
8-10-04		BOB/NAW							1	1	1	1		DEMATE SAVER
8-12-04		NAW			1	1	1	1			1	1		GND & CHASSIS
8-12-04		NAW	1	1			1	1	1	1				SOURCE TEST
8-14-04		NAW			1	1	1	1			1	1		GND & CHASSIS
8-14-04		NAW	1	1			1	1	1	1				SOURCE TEST
8-14-04		NAW			1	1	1	1	1	1	1	1		GND & CHASSIS
8-14-04		NAW			1	1	1	1	1	1	1	1		GND & CHASSIS
8-18-04		NAW			1	1	1	1			1	1		GND & CHASSIS
8-18-04		NAW	1	1			1	1	1	1				SOURCE TEST
8-19-04		NAW			1	1	1	1			1	1		GND & CHASSIS
8-19-04		NAW	1	1			1	1	1	1				SOURCE TEST

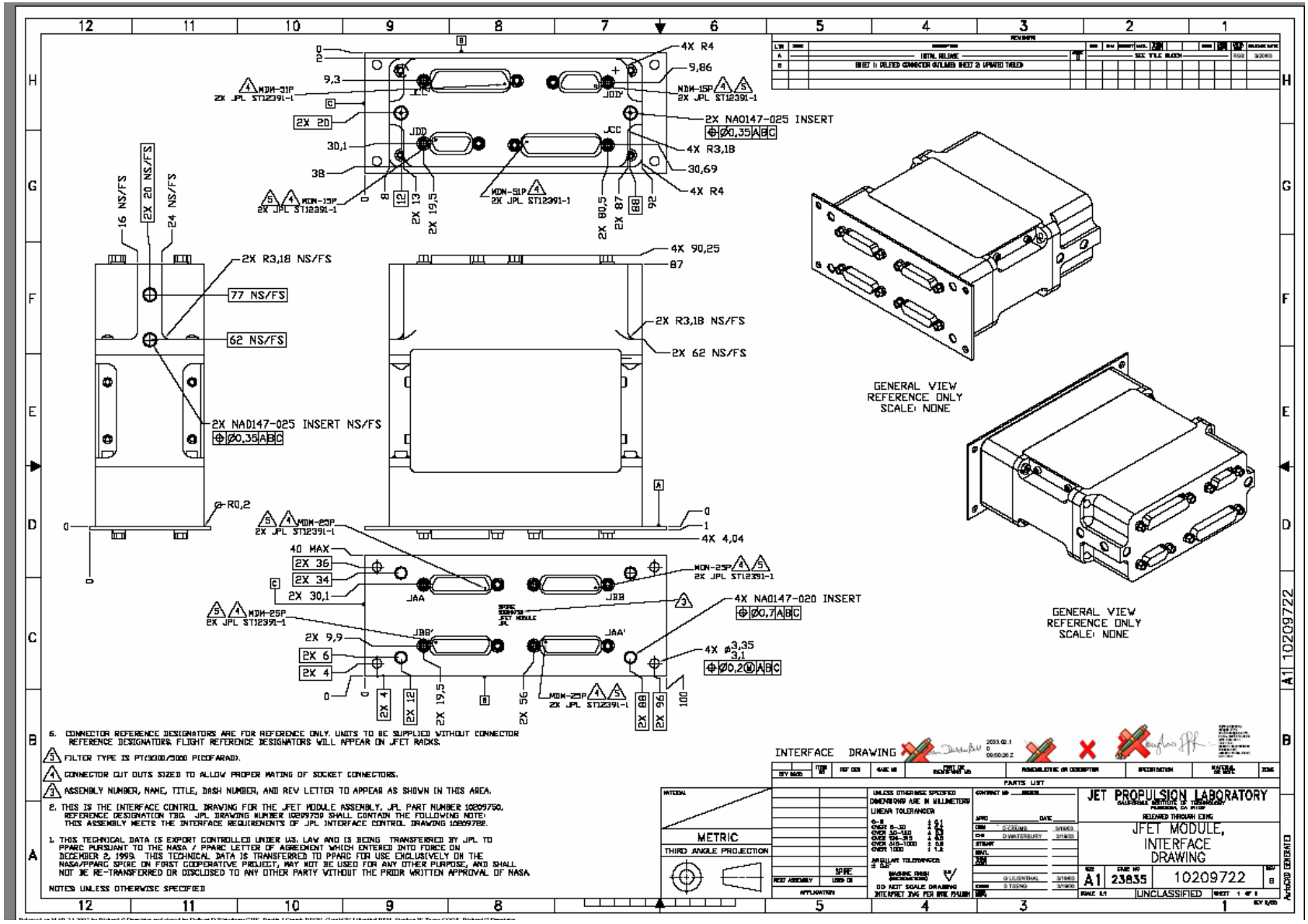
Attachment of HRCR Items # 24 & # 25: Mate/Demate & Operation Logs (PWB S/N 029)

USE THE "NOTE" COLUMN TO DESCRIBE ACTIONS

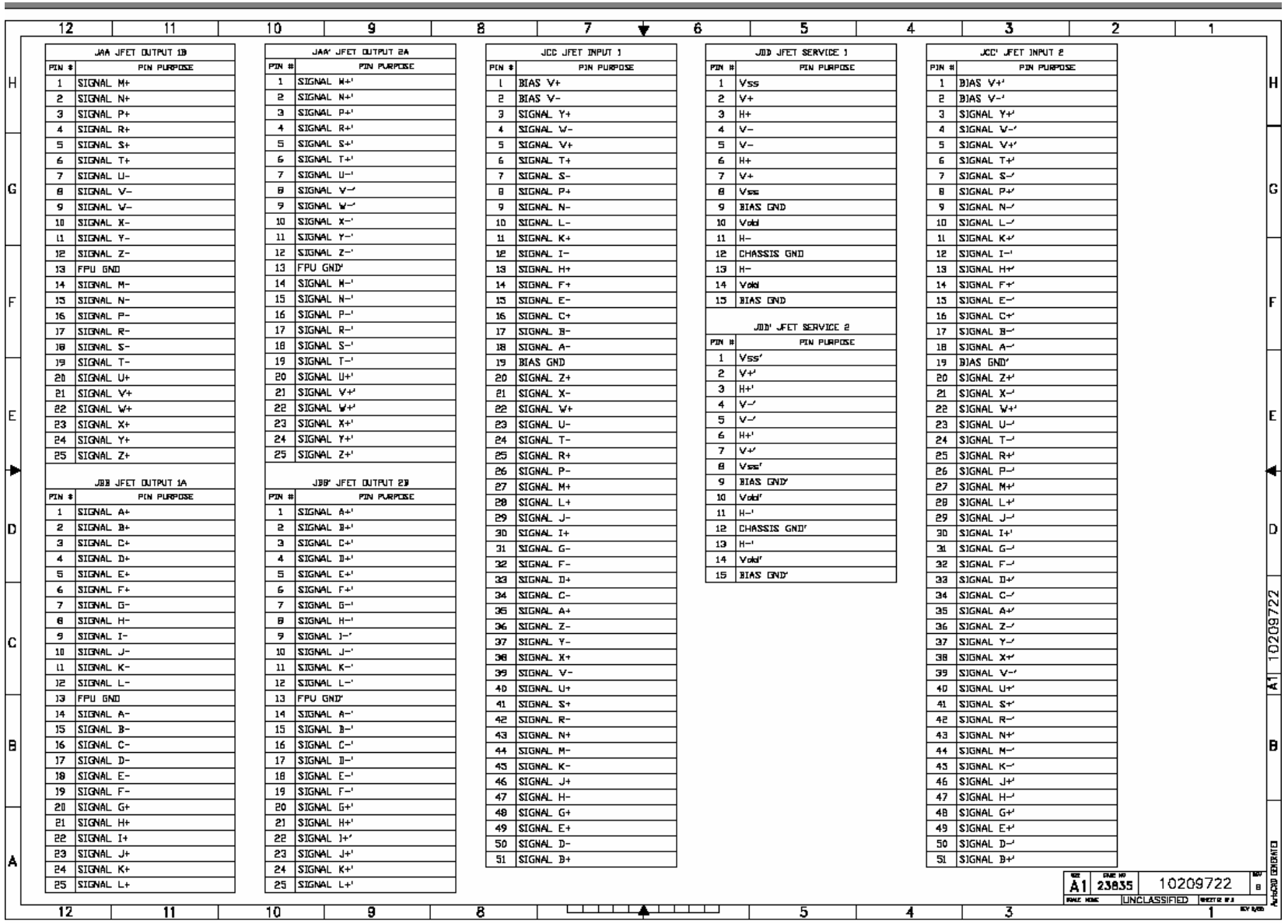
DEVICE/BRD S/N: 029 (44) PROJECT: SPIRE/ JFET BOARD

DATE	TIME	TECH	PWR ON	PWR OFF	MATE				DEMATE				TRANSFORT	NOTE
					JAA	JBB	JCC	JDD	JAA	JBB	JCC	JDD		
3/16/04	2:00 PM	NAN			✓	✓	✓	✓						GND & CHASSIS, SAVERS ON
4/8/04		NAN												GND & CHASSIS "
6/7/04		NAN												GND & CHASSIS "
6/7/04		NAN	✓	✓										SOURCE "
7/16/04		NAN												GND & CHASSIS "
7/16/04		NAN	✓	✓										SOURCE "
8/4/04		NAN												GND & CHASSIS "
8/4/04		NAN	✓	✓										SOURCE "
8/4/04		NAN							✓	✓	✓	✓		DEMATE SAVER
8/9/04		NAN			✓	✓	✓	✓			✓	✓		GND & CHASSIS.
8/9/04		NAN	✓	✓			✓	✓	✓	✓				SOURCE TEST
8/12/04		NAN			✓	✓	✓	✓			✓	✓		GND & CHASSIS
8/12/04		NAN	✓	✓			✓	✓	✓	✓				SOURCE TEST
8/13/04		NAN			✓	✓	✓	✓			✓	✓		GND & CHASSIS
8/13/04		NAN	✓	✓			✓	✓	✓	✓				SOURCE TEST
8/18/04		NAN			✓	✓	✓	✓			✓	✓		GND & CHASSIS
8/18/04		NAN	✓	✓			✓	✓	✓	✓				SOURCE TEST
8/19/04		NAN			✓	✓	✓	✓			✓	✓		GND & CHASSIS
8/19/04		NAN	✓	✓			✓	✓	✓	✓				SOURCE TEST

Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 1 of 2)



Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 2 of 2)



JAA JFET OUTPUT 1B

PIN #	PIN PURPOSE
1	SIGNAL M+
2	SIGNAL N+
3	SIGNAL P+
4	SIGNAL R+
5	SIGNAL S+
6	SIGNAL T+
7	SIGNAL U-
8	SIGNAL V-
9	SIGNAL W-
10	SIGNAL X-
11	SIGNAL Y-
12	SIGNAL Z-
13	FPU GND
14	SIGNAL M-
15	SIGNAL N-
16	SIGNAL P-
17	SIGNAL R-
18	SIGNAL S-
19	SIGNAL T-
20	SIGNAL U+
21	SIGNAL V+
22	SIGNAL W+
23	SIGNAL X+
24	SIGNAL Y+
25	SIGNAL Z+

JBB JFET OUTPUT 1A

PIN #	PIN PURPOSE
1	SIGNAL A+
2	SIGNAL B+
3	SIGNAL C+
4	SIGNAL D+
5	SIGNAL E+
6	SIGNAL F+
7	SIGNAL G-
8	SIGNAL H-
9	SIGNAL I-
10	SIGNAL J-
11	SIGNAL K-
12	SIGNAL L-
13	FPU GND
14	SIGNAL A-
15	SIGNAL B-
16	SIGNAL C-
17	SIGNAL D-
18	SIGNAL E-
19	SIGNAL F-
20	SIGNAL G+
21	SIGNAL H+
22	SIGNAL I+
23	SIGNAL J+
24	SIGNAL K+
25	SIGNAL L+

JAA' JFET OUTPUT 2A

PIN #	PIN PURPOSE
1	SIGNAL M+'
2	SIGNAL N+'
3	SIGNAL P+'
4	SIGNAL R+'
5	SIGNAL S+'
6	SIGNAL T+'
7	SIGNAL U-'
8	SIGNAL V-'
9	SIGNAL W-'
10	SIGNAL X-'
11	SIGNAL Y-'
12	SIGNAL Z-'
13	FPU GND'
14	SIGNAL M-'
15	SIGNAL N-'
16	SIGNAL P-'
17	SIGNAL R-'
18	SIGNAL S-'
19	SIGNAL T-'
20	SIGNAL U+'
21	SIGNAL V+'
22	SIGNAL W+'
23	SIGNAL X+'
24	SIGNAL Y+'
25	SIGNAL Z+'

JBB' JFET OUTPUT 2B

PIN #	PIN PURPOSE
1	SIGNAL A+'
2	SIGNAL B+'
3	SIGNAL C+'
4	SIGNAL D+'
5	SIGNAL E+'
6	SIGNAL F+'
7	SIGNAL G-'
8	SIGNAL H-'
9	SIGNAL I-'
10	SIGNAL J-'
11	SIGNAL K-'
12	SIGNAL L-'
13	FPU GND'
14	SIGNAL A-'
15	SIGNAL B-'
16	SIGNAL C-'
17	SIGNAL D-'
18	SIGNAL E-'
19	SIGNAL F-'
20	SIGNAL G+'
21	SIGNAL H+'
22	SIGNAL I+'
23	SIGNAL J+'
24	SIGNAL K+'
25	SIGNAL L+'

JCC JFET INPUT 1

PIN #	PIN PURPOSE
1	BIAS V+
2	BIAS V-
3	SIGNAL Y+
4	SIGNAL W-
5	SIGNAL V+
6	SIGNAL T+
7	SIGNAL S-
8	SIGNAL P+
9	SIGNAL N-
10	SIGNAL L-
11	SIGNAL K+
12	SIGNAL I-
13	SIGNAL H+
14	SIGNAL F+
15	SIGNAL E-
16	SIGNAL C+
17	SIGNAL B-
18	SIGNAL A-
19	BIAS GND
20	SIGNAL Z+
21	SIGNAL X-
22	SIGNAL W+
23	SIGNAL U-
24	SIGNAL T-
25	SIGNAL R+
26	SIGNAL P-
27	SIGNAL M+
28	SIGNAL L+
29	SIGNAL J-
30	SIGNAL I+
31	SIGNAL G-
32	SIGNAL F-
33	SIGNAL D+
34	SIGNAL C-
35	SIGNAL A+
36	SIGNAL Z-
37	SIGNAL Y-
38	SIGNAL X+
39	SIGNAL V-
40	SIGNAL U+
41	SIGNAL S+
42	SIGNAL R-
43	SIGNAL N+
44	SIGNAL M-
45	SIGNAL K-
46	SIGNAL J+
47	SIGNAL H-
48	SIGNAL G+
49	SIGNAL E+
50	SIGNAL D-
51	SIGNAL B+

JDD JFET SERVICE 1

PIN #	PIN PURPOSE
1	Vss
2	V+
3	H+
4	V-
5	V-
6	H+
7	V+
8	Vss
9	BIAS GND
10	Vdd
11	H-
12	CHASSIS GND
13	H-
14	Vdd
15	BIAS GND

JDD' JFET SERVICE 2

PIN #	PIN PURPOSE
1	Vss'
2	V+'
3	H+'
4	V-'
5	V-'
6	H+'
7	V+'
8	Vss'
9	BIAS GND'
10	Vdd'
11	H-'
12	CHASSIS GND'
13	H-'
14	Vdd'
15	BIAS GND'

JCC' JFET INPUT 2

PIN #	PIN PURPOSE
1	BIAS V+'
2	BIAS V-'
3	SIGNAL Y+'
4	SIGNAL W-'
5	SIGNAL V+'
6	SIGNAL T+'
7	SIGNAL S-'
8	SIGNAL P+'
9	SIGNAL N-'
10	SIGNAL L-'
11	SIGNAL K+'
12	SIGNAL I-'
13	SIGNAL H+'
14	SIGNAL F+'
15	SIGNAL E-'
16	SIGNAL C+'
17	SIGNAL B-'
18	SIGNAL A-'
19	BIAS GND'
20	SIGNAL Z+'
21	SIGNAL X-'
22	SIGNAL W+'
23	SIGNAL U-'
24	SIGNAL T-'
25	SIGNAL R+'
26	SIGNAL P-'
27	SIGNAL M+'
28	SIGNAL L+'
29	SIGNAL J-'
30	SIGNAL I+'
31	SIGNAL G-'
32	SIGNAL F-'
33	SIGNAL D+'
34	SIGNAL C-'
35	SIGNAL A+'
36	SIGNAL Z-'
37	SIGNAL Y-'
38	SIGNAL X+'
39	SIGNAL V-'
40	SIGNAL U+'
41	SIGNAL S+'
42	SIGNAL R-'
43	SIGNAL N+'
44	SIGNAL M-'
45	SIGNAL K-'
46	SIGNAL J+'
47	SIGNAL H-'
48	SIGNAL G+'
49	SIGNAL E+'
50	SIGNAL D-'
51	SIGNAL B+'

Attachment of HRCR Item # 11:

SPIRE

Handling Document

Field Effect Transistor (JFET) Module

10209750-1

Prepared by: Kalyani Sukhatme

10 September, 2003

Hardware Handling Guidelines

Contamination: Open shipment suitcase in a FED-STD-209 Class 10,000 clean room (ISO 14644-1 class 7) or better. Handle hardware with gloves.

ESD: Handle with grounding straps, ESD-safe gloves and ESD smocks at an ESD-safe workstation. Maintain shorting plugs on the unit whenever ESD is a concern. Refer to attached electrical handling document for other important safety precautions.

Fragile: Do not drop or otherwise shock the hardware including the shipping suitcase and container.

Humidity Sensitive: Place hardware in a humidity controlled Class 10,000 clean room. Maintain humidity level at 35%-50% RH typical, for ESD safety.

SPIRE JFET Electrical Handling Document

1. Introduction

This document provides guidelines for electrical handling for the SPIRE JFET Module.

1.1 Hardware Description

Each JFET module has two sets of 24 JFET channels. The JFET channels are populated on 1.0 micron thick Silicon Nitride membranes which provides thermal isolation. The operating temperature for these JFETs is ~120 K. The process of powering up the JFETs dissipates heat into the membrane resulting in a temperature increase with respect to the base temperature (4K to 10 K). Higher the power dissipation, higher is the temperature of the JFETs.

Each JFET channel consists of a matched pair of FETs (Figure 1.1-1) with a requirement for the offset voltage of less than **15 mV** between the matched pair. [The characteristic offset voltage is the difference between the source voltages (V_{sa} and V_{sb} with respect to ground) of the two FETs.]

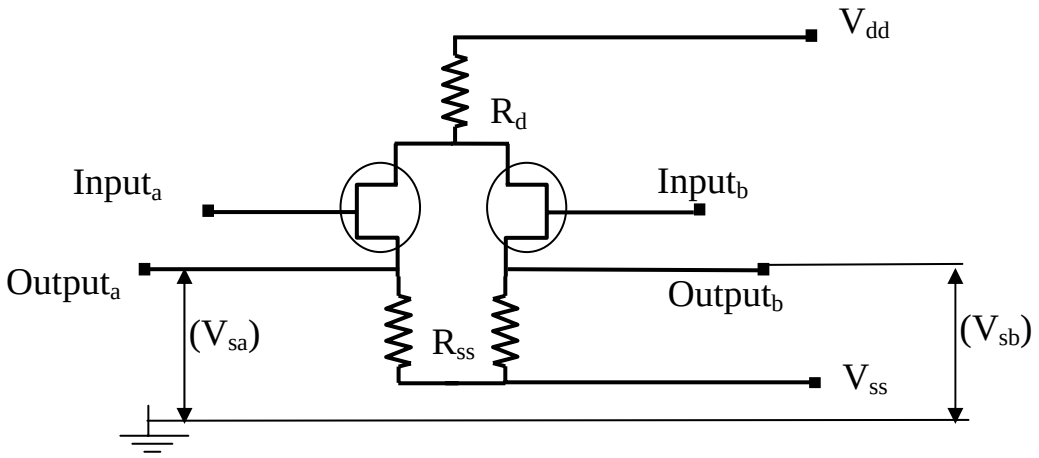


Figure 1.1-1

The Gates of the JFETs are the 'Inputs' of the circuit and the Sources (V_{sa} and V_{sb}) of the JFETs are the outputs, as marked in Figure 1.1-1. Vdd and Vss are the power lines for the circuit.

Handling

1. **The JFET Module is Contamination Sensitive**: Handle the unit with Gloves only in a FED-STD-209 Class 100000 clean room (ISO 14644-1 class 7) or better.

2. **The JFET Module is ESD Sensitive**: Please handle with appropriate ESD hardware handling procedures. Handle with grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.

3. **The JFET Module is Fragile**: Please do not drop or otherwise shock the unit. Please DO NOT remove the cover of the JFET Module.

Power ON Procedure

1. The JFET Module should be powered on **WITH the shorting plugs** (JPL Supplied Protection connectors) in place and with the **inputs shorted to ground.** Pins #9 and #15 on the 15-pin MDM connectors on the JFET Module are the bias grounds on the module. These pins should also be shorted to the power supply ground. The unit may be powered up without the shorting plug only when the inputs are connected to the detector system.

Under no circumstances the unit should be powered up without the inputs shorted to ground either via the shorting plug (JPL Supplied) or via the detector system.

2. Do not exceed a voltage of +5 V for the Vdd line and –5 V for the Vss line of the JFET Module.

3. When removing the shorting plugs from the unit for installation into the instrument, please use standard ESD precautions including grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.

Electrical Check-out Test: Characteristic Offset Voltage Measurement

1) Verify that the gates of the JFET channels (Inputs) are shorted together and grounded.
2) Apply the power supply ground to the bias ground pins on the unit (Pins 9 and 15 on the 15-pin MDM connectors)
3) Power on the JFET modules with Vdd = +3 V and Vss = -1.5 V
4) Verify that the handheld multimeter is in calibration.
5) Connect one side of the handheld multimeter to ground (Power supply ground).
6) And measure the voltage with respect to ground of each side (V_{sa} and V_{sb}) of each channel.
7) Calculate the characteristic offset voltage (V_{offset}) for each channel ($V_{offset}= V_{sa}-V_{sb}$)
8) Compare the values for each of the channels with the specific datasheet provided with the unit. The datasheets accompanying the unit also provides the values for the drain and source currents for a similar test performed at JPL.

REFER TO MEASURED SOURCE VOLTAGE DATA FOR ACTUAL HARDWARE. Here is an example of the source voltage values and the drain and the source currents obtained for such a test at room temperature are given in the Table 4-1

T, JFET	rm T	
Vdd	3 V	
Vss	-1.5 V	
Idd	1.564 mA	
Iss	1.5686 mA	
Channel #	(V)	DELTA (V)
1	1.130	0
	1.130	
2	1.075	0.001
	1.074	
3	0.781	0.001
	0.780	
4	1.088	0.005
	1.093	
5	0.834	0.001
	0.833	
6	1.012	0.003
	1.015	
7	0.785	0.002
	0.787	
8	1.148	0.004
	1.144	
9	0.753	0
	0.753	

10	0.693	0.008
	0.701	
11	1.110	0.004
	1.114	
12	0.758	0.001
	0.759	
13	0.832	0.002
	0.830	
14	1.264	0.001
	1.265	
15	1.206	0
	1.206	
16	0.818	0.001
	0.819	
17	0.526	0.005
	0.521	
18	1.423	0
	1.423	
19	0.773	0.002
	0.775	
20	0.873	0.004
	0.877	
21	1.387	0.006
	1.393	
22	1.417	0.003
	1.420	
23	0.887	0.002
	0.889	
24	0.888	0.003
	0.891	

- END OF -
Attachment of HRCR Item # 11:
JFET Module Handling Document

Attachment of HRCR Item # 19:

Open PFR on Similar Hardware

PFR	**Z82995**
PFR	**Z82997**
PFR	**Z82999**
PFR	**Z83353**
PFR	**Z83666**
PFR	**Z83673**
PFR	**Z84063**
PFR	**Z84064**

END OF

HRCR PACKAGE