



# SPIRE Technical Note

Ref: SPIRE-RAL-NOT-002709

Issue: 1.0

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Temperatures of spectrometer BDAs during PFM3

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## Reported temperatures of spectrometer BDAs for “Dark” loadcurve conditions.

Usual stuff for deriving the temperatures except now we have the advantage of having measured the spectrometer JFET gains warm (see appendix).

Table 1 gives the measurements made taken from the log description of “dark” loadcurves. Actually one of these was with the window open but I have included it anyway as the thermistors and dark bolometers did not significantly change temperature. The absolute accuracy of the results is somewhat dubious as we can see from the table and more from the plots in figures 1 (only truly dark measurements on blown up y-axis) and figure 2 (three dark measurements and the room background on larger y-axis scale). The scatter is too large from bolometer to bolometer to be explained by gain variation and there is a clear need to make some fundamental correction the JPL calibration values for these detectors.

**Table 1: Measurement data and reported temperatures.**

OBSID	File Prefix	Description of measurement	Date/Time	SubK Temp	SSW T1	SSW DK1	SLW T1	SLW DK1
0x3000E22C	ILT_PERF_DAB_S_SinglePhase_3000E22C_	Dark	10 May 2006 18:37	289.3	300	290.5	275	301
0x3000E232	ILT_PERF_DAB_S_SinglePhase_3000E232_	Dark; different bias phase	10 May 2006 19:25	289.6	299	290	266	298
0x3000E4D1	ILT_PERF_DAB_S_SinglePhase_3000E4D1_	Dark	6 June 2006 10:09	288.5	302	290	283	305
0x3000E559	ILT_PERF_DAB_S_SinglePhase_3000E559_	Room background	7 June 2006 20:23	288.5	302	291	282	308
0x3000E562	ILT_PERF_DAB_S_SinglePhase_3000E562_	Dark	8 June 2006 08:22	288.6	302.5	290.5	283	306



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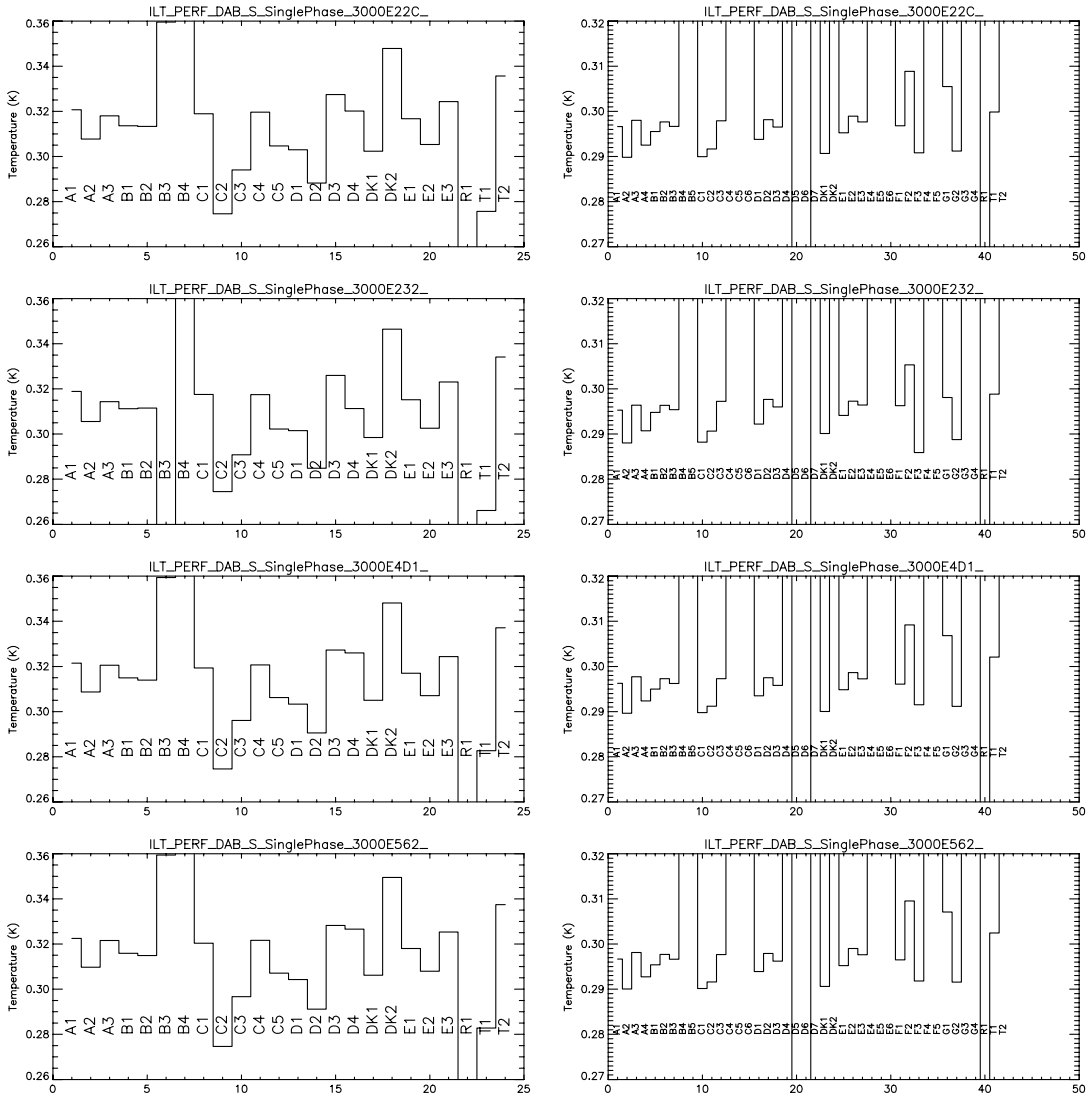


Figure 1: True dark temperatures per detector. Left column SLW; right SSW.



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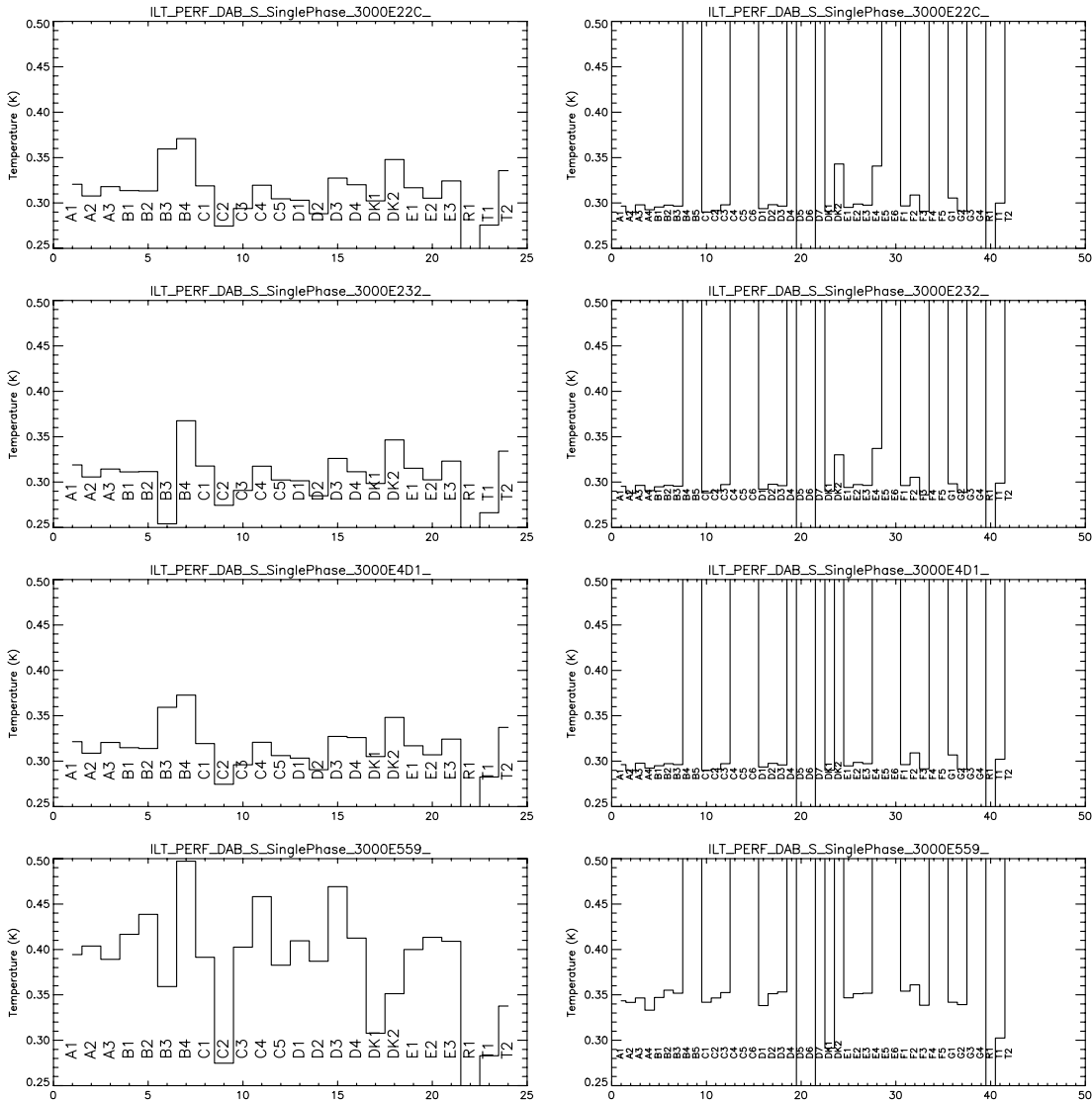


Figure 2: First three rows are dark as figure 1; last is room background.



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### Appendix: Spectrometer JFET Gain Calibration

A standard loadcurve was taken with the spectrometer JFETs attached to the QM2 electronics but with “safe” connectors attached that result in the bias being directly applied to the JFET inputs. Thus the bias is measured directly through the entire electronics chain allowing the gain of the system to be verified independently of any affects due to the presence of the bolometers or other resistance. The net gain, after rmove of known DRCU gains, are given in the following table. The VSS applied during the measurement was -1.49 V at the output of the DRCU – there is an approximate 0.2 V along the harness to the JFETs.

SLW ModuleSN022 Board SN055		SSW ModuleSN023 Board SN057		SSW ModuleSN023 Board SN054	
Channel Name	Measured JFET Gain	Channel Name	Measured JFET Gain	Channel Name	Measured JFET Gain
R1	0.972902	R1	0.966490	N /C	
T1	0.970925	A4	0.966567	N /C	
C1	0.972505	A3	0.965276	N /C	
DK1	0.965534	A2	0.966791	N /C	
B1	0.972177	A1	0.962773	N /C	
D1	0.971274	DK1	0.963910	N /C	
E1	0.972679	B3	0.964738	E5	0.966475
A1	0.970774	B2	0.966812	E4	0.965099
C2	0.00301509	B1	0.964809	D7	0.964490
D2	0.972847	C3	0.966335	D6	0.965323
B2	0.969908	C2	0.966602	D5	0.965093
E2	0.972830	C1	0.964377	D4	0.965260
A2	0.971082	D3	0.965462	C6	0.965458
C3	0.970206	D2	0.966996	C5	0.966806
D3	0.971067	D1	0.965709	C4	0.964972
B3	0.972613	E3	0.965862	B5	0.965687
E3	0.970979	E2	0.964826	B4	0.960917
C4	0.970189	E1	0.967200	T2	0.936779
DK2	0.970992	F3	0.965943	G3	0.966101
D4	0.970738	F2	0.966602	G4	0.963477
C5	0.972466	F1	0.965880	DK2	0.965119
B4	0.970875	G1	0.966546	F5	0.966096
A3	0.970286	T1	0.966471	F4	0.966267
T2	0.972189	G2	0.965001	E6	0.962968