SPIRE-RAL-MOM-002581

QM-2 DRCU Re-Acceptance Test Meeting – 10-Feb-2006

Thurs

Equipment set up in
All 3 subsystems tested with LTU & Test sequences – results for SCU to be e-mailed.
Tests OK

Control loops tested only at very basic level.

Need to test how DRCU reacts to unknown commands. Tested with a couple of commands – Commands are NOT rejected by DPU – identified as executed successfully! But flags raised by the DCU that commands are unknown. Hence still a problem with DPU as command should not have passed.

Test not yet done on SCU & MCU.

Friday

Attempted PCAL flash – 1st with original command list as used for earlier tests. Fault reoccurred.

New command list produced with different delay – but problem still present – although symptoms slightly different.

15 PCAL cycles set up – not all executed.

HK is polled in real time, can affect timing (jitter). If timing then problem could also affect PTC and mechanisms. 400 commands should take 800ms to execute.

Lines of Investigation

Repeat test with DRCU simulator to rule out DPU. If problem not present then points to DPU – DRCU I/F issue.

Stop the HK – to reduce demand on low speed I/F. Test could be done over weekend.

Put logic analyser/scope on to verify if commands are being sent across I/F. CEA could support this activity on Tues/Wednesday of next week.

Before end of day

Need to do HK timing test – test all subsystems SMEC, BSM, PCAL & ENG
Boot up MCU using nominal boot sequence.
Tests of mechanisms will depend on how representative FPU simulation is.

Issues

Data pack – none provided apart from test reports – only paper copy handed to Sunil – need electronic copy. New ICD needed – should be available Tuesday.
FM delivery
Due to modified planning (SMEC availability) we will use the QM2 for the next test campaign, consequently the PFM DRCU and WIH is needed end April.

Telecon to discuss PCAL commanding
15/2/06

Jean Louis, Christophe, Henri, Ken, Asier, Eric

Since Friday, repeat of PCAL flashes with 1 and 2 msec delays, with and without HK running.
No errors reported.
All set up the same as on Friday.
Tests to be carried out by IFSI, not complete yet.
Data rate has been supplied to IFSI so they can use simulator for test.
How about using a logic analyser to test commands on the line?
If we can repeat the anomaly there is nothing to analyse.
SCU current stays either high or low.
FPU simulator to record parameters such as PCAL current/voltage.
Power recycle of DRCU on Friday, no errors following that.
Normal power sequence is DPU then DRCU.
Try restarting with the standard power on sequence.
External source of interference?
MCU prime to redundant harness was changed on Friday, FPU to LTU.
Now changed back to prime.
DPU has not been restarted since Friday.

To store current HK on the LTU, run any script at a given frequency.
This generates a text file which can be studied.

Missing frames are blocks corresponding to a half cycle not individual frames.

Plan is:
Power down
Power up in the standard sequence as carried out on Friday.
Check for anomalies.
Measure resistance between DPU and DRCU ground planes.