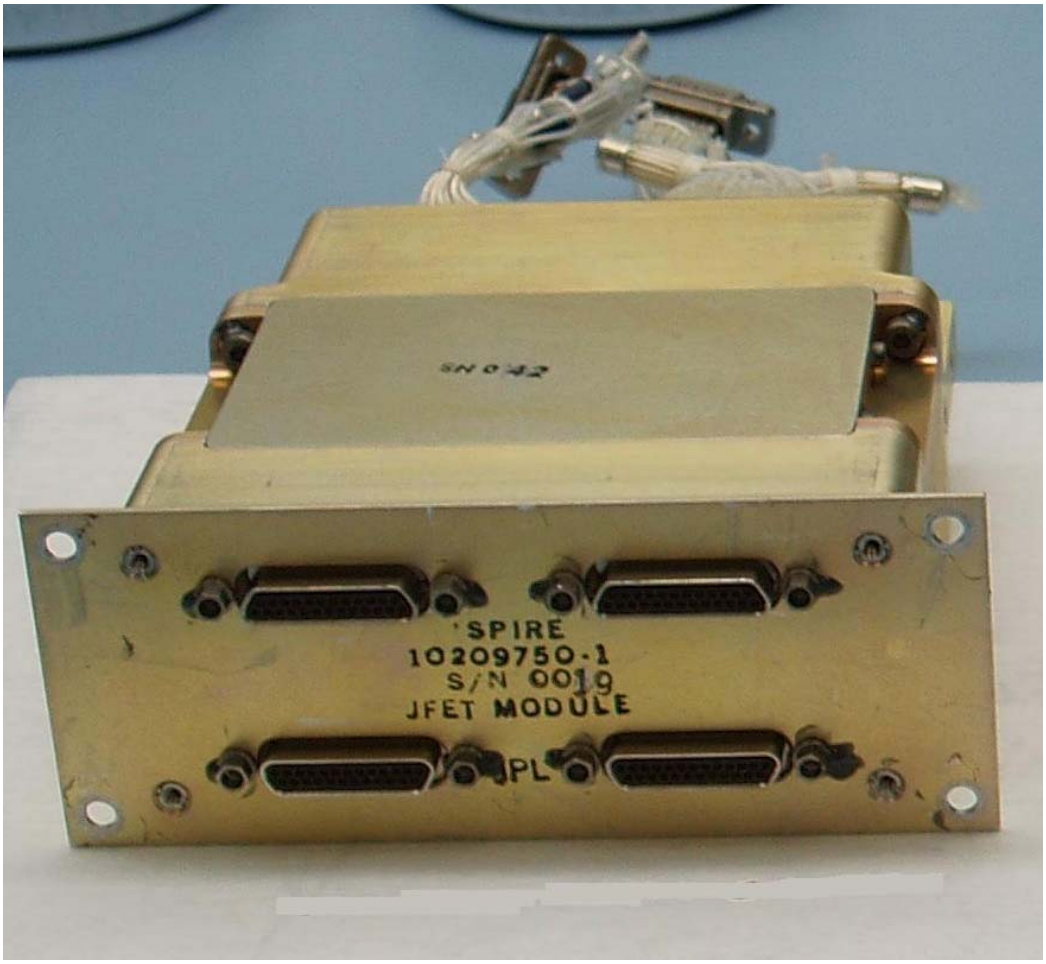
JPL Hardware Requirements Certification Review – SPIRE Element No. D-32241

Assembly / Subsystem		PEM		Phone		Section		Date
SPIRE		Martin Herman		(818) 354-8541		385		10 June, 2005
Drawing/ Part No.	**Dwg. Rev.**	**Nomenclature**		**Serial No.**	**Model**	**Type**	**Final IR No.**	**Mass (Meas. / Req.)**
10209750-1	B	JFET Module		019	FLT-Spare	N/A	926200	276 gm / 305 gm

Check applicable answer and provide explanation in remarks column	YES	NO	NA	Remarks	Data Attachments	Signature & Date
1. Are all drawings and specifications complete, approved, released and frozen?	X				14. Latest Top Assembly drawings ☒ Attached ☐ None	Cognizant Engineer Stew Tseng 6/10/05
2. Do the released drawings and specifications reflect all approved changes?	X				15. List of open ECRs ☐ Attached ☒ None	PEM R. Vaguney (for MH) 6/10/05
3. Is hardware identical to other hardware delivered? If no, provide difference list.	X				16. Waivers (RFW request for waiver) ☒ Attached ☐ None	QA Engineer Scott Hughes 6/20/05
4. Does the hardware meet its functional requirements, specifications, waivers, ICDs?	X			EIDP attached. Also see item # 8 attachments.	17. Open MRB ☐ Attached ☒ None	Environments/Reliability A-Lee
5. Are all IR and MRB dispositioned and concurred by QA?	X				18. Open PFR on this H/W ☐ Attached ☒ None	Mission Assurance Mgr. A-Lee
6. Is complete as-built list information included in the build book?	X				19. Open PFR on similar H/W ☐ Attached ☒ None	Project Office Margaret A. Levenson
7. Have all required environmental tests & analyses been completed?	X			ETAS attached	20. Handling Document → See Item 11 ☒ Attached ☐ None	PI James J. Bock 6/10/05
8. Is all required assembly and/or subsystem level functional testing complete?	X			Performance Test Data Attached. Also see EIDP in item # 4.	21. Shortage List ☐ Attached ☒ None	
9. Have all piece parts, processes and materials been approved by JPL?	X				22. Requirements Verification Matrix ☒ Attached (See #4, #7, #8) ☐ None	
10. Does this hardware meet all contamination control requirements?	X			Parts, processes and MIUL met all contamination control and out-gassing requirements.	23. Qualification Status ☒ Attached ☐ None	
11. Are all shipping containers, shipping and special handling procedures ready?	X			See Attached Document D-26790	24. Mate / Demate Record ☒ Attached ☐ None	
12. Is additional work required to bring this hardware to flight (flight-spare) readiness?		X			25. Operating Log ☒ Attached (See Item # 24) ☐ None	
13. Is this hardware acceptable for flight?	X				26. MICD ☒ Attached ☐ None	


SPIRE
10209750-1
S/N 0019
JFET MODULE
PL

RAL EIDP Table of Contents Versus JPL HRCR Check List Item Numbers

RAL EIDP Section Number	RAL EIDP Title	JPL HRCR Check List Item Number	Notes
1	Shipping Documents		Shipper and Final IR
2	Transportation, Packing, Handling & Integration Procedures	11	Special Handling Document D-26790
3	Certificate of Conformance / Delivery Review Board MOM		HRCR book is the C of C
4	As Built Configuration Status List	1 & 2	Assembly Drawings
5	List of Waivers	4	RFW (request for waiver) Attached
6	Copies of Waivers	4 & 7	RFW (request for waiver) Attached
7	List of Non-Conformance Reports		See RFW in 4 & 7
8	Copies of Non-Conformance Reports		See RFW in 4 & 7
9	Cleanliness Statement		Final IR QA Inspection
10	Operational Manual		NA
11	Top Level Drawings (inc. Family Tree)	14	Top Assembly Drawing
12	Interface Drawings	26	MICD Drawing
13	Functional, Block & Mechanical Drawings		NA
14	Electrical Circuit Drawings		NA
15	Serialized Components List		In build books – not shipped
16	Mass Properties/ Power Budget	HRCR Check List Page 1	Mass listed in HRCR check list
17	Qualification Status List / Test Matrix	23	Qualification Unit Test Matrix
18	Test Reports	4, 7, 8, 23	
19	Open Work / Deferred Work / Open Tests		NA
20	Calibration Data		NA
21	Historical Record	23	Qualification Unit Test Matrix
22	Manufacturing Logbook(s)		In build books – not shipped
23	Operating Time / Cycle Record	25	
24	Connector Mating Record	24	
25	Age Sensitive Items Record		NA
26	Pressure Vessels – History/Test Record		NA
27	Temporary Installation Record		NA
28	Reference List of EIDPs (Lower level)		NA
29	Other Useful Information		NA

JPL Hardware Requirements Certification Review (HRCR)

Junction Field Effect Transistor (JFET) Flight Module

10209750-1 S/N 019

SPIRE Element
Herschel Space Observatory Project

June 10, 2005

Configuration of Module, Boards & Membranes

Module 10209750-1	S/N 19	S/N 19
PWB 10209760-1	S/N 42	S/N 44
Membrane 10209758-1	J6.15.6	J6.11.1

Attachment of HRCR Items #1
Drawing Release Status

ALL ASSEMBLY & PARTS DRAWINGS ARE RELEASED IN PDMS

Released Drawings:

10209719-1 assembly built per released Rev. A drawing (studlock)

10209722-1 assembly built per released Rev. B drawing (interface drawing)

10209750-1 assembly built per released Rev. B drawing (module assy)

10209751-1 assembly built per released Rev. B drawing (chassis 1)

10209752-1 assembly built per released Rev. A drawing (chassis 2)

10209753-1 assembly built per released Rev. A drawing (chassis 3)

10209754-1 assembly built per released Rev. C drawing (mount)

10209756-1 assembly built per released Rev. B drawing (chassis lid)

10209757-1 assembly built per released Rev. A drawing (membrane)

10209758-1 assembly built per released Rev. A drawing (membrane assy)

10209759-1,-2,-4 redlined Rev. B drawing (gasket)

10209760-1 assembly built per released Rev. C drawing (board assembly)

10209761-1 assembly built per released Rev. C drawing (solder connector)

10209769-1 assembly built per released Rev. A drawing (stiffener)

10209777-1 assembly built per released Rev. B drawing (board)

10209858-2 assembly built per released Rev. A drawing (special fastener)

10217636-1 assembly built per released Rev. A drawing (clip)

Attachment of HRCR Item #4: EIDP (End Item Data Package)

EIDP Coverpage For JFET Testing

Unit Identfication		
Name	:	JFET PFM Module
Part #	:	10209750-1
S/N	:	#019

Environmemtal Testing	Axes Tested	Temp	Duration/# of Cycle	Requirement	Source	Waiver
Random Vibration Test	X, Y, Z	Rm T	1 min/axis	X, Y, Z	SSSD, JFET-DES-07	
High Level Sine Vibe Test	None	NA	NA	X, Y, Z	SSSD, JFET-DES-07	HR-SP-JPL-RFW-005
Bakeout	NA	80 C	25.75 hrs	> 24 HRS		
Thermal Cycles	NA	RmT to 80 K	3	Minimum 1	D-20549	

Performance Characteristics		Specification		Source	Waiver
Power needed for <11 bad channels (Min Perf.)	7.20 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	HR-SP-JPL-RFW-004
Power needed for <4 bad channels (Design Value)	7.67 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	
Power needed for 100 % Yield per unit	8.65 mW	NA		NA	
Median Noise at < 11 bad chs.	8.47 nV/rtHz	<15 nV/rtHz Min Performance	<7 nV/rtHz Design Value	SSSD, JFET-PER-01	
Median Noise at < 4 bad chs.	7.25 nV/rtHz			SSSD, JFET-PER-01	
Median Noise at 100 % Yield.	6.76 nV/rtHz			SSSD, JFET-PER-01	
# of Channels over the max. offset voltage	0	< 15 mV		SSSD, BDA-DRCU-27	
Common Mode Rejection Ratic	< -60 dB by design, as measured in EM4 unit			SSSD, BDA-DRCU-11	

Board Level Details		Board SN 042 (JAA-JDD)		Board SN 044 (JAA'-JDD')		Source
# Channels Tested	:	24		24		
Median Noise at 3.5 mW	:	7.97 nV/rtHz		8.71 nV/rtHz		SSSD, JFET-PER-01
# of good channels at 3.5 mW	:	18	75% Yield	18	75% Yield	SSSD, JFET-PER-02
Power Needed for 100 % Yield	:	4.22 mW		4.43 mW		SSSD, JFET-PER-02
Median Noise at High Power (w/ 100 % Yield)		6.64 nV/rtHz		6.85 nV/rtHz		SSSD, JFET-PER-01
Median Gain at High Power		0.98		0.98		NA
Heater Resistance, 4K Reference value	:	2.74 kΩ		2.45 kΩ		NA

Definitions		
Good Channels	:	Noise less than a min. performance value of 15 nV/rtHz
Yield	:	# of Good Channels / 24
Filenames		
Noise Measurements	:	JFET_Mod19_brd42,44_Noise.pdf
Source Voltages (RmT, 4K)	:	JFET Module 18,19 voltage data, 25,48,42,44 04185.pdf

Notes

1) The Base temperature for all performance characterization was 4K

2) All Noise Measurements were made with the inputs shorted to ground

3) Type of membranes: SN042: 48% Overetched; SN044: 39% Overetched

Attachment of HRCR Item # 4: RFW (Request For Waiver)

		RFW/RFD Number:	HR-SP-JPL-RFW-21
Spacecraft / Project	Herschel	**Originator's Name**	Steve Tseng
System / Experiment / Model	**1.1 SPIRE**	**Signature / Date**	
Sub-System	detectors	**Request Type** (Highlight applicable request)	Waiver (RFW) / Deviation (RFD)
Assembly	JFET modules	1.1.1.1 Organisation	Jet Propulsion Laboratory
Sub-Assembly		**Ref. Doc. / Drwg No.**	SPIRE-JPL-PRJ-000456
Item		**References**	
Serial No.			
RFW/RFD Title	**JFET Power Dissipation s/n 019**		

End Items(s) Affected (Hardware, Software)		
Name	**CI-Number**	**Model(s)**
JFET Module p/n 10209750 s/n 019		PFM

Requirement / Interface Documents Affected				
Specification/Drawing Title	**Number**	**Issue**	**Date**	**App. Paragraph**
BDA-SSSD	SPIRE-JPL-PRJ-0004456	3.2	7/1/03	JFET-PER-01 JFET-PER-02 JFET-TEC-05

Description of Deviation / Discrepancy / Non-Conformance

Requirement states that dissipation of photometer JFETs is to be less than 7 mW average, while supplying 90% of channels with voltage noise < 15 nV/rtHz according to BDA-SSSD JFET-PER-01, JFET-PER-02, JFET-TEC-05. Measured JFET performance of the JFETs indicates that 7.20 mW of power dissipation will be required to meet the specified yield and noise performance specifications.

Other Items or Requirements (Potentially) Affected

Overall sensitivity of the bolometer sub-system is affected by JFET noise performance. JFET power dissipation impacts the heat sink temperature of the 3He refrigerator and may in turn increase the base detector temperature. Dissipation of JFETs affects power dissipation on cryostat.

Need for RFW/RFD and Rationale for Acceptance

Measured JFET performance of JFETs indicates that 7.20 mW of power dissipation will be required to meet the specified yield and noise performance specifications. JPL is unable to significantly alter the JFET fabrication process in order to meet the power specification without undue risk to the stated PFM/FS delivery dates. Furthermore, JPL requests a full system optimisation to revisit the noise and power requirements on the JFETs. The JFET modules can meet the noise design value with 100 % yield at 8.65 mW.

	Approved	Rejected	Name	Date
Engineering:				
Product Assurance:				
CCB-Chairman:				
Principal Investigator				
Product Assurance:				
Co-Investigator				
Prime Contractor				
ESA Project Office				

Attachment of HRCR Item #7: RFW (Request For Waiver)

CCLRC Rutherford Appleton Laboratory	REQUEST FOR WAIVER / DEVIATION (RFW/RFD)	PRODUCT ASSURANCE Space Science and Technology Department

RFW/RFD Number:	HR-SP-JPL-RFW-005v1

Spacecraft / Project	Herschel	**Originator's Name**	Kalyani Sukhatme	
System / Experiment / Model	SPIRE	**Signature / Date**		
Sub-System	detectors	**Request Type** (Highlight applicable request)	Waiver (RFW)	Deviation (RFD)
Assembly		**Organisation**	Jet Propulsion Laboratory	
Sub-Assembly		**Ref. Doc. / Drwg No.**	SPIRE-JPL-PRJ-000456	
Item		**References**		
Serial No.				

RFW/RFD Title	BDA and JFET module sine test deletion

End Items(s) Affected (Hardware, Software)		
Name	**CI-Number**	**Model(s)**
Bolometric Detector Assemblies JFET Modules		CQM, PFM, FS CQM, PFM, FS

Requirement / Interface Documents Affected				
Specification/Drawing Title	**Number**	**Issue**	**Date**	**App. Paragraph**
BDA-SSSD (SPIRE-JPL-PRJ-000456)		3.2	Jan 7, 2003	BDA-DES-10, JFET-DES-07

Description of Deviation / Discrepancy / Non-Conformance

High Level Sine- Vibe Test is not performed on these units

Other Items or Requirements (Potentially) Affected

Need for RFW/RFD and Rationale for Acceptance

The hardware has to be qualified under a cold vibration test and is installed in the cold vibration facility for the purpose of the test. The high level sine vibration test configuration will put the hardware and the personnel at risk since the cold vibration facility is not structurally capable of withstanding the high levels. Obtaining additional resources (cost and schedule) for developing a new set-up is not feasible at this time.

Up issue RFW to 5v1 with this note added

There is no Requirement to do a high level sine test on previously Qualified units, Only Random Acceptance level test are required.

	Approved	Rejected	Name	Date
Engineering:	REF SPIRE – RAL-MOM-002250		Digitally signed by Eric Clark Date: 2004.12.22 08:57:49 Z	20 December 04
Product Assurance:				20 December 04
CCB-Chairman:				
Principle Investigator				
Product Assurance:				
Co-Investigator				
Prime Contractor				
ESA Project Office				

Attachment of HRCR Item #7: ETAS (Environmental Test Summary)

ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)

AUTHORIZATION SECTION

PROJECT: Herschel		LOG NO.: HS041	
SUBSYSTEM/ASSEMBLY TITLE: JFET Modules S/N 18,19			DATE ISSUED: 4/13/05
ENCE DESIGNATION NUMBER	PART NO. (IF MULTIPLE, ATTACH LIST): 10209750-1	REV.	SERIAL NO.: 018,019

HARDWARE TYPE: ☐ EM QUAL ☒ FLIGHT ☐ FLIGHT SPARE ☐ OTHER — PRE-ENVIRONMENTAL INSPECTION REPORT NUMBER (ATTACH IR)

WIRING HARNESS: ☐ EM QUAL ☐ FLIGHT ☐ EM ☐ SE — PART NO. — REV. — SERIAL NO.

TEST DESCRIPTION (CHECK ALL APPLICABLE): ☐ SINE VIBRATION ☒ RANDOM VIBRATION ☐ PYROSHOCK ☒ THERMAL VAC. ☐ ACOUSTIC ☐ EMC ☐ THERMAL ATMOSPHERE ☐ OTHER _____

TYPE OF TEST: ☐ QUALIFICATION ☒ PROTO FLIGHT ☐ FLIGHT ACCEPTANCE ☐ RETEST

WILL ALL TESTS/LEVES/DURATIONS REQUIRED BY THE PROJECT DOCUMENTS BE PERFORMED ON THIS UNIT? ☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) ENTER PROJ. DOC. NO. AND REV. ____

HAS THE UNIT PASSED ALL PRE-ENVIRONMENTAL FUNCTIONAL TESTS? ☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION

HAVE ALL DESIGN ANALYSES BEEN COMPLETED AND REQUIRED CHANGES BEEN IMPLEMENTED? ☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION

IS THE TEST ARTICLE IDENTICAL TO OTHER FLIGHT UNITS? ☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION

ARE ALL PFRs AGAINST THIS UNIT CLOSED? ☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION

HAVE ALL WAIVERS AND ECRs BEEN APPROVED AND ARE THEY INCORPORATED? ☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION

TEST AUTHORIZED BY

COGNIZANT ENGINEER	DATE	TECHNICAL MGR./INSTR MRG./PI PREP REP	DATE	ENVIRONMENTAL REQUIREMENTS ENG.	DATE
[signature]	4/13/05	[signature]	4/13/05	[signature]	4/13/05

SUMMARY SECTION

TEST AGENCY (IF MULTIPLE, ATTACH SUMMARY AND TEST DATES): JPL Building 144	TEST INITIATION DATE: 04/22/05	ACCUMULATED OPERATING HOURS PRIOR TO FIRST ENVIRONMENTAL TEST
SERIAL NUMBERS ACTUALLY TESTED	TEST TERMINATION DATE	OPERATING HOURS DURING ENVIRONMENTAL EXPOSURE

TEST DESCRIPTION

VIBRATION	ACOUSTIC	PYROSHOCK SHOCK	☒ THERMAL VACUUM	☐ TEMPERATURE ATMOSPHERE	☐ OTHER
AXES: X Y Z		AXES: X Y Z	PRESSURE: <10E-5 <77K		
SINE VIBRATION ☐☐☐	☐		NO OF CYCLES: 2<= # <=3	NO OF CYCLES:	____
RANDOM VIBRATION ☒☒☒		SHOCKS/AXIS:			

☐ EMC	☐ COND. SUSC.	☐ COND. EMIS.	☐ ISOLATION	TEMP. LEVEL (°c) AND ACCUMULATED DURATION (HRS.)
☐ ESD	☐ RAD. SUSC.	☐ RAD. EMIS.	☐ MAGNETICS	HOT: ____°c, ____h COLD: ____°c, ____h
				HOT: ____°c, ____h COLD: ____°c, ____h

WERE THERE ANY PFRs GENERATED DURING ENVIRONMENTAL TESTS? ☐ YES ☑ NO (IF NO, ATTACH EXCEPTIONS LIST)	LIST PFR NOS. / BRIEF EXPLANATION
ARE THE POST ENVIRONMENTAL DAMAGE INSPECTIONS COMPLETE? ☑ YES ☐ NO (IF YES, ATTACH A COPY OF THE INSPECTION REPORTS. IF NO, ATTACH EXPLANATION)	LIST PFR NOS. / BRIEF EXPLANATION
WERE ALL PLANNED TESTS/LEVELS/DURATIONS ACHIEVED? ☑ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST)	LIST PFR NOS. / BRIEF EXPLANATION

☐ TESTS HAVE NOT BEEN SUCCESSFULLY COMPLETED. SEE THE ATTACHED SUMMARY FOR ACTIONS THAT NEED TO BE TAKEN.

COGNIZANT ENGINEER	DATE	TECHNICAL MGR./INSTR MRG./PI PREP REP	DATE	ENVIRONMENTAL REQUIREMENTS ENG.	DATE
[signature]	6/2/05	[signature]	6/3/05		

☐ HARDWARE HAS SUCCESSFULLY COMPLETED THE ENVIRONMENTAL TESTS LISTED ON THIS FORM OR REMAINING ACTIONS HAVE BEEN TAKEN, INCLUDING RETEST.

COGNIZANT ENGINEER	DATE	TECHNICAL MGR./INSTR MRG./PI PREP REP	DATE	ENVIRONMENTAL REQUIREMENTS ENG.	DATE
[signature]	6/3/05	[signature]	6/7/05	[signature]	6-3-05

PAGE 1 JPL 2053 R 1/96 FF

Attachment of HRCR Item #7: ETAS (Environmental Test Summary)

ENVIRONMENTAL TE AUTHORIZATION AND SUMMARY (ETAS)
ENVIRONMENTAL TEST SUMMARY

HARDWARE	S/N	ETAS	TEST ENVIRONMENT LEVELS & DURATION	DATE TEST PERFORMED	TEST AGENCY	PASS/ FAIL	COMMENTS
SPIRE JFET (10209750-1)	018,019	HSO41	**X, Y, and Z** 1 minute Random Vibe Frequency [Hz] / Spec [g^2/Hz] 20 / 0.01 100 / 0.05 300 / 0.05 499 / 0.0214 500 / 0.0214 2000 / 0.00214 Each axis1/4 g sine sweep 20-2000 Hz each axis 2-3 vaccuum thermal cycles. <10E-5 mbar, <70K				

PAGE 3 JPL 2583 R 1/98 FF

Attachment of HRCR Item #7: ETAS (Environmental Test Summary)

JPL

ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)

OTHER AUTHORIZATION PROVISIONS AND EXPLANATIONS

T[illegible] is a 3-axis warm vibration test (room temp) done on the JFET flight modules SN0[illegible]6 and 0[illegible]7. The test will be [illegible] with the JFET unit mounted inside a mock-up JFET rack. The unit will be assessed both before and after the test with visual inspections and electrical checkouts. 3 response accelerometers will be mounted onto the JFET rack in order to give response data.

2 to 3 vacuum thermal cycles will also be completed.

3 thermal cycles were completed (rm T to 4K)

PAGE 2 JPL 2683 R 1/98 FF

Attachment of HRCR Item # 8: Test Data - Source Voltage Data

JFET SOURCE VOLTAGE MEASUREMENT

PERF TEST Post Vibe, post bake, SN18,19 module, grn dewar, Helium.

			power cable		pwr1 1,2 A		pwr2 3,4A		pwr3 1,2B	pwr4	pwr3 3,4B	
			Date		5/5/2005		5/5/2005		5/5/2005		5/5/2005	
			T. plate		4K		4K		4K		4K	
					4K		4K		4K		4K	
			Vdd		3		3		3		3	
			Vss		-1.5		1.5		-1.5		-1.5	
			Vdd'		2.656		2.697		2.725		2.665	
			Vss'		-1.153		-1.194		-1.222		-1.163	
			Idd		1.3232		1.1657		1.0586		1.2872	
			Iss		1.3219		1.1644		1.0574		1.286	
			SN		25		48		42		44	
Board channel correla		Channel #				DELTA		DELTA		DELTA		DELTA
15		1	a		1.017	0	0.855	0.001	0.680	0.001	0.705	0
			b		1.017		0.854		0.681		0.705	
14		2	a		1.445	0.01	0.711	0.001	0.688	0	0.701	0.001
			b		1.435		0.710		0.688		0.700	
13		3	a		0.707	0.004	0.695	0.001	0.701	0	0.993	0.002
			b		0.711		0.694		0.701		0.995	
12		4	a		1.264	0.006	0.783	0.004	0.716	0.004	0.949	0
			b		1.270		0.787		0.720		0.949	
10		5	a		0.702	0.001	0.823	0.001	1.481	0.009	0.416	0.01
			b		0.703		0.824		1.472		0.406	
9		6	a		0.705	0.001	1.024	0.006	0.696	0.002	0.738	0.005
			b		0.704		1.030		0.694		0.733	
8		7	a		1.537	0.013	1.076	0.005	0.813	0.005	0.554	0.002
			b		1.550		1.081		0.808		0.556	
7		8	a		1.206	0.011	0.751	0.001	0.747	0.007	0.711	0.003
			b		1.217		0.752		0.740		0.714	
6		9	a		1.332	0.013	0.441	0.006	0.676	0.001	0.687	0.001
			b		1.345		0.447		0.677		0.686	
5		10	a		0.669	0.001	0.310	0.003	0.695	0.002	0.840	0.002
			b		0.668		0.313		0.697		0.842	
4		11	a		1.217	0.008	0.516	0.001	0.800	0.003	0.731	0.001
			b		1.209		0.517		0.797		0.732	
3		12	a		0.701	0	0.605	0.01	0.644	0.001	1.079	0.014
			b		0.701		0.615		0.645		1.093	
28		13			1.478	0.008	0.834	0.001	0.783	0.005	1.200	0.008
			b		1.470		0.833		0.778		1.208	
27		14	a		0.682	0.005	0.824	0.002	0.773	0.002	0.751	0.002
			b		0.677		0.822		0.775		0.753	
26		15	a		0.701	0.011	0.756	0.005	0.588	0.006	0.701	0.001
			b		0.712		0.751		0.594		0.700	
25		16	a		0.647	0.005	0.727	0.001	0.735	0.007	0.985	0.006
			b		0.642		0.728		0.742		0.991	
24		17	a		0.662	0.001	0.712	0.001	0.231	0.01	0.989	0
			b		0.661		0.713		0.241		0.989	
23		18	a		0.722	0.001	0.705	0	1.135	0.009	0.706	0.001
			b		0.721		0.705		1.144		0.705	
22		19	a		0.685	0.001	0.715	0.004	0.681	0.002	0.742	0.001
			b		0.684		0.719		0.683		0.743	
21		20	a		0.699	0.001	0.853	0.001	0.697	0.001	1.222	0.006
			b		0.700		0.854		0.698		1.228	
19		21	a		0.985	0.002	0.609	0.001	0.675	0.003	0.719	0.004
			b		0.983		0.608		0.672		0.723	
18		22	a		1.140	0.011	0.737	0.001	0.705	0	0.928	0.004
			b		1.151		0.736		0.705		0.932	
17		23	a		0.955	0.009	0.830	0.004	0.784	0.005	1.292	0.006
			b		0.964		0.826		0.789		1.298	
16		24	a		1.350	0.011	0.783	0.003	0.688	0.003	0.969	0.001
			b		1.339		0.786		0.685		0.968	

JFET SOURCE VOLTAGE MEASUREMENT

power cable			pwr 3 1,2 B		pwr4 3,4B		pwr1 1,2A		pwr2 3,4A	
Date			5/19/2005		5/19/2005		5/19/2005		5/19/2005	
T, plate			Rm T		Rm T		Rm T		Rm T	
			Rm T		Rm T		Rm T		Rm T	
Vdd			3		3		3		3	
Vss			-1.5		-1.5		-1.5		-1.5	
Vdd'			2.625		2.689		2.705		2.642	
Vss'			-1.122		-1.166		-1.202		-1.139	
Idd			1.4164		1.254		1.1174		1.3541	
Iss			1.4151		1.2527		1.116		1.3528	
SN			25		48		42		44	
Channel #				DELTA		DELTA		DELTA		DELTA
1	a		1.260	0.002	1.111	0.001	0.960	0	0.962	0.001
	b		1.262		1.112		0.960		0.961	
2	a		1.670	0.011	0.973	0	0.968	0.001	0.955	0.001
	b		1.659		0.973		0.967		0.956	
3	a		0.959	0.004	0.957	0.001	0.980	0	1.237	0.004
	b		0.963		0.956		0.980		1.241	
4	a		1.495	0.007	1.052	0.003	0.995	0.002	1.194	0
	b		1.502		1.055		0.997		1.194	
5	a		0.980	0.001	1.098	0	1.738	0.01	0.680	0.007
	b		0.981		1.098		1.728		0.673	
6	a		0.984	0.001	1.274	0.008	0.976	0.006	0.992	0.003
	b		0.985		1.282		0.970		0.989	
7	a		1.757	0.011	1.341	0.004	1.083	0.002	0.817	0.002
	b		1.768		1.345		1.081		0.819	
8	a		1.446	0.011	1.010	0.001	1.025	0.005	0.969	0.003
	b		1.457		1.011		1.020		0.972	
9	a		1.563	0.013	0.723	0.006	0.961	0.002	0.952	0.002
	b		1.576		0.729		0.959		0.950	
10	a		0.934	0	0.609	0.003	0.973	0.001	1.107	0.002
	b		0.934		0.612		0.974		1.109	
11	a		1.457	0.009	0.800	0.002	1.077	0.001	1.000	0.002
	b		1.448		0.802		1.076		1.002	
12	a		0.979	0.001	0.878	0.009	0.934	0	1.327	0.014
	b		0.978		0.887		0.934		1.341	
13			1.720	0.008	1.107	0.001	1.080	0.007	1.447	0.009
	b		1.712		1.108		1.073		1.456	
14	a		0.961	0.002	1.092	0	1.054	0.002	1.019	0.002
	b		0.959		1.092		1.056		1.021	
15	a		0.971	0.009	1.016	0.003	0.877	0.006	0.961	0
	b		0.980		1.013		0.883		0.961	
16	a		0.934	0.002	0.995	0	1.018	0.006	1.235	0.006
	b		0.932		0.995		1.024		1.241	
17	a		0.932	0.001	0.972	0.002	0.531	0.01	1.233	0.002
	b		0.931		0.974		0.541		1.235	
18	a		0.982	0	0.972	0.002	1.399	0.009	0.960	0.001
	b		0.982		0.970		1.408		0.961	
19	a		0.951	0.001	0.974	0.005	0.965	0	0.991	0.003
	b		0.952		0.979		0.965		0.994	
20	a		0.962	0.001	1.106	0.002	0.975	0.002	1.457	0.006
	b		0.963		1.108		0.977		1.463	
21	a		1.235	0.002	0.870	0.001	0.958	0.004	0.972	0.002
	b		1.233		0.871		0.954		0.974	
22	a		1.380	0.011	0.996	0.001	0.983	0.002	1.172	0.006
	b		1.391		0.997		0.985		1.178	
23	a		1.205	0.008	1.081	0.003	1.059	0.004	1.524	0.006
	b		1.213		1.078		1.063		1.530	
24	a		1.580	0.012	1.036	0.001	0.967	0.001	1.213	0.002
	b		1.568		1.037		0.966		1.211	

Attachment of HRCR Item # 8: Noise Test Data

	Pwr1	Pwr7	Pwr9	Pwr8	Pwr2	Pwr5b	Pwr3	Pwr5	Pwr4	Pwr11
Vdd (V)	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8
Vss (V)	-1.58	-1.55	-1.55	-1.5	-1.5	-1.45	-1.4	-1.35	-1.3	-1.3
Vdd' (V)	2.506	2.51	2.51	2.517	2.516	2.522	2.529	2.535	2.541	2.542
Vss' (V)	-1.292	-1.266	-1.266	-1.222	-1.222	-1.179	-1.135	-1.091	-1.048	-1.047
Idd (mA)	1.128	1.1136	1.1135	1.0894	1.0895	1.0652	1.0412	1.0165	0.9922	0.9921
Iss (mA)	1.0921	1.0777	1.0776	1.0536	1.0538	1.0296	1.0056	0.981	0.9568	0.9568
I (mA)	1.11005	1.09565	1.09555	1.0715	1.07165	1.0474	1.0234	0.99875	0.9745	0.97445
P (mW)	4.2159699	4.1371744	4.1367968	4.0063385	4.0058277	3.8764274	3.7497376	3.6214675	3.4974805	3.49730105
	-16	-6	-6	-6	-16	-6	-16	-16	-16	-6
Channel Num		Vn @150 Hz	Vn @150 Hz	Vn @150 Hz		Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz
Channel: 1	6.69	6.75	7.56	6.06	7.43	7.26	8.26	11.47	14.99	13.58
Channel: 2	6.01	5.86	6.31	5.97	6.96	7.09	7.53	7.17	9.05	8.37
Channel: 3	7.18	8.67	7.30	9.54	10.12	12.82	15.02	26.10	29.51	29.60
Channel: 4	6.40	6.26	5.64	6.57	6.04	7.74	5.89	6.04	5.27	7.49
Channel: 5	7.19	5.93	6.05	5.74	6.61	7.04	6.62	6.25	6.65	6.78
Channel: 6	6.26	5.08	5.74	5.37	6.07	5.45	6.62	6.98	7.83	9.50
Channel: 7	6.25	6.41	6.35	6.57	5.94	6.36	5.70	6.95	7.31	7.31
Channel: 8	5.79	5.71	5.94	6.83	5.62	6.48	5.16	6.18	5.87	5.99
Channel: 9	8.05	7.93	6.88	6.81	7.57	7.21	7.10	7.90	7.98	8.06
Channel: 10	6.06	5.72	7.29	7.07	5.65	4.57	5.87	6.84	6.98	6.75
Channel: 11	9.79	12.06	11.25	14.66	9.60	19.59	25.47	31.23	39.25	38.29
Channel: 12	12.74	15.79	15.18	21.30	20.52	28.62	31.92	33.70	36.35	39.78
Channel: 13	5.51	5.75	7.75	7.01	7.53	8.27	9.01	13.27	12.85	15.01
Channel: 14	6.34	7.09	6.58	7.34	7.11	6.84	8.85	8.21	10.28	10.44
Channel: 15	6.28	6.73	6.88	8.59	6.35	5.76	8.48	8.00	7.58	9.05
Channel: 16	5.73	6.21	7.55	6.59	6.21	6.96	6.29	7.11	5.53	6.16
Channel: 17	7.54	5.59	7.61	6.32	5.93	6.37	7.32	8.06	7.84	9.40
Channel: 18	6.11	6.52	6.20	6.74	4.61	6.78	6.44	6.26	6.69	6.04
Channel: 19	11.33	14.60	13.32	11.83	11.03	10.78	10.93	10.15	9.03	11.05
Channel: 20	9.19	6.70	8.75	10.50	8.88	9.11	12.52	16.84	16.23	17.14
Channel: 21	8.03	10.26	8.56	10.04	9.58	8.37	6.98	8.64	7.75	6.48
Channel: 22	8.08	7.18	8.10	6.85	9.53	7.17	10.78	12.19	18.02	16.44
Channel: 23	10.16	10.42	11.84	11.38	12.30	14.74	15.60	19.97	23.76	23.15
Channel: 24	6.59	5.06	5.74	6.34	5.83	7.33	6.58	7.35	7.96	7.63
Median	6.64	6.61	7.30	6.84	7.04	7.19	7.43	8.03	7.97	9.22
Overall Mean	7.47	7.68	7.93	8.42	8.04	9.11	10.04	11.79	12.94	13.31
Good Mean	7.47	7.33	7.62	7.86	7.50	7.75	7.65	8.16	8.19	8.24
MP Reqd					15			15		
Yield	**1.00**	**0.96**	**0.96**	**0.96**	**0.96**	**0.92**	**0.83**	**0.79**	**0.75**	**0.71**
# Good Ch.	24	23	23	23	23	22	20	19	18	17
# Bad Ch.	0	1	1	1	1	2	4	5	6	7

JFET_Mod19_brd42_Noise_perf.xls

Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise

	Pwr7	Pwr4	Pwr5	Pwr5b	Pwr1	Pwr2	Pwr3
Vdd (V)	2.8	2.8	2.8	2.8	2.8	2.8	2.8
Vss (V)	-1	-1.1	-1.15	-1.18	-1.2	-1.3	-1.4
Vdd' (V)	2.531	2.516	2.508	2.504	2.5	2.485	2.471
Vss' (V)	-0.738	-0.823	-0.866	-0.892	-0.908	-0.992	-1.078
Idd (mA)	1.0317	1.0905	1.1201	1.1375	1.1542	1.2117	1.2697
Iss (mA)	0.992	1.0506	1.0802	1.0975	1.1134	1.1707	1.2286
I (mA)	1.01185	1.07055	1.10015	1.1175	1.1338	1.1912	1.24915
P (mW)	3.30773765	3.57456645	3.7119061	3.79503	3.8639904	4.1418024	4.43323335
	-6	-16	-16	-6	-16	-16	-16

Channel Num	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz			Vn @150 Hz
Channel: 1	10.45	10.10	7.47	6.89	7.06	6.53	7.76
Channel: 2	9.56	8.41	6.09	6.24	7.76	6.66	6.53
Channel: 3	16.72	12.62	8.99	8.92	7.78	6.79	6.71
Channel: 4	15.33	8.75	7.79	7.23	6.85	7.35	6.13
Channel: 5	11.53	6.96	6.42	5.22	5.51	7.64	8.38
Channel: 6	44.95	32.69	27.20	21.21	13.16	7.70	6.33
Channel: 7	20.91	17.27	15.93	11.12	7.36	6.44	6.58
Channel: 8	11.03	6.84	6.90	8.29	6.88	6.27	7.86
Channel: 9	7.48	6.94	4.77	5.89	4.78	7.09	6.42
Channel: 10	19.25	21.25	20.28	19.19	18.68	16.46	11.46
Channel: 11	13.67	8.52	7.66	7.77	10.04	12.44	9.73
Channel: 12	12.74	9.23	10.65	11.55	8.04	9.26	7.99
Channel: 13	17.83	8.66	7.16	6.24	6.87	6.78	6.68
Channel: 14	16.00	8.22	8.54	6.59	6.68	7.24	6.26
Channel: 15	8.08	7.16	10.05	9.14	7.14	6.28	6.82
Channel: 16	7.07	6.75	5.38	6.58	7.65	8.42	6.88
Channel: 17	8.15	7.34	10.34	9.24	5.96	6.03	6.07
Channel: 18	9.21	9.03	9.80	6.84	8.15	8.48	8.34
Channel: 19	8.44	6.20	7.82	6.59	6.47	7.59	7.20
Channel: 20	12.29	7.91	9.15	6.72	6.81	6.86	6.34
Channel: 21	37.52	25.30	19.17	14.50	9.78	7.24	7.56
Channel: 22	11.90	8.95	8.86	8.41	9.09	9.53	8.84
Channel: 23	19.22	16.38	14.86	14.16	8.30	6.15	6.62
Channel: 24	20.56	15.63	12.62	8.70	7.33	8.80	8.91
Median	12.52	8.71	8.93	8.03	7.34	7.24	6.85
Overall Mean	15.41	11.55	10.58	9.30	8.09	7.92	7.43
Good Mean	10.12	8.26	8.57	8.31	7.63	7.55	7.43
MP Reqd			15		15		
Yield	**0.58**	**0.75**	**0.83**	**0.92**	**0.96**	**0.96**	**1.00**
# Good Ch.	14	18	20	22	23	23	24
# Bad Ch.	10	6	4	2	1	1	0

JFET_Mod19_brd44_Noise_perf.xls

Attachment of HRCR Item # 9: SPIRE MIUL Cover Page

MIUL = Material Identification & Utilization List

Declared Materials List's and Processes List are not included in this HRCR

Materials and Processes List

SPIRE

JPL D-25725

REV B
1/05/04

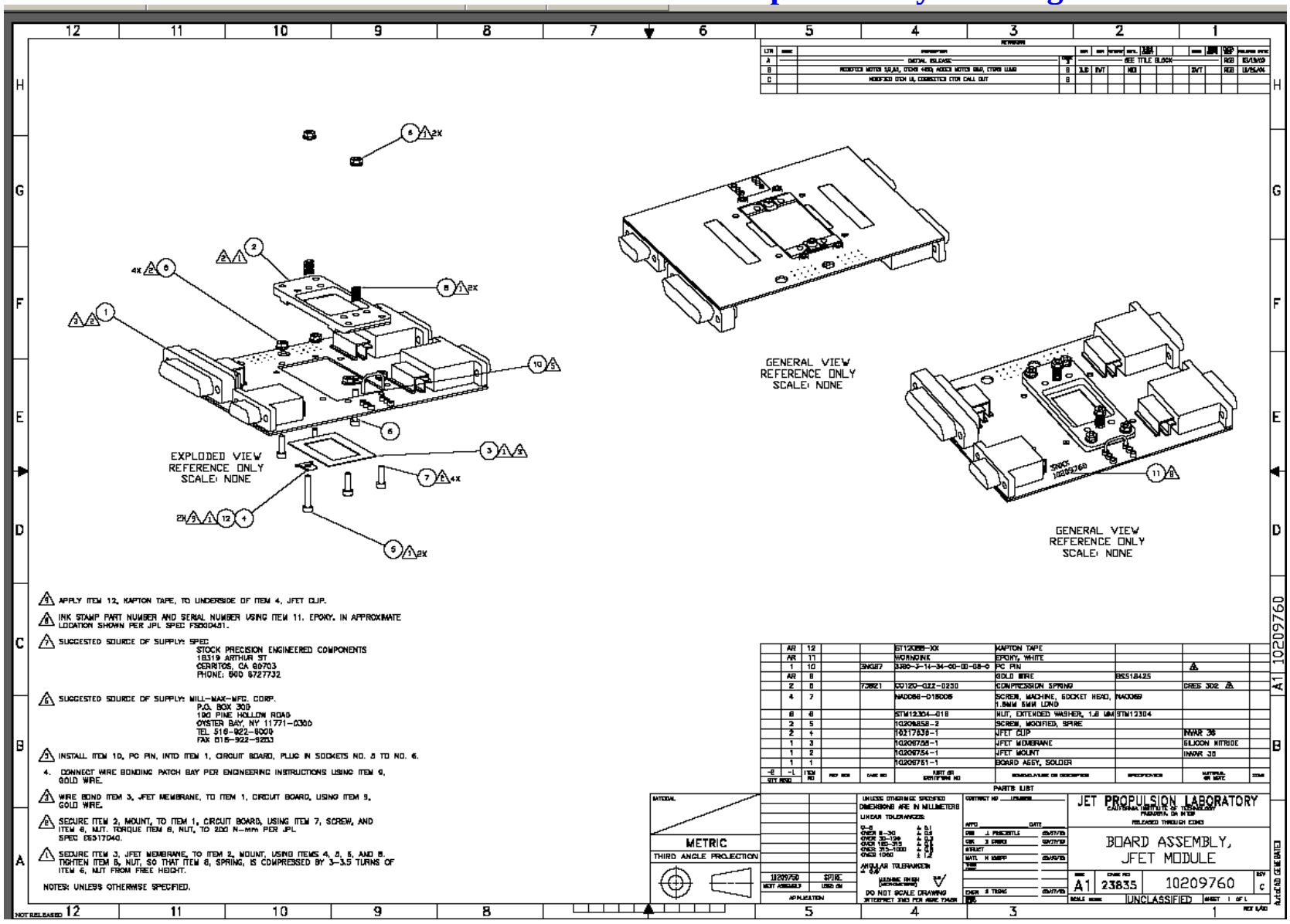
This technical data is export controlled under U.S. law and is being transferred by JPL to ESA for use exclusively on the Herschel/Planck projects. The information may not be used for any other purposes, and shall not be re-transferred or disclosed to any other party without the prior written approval of NASA.

Reviewed by: _____
M. Knopp M&P Engineer

Attachment of HRCR Item # 11:

See End of This HRCR Package for "JFET Module Handling Document"

Attachment of HRCR Item # 14: JFET Module Top Assembly Drawing 10209750-1



Attachment of HRCR Item # 23: Qualification Compliance Test

Qualification Model JFET Module

EIDP Coverpage For JFET Testing

Unit Identfication							
Name	:	JFET QM Module					
Part #	:	10209750-1					
S/N	:	#001					

Environmemtal Testing						
	Axes Tested	Temperature	Duration/# of Cycle	Requirement	Source	Waiver
Random Vibration Tes:	X, Y, Z	100 K	2 min/axis	X, Y, Z	SSSD, JFET-DES-C7	
High Level Sine Vibe Test	None	NA	NA	X, Y, Z	SSSD, JFET-DES-C7	HR-SP-JPL-RFW_005
Bakeout	NA	80 C	72 Hours	80C, 72 Hrs	D-20549	
Thermal Cycles	NA	RmT to 90 K	27	Minimum 15	D-20549	

Performance Characteristics						
		Specification		Source		Waiver
Power needed for <11 bad channels (Min Perf.)	9.1 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD. JFET-TEC-C5, JFET-PER-02		RFW in process
Power needed for <4 bad channels (Design Value)	10.8 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD. JFET-TEC-C5, JFET-PER-02		
Power needed for 100 % Yield per unit	13.6 mW	NA		NA		
Median Noise at < 11 bad chs.	7.13 nV/rtHz	<15 nV/rtHz Min Performance		SSSD, JFET-PER-01		
Median Noise at < 4 bad chs.	6.1 nV/rtHz		<7 nV/rtHz Design Value	SSSD, JFET-PER-01		
Median Noise at 100 % Yield.	6.97 nV/rtHz			SSSD, JFET-PER-01		
# of Channels over the max. offset voltage	0	< 15 mV for CQM < 15 mV for PFM/FS			SSSD. BDA-DRCJ-27	
Common Mode Rejection Ratio	< -60 dB by design, as measured in EM4 unit				SSSD. BDA-DRCJ-11	

Board Level Detail						
	Board SN 001				Source	
# Channels Tested :	24					
Median Noise at 3.5 mW :	18 nV/rtHz				SSSD, JFET-PER-C1	
# of good channels at 3.5 mW :	7	29% Yield			SSSD, JFET-PER-C2	
Power Needed for 100 % Yield :	6.75 mW				SSSD, JFET-PER-C2	
Median Noise at High Power (w/ 100 % Yield)	6.97 nV/rtHz				SSSD, JFET-PER-C1	
Median Gain at High Power	0.98				NA	

Definitions		
Good Channels	:	No se less than a min. performance value of 15 nV/rtHz
Yield	:	# of Good Channels / 24
Filenames		
Noise Measurements	:	QualJFETPostVibeNoise_Summary.pdf

Notes	
1)	The Base temperature for a performance characterization was 4K
2)	All Noise Measurements were made with the inputs shorted to ground

Attachment of HRCR Item # 24 & #25: Mate/Demate & Operation Logs

Hardware ID JFET SN 18, 19							
Date	Time	AIDS	Power	Mate	Demate	Transport	Notes
18-Apr	9:00 AM	245298				X	103 -> 183
18-Apr	10:00 AM	245298		X			Mate All Connectors
18-Apr	11:00 AM	245298					Measure all resistances
18-Apr	1:00 PM	245298	X				30 min each board, warm S.V. test (blue dewar)
20-Apr	9:00 AM	245298					Assemble into CSF
22-Apr	7:30 AM	245298			X		Remove all shorting connectors, close out CSF
22-Apr	8:00 AM	245298				X	183->144
22-Apr	9:00 AM	245298					Pump out
22-Apr	10:00 AM	245298					Run 3-axis warm shake
22-Apr	2:00 PM	245298				X	144->183
22-Apr	3:00 PM	245298		X			Install shorting connectors
22-Apr	4:00 PM	245298				X	Remove JFETs from CSF, bag and tag in flight cabinet
3-May	8:00 AM	245395		X			Install into Green Dewar
3-May	10:00 AM	245395					Pump out
3-May	11:00 AM	245395	X				30 min each board, warm S.V. test (green dewar)
4-May	8:00 AM	245395					Transfer LN2
4-May	7:00 PM	245395					Transfer Helium
5-May	8:00 AM	245395	X				30 min each board, cold S.V. test (green dewar)
6-May	8:00 AM	245395	X				3 hours, board 44, noise
5/7-5/9		245395					warm dewar
9-May	8:00 AM	245395					cool dewar to 4K
10-May	8:00 AM	245395	X				8 hours, board 44, noise
11-May	8:00 AM	245395	X				6 hours, board 42, noise
11-May	2:00 PM	245395	X				6 hours, board 48, noise
12-May	8:00 AM	245395	X				6 hours, board 48, noise
12-May	2:00 PM	245395	X				6 hours, board 25, noise
13-May	8:00 AM	245395	X				6 hours, board 25, noise
13-May	2:00 PM	245395	X				4 hours, board 42, noise
13-May	6:00 PM	245395	X				2 hours, board 25, gain
5/14-5/16		245395					warm dewar
16-May	8:00 AM	245395					cool dewar to 4K
17-May	8:00 AM	245395	X				4 hours, board 42, gain and CMRR
17-May	12:00 PM	245395	X				4 hours, board 44, gain and CMRR
18-May	4:00 PM	245395	X				4 hours, board 48, gain and CMRR
19-May		245395					warm dewar
20-May	8:00 AM	245395					cool dewar to 4K
20-May	7:00 PM	245395					Meaure heater resistances
5/21-5/22		245395					Warm Dewar
23-May	8:00 AM	245395	X				30 min each board, warm S.V. test (blue dewar)
23-May	2:00 PM	245395			X	X	Demate, Transport 183->103

Attachment of HRCR Item # 24 & #25: Mate/Demate & Operation Logs (continued)

OPERATION LOG SHEET -- SPIRE JFET BOARDS MODULE

USE THE "NOTE" COLUMN TO DESCRIBE ACTIONS

DEVICE (BRD) S/N: 042 (56) PROJECT: SPIRE/ JFET BOARD

DATE	TIME	TECH	PWR ON	PWR OFF	MATE				DEMATE				TRANSFORT	NOTE
					JAA	JBB	JCC	JDD	JAA	JBB	JCC	JDD		
11-01-04	9:30AM	103199			✓	✓	✓	✓	—	—	—	—		SAVERS INSTALLED
11-23-04	9:30AM	103199			—	—	—	—	—	—	—	—		GND & CHASSIS "
12-10-4	7:00AM	103199			—	—	—	—	—	—	—	—		GND & CHASSIS
12-10-4	12:00NN	103199	✓	✓	—	—	—	—	—	—	—	—		SOURCE TEST
3/-17-05		103199			—	—	—	—	—	—	—	—		GND & CHASSIS
3-17-05		103199	✓	✓	—	—	—	—	—	—	—	—		SOURCE TEST
3-31-05	1:00PM	103199			—	—	—	—	—	—	—	—		GND & CHASSIS
3-31-05	1:00PM	103199	✓	✓	—	—	—	—	—	—	—	—		SOURCE TEST
4-5-05	1:00PM	103199			✓	✓	✓	✓	✓	✓	✓	✓		GND & CHASSIS
4-5-05	1:00PM	103199	✓	✓			✓	✓			✓	✓		SOURCE TEST
4-6-05	9:00PM	103199			✓	✓	✓	✓	✓	✓	✓	✓		GND & CHASSIS
4-6-05	9:00PM	103199	✓	✓			✓	✓			✓	✓		SOURCE TEST
6-10-5		103199	✓	✓	✓	✓			✓	✓				SOURCE TEST

NOTE: CONNECTOR ARE RE-USE. FROM ASSY 1020976I-1 S/N 035, ATDS # 240885, IR#923860 NOV 1/25/05

Attachment of HRCR Items # 24 & # 25: Mate/Demate & Operation Logs

OPERATION LOG SHEET -- SPIRE JFET BOARDS MODULE

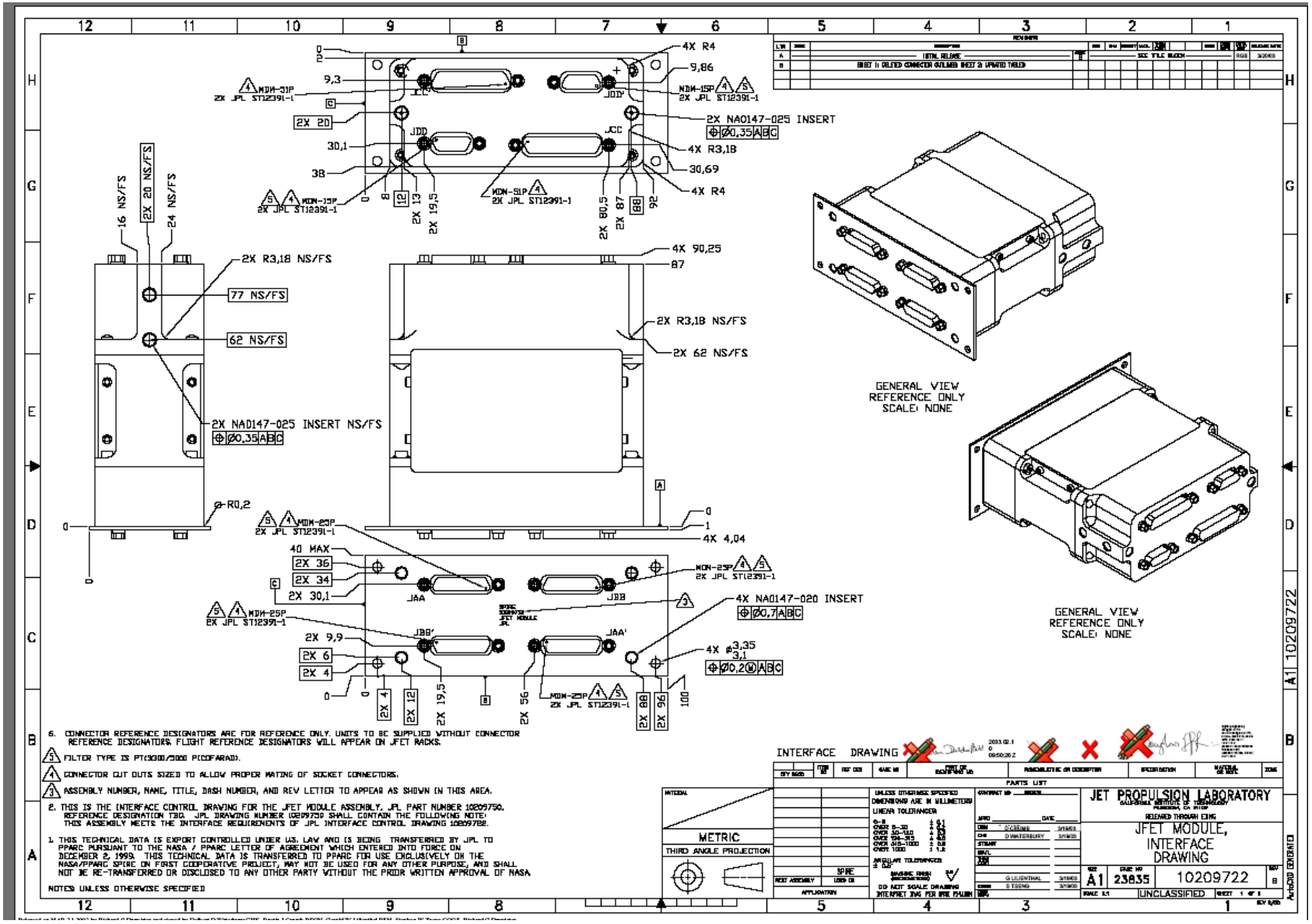
USE THE "NOTE" COLUMN TO DESCRIBE ACTIONS

DEVICE (BRD) S/N: 044 (58) PROJECT: SPIRE/ JFET BOARD

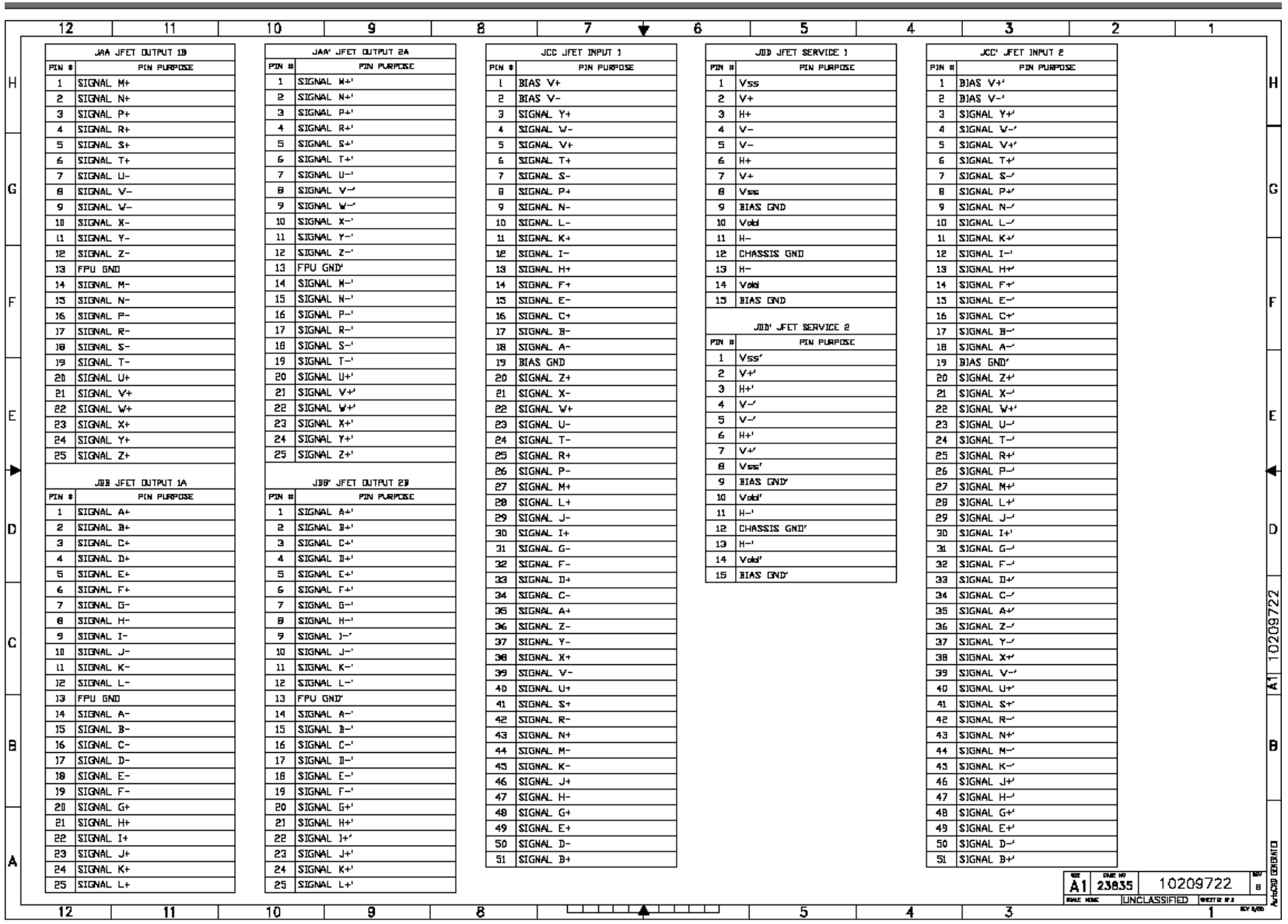
DATE	TIME	TECH	PWR ON	PWR OFF	MATE				DEMATE				TRANSFORT	NOTE
					JAA	JBB	JCC	JDD	JAA	JBB	JCC	JDD		
11/4/04		NAN			✓	✓	✓	✓	—	—	—	—		GND & CHASSIS – SPWER ON
11/12/05		NAN			—	—	—	—	—	—	—	—		GND & CHASSIS – "
1/24/05	10:00	NAN			–	–	–	–	–	–	–	–		GND & CHASSIS "
1/24/05	11:00	NAN	✓	✓	–	–	–	–	–	–	–	–		SOURCES TEST "
3-30-05		NAN			–	–	–	–	–	–	–	–		GND & CHASSIS "
3-30-05		NAN	✓	✓	–	–	–	–	–	–	–	–		SOURCE TEST "
4-5-05		NAN			✓	✓	✓	✓	✓	✓	✓	✓		GND & CHASSIS —
4-5-05		NAN	✓	✓			✓	✓			✓	✓		SOURCE TEST
4-6-05	2:00	NAN	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		SOURCE
4-6-05	2:00	NAN					✓	✓			✓	✓		GND & CHASSIS
6-10-5		NAN	✓	✓	✓	✓			✓	✓				SOURCE

NOTE: CONNECTORS ARE RE-USED, FROM BRD S/N: 027

Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 1 of 2)



Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 2 of 2)



JAA JFET OUTPUT 1B

PIN #	PIN PURPOSE
1	SIGNAL M+
2	SIGNAL N+
3	SIGNAL P+
4	SIGNAL R+
5	SIGNAL S+
6	SIGNAL T+
7	SIGNAL U-
8	SIGNAL V-
9	SIGNAL W-
10	SIGNAL X-
11	SIGNAL Y-
12	SIGNAL Z-
13	FPU GND
14	SIGNAL M-
15	SIGNAL N-
16	SIGNAL P-
17	SIGNAL R-
18	SIGNAL S-
19	SIGNAL T-
20	SIGNAL U+
21	SIGNAL V+
22	SIGNAL W+
23	SIGNAL X+
24	SIGNAL Y+
25	SIGNAL Z+

JBB JFET OUTPUT 1A

PIN #	PIN PURPOSE
1	SIGNAL A+
2	SIGNAL B+
3	SIGNAL C+
4	SIGNAL D+
5	SIGNAL E+
6	SIGNAL F+
7	SIGNAL G-
8	SIGNAL H-
9	SIGNAL I-
10	SIGNAL J-
11	SIGNAL K-
12	SIGNAL L-
13	FPU GND
14	SIGNAL A-
15	SIGNAL B-
16	SIGNAL C-
17	SIGNAL D-
18	SIGNAL E-
19	SIGNAL F-
20	SIGNAL G+
21	SIGNAL H+
22	SIGNAL I+
23	SIGNAL J+
24	SIGNAL K+
25	SIGNAL L+

JAA' JFET OUTPUT 2A

PIN #	PIN PURPOSE
1	SIGNAL M+'
2	SIGNAL N+'
3	SIGNAL P+'
4	SIGNAL R+'
5	SIGNAL S+'
6	SIGNAL T+'
7	SIGNAL U-'
8	SIGNAL V-'
9	SIGNAL W-'
10	SIGNAL X-'
11	SIGNAL Y-'
12	SIGNAL Z-'
13	FPU GND'
14	SIGNAL M-'
15	SIGNAL N-'
16	SIGNAL P-'
17	SIGNAL R-'
18	SIGNAL S-'
19	SIGNAL T-'
20	SIGNAL U+'
21	SIGNAL V+'
22	SIGNAL W+'
23	SIGNAL X+'
24	SIGNAL Y+'
25	SIGNAL Z+'

JBB' JFET OUTPUT 2B

PIN #	PIN PURPOSE
1	SIGNAL A+'
2	SIGNAL B+'
3	SIGNAL C+'
4	SIGNAL D+'
5	SIGNAL E+'
6	SIGNAL F+'
7	SIGNAL G-'
8	SIGNAL H-'
9	SIGNAL I-'
10	SIGNAL J-'
11	SIGNAL K-'
12	SIGNAL L-'
13	FPU GND'
14	SIGNAL A-'
15	SIGNAL B-'
16	SIGNAL C-'
17	SIGNAL D-'
18	SIGNAL E-'
19	SIGNAL F-'
20	SIGNAL G+'
21	SIGNAL H+'
22	SIGNAL I+'
23	SIGNAL J+'
24	SIGNAL K+'
25	SIGNAL L+'

JCC JFET INPUT 1

PIN #	PIN PURPOSE
1	BIAS V+
2	BIAS V-
3	SIGNAL Y+
4	SIGNAL W-
5	SIGNAL V+
6	SIGNAL T+
7	SIGNAL S-
8	SIGNAL P+
9	SIGNAL N-
10	SIGNAL L-
11	SIGNAL K+
12	SIGNAL I-
13	SIGNAL H+
14	SIGNAL F+
15	SIGNAL E-
16	SIGNAL C+
17	SIGNAL B-
18	SIGNAL A-
19	BIAS GND
20	SIGNAL Z+
21	SIGNAL X-
22	SIGNAL W+
23	SIGNAL U-
24	SIGNAL T-
25	SIGNAL R+
26	SIGNAL P-
27	SIGNAL M+
28	SIGNAL L+
29	SIGNAL J-
30	SIGNAL I+
31	SIGNAL G-
32	SIGNAL F-
33	SIGNAL D+
34	SIGNAL C-
35	SIGNAL A+
36	SIGNAL Z-
37	SIGNAL Y-
38	SIGNAL X+
39	SIGNAL V-
40	SIGNAL U+
41	SIGNAL S+
42	SIGNAL R-
43	SIGNAL N+
44	SIGNAL M-
45	SIGNAL K-
46	SIGNAL J+
47	SIGNAL H-
48	SIGNAL G+
49	SIGNAL E+
50	SIGNAL D-
51	SIGNAL B+

JDD JFET SERVICE 1

PIN #	PIN PURPOSE
1	Vss
2	V+
3	H+
4	V-
5	V-
6	H+
7	V+
8	Vss
9	BIAS GND
10	Vdd
11	H-
12	CHASSIS GND
13	H-
14	Vdd
15	BIAS GND

JDD' JFET SERVICE 2

PIN #	PIN PURPOSE
1	Vss'
2	V+'
3	H+'
4	V-'
5	V-'
6	H+'
7	V+'
8	Vss'
9	BIAS GND'
10	Vdd'
11	H-'
12	CHASSIS GND'
13	H-'
14	Vdd'
15	BIAS GND'

JCC' JFET INPUT 2

PIN #	PIN PURPOSE
1	BIAS V+'
2	BIAS V-'
3	SIGNAL Y+'
4	SIGNAL W-'
5	SIGNAL V+'
6	SIGNAL T+'
7	SIGNAL S-'
8	SIGNAL P+'
9	SIGNAL N-'
10	SIGNAL L-'
11	SIGNAL K+'
12	SIGNAL I-'
13	SIGNAL H+'
14	SIGNAL F+'
15	SIGNAL E-'
16	SIGNAL C+'
17	SIGNAL B-'
18	SIGNAL A-'
19	BIAS GND'
20	SIGNAL Z+'
21	SIGNAL X-'
22	SIGNAL W+'
23	SIGNAL U-'
24	SIGNAL T-'
25	SIGNAL R+'
26	SIGNAL P-'
27	SIGNAL M+'
28	SIGNAL L+'
29	SIGNAL J-'
30	SIGNAL I+'
31	SIGNAL G-'
32	SIGNAL F-'
33	SIGNAL D+'
34	SIGNAL C-'
35	SIGNAL A+'
36	SIGNAL Z-'
37	SIGNAL Y-'
38	SIGNAL X+'
39	SIGNAL V-'
40	SIGNAL U+'
41	SIGNAL S+'
42	SIGNAL R-'
43	SIGNAL N+'
44	SIGNAL M-'
45	SIGNAL K-'
46	SIGNAL J+'
47	SIGNAL H-'
48	SIGNAL G+'
49	SIGNAL E+'
50	SIGNAL D-'
51	SIGNAL B+'

Attachment of HRCR Item # 11:

JFET Module

Handling Document D-26790

Field Effect Transistor (JFET) Module 10209750-1

Prepared by: Kalyani Sukhatme 10 September, 2003

Revised by: Roger Welker & Steve Tseng 15 June, 2005

1. Introduction

This document provides guidelines for electrical handling for the SPIRE JFET Module.

1.1 Hardware Description

Each JFET module has two sets of 24 JFET channels. The JFET channels are populated on 1.0 micron thick Silicon Nitride membranes which provides thermal isolation. The operating temperature for these JFETs is ~120 K. The process of powering up the JFETs dissipates heat into the membrane resulting in a temperature increase with respect to the base temperature (4K to 10 K). Higher the power dissipation, higher is the temperature of the JFETs.

Each JFET channel consists of a matched pair of FETs (Figure 1.1-1) with a requirement for the offset voltage of less than **15 mV** between the matched pair. [The characteristic offset voltage is the difference between the source voltages (V_{sa} and V_{sb} with respect to ground) of the two FETs.]

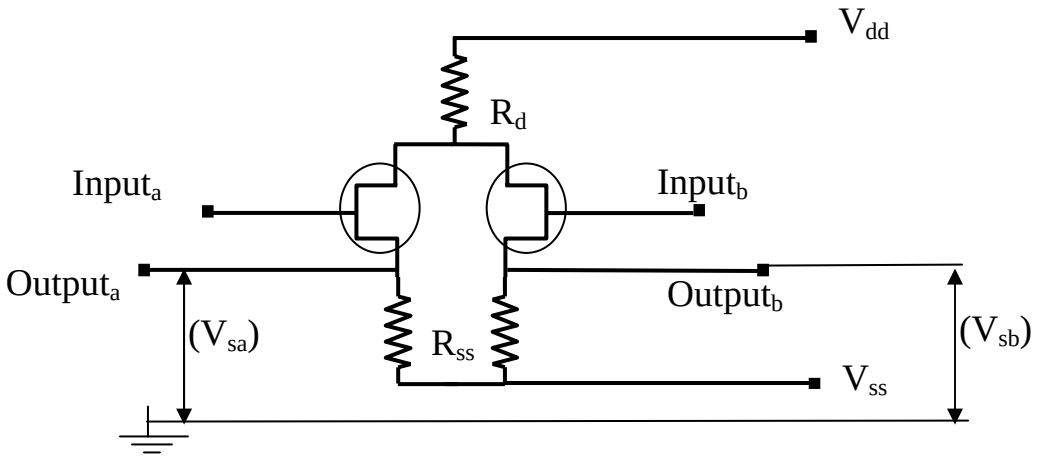


Figure 1.1-1

The Gates of the JFETs are the 'Inputs' of the circuit and the Sources (V_{sa} and V_{sb}) of the JFETs are the outputs, as marked in Figure 1.1-1. Vdd and Vss are the power lines for the circuit.

2. Handling

1. **The JFET Module is Contamination Sensitive**: Open shipment suitcase in an ISO 14644 Class 7 (FED-STD-209 Class 10,000) or cleaner cleanroom. Handle hardware with approved[1] nitrile or polyurethane ESD safe cleanroom gloves.

[1] JPL approved ESD safe cleanroom gloves are:

Nitrile:

Ansell-Edmont Nitrilite	http://www.ansellpro.com/ce/products3.asp?pid=87
Ansell-Edmont Nitrilite Silky	http://www.ansellpro.com/ce/products3.asp?pid=149
Ansell-Edmont Silky Ultra-Clean	http://www.ansellpro.com/ce/products3.asp?pid=150
Safeskin Critical (white)	http://www.safeskin.com/crit_nt_glv.asp

Polyurethane:

Wilshire Technology DuraCLEAN call in US, 323-259-6469 for ordering information

D-26790

2. **The JFET Module is ESD Sensitive**:

Please handle with appropriate ESD hardware handling procedures. Handle with grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.

ESD: Handle with approved[2] wrist straps, ESD-safe gloves and ESD smocks at an approved ESD protected workstation[3]. All personnel within 1 meter of unprotected ESD sensitive hardware shall be certified for ESD awareness[4]. Maintain shorting plugs on the unit at all times, except when the unit is installed in the final assembly of the SPIRE instrument. JFET modules are shipped with two shorting plugs for ESD protection. Refer to attached electrical handling document for other important safety precautions. Follow all instructions for the use of wrist straps, ESD smocks, static protected work areas, ionizers, packing/unpacking and cable handling per JPL standard D-1348, rev. F (This document is available through the public domain by the following URL: http://acquisition.jpl.nasa.gov/rfp/miri/dewar/DL-2671-584331/JPL_D-1348.pdf).

ESD - Ionizer: Prior to mate or demate of any connector, turn on an ionizer approved[5] for ESD sensitive components in clean room environment at least 5 minutes in advance and place/hold both sides of the connections in front of the ionized air stream for a minimum of 10 seconds before mating/demating operation. Position the ionizer near the hardware within the required distance per manufacturer's manual. Different makes and models of ionizers have different positioning requirements. During the mating/demating operations, it is necessary to follow the requirements for handling ESD sensitive hardware.

ESD - Connection to GSE: It is essential to ensure that all signal and bias lines of the GSE are grounded prior to mating the JFET hardware to the GSE. A save-to-mate check must be performed prior to connecting the JFET to the GSE. No excessive voltages and currents on all signal and bias lines shall be observed while the hardware is connected.

QA Oversight: Quality Assurance personnel should witness all handling, electrical testing, operation and integration of JFET flight hardware. At a minimum, a "two person" rule should be invoked at all times, where oversight by an independent party is provided to ensure hardware safety during handling, test and integration operations.

Humidity Sensitive: Place hardware in a humidity controlled ISO 14644 Class 7 (FED-STD 209 Class 10,000) cleanroom. Maintain humidity level at 35%-50% RH typical, for ESD safety.

---

[2] JPL approved wrist straps are:
Speidel Twist-o-Flex ™ brand metal expansion bracelet wrist straps
3M model 4600 adjustable molded thermoplastic wrist straps

[3] All work areas shall be certified and operated in compliance with the requirements of the following subsections sections of JPL-STD D-1348 rev. F section 2.3: subsections: 6, 8-11, 14-19, 21, 23 – 27, 29 – 36, 38 – 43 and 45.

[4] All personnel shall be trained and certified to the requirements of section 2.3.3 of JPL STD_D-1348 rev. F.

[5] The ionizer performance shall be verified to comply with the requirements of JPL-STD-D-1348 rev. F, Table 1 for devices with human body model ESD sensitivity less than 50 volts. The ionizer shall discharge from ± 1000 volts to less than ± 20 volts in less than 20 seconds and have a float potential of less than ± 20 volts.

3. **The JFET Module is Fragile**: Please do not drop or otherwise shock the unit including the shipping suitcase and container. Do not remove the cover of the JFET Module.

D-26790

3. Power ON Procedure

1. The JFET Module should be powered on **WITH the shorting plugs** (JPL Supplied Protection connectors) in place and with the **inputs shorted to ground.** Pins #9 and #15 on the 15-pin MDM connectors on the JFET Module are the bias grounds on the module. These pins should also be shorted to the power supply ground. The unit may be powered up without the shorting plug only when the inputs are connected to the detector system.

   Under no circumstances the unit should be powered up without the inputs shorted to ground either via the shorting plug (JPL Supplied) or via the detector system.

2. Do not exceed a voltage of +5 V for the Vdd line and –5 V for the Vss line of the JFET Module.

3. When removing the shorting plugs from the unit for installation into the instrument, please use standard ESD precautions including grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.

4. Electrical Check-out Test: Characteristic Offset Voltage Measurement

1) Verify that the gates of the JFET channels (Inputs) are shorted together and grounded.
2) Apply the power supply ground to the bias ground pins on the unit (Pins 9 and 15 on the 15-pin MDM connectors)
3) Power on the JFET modules with Vdd = +3 V and Vss = -1.5 V
4) Verify that the handheld multimeter is in calibration.
5) Connect one side of the handheld multimeter to ground (Power supply ground).
6) And measure the voltage with respect to ground of each side (V_{sa} and V_{sb}) of each channel.
7) Calculate the characteristic offset voltage (V_{offset}) for each channel ($V_{offset}= V_{sa}-V_{sb}$)
8) Compare the values for each of the channels with the specific datasheet provided with the unit. The datasheets accompanying the unit also provides the values for the drain and source currents for a similar test performed at JPL.

REFER TO MEASURED SOURCE VOLTAGE DATA FOR ACTUAL HARDWARE. Here is an example of the source voltage values and the drain and the source currents obtained for such a test at room temperature are given in the Table 4-1

T, JFET	rm T
Vdd	3 V
Vss	-1.5 V
Idd	1.564 mA
Iss	1.5686 mA

Channel #	(V)	DELTA (V)
1	1.130	0
	1.130	
2	1.075	0.001
	1.074	
3	0.781	0.001
	0.780	
4	1.088	0.005
	1.093	
5	0.834	0.001
	0.833	
6	1.012	0.003
	1.015	
7	0.785	0.002
	0.787	
8	1.148	0.004
	1.144	
9	0.753	0
	0.753	
10	0.693	0.008
	0.701	
11	1.110	0.004
	1.114	
12	0.758	0.001
	0.759	
13	0.832	0.002
	0.830	
14	1.264	0.001
	1.265	
15	1.206	0
	1.206	
16	0.818	0.001
	0.819	
17	0.526	0.005
	0.521	
18	1.423	0
	1.423	
19	0.773	0.002
	0.775	
20	0.873	0.004
	0.877	
21	1.387	0.006
	1.393	
22	1.417	0.003
	1.420	
23	0.887	0.002

	0.889	
24	0.888	0.003
	0.891	

- END OF -
Attachment of HRCR Item # 11:
"JFET Module Handling Document D-26790"

END OF

HRCR PACKAGE