JPL Hardware Requirements Certification Review – SPIRE Element No. D-32239

JPL Hardware Requirements Certification Review - SPIRE Element No. D-32239 Assembly / Subsystem PEM Phone Section Date (818) 354-8541 **SPIRE Martin Herman** 385 17 June. 2005 Nomenclature Final IR No. Drawing/ Part No. Dwg. Rev. Serial No. Model Mass (Meas. / Reg.) Type 10209750-1 В **JFET Module** 017 **FLT-Spare** N/A 926198 273.5 gm / 305 gm Y Check applicable answer and provide N N E S Remarks **Data Attachments** Signature & Date 0 explanation in remarks column A Cognizant Engineer 1. Are all drawings and specifications 14. Latest Top Assembly drawings X Here Tong 6/17/01 complete, approved, released and frozen? None PEM 2. Do the released drawings and 15. List of open ECRs X specifications reflect all approved changes? Attached None QA/∉ngineer/ 16. Waivers (RFW request for waiver) 3. Is hardware identical to other hardware X delivered? If no, provide difference list. None 4. Does the hardware meet its functional EIDP attached. 17. Open MRB Environments/Reliability X -120 6/17/05 Also see item # 8 attachments. Attached None requirements, specifications, waivers, ICDs? 18. Open PFR on this H/W 5. Are all IR and MRB dispositioned and Mission Assurance Mgr. X -1-00 6/17/09 concurred by QA? Attached None Project Office 19. Open PFR on similar H/W 6. Is complete as-built list information X Attached included in the build book? None 20. Handling Document → See Item 11 7. Have all required environmental tests & X ETAS attached analyses been completed? None 8. Is all required assembly and/or Performance Test Data Attached. 21. Shortage List X subsystem level functional testing complete? Also see EIDP in item # 4. Attached None 22. Requirements Verification Matrix 9. Have all piece parts, processes and X Attached (See #4, #7, #8) None materials been approved by JPL? Parts, processes and MIUL met all 23. Qualification Status 10. Does this hardware meet all X contamination control and out-gassing None contamination control requirements? requirements. 24. Mate / Demate Record 11. Are all shipping containers, shipping and X See Attached Document D-26790 special handling procedures ready? None 12. Is additional work required to bring this 25. Operating Log X Attached (See Item # 24) hardware to flight (flight-spare) readiness? None 26. MICD X 13. Is this hardware acceptable for flight? None

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RAL EIDP Table of Contents Versus JPL HRCR Check List Item Numbers

RAL EIDP Section Number	RAL EIDP Title	JPL HRCR Check List Item Number	Notes
1	Shipping Documents		Shipper and Final IR
2	Transportation, Packing, Handling & Integration Procedures	11	Special Handling Document D-26790
3	Certificate of Conformance / Delivery Review Board MOM		HRCR book is the C of C
4	As Built Configuration Status List	1 & 2	Assembly Drawings
5	List of Waivers	4	RFW (request for waiver) Attached
6	Copies of Waivers	4 & 7	RFW (request for waiver) Attached
7	List of Non-Conformance Reports		See RFW in 4 & 7
8	Copies of Non-Conformance Reports		See RFW in 4 & 7
9	Cleanliness Statement		Final IR QA Inspection
10	Operational Manual		NA
11	Top Level Drawings (inc. Family Tree)	14	Top Assembly Drawing
12	Interface Drawings	26	MICD Drawing
13	Functional, Block & Mechanical Drawings		NA
14	Electrical Circuit Drawings		NA
15	Serialized Components List		In build books – not shipped
16	Mass Properties/ Power Budget	HRCR Check List Page 1	Mass listed in HRCR check list
17	Qualification Status List / Test Matrix	23	Qualification Unit Test Matrix
18	Test Reports	4, 7, 8, 23	
19	Open Work / Deferred Work / Open Tests		NA
20	Calibration Data		NA
21	Historical Record	23	Qualification Unit Test Matrix
22	Manufacturing Logbook(s)		In build books – not shipped
23	Operating Time / Cycle Record	25	
24	Connector Mating Record	24	
25	Age Sensitive Items Record		NA
26	Pressure Vessels – History/Test Record		NA
27	Temporary Installation Record		NA
28	Reference List of EIDPs (Lower level)		NA
29	Other Useful Information		NA

JPL Hardware Requirements Certification Review (HRCR)

Junction Field Effect Transistor (JFET) Flight Module

10209750-1 S/N 017

SPIRE Element
Herschel Space Observatory Project

June 17, 2005

Configuration of Module, Boards & Membranes

Module 10209750-1	S/N 17	S/N 17
PWB 10209760-1	S/N 041	S/N 043
Membrane 10209758-1	J6.11.3	J6.16.1

Attachment of HRCR Items #1 Drawing Release Status

ALL ASSEMBLY & PARTS DRAWINGS ARE RELEASED IN PDMS

Released Drawings:

10209719-1	assembly built per released Rev. A drawing (studlock)
10209722-1	assembly built per released Rev. B drawing (interface drawing)
10209750-1	assembly built per released Rev. B drawing (module assy)
10209751-1	assembly built per released Rev. B drawing (chassis 1)
10209752-1	assembly built per released Rev. A drawing (chassis 2)
10209753-1	assembly built per released Rev. A drawing (chassis 3)
10209754-1	assembly built per released Rev. C drawing (mount)
10209756-1	assembly built per released Rev. B drawing (chassis lid)
10209757-1	assembly built per released Rev. A drawing (membrane)
10209758-1	assembly built per released Rev. A drawing (membrane assy)
10209759-1,-2	2,-4 redlined Rev. B drawing (gasket)
10209760-1	assembly built per released Rev. C drawing (board assembly)
10209761-1	assembly built per released Rev. C drawing (solder connector)
10209769-1	assembly built per released Rev. A drawing (stiffener)
10209777-1	assembly built per released Rev. B drawing (board)
10209858-2	assembly built per released Rev. A drawing (special fastener)
10217636-1	assembly built per released Rev. A drawing (clip)

Attachment of HRCR Item #4: EIDP (End Item Data Package)

·	tachment of HKC	I	Item π·	4. 12112	r (Em	i item D	ala I acnago	=)
			EIDP	Coverpage	For JFE1	Testing]	
	Unit Identfication							
	Name	:	JFET PF	M Module				
	Part #	-		9750-1				
	S/N			17				
		•						
	Environmemtal Testing							
			Axes		Duration/#			
			Tested	Temp	of Cycle	Requirement	Source	Waiver
							SSSD,	
_	Random Vibration Test	_	X, Y, Z	Rm T	1 min/axis	X, Y, Z	JFET-DES-07	LID OD IDI
	High Level Sine Vibe Test		None	NA	NA.	X, Y, Z	SSSD, JFET-DES-07	HR-SP-JPL- RFW-005
	Bakeout		NA	80 C	24 hrs	> 24 HRS	31 21-023-01	111 11-000
				RmT to 80 K	24 1115		D 20540	
	Thermal Cycles		NA	TAIL TO CO IX	2	Minimum 1	D-20549	
	Performance Characteristics	;						
				Specifi	cation		Source	Waiver
	Power needed for <11 bad channels			11 mW fo			SSSD.	HR-SP-JPL-
	(Min Perf.)		6.59 mW	7 mW for		JFET-TEC	-05, JFET-PER-02	RFW-004
	Power needed for <4 bad channels			11 mW fo	r CQM,		SSSD,	
	(Design Value)		7.07 mW	7 mW for	PFM/FS	JFET-TEC	-05, JFET-PER-02	
	Power needed for 100 %							
	Yield per unit		7.76 mW	N/	١		NA	
	Median Noise at < 11 bad chs.		9.72 nV/rtHz	<15 nV/rtHz	<7 nV/rtHz	SSSD,	JFET-PER-01	
	Median Noise at < 4 bad chs.		8.42 nV/rtHz	Min	Design	SSSD,	JFET-PER-01	
	Median Noise at 100 % Yield.		7.55 nV/rtHz	Performance	Value	SSSD,	JFET-PER-01	
	# of Channels over the						SSSD,	
	max. offset voltage	_	0	< 15 mV			BDA-DRCU-27	
	Common Mode Rejection Ratio		< -60 dB by de	esign, as meas	ured in EM4	unit	SSSD, BDA-DRCU-11	
	Board Level Details							
				SN 041		rd SN 043	e	
				-JDD)		(A'-JDD')	Source	
	# Channels Tested	:	24		24		SSSD.	
	Median Noise at 3.5 mW		0.05 m	V/rtHz	9.0	9 nV/rtHz	JFET-PER-01	
	# of good channels		8.0311	87.5%	8.0	87.5%	SSSD.	
	at 3.5 mW	:	21	Yield	21	Yield	JFET-PER-02	
	Power Needed for						SSSD,	
	100 % Yield	:	3.99 mW		3.77 mW		JFET-PER-02	
	Median Noise at High Power (w/ 100						SSSD,	
	% Yield)		7.47 n	V/rtHz	7.5	6 nV/rtHz	JFET-PER-01	
	Median Gain at High Power		0.	98		0.97	NA	
	Heater Resistance, 4K Reference							
	value	:	2.42	2 kΩ	3	.25 kΩ	NA	
	Definitions							
	Good Channels	:	Noise less that	n a min. perfor	mance value	of 15 nV/rtHz		
	Yield	:	# of Good Cha	nnels / 24				
	Filenames							
	Noise Measurements	:	JFET_Mod17	brd41_Noise_	perf.pdf			
	Source Voltages (RmT, 4K)	:	JFET Module	16, 17 voltage	data, 40,45,4	1,43 040105.pdf		
	Notes							
1)	The Base temperature for all performa	anc	e characterizati	on was 4K				
21	All Noise Measurements were made v							
-,			and in parts still	a to ground				

SN043: 41% Overetched

Attachment of HRCR Item #7: RFW (Request For Waiver)

CCLRC Rutherford Appleton Laboratory	REQUEST	FOR WAIVE (RFW/RF		VIATION	Spa			SURANCE d Technolog nent
		RF	W/RFD	Number:	HF	R-SF	P-JPL-R	FW-005
Spacecraft / Project	Herschel		Origina	ator's Name		Kalv	ani Sukhatr	ne
System / Experiment / Model	SPIRE			ure / Date		,		
Sub-System	detectors			st Type nt applicable requ	est)	Wa	ver (RFW)	Deviation (RFD)
Assembly			Organi			_		on Laboratory
Sub-Assembly			Ref. Do	oc. / Drwg No		S	PIRE-JPL-F	PRJ-000456
Item			Refere	nces				
Serial No.			1,01010					
RFW/RFD Title	BDA and JFE	T module sine te	st deleti	on				
					,			
Name		Items(s) Affecte	d (Hardw CI-Nu		9)		Mos	lel(s)
Bolometric Detector Asser			CI-NU	IIIDei		COM	I, PFM, FS	(s)
JFET Modules	IIblies						1, PFM, FS	
	Requ	iirement / Interfa	ce Docu	ments Affect	ed			
Specification/Drawin		Number		Issue	Da	$\overline{}$		Paragraph
BDA-SSSD (SPIRE-JPL-P 000456)	RJ-			3.2	Jan 200		BDA-DES- 07	10, JFET-DES
,		of Deviation / Di d on these units	screpan	cy / Non-Cont				
,	t is not performe				forma	nce		
High Level Sine- Vibe Test	t is not performed Other Its	d on these units ems or Requiren or RFW/RFD and	nents (Po	otentially) Affo	forma	nce		
The hardware has to be opurpose of the test. The since the cold vibration fresources (cost and scheller is no Requirement test are required.	Other Its Need for qualified under high level sine facility is not streedule) for devel high note added to do a high level.	ems or Requirent or RFW/RFD and a cold vibration vibration test cor ructurally capabl oping a new set- ed vel sine test on p	Rationa Rationa test and nfigurati e of with up is no	btentially) Afformation in the for Accepta is installed in on will put the standing the teasible at t	ance in the ce high his tir	nce cold v dware levels ne.	ibration fac and the po . Obtaining	ersonnel at ris gadditional ceptance leve
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Attachment of HRCR Item #7: ETAS (Environmental Test Summary)

	ENV	/IRONMENTAL T	EST A	AUTHORIZA	TION	AND SUMMAR	RY (ETAS)	
		AUTHO	RIZA	TION SECTION	1			
PROJECT					LOG N			
Herschel					HS04	0		
SYSTEM/ASSEMBLY T							4/12/05	D
REFERENCE DESIGNATION	NUMBER	PART NO. (IF MULTIPLE	ATTACH	(LIST)	REV.		SERIAL NO.	
		10209750-1					016,017	
HARDWARE TYPE	_	_			PRE-B	NVIRONMENTAL INSPEC	TION REPORT N	JMBER (ATTACH IR)
EM QUAL	☑ FLIGHT	FLIGHT SPARE	_	OTHER			CERTAL NO.	
WIRING HARNESS	FLIGHT		PAF	RT NO.	REV.		SERIAL NO.	
TEST DESCRIPTION (CHEC		EM SE			TYPE	OF TEST	1	
SINE VIBRATION	PYROSHOCK	☐ ACOUSTIC ☐ EMC	П	OTHER		IALIFICATION	☐ FUGHT	ACCEPTANCE
RANDOM VIBRATION	THERMAL VAC.	☐ THERMAL ATMOSPHER	_		_	OTO FLIGHT	RETEST	
		THE PROJECT DOCUMENTS		ORMED ON THIS UN				
✓ YES	NO (IF NO, ATTACH		ENT	ER PROJ. DOC. NO.	AND REV	·		
HAS THE UNIT PASSED ALI								
⊠ YES	NO (IF NO, ATTACH			EF EXPLANATION				
	_	ND REQUIRED CHANGES BE		EMENTED? EF EXPLANATION				
IS THE TEST ARTICLE IDEN	NO (IF NO, ATTACH		Dru	EF EAPLANATION				
YES	NO (IF NO, ATTACH		BRII	EF EXPLANATION				
ARE ALL PERS AGAINST TH		Exocr novo con						
⊠ YES	NO (IF NO, ATTACH	EXCEPTIONS LIST)	BRII	EF EXPLANATION				
	CRS BEEN APPROVED AN	NO ARE THEY INCORPORATE	D?					
☑ YES	NO (IF NO, ATTACH	EXCEPTIONS LIST)	BRII	F EXPLANATION				
COGNIZANT ENGINEER	Inde 4/13	DATE TECHNICAL MGRJIN	ISTR MR	ORIZED BY GJPI PREP REP	DATE (3/05	Environmental re	EQUIREMENTS EN	13/05 DATE
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Attachment of HRCR Item #7: ETAS (Environmental Test Summary)

ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS) OTHER AUTHORIZATION PROVISIONS AND EXPLANATIONS is a 3-axis warm vibration test (room temp) done on the JFET flight modules SN016 and 017. The test will be done with the JFET unit mounted inside a mock-up JFET rack. The unit will be assessed both before and after the test with visual inspections and electrical checkouts. 3 response accelerometers will be mounted onto the JFET rack in order to give response data. 2 to 2 vacuum thermal cycles will also be completed. 2 JPL 2683 R 1/98 FF

Attachment of HRCR Item #7: ETAS (Environmental Test Summary)



ENVIRONMENTAL TES UTHORIZATION AND SUMMARY (ETAS) ENVIRONMENTAL TEST SUMMARY

HARDWARE	S/N	ETAS	TEST ENVIRONMENT LEVELS & DURATION	DATE TEST PERFORMED	TEST AGENCY	PASS/ FAIL	COMMENTS
SPIRE JFET (10209750-1)	016,01 7	HSO40	X, Y, and Z 1 minute Random Vibe Frequency Spec [Hz] [g^2.Hz] 20 0.01 100 0.05 300 0.05 499 0.0214 500 0.0214 2000 0.00214 Each axis 1/4 g sine sweep 20- 2000 Hz each axis 2-3 vaccuum thermal cycles. <10E-5 mbar,				
		34.					
		:					

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Attachment of HRCR Item #8: Test Data - Source Voltage Data

JFET S	OURCE	VOLTA	GE MEA Post bake,															
			pwr1 1,2A		pwr2 3.4A		pwr3 1,2 B		pwr4 3,4B		pwr1 1,2A		pwr2 3,4A		pwr3 1,2 B		pwr4 3.4B	
Date				2005	5/24/	2005		2005	5/24/	2005	5/31/	2005	5/31/	2005	5/31/	2005	5/31/	2005
T, plate			4k		4K		4k		4K		Rn		Rm		Rn		Rm	
1744			4k		4K		4K		4K		Rn		Rm		Rn		Rm	
Vdd Vss			-1		1.		-1		-1.		-1		-1.		-1		-1	
Vdd'			2.748		2.779		2.676	.0	2.762	.0	2.721		2.748		2.651		2.736	
Vss'			-1.245		-1.277		-1.174		-1.26		-1.218		-1.246		-1.148		-1.233	
ldd Iss			0.9		0.84 0.84		1.2- 1.2-		0.91 0.91		1.08 1.0		0.98	504 49	1.3	22	0.99	
SN				0	4		4		4:		4		8		4		4	
Channel #			0.704	DELTA		DELTA	0.070	DELTA	0.775	DELTA		DELTA		DELTA		DELTA		DELTA
1	a b		0.701 0.703	0.002	0.860 0.859	0.001	0.276 0.273	0.003	0.775 0.780	0.005	0.987	0.003	1.158	0	0.553 0.553	0	1.057 1.062	0.005
2	a		0.716	0.002	0.147	0.006	0.734	0.007	0.699	0.004	1.005	0.001	0.468	0.006	0.997	n nne	0.983	0.002
	b		0.718	0.002	0.141	0.000	0.727	0.007	0.703	0.004	1.004	0.001	0.462	0.000	0.991	0.008	0.985	0.002
3	a b		0.874 0.880	800.0	0.139 0.144	0.005	0.697 0.701	0.004	0.814 0.809	0.005	1.155	0.005	0.461	0.001	0.961 0.965	0.004	1.098 1.090	0.008
_	a		0.697	0.000	0.356	0.000	0.678	_	0.771	0.004	0.987	0.004	0.400	0.004	0.946	0.000	1.055	0.000
4	b		0.699	0.002	0.354	0.002	0.678	0	0.772	0.001	0.986	0.001	0.666	0.004	0.944	0.002	1.057	0.002
5	a b		0.841 0.842	0.001	0.912 0.908	0.004	0.683 0.685	0.002	0.662 0.662	0	1.123	0.002	1.213	0.003	0.965 0.969	0.004	0.947	0
	a		0.789		0.584		0.729		0.002		1.070		0.889		0.993		1.024	
6	b		0.792	0.003	0.589	0.005	0.728	0.001	0.732	0.004	1.072	0.002	0.894	0.005	0.993	. 0	1.021	0.003
7	a		0.889 0.880	0.009	0.913 0.917	0.004	0.753 0.758	0.003	0.773 0.771	0.002	1.171	0.009	1.218	0.003	1.014 1.016	0.002	1.070	0
	b a		0.708		0.919		0.770		0.771		0.998		1.218		1.010		0.972	
8	b		0.710	0.002	0.917	0.002	0.773	0.003	0.689	0.004	1.000	0.002	1.214	0.002	1.033	0.002	0.976	0.004
9	a		0.751	0.007	1.074	0.001	0.761	0.002	0.640 0.647	0.007	1.039	0.005	1.370 1.370	0	1.029 1.032	0.003	0.934 0.940	0.008
	b a		0.758 0.698		1.073 0.118		0.763 0.843		0.723	_	0.992		0.458		1.109		1.011	
10	b		0.700	0.002	0.116	0.002	0.845	0.002	0.723	0	0.993	0.001	0.453	0.003	1.110	0.001	1.011	0
11	a		0.710 0.712	0.002	0.906	0.002	0.668	0.001	0.693	0.002	1.005	0	1.214	0.002	0.945 0.945	0	0.993	0.003
<u> </u>	a a		0.712		0.908 0.910		0.667		0.691 1.162		1.005 0.998		1.216 1.224		1.010		0.990 1.441	
12	b		0.702	0.002	0.909	0.001	0.742	0.003	1.156	0.006	0.995	0.003	1.225	0.001	1.013	0.003	1.435	0.008
13	a b		0.715 0.716	0.001	0.227 0.235	800.0	0.448 0.461	0.013	0.288 0.278	0.01	1.013	0.002	0.559 0.565	0.006	0.731 0.745	0.014	0.597 0.586	0.011
- 14	a		0.710		1.108	0.004	0.401	0.005	0.276	0.004	0.962	0.000	1.410	0.004	0.743	0.007	1.002	0.000
14	b		0.664	0.003	1.104	0.004	0.620	0.005	0.700	0.004	0.965	0.003	1.409	0.001	0.892	0.007	1.008	0.008
15	a b		0.681 0.679	0.002	0.362 0.371	0.009	0.687 0.691	0.004	0.722 0.720	0.002	0.975 0.975	0	0.683	0.009	0.962 0.963	0.001	1.011	0.002
1,0	a		0.708	0.000	0.156	0.005	0.711	0.002	0.654	0.003	1.003	0.002	0.484	0.004	0.976	. 0	0.947	0.002
16	b		0.705	0.003	0.151	0.000	0.709	0.002	0.651	0.003	1.001	0.002	0.480	0.004	0.976	. "	0.945	0.002
17	a b		0.739 0.737	0.002	0.250 0.258	800.0	0.711	0.001	0.678 0.680	0.002	1.029	0.002	0.573	0.008	0.980 0.982	0.002	0.969	0.002
- 10	a		0.689	0.004	0.527	0.006	0.729	0.004	0.801	0.001	0.989	0.001	0.839	0.005	0.997	0.004	1.086	0.002
18	b		0.685	0.004	0.533	0.000	0.733	0.004	0.802	0.001	0.988	0.001	0.844	0.005	1.001	0.004	1.088	0.002
19	a b		0.691 0.691	0	1.008	0.001	0.695 0.692	0.003	0.724 0.729	0.005	0.982 0.981	0.001	1.326 1.326	0	0.963 0.961	0.002	1.008	0.005
20	a		0.659	0.003	0.360	0.001	0.728	0.003	0.710	0.004	0.963	0.002	0.691	0.004	0.992	0.003	1.011	0.002
	ь		0.656	. 0.000	0.359	0.001	0.731	0.000	0.714	0.001	0.961	0.002	0.695	0.001	0.995 1.258		1.013	
21	a b		0.699 0.702	0.003	0.344	0.007	1.005 1.008	0.003	0.699 0.698	0.001	0.992	0.001	0.660	0.007	1.282	0.004	0.988	0.001
22	a		0.687	0.001	0.237	0.011	0.737	0.001	0.726	0.003	0.977	0	0.557	0.01	1.003	. 0	1.009	0.002
	b a		0.688 0.727	. 0.001	0.248 0.296		0.738 0.696		0.729 0.787		0.977 1.013		0.567 0.614		1.003 0.962		1.011 1.068	
23	b		0.727	- 0	0.290	0.008	0.695	0.001	0.785	0.002	1.014	0.001	0.610	0.004	0.960	0.002	1.066	0.002
24	a		0.676	0.003	0.436	0.005	0.785	0.003	0.674	0.003	0.986	0.002	0.750	0.003	1.044	0.003	0.958	0.005
	b a		0.679		0.441		0.788		0.677		0.968		0.753		1.047		0.963	
25	b			0		0		0		0		0		0		0		0
26	a			0		0		0		0		0		0		0		0
27	b a			. 0		0		0		0		0		0		. 0		. 0
	b a																	
28	b			. 0		0		0		0		0		0		. 0		. 0
29	a b			0		0		0		0		0		0		0		0
30	a b			0		0		0		0		0		0		0		0
	0																	

Attachment of HRCR Item #8: Noise Test Data

	Pwr1	Pwr2	Pwr11	Pwr5	Pwr4	Pwr3	Pwr7	Pwr9	Pwr8	Pwr10
Vdd (V)	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8
Vss (V)	-1.6	-1.4	-1.3	-1.26	-1.23	-1.2	-1.1	-1.08	-1.05	-1
Vdd' (V)	2.539	2.527	2.499	2.453	2.486	2.509	2.527	2.513	2.535	2.504
Vss' (V)	-1.26	-1.09	-1.005	-0.971	-0.946	-0.921	-0.836	-0.819	-0.793	-0.754
ldd (mA)	1.3316	1.2143	1.155	1.1313	1.1136	1.096	1.0358	1.0238	1.0058	0.9757
Iss (mA)	1.2975	1.1806	1.1215	1.0979	1.0802	1.0626	1.0028	0.9908	0.9729	0.9429
I (mA)	1.31455	1.19745	1.13825	1.1146	1.0969	1.0793	1.0193	1.0073	0.98935	0.9593
P (mW)	4.99397545	4.33117665	3.988428	3.8163904	3.7645608	3.701999	3.4279059	3.3563236	3.2925568	3.1253994
	-8	-8		-8	-8	-8	-8	-8	-8	-8
Channel Num			Vn @150 Hz							
Channel: 1	10.77	7.89	6.84	6.04	7.18	7.02	6.61	6.63	7.82	7.10
Channel: 2	6.63	6.95	5.91	5.85	5.75	6.20	9.11	10.37	9.51	12.74
Channel: 3	6.34	5.79	7.23	6.84	6.46	7.35	6.75	7.10	7.96	9.57
Channel: 4	5.71	5.88		5.73	5.97	5.74	5.69	6.87	7.77	10.32
Channel: 5	7.65	6.12	7.67	5.34	6.32	8.15	8.16	9.34	12.47	16.33
Channel: 6	6.75	9.34	7.69	8.11	6.00	8.83	10.82	12.11	16.75	21.29
Channel: 7	10.05	11.14	10.27	14.33	15.91	16.97	21.74	20.87	22.51	22.82
Channel: 8	7.75	8.91	9.25	12.54	13.21	13.84	20.69	22.98	23.65	21.23
Channel: 9	10.43	11.30	9.40	8.13	9.30	7.19	8.38	8.33	8.15	11.48
Channel: 10	7.85	5.67	6.33	6.52	5.84	6.16	7.65	9.17	8.64	11.31
Channel: 11	6.43	6.44	7.33	7.54	6.64	6.34	10.09	11.52	14.37	23.12
Channel: 12	7.46	7.00	7.62	6.35	8.83	7.75	8.96	8.58	10.68	10.25
Channel: 13	7.15	8.02	11.25	9.75	11.69	12.26	11.76	10.00	9.48	8.94
Channel: 14	8.28	6.28	6.87	8.67	8.89	7.22	9.66	12.59	14.31	18.41
Channel: 15	8.33	8.28	7.99	9.73	10.48	7.01	9.53	10.02	11.83	15.15
Channel: 16	5.75	7.38	7.03	6.29	7.44	6.62	6.14	6.66	5.61	7.90
Channel: 17	11.08	11.47	11.92	10.30	12.34	10.47	11.28	10.78	8.74	10.84
Channel: 18	5.74	5.95		6.98	6.14	7.98	6.66	8.24	6.51	9.27
Channel: 19	13.32	13.38	10.74	16.17	16.10	15.55	18.74	18.74	20.73	18.62
Channel: 20	7.29	8.65		8.04	7.84	7.98	11.07	11.73	14.04	21.39
Channel: 21	7.44	5.59	6.68	8.92	7.76	6.29	8.13	9.36	7.91	10.11
Channel: 22	13.74	14.82	12.43	15.13	14.86	13.88	13.84	15.11	16.03	15.44
Channel: 23	6.04	5.79		8.55	4.91	6.49	7.32	7.64	9.08	9.30
Channel: 24	8.97	9.42	8.53	9.19	7.50	7.85	8.99	9.17	8.10	8.94
Median	7.55	7.64	7.47	8.12	7.63	7.55	9.05	9.68	9.49	11.39
Overall Mean	8.21	8.23		8.79	8.89	8.80	10.32	11.00	11.78	13.83
Good Mean	8.21	8.23	7.97	8.17	8.24	8.12	8.88	9.31	9.63	9.86
MP Reqd					15					
Yield	1.00	1.00		0.92	0.92		0.88	0.83	0.79	0.58
# Good Ch.	24	24		22	22	22	21	20	19	14
# Bad Ch.	0	0	0	2	2	2	3	4	5	10

JFET_Mod17_brd41_Noise_perf.xls

Attachment of HRCR Item #8: Test Data - Source Voltage & Noise

	Pwr12	Pwr2	Pwr3	Pwr4	Pwr1	Pwr10	Pwr5	Pwr8	Pwr13	Pwr11	Pwr7	Pwr5b	Pwr9
Vdd (V)	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8
Vss (V)	-1.7	-1.6	-1.55	-1.52	-1.5	-1.5	-1.45	-1.42	-1.41	-1.41	-1.4		-1.3
Vdd' (V)	2.532	2.543	2.548	2.541	2.554	2.553	2.558	2.562	2.563	2.563	2.564	2.569	2.574
Vss' (V)	-1.438	-1.35	-1.305	-1.278	-1.26	-1.26	-1.212	-1.19	-1.181	-1.181	-1.172	-1.127	-1.083
Idd (mA)	1.0289	0.986	0.964	0.951	0.9421	0.9423	0.9207	0.9074	0.9036	0.9032	0.8988		0.8548
Iss (mA)	0.9938	0.951	0.9291	0.9161	0.9073	0.9075	0.886	0.8728	0.8689	0.8686	0.8642	0.8422	0.8205
I (mA)	1.01135	0.9685	0.94655	0.93355	0.9247	0.9249	0.90335	0.8901	0.88625	0.8859	0.8815		0.83765
P (mW)	4.01506	3.7703705	3.64705715	3.56522745	3.5268058	3.5266437	3.4056295	3.3396552	3.31812	3.3168096	3.293284	3.1765272	3.06328605
	-6	-6	-6	-6	-14	-12	-6	-8	-6	-6	-6	-6	-8
Channel Num	Vn @150 H			Vn @150 Hz		Vn @150 Hz			_	Vn @150 Hz	Vn @150 Hz		Vn @150 Hz
Channel: 1	7.25	6.29	6.26	5.43	6.49	5.64	6.82	6.30	6.57	7.30	7.26		6.39
Channel: 2	7.05	8.01	8.80	7.89	10.55	9.06	11.49	13.56	12.99	13.56	14.33		22.13
Channel: 3	8.43	7.03	5.75	9.71	8.09	10.66	11.26		11.43	11.31	13.82		19.65
Channel: 4	7.12	6.99	6.59	7.16	7.67	9.14	13.39		12.75	12.43	12.00		25.75
Channel: 5	7.20	7.41	8.13	7.57	6.25	7.18	7.19	7.22	7.34	7.71	6.94		9.26
Channel: 6	6.58	6.49	7.77	8.16	7.14	9.12	8.75	9.13	7.46	8.46	8.36		11.00
Channel: 7	8.48	8.05	7.52	7.27	7.10	7.92	8.06	7.24	7.52	8.16	8.89		10.18
Channel: 8	7.20	8.31	8.56	6.94	7.18	6.97	6.42	7.09	7.49	7.26	7.28		8.07
Channel: 9	8.20	6.56	7.00	6.42	6.99	6.55	7.21	5.13	6.90	6.09	6.72		6.47
Channel: 10	6.25	6.68	8.23	8.24	8.72	9.27	11.20	11.27	11.64	12.27	12.82		18.32
Channel: 11	7.42	7.03	7.21	7.86	7.71	7.66	9.41	11.38	9.89	10.06	10.28		17.38
Channel: 12	6.65	7.79	7.04	6.94	7.79	7.62	8.51	10.66	8.10	10.02	9.40		14.37
Channel: 13	8.87	7.45	8.51	7.49	7.60	8.12	8.13	9.39	7.97	9.25	7.64		13.82
Channel: 14	8.23	9.28	8.21	7.02	7.30	6.48	7.33	8.19	6.55	18.74	7.91		12.23
Channel: 15	8.67	7.64	10.25	9.99	9.31	9.98	10.03	9.11	9.22	8.83	9.93		10.58
Channel: 16	7.24	7.49	7.03	5.88	6.68	7.73	6.31	7.35	7.19	10.19	8.03		11.00
Channel: 17	7.96	10.37	13.01	16.15	18.58	19.31	24.10	29.70	33.71	35.15	33.03	47.31	49.04
Channel: 18	6.72	6.37	6.66	7.48	6.17	7.18	6.33	6.32	7.82	9.84	8.00		10.67
Channel: 19	12.99	11.75	7.54	10.77	8.98	10.76	12.58	14.58	16.39	18.96	15.59		28.48
Channel: 20	8.83	12.14	17.00	18.36	21.20	18.27	21.51	19.01	21.52	23.13	22.00		22.50
Channel: 21	6.85	6.91	8.55	10.45	34.31	9.81	10.49	14.18	15.55	15.22	15.38		22.95
Channel: 22	11.79	14.31	13.72	15.19	13.36	15.62	15.25	17.96	17.04	16.42	18.62		25.98
Channel: 23	6.98	8.61	8.46	11.91	9.57	9.52	13.52	14.00	12.97	14.73	17.50		25.89
Channel: 24	10.51	11.21	10.83	10.87	14.31	10.75	10.62	11.76	11.92	12.11	12.22		11.01
Median	7.34	7.56	8.17	7.87	7.75	9.09	9.72	10.47	9.56	10.75			14.09
Overall Mean	8.06	8.34	8.69	9.21	10.38	9.60	10.66	11.36	11.58	12.80			17.21
Good Mean	8.06	8.34	8.33	8.16	8.33	8.43	9.29		9.14	9.98	9.55	8.96	10.39
MP Reqd							15		0.55				0.00
Yield	0.00	0.00	0.00		0.00	0.00	0.00		0.00	0.00			0.00
# Good Ch.	0	0	0	0	0	0	0	0	0	0	-	_	0
# Bad Ch.	24	24	24	24	24	24	24	24	24	24	24	24	24

JFET_Mod17_brd43_Noise_perf.xls

Attachment of HRCR Item # 9: SPIRE MIUL Cover Page

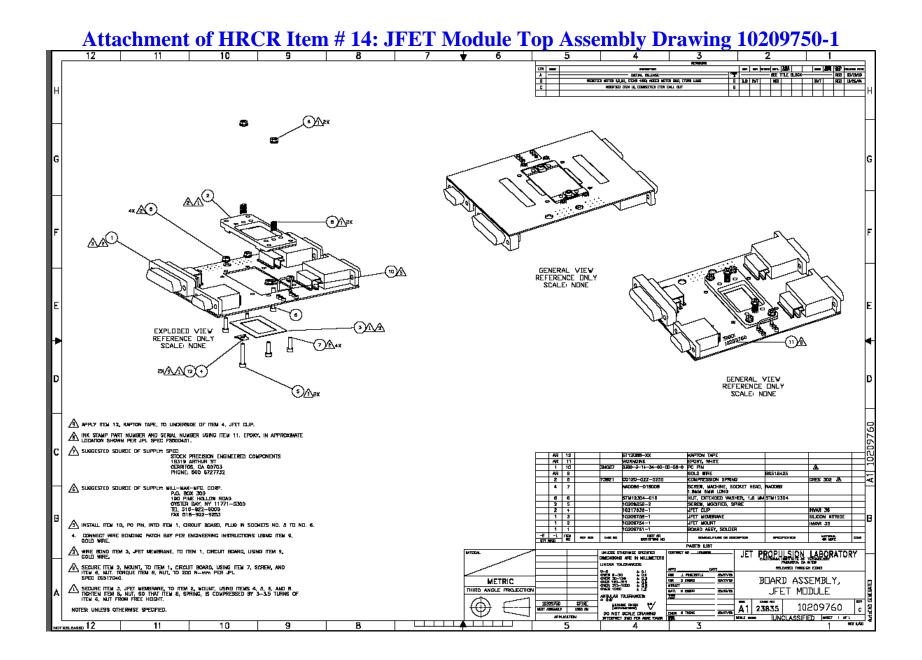
MIUL = Material Identification & Utilization List

Declared Materials List's and Processes List are not included in this HRCR

Materials and Processes List
SPIRE
JPL D-25725
REV B 1/05/04
S .
This technical data is export controlled under U.S. law and is being transferred by JPL to ESA for use exclusively on the Herschel/Planck projects. The information may not be used for any other purposes, and shall not be re-transferred or disclosed to any other party without the prior written approval of NASA.
Reviewed by: M. Knopp M&P Engineer

Attachment of HRCR Item #11:

See End of This HRCR Package for "JFET Module Handling Document"



Page 17 of 29

Attachment of HRCR Item #23: Qualification Compliance Test

Qualification Model JFET Module

Coverbage	HOT ILL	LOSTINA
COTTINGUE		I Carulla

		EID	P Coverpage	FOR JEEL 16	sung	ļ		
Unit Identfication								
Name	:	JFET Q	M Module					
Part #	:	1020	9 750-1					
S/N	:	#I	0 01					
Emissesses tel Testino								
Environmemtal Testing	_	-						
		Axes		Duration/# of		6		
	\vdash	Tested	Temperature	Cycle	Requirement	Source SSSD.	Waiver	
Random Vibration Test		X, Y. Z	100 K	2 min/axis	x v z	JFET-DES-C7		
Railbolli Vibration Tes.	\vdash	A, r. Z	100 K	2111111/4315	Λ, 1, 4	SSSD.	HR-SP-JP	
High Level Sine Vibe Test		None	NA NA	NA NA	X, Y, Z	JFET-DES-07	RFW_005	
Bakeout	T	NA.	80 C	72 Hours	90C, 72 Hrs	D-20549		
Thermal Cycles	\vdash	NA.	RmT to 90 K	27	Minimum 15	D-20549	1	
Performance Characteristics								
	┖		Specif	ication	S	ource	Waiver	
Power needed for <11 bad			11 mW f	or CQM,	s	SSD.	RFW in	
channels (Min Perf.)		9.1 mW	7 mW for	PFM/FS	JFET-TEC-0	5, JFET-PER-02	process	
Power needed for <4 bad	Г		11 mW f	or CQM,	S	SSD.		
channels (Design Value)	┖	10.8 mW	7 mW for	PFM/FS	JFET-TEC-0			
Power needed for 100 %								
Yield per unit	╙	13.5 mW		A				
Median Noise at < 11 bad chs.	╙	7.13 nV/rtHz	<15 nV/rtHz		SSSD, J			
Median Noise at < 4 bad chs.	┖	8.1 nV/rtHz	Min	<7 nV/rtHz		FET-PER-01		
Median Noise at 100 % Yield.	┖	6.97 nV/rtHz		Design Value	SSSD, J	FET-PER-01		
# of Channels over the			< 15 mV for C0			SSSD.		
max. offset voltage	╙	0	< 15 mV for PF		BDA-DRCJ-27			
S No do Boissána Bair						SSSD. BDA-DRCJ-11		
Common Mode Rejection Ratio		< -60 dB by d	esign, as meas	ured in EM4 un	rt	BDA-DRCJ-11		
Board Level Detail	_					_		
<u></u>	⊢		I SN 001			Source		
# Channels Tested	1:	24						
Madia Naisa a S F add	ļ		UI-III-	1		SSSD,		
Median Noise at 3.5 mW	1:	18 n	/V/rtHz			JFET-PER-01 SSSD.		
# of good channels at 3.5 mW	[.	7	29% Yield	I		JFET-PER-02		
Power Needed for	÷	,	2870 11810	 		SSSD,	+	
100 % Yield		6.75 mW		I		JFET-PER-02		
Median Noise at High Power (w/	Ė	3.13 11 14	-			SSSD,	1	
100 % Yield)		6.97	nV/rtHz	1		JFET-PER-01		
Median Gain at High Power	Т	0	.98.			NA		
_	Γ							
	Γ			•				
Definitions	Г							
Good Channels	:	No se less than	ı ı a min. performar	nce value of 15 n\	//rtHz			
Yield	:	≖ of Good Chai						
Filenames	T							
Noise Measurements	:	QualJFETPost	u VibeNoise Summ	arv.pdf				
	Ė							
Notes	T							
The Base temperature for a performa	ITCE	characterization	nwas 4K					
All Noise Measurements were made v							1	
	Π							

Attachment of HRCR Item # 24 & #25: Mate/Demate & Operation Logs

Date	Time	AIDS	Power	Mate	Demate	Transport	Notes
1-Apr	8:00 AM	245138				х	103 -> 183
1-Apr	9:00 AM	245138		х			Mate All Connectors
1-Apr	10:00 AM	245138					Measure all resistances
1-Apr	1:00 PM	245138	Х				30 min each board, warm S.V. test (green dewar)
12-Apr	8:00 AM	245138					Assemble into CSF
13-Apr	7:30 AM	245138			х		Remove all shorting connectors, close out CSF
15-Apr	8:00 AM	245138				х	183->144
15-Apr	9:00 AM	245138					Pump out
15-Apr	9:30 AM	245138					Run 3-axis warm shake
15-Apr	2:00 PM	245138				Х	144->183
16-Apr	8:00 AM	245138		Х			Install shorting connectors
16-Apr	9:00 AM	245138				Х	Remove JFETs from CSF
18-Apr	9:00 AM	245138		Х			Install into blue dewar
18-Apr	10:00 AM	245138	х				Take source voltage measurements
18-Apr	11:00 AM	245138			х		Remove from blue dewar, store in flight cabinet
20-May	8:00 AM	245396		х			Install into green dewar
20-May	9:00 AM	245396					Pump out
20-May	10:00 AM	245396	Х				30 min each board, warm S.V. test (green dewar)
23-May	1:00 PM	245396					Transfer LN2
23-May	8:00 PM	245396					Transfer Helium
24-May	8:00 AM	245396	х				30 min each board, cold S.V. test (green dewar)
24-May	10:00 AM	245396	х				8 hours, board 40 noise
24-May	6:00 PM	245396	х				3 hours, board 45 noise
25-May	8:00 AM	245396	Х				6 hours, board 45 noise
25-May	2:00 PM	245396	х				6 hours, board 41 noise
26-May	8:00 AM	245396	х				10 hours, board 43 noise
27-May	8:00 AM	245396					warm dewar
31-May	8:00 AM	245396					pump out
31-May	9:00 AM	245396	Х				30 min each board, warm S.V. test (green dewar)
31-May	1:00 PM	245396					cool dewar
1-Jun	8:00 AM	245396	х				30 min each board, cold S.V. test (green dewar)
2-Jun	10:00 AM	245396					2 hours, board 40, gain and CMRR
2-Jun	12:00 PM	245396					2 hours, baord 45, gain and CMRR
2-Jun	2:00 PM	245396	х				2 hours, board 41, gain and CMRR
2-Jun	4:00 PM	245396					2 hours, board 43, gain and CMRR
3-Jun	8:00 AM	245396					8 hours, board 43 noise
3-Jun	6:00 PM	245396					warm dewar
6-Jun	8:00 AM	245396					30 min each board, warm S.V. test (green dewar)
6-Jun	1:00 PM	245396			х	х	Demate, Transport 183->103
		3.2220			7.		

Attachment of HRCR Item # 24 & #25: Mate/Demate & Operation Logs (continued)

OPERATION LOG SHEET -- SPIRE JFET BOARDS MODULE USE THE "NOTE" COLUMN TO DESCRIBE ACTIONS DEVICE (BRD) S/N: 04 (55) PROJECT: SPIRE/JFET BOARD PWR PWR MATE DEMATE DATE TIME **TECH** NOTE ON OFF JAA JBB JCC JDD JAA JBB JCC JDD TRANSFORT 11-D1-04 9:30AM 103199 V V SAVERS INSTALLED 11-18-04 103199 END9 CHASER 11 12-10-4 7:00 PM 103799 -GND5 CHASSIS " 12-10-04 1:00 PM 103199 SOURCE TEST " 2-9-05 103199 AND & CHASSIS " -2-9-05 103199 V -V SOURCE TEST " -3-21-05 11:00 103199 V V V GND & CHASEIS -V 3-21-05 11:00 103199 V V V V GOUPLE TEST 3/24-05 ST GND & CHASSI V V r v 3/24-05 ST V v V r V V SOURCE TEST 3-28-05 GND & CATASSIS ~ ~ V v 3-28-5 V V v SOUPLE v 6-17-01 NÃU V SHPTP45 STURRO SOURCES, T

NOTE: CONNECTORS ARE RE-USE. FROM 4384 # 10209761-1 SIN 045, MDS # 240895, 18# 923860 WEN 10-5-04

Attachment of HRCR Items # 24 & # 25: Mate/Demate & Operation Logs

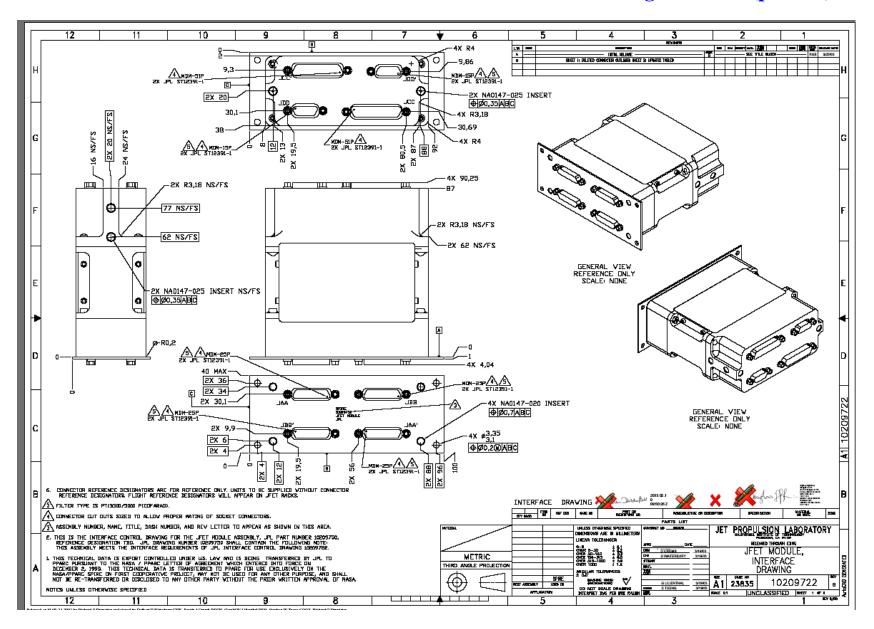
OPERATION LOG SHEET -- SPIRE JFET BOARDS MODULE

USE THE "NOTE" COLUMN	TO DESCRIBE ACTIONS
-----------------------	---------------------

DATE	TIME	TECH	PWR	PWR		MA					IATE			NOTE
100000000000000000000000000000000000000			ON	OFF			JCC	JDD	JAA	JBB	JCC	JDD	TRANSFORT	NAME OF THE PARTY
1-01-04	9:30AM				V	~	V	r	_	-	-	-		SAVERS INSTALLED V
1-23-04	of distry	103199			-	_	1	-	-	_	-	1		GND & CHHSENS TEST U
2-10-04	7:00 AM	103199			-	_	-	-	-	_	_	-		GND9 CHASSIS TEST "
2-10-04	1000 AM	103199	1		-	-	-	-	-	-	_	-		SOURCE TEST
-9-05		103199			-	-	-	-	-	-	-	-		and a charsis "
-9-05		103249	V		-			-	-	-	-	-		STUPLE TEST
122/05		103199	-		-	-	-	-	-	-	-	-		GND & CHISSES
122/05		103199.	V	v	-	-	-	_	_	-	-	-		Source TEST ".
123/05		103199	-		-	-	-	-	-	-	-	-		GND & CHASSIS"
123/05		103199	L	v	-	,	-	-	-		-	-		SOURCE "
-24-05		ST												OND & CHASEIS
-24-05		ST	V	L										SOURCE TEST
-28-05		ST ST										6		GND & COTASSES
-28-05			V	c										SOUPCE TEST
-19-05		NAN	V	U	V	V	V	V					SHOPTING. P.C	SAVER ON SOURCE TE
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NOTE: CONDECTOR ARE RE USE. FROM ASSY # 10209761-1 S/N: 023, A103# 240873, 18#923860 NOW 1/2565

Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 1 of 2)



Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 2 of 2)

l —	12 11	10 9	8		6		5	4	3	2	1
	JAA JEET DUTPUT 139	JAA' JEET DUTPUT ZA		JCC JFET INPUT 1			JDD JFET SERVICE 1		JCC' JFET INPUT 2		
11	PIN # PIN PURPOSE	PIN # PIN PURPLISE	PIN			PIN #			PIN # PIN PURPUSE		l.
H	1 SIGNAL M+	1 SIGNAL H+'	L	BIAS V+	_	1	Vss	_	1 BIAS V+'		Į.
	2 SIGNAL N+	2 SIGNAL N+'	5	BIAS V-	_	2	V+	4	5 BIAS A-1		
	3 SIGNAL P+	3 SIGNAL P+'	3	SIGNAL Y+	→ ⊦	3	H+	4	3 SIGNAL Y+		
H	4 SIGNAL R+	4 SIGNAL R+' 5 SIGNAL S+'	4	SIGNAL V+		4	V- V-	4	4 SIGNAL V-'		
	5 SIGNAL 2+ 6 SIGNAL T+	6 SIGNAL T+1	5	SIGNAL T+	\dashv \vdash	5	H+	4	5 SIGNAL V+' 6 SIGNAL T+'	_	
	7 SIGNAL U-	7 SIGNAL U-1	7	SIGNAL 2-		7	V+	-	7 SIGNAL S-/	_	
G	8 SIGNAL V-	B SIGNAL V-		SIGNAL P+	\dashv \vdash	-	Vss	+	B SIGNAL P+'		l l
-	9 SIGNAL V-	9 SIGNAL W-	9	SIGNAL N-	\dashv \vdash	9	DIAS CAIE	┨	9 SIGNAL N-		ľ
	10 SIGNAL X-	10 SIGNAL X-	10	SIGNAL L-	\dashv	10	Valid	┨	10 SIGNAL L-		
	II SIGNAL Y-	11 SIGNAL Y-'	11	SIGNAL K+	\dashv \vdash	11	H=	1	11 SIGNAL K+		
Н	12 SIGNAL Z-	12 SIGNAL Z-'	12	SIGNAL I-	\dashv \vdash	12	CHASSIS GND	1	12 SIGNAL I-1		
	13 FPU GND	13 FPU GND	13	SIGNAL H+	\dashv \vdash	13	H-	1	13 SIGNAL H+		
	14 SIGNAL M-	14 SIGNAL H-'	14	SIGNAL F+	\neg	14	Volai	1	14 SIGNAL F+'		
F	13 SIGNAL N-	15 SIGNAL N-'	15	SIGNAL E-			BIAS GND ZAIE]	15 SIGNAL E-		
	16 SIGNAL P-	16 SIGNAL P-'	16	SIGNAL C+			•	1	16 SIGNAL C+*		[
	17 SIGNAL R-	17 SIGNAL R-'	17	SIGNAL B-	┚┡		JODY JEET SERVICE 2	4	17 SIGNAL B-		
	10 SIGNAL S-	18 SIGNAL S-'	18	SIGNAL A-		PIN #		4	18 SIGNAL A-		ļ
Н	19 SIGNAL T-	19 SIGNAL T-'	19	BIAS GND		1	Vss'	4	19 BIAS GND'		
	20 SIGNAL U+	20 SIGNAL U+'	20	SIGNAL Z+		2	V+'	4	20 SIGNAL Z+'		
	21 SIGNAL V+	21 SIGNAL V+'	21	SIGNAL X-		3	H+'	4	21 SIGNAL X-		
F	22 SIGNAL W+	22 SIGNAL V+'	22			5	V-'	4	22 SIGNAL W+'		li li
-	23 SIGNAL X+	23 SIGNAL X+'	23	SIGNAL U-		6	H+'	4	23 SIGNAL U-		[
	24 SIGNAL Y+	24 SIGNAL Y+'	24	SIGNAL T-		7	A+,	4	24 SIGNAL T-		
	25 SIGNAL Z+	25 SIGNAL Z+'	25	SIGNAL R+	— ⊦	-	Vss'	+	25 SIGNAL R+'		
	JEE JEET DUTPUT 1A	JEB JEET DUTPUT 20	26	SIGNAL P-	— ⊦	9	SIAS GND	+	26 SIGNAL P-		†
	PIN # PIN PLRPUSE	PIN # PIN PURPLISE	27	SIGNAL M+		10	Vald'	+	27 SIGNAL M+'		
	1 SIGNAL A+	1 SIGNAL A+1	28	SIGNAL L+	—	11	H-'	┨	28 SIGNAL L+'		
ln l	2 SIGNAL B+	2 SIGNAL II+'	29	SIGNAL J-	—	12	CHASSIS GND'	┨	29 \$1GNAL J-		l,
	3 SIGNAL C+	3 SIGNAL C+1	30	SIGNAL I+	—	13	H-'	1	31 SIGNAL I+' 21 SIGNAL G-'		
	4 SIGNAL D+	4 SIGNAL II+'	31	SIGNAL G-	—	14	Vokal'	1	32 SIGNAL G-		
	5 SIGNAL E+	5 SIGNAL E+1	323	SIGNAL I+	—		BIAS GND	1	32 SIGNAL F-/	_	
П	6 SIGNAL F+	6 SIGNAL F+'	34	SIGNAL C-	— '			_	34 SIGNAL DP	_	,
	7 SIGNAL G-	7 SIGNAL G-'	36		_				35 SIGNAL A+/		
	6 SIGNAL H-	B SIGNAL H-'	36		-				36 SIGNAL Z-/		ľ
	9 SIGNAL I-	9 SIGNAL 1-'	37	SIGNAL Y-	\dashv				37 SIGNAL Y-		
	10 SIGNAL J-	10 ZIGNAL J-'	36	SIGNAL X+	_				38 SIGNAL X+	_	ļ
	II SIENAL K-	11 SIGNAL K-'	39	SIGNAL V-	_				39 SIGNAL V-'		
	12 SIGNAL L-	12 SIGNAL L-'	4D		\neg				4D SIGNAL U+	\neg	
П	13 FPU GND	13 FPU GND	41	SIGNAL S+	\neg				41 SIGNAL S+	\neg	Ī
	14 SIGNAL A-	14 SIGNAL A-	42						42 SIGNAL R-		
	15 SIGNAL B-	15 SIGNAL B-'	43	SIGNAL N+					43 \$1GNAL N+*	\neg	
B	16 SIGNAL C-	16 SIGNAL C-'	44	SIGNAL M-					44 SIGNAL M-		
	17 SIGNAL D-	17 SIGNAL II-'	45	SIGNAL K-					43 SIGNAL K-		
	18 SIGNAL E-	18 SIGNAL E-'	46	SIGNAL J+					46 SIGNAL J+'		
	19 SIGNAL F-	19 SIGNAL F-'	47	SIGNAL H-					47 SIGNAL H-		Ļ
П	20 SIGNAL G+	20 SIGNAL G+'	48	SIGNAL G+					4B SIGNAL G+		
	21 SIGNAL H+	21 SIGNAL H+'	49	SIGNAL E+					49 SIGNAL E+		
	22 SIGNAL I+	22 SIGNAL 1+'	50						50 SIGNAL D-		
A	23 SIGNAL J+	23 SIGNAL J+'	51	SIGNAL B+					51 SIGNAL B+		
	24 SIGNAL K+	24 SIGNAL K+1							97.	FAE HP	10200722
$1 \mid$	25 SIGNAL L+	25 SIGNAL L+'							<u>A1</u>	23835	10209722 B
1 –	12 11	10 9	8			_	5	4	3 BAZ H	- JUNCL	SSIFED HETE FI
	14	10 9	0				j j	4	1 3		1 -

Attachment of HRCR Item #11:

JFET Module Handling Document D-26790

Field Effect Transistor (JFET) Module 10209750-1

Prepared by: Kalyani Sukhatme 10 September, 2003

Revised by: Roger Welker & Steve Tseng 15 June, 2005

D-26790

1. Introduction

This document provides guidelines for electrical handling for the SPIRE JFET Module.

1.1 Hardware Description

Each JFET module has two sets of 24 JFET channels. The JFET channels are populated on 1.0 micron thick Silicon Nitride membranes which provides thermal isolation. The operating temperature for these JFETs is ~120 K. The process of powering up the JFETs dissipates heat into the membrane resulting in a temperature increase with respect to the base temperature (4K to 10 K). Higher the power dissipation, higher is the temperature of the JFETs.

Each JFET channel consists of a matched pair of FETs (Figure 1.1-1) with a requirement for the offset voltage of less than **15 mV** between the matched pair. [The characteristic offset voltage is the difference between the source voltages $(V_{sa} \text{ and } V_{sb} \text{ with respect to ground})$ of the two FETs.]

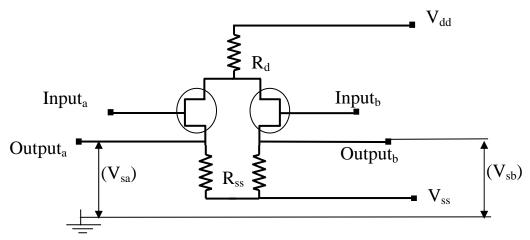


Figure 1.1-1

The Gates of the JFETs are the 'Inputs' of the circuit and the Sources (V_{sa} and V_{sb}) of the JFETs are the outputs, as marked in Figure 1.1-1. Vdd and Vss are the power lines for the circuit.

2. Handling

1. **The JFET Module is Contamination Sensitive**: Open shipment suitcase in an ISO 14644 Class 7 (FED-STD-209 Class 10,000) or cleaner cleanroom. Handle hardware with approved nitrile or polyurethane ESD safe cleanroom gloves.

D-26790

Nitrile:

Ansell-Edmont Nitrilite http://www.ansellpro.com/ce/products3.asp?pid=87
Ansell-Edmont Nitrilite Silky http://www.ansellpro.com/ce/products3.asp?pid=149
http://www.ansellpro.com/ce/products3.asp?pid=87
http://www.ansellpro.com/ce/products3.asp?pid=149
http://www.ansellpro.com/ce/products3.asp?pid=150

Safeskin Critical (white) http://www.safeskin.com/crit_nt_glv.asp

Polyurethane:

Wilshire Technology DuraCLEAN call in US, 323-259-6469 for ordering information

¹ JPL approved ESD safe cleanroom gloves are:

2. The JFET Module is ESD Sensitive:

Please handle with appropriate ESD hardware handling procedures. Handle with grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.

ESD: Handle with approved² wrist straps, ESD-safe gloves and ESD smocks at an approved ESD protected workstation³. All personnel within 1 meter of unprotected ESD sensitive hardware shall be certified for ESD awareness⁴. Maintain shorting plugs on the unit at all times, except when the unit is installed in the final assembly of the SPIRE instrument. JFET modules are shipped with two shorting plugs for ESD protection. Refer to attached electrical handling document for other important safety precautions. Follow all instructions for the use of wrist straps, ESD smocks, static protected work areas, ionizers, packing/unpacking and cable handling per JPL standard D-1348, rev. F (This document is available through the public domain by the following URL: http://acquisition.jpl.nasa.gov/rfp/miri/dewar/DL-2671-584331/JPL D-1348.pdf).

ESD - Ionizer: Prior to mate or demate of any connector, turn on an ionizer approved⁵ for ESD sensitive components in clean room environment at least 5 minutes in advance and place/hold both sides of the connections in front of the ionized air stream for a minimum of 10 seconds before mating/demating operation. Position the ionizer near the hardware within the required distance per manufacturer's manual. Different makes and models of ionizers have different positioning requirements. During the mating/demating operations, it is necessary to follow the requirements for handling ESD sensitive hardware.

ESD - Connection to GSE: It is essential to ensure that all signal and bias lines of the GSE are grounded prior to mating the JFET hardware to the GSE. A save-to-mate check must be performed prior to connecting the JFET to the GSE. No excessive voltages and currents on all signal and bias lines shall be observed while the hardware is connected.

QA Oversight: Quality Assurance personnel should witness all handling, electrical testing, operation and integration of JFET flight hardware. At a minimum, a "two person" rule should be invoked at all times, where oversight by an independent party is provided to ensure hardware safety during handling, test and integration operations.

Humidity Sensitive: Place hardware in a humidity controlled ISO 14644 Class 7 (FED-STD 209 Class 10,000) cleanroom. Maintain humidity level at 35%-50% RH typical, for ESD safety.

3. **The JFET Module is Fragile**: Please do not drop or otherwise shock the unit including the shipping suitcase and container. Do not remove the cover of the JFET Module.

Speidel Twist-o-Flex TM brand metal expansion bracelet wrist straps 3M model 4600 adjustable molded thermoplastic wrist straps

² JPL approved wrist straps are:

³ All work areas shall be certified and operated in compliance with the requirements of the following subsections sections of JPL-STD D-1348 rev. F section 2.3: subsections: 6, 8-11, 14-19, 21, 23 – 27, 29 – 36, 38 – 43 and 45.

⁴ All personnel shall be trained and certified to the requirements of section 2.3.3 of JPL STD D-1348 rev. F.

⁵ The ionizer performance shall be verified to comply with the requirements of JPL-STD-D-1348 rev. F, Table 1 for devices with human body model ESD sensitivity less than 50 volts. The ionizer shall discharge from \pm 1000 volts to less than \pm 20 volts in less than 20 seconds and have a float potential of less than \pm 20 volts.

3. Power ON Procedure

D-26790

- 1. The JFET Module should be powered on **WITH the shorting plugs** (JPL Supplied Protection connectors) in place and with the **inputs shorted to ground.** Pins #9 and #15 on the 15-pin MDM connectors on the JFET Module are the bias grounds on the module. These pins should also be shorted to the power supply ground. The unit may be powered up without the shorting plug only when the inputs are connected to the detector system.
 - Under no circumstances the unit should be powered up without the inputs shorted to ground either via the shorting plug (JPL Supplied) or via the detector system.
- 2. Do not exceed a voltage of +5 V for the Vdd line and -5 V for the Vss line of the JFET Module.
- 3. When removing the shorting plugs from the unit for installation into the instrument, please use standard ESD precautions including grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.

4. Electrical Check-out Test: Characteristic Offset Voltage Measurement

- 1) Verify that the gates of the JFET channels (Inputs) are shorted together and grounded.
- 2) Apply the power supply ground to the bias ground pins on the unit (Pins 9 and 15 on the 15-pin MDM connectors)
- 3) Power on the JFET modules with Vdd = +3 V and Vss = -1.5 V
- 4) Verify that the handheld multimeter is in calibration.
- 5) Connect one side of the handheld multimeter to ground (Power supply ground).
- 6) And measure the voltage with respect to ground of each side (V_{sa} and V_{sb}) of each channel.
- 7) Calculate the characteristic offset voltage (V_{offset}) for each channel ($V_{offset} = V_{sa} V_{sb}$)
- 8) Compare the values for each of the channels with the specific datasheet provided with the unit. The datasheets accompanying the unit also provides the values for the drain and source currents for a similar test performed at JPL.

REFER TO MEASURED SOURCE VOLTAGE DATA FOR ACTUAL HARDWARE. Here is an example of the source voltage values and the drain and the source currents obtained for such a test at room temperature are given in the Table 4-1

	rm T
	3 V
	-1.5 V
1	.564 mA
1.	5686 mA
(V)	DELTA (V)
1.130	0
1.130	O
1.075	0.001
1.074	0.001
0.781	0.001
0.780	0.001
1.088	0.005
1.093	0.005
0.834	0.001
	(V) 1.130 1.130 1.075 1.074 0.781 0.780 1.088 1.093

1	0.833	
	1.012	
6	1.015	0.003
7	0.785	0.002
/	0.787	0.002
8	1.148	0.004
0	1.144	0.004
9	0.753	0
9	0.753	U
10	0.693	0.008
10	0.701	0.000
11	1.110	0.004
11	1.114	0.004
12	0.758	0.001
12	0.759	0.001
13	0.832	0.002
13	0.830	0.002
14	1.264	0.001
17	1.265	0.001
15	1.206	0
13	1.206	U
16	0.818	0.001
10	0.819	0.001
17	0.526	0.005
17	0.521	0.000
18	1.423	0
10	1.423	U
19	0.773	0.002
17	0.775	0.002
20	0.873	0.004
20	0.877	0.004
21	1.387	0.006
21	1.393	0.000
22	1.417	0.003
52	1.420	0.000
23	0.887	0.002
23	0.889	0.002
24	0.888	0.003
24	0.891	0.000

- END OF Attachment of HRCR Item # 11:
"JFET Module Handling Document D-26790"

END OF

HRCR PACKAGE