JPL Hardware Requirements Certification Review – SPIRE Element No. D-32238

Assembly / Subsystem		PEM	Phone		Section		Date
SPIRE		Martin Herman	(818) 354-8541		385		17 June, 2005
Drawing/ Part No.	Dwg. Rev.	Nomenclature	Serial No.	Model	Type	Final IR No.	Mass (Meas. / Req.)
10209750-1	B	JFET Module	016	FLT-Spare	N/A	926198	273.4 gm / 305 gm

Check applicable answer and provide explanation in remarks column	YES	NO	NA	Remarks	Data Attachments	Signature & Date
1. Are all drawings and specifications complete, approved, released and frozen?	X				14. Latest Top Assembly drawings ☒ Attached ☐ None	Cognizant Engineer Steve Tsang 6/17/05
2. Do the released drawings and specifications reflect all approved changes?	X				15. List of open ECRs ☐ Attached ☒ None	PEM 6/17/05
3. Is hardware identical to other hardware delivered? If no, provide difference list.	X				16. Waivers (RFW request for waiver) ☒ Attached ☐ None	QA Engineer 6-17-05
4. Does the hardware meet its functional requirements, specifications, waivers, ICDs?	X			EIDP attached. Also see item # 8 attachments.	17. Open MRB ☐ Attached ☒ None	Environments/Reliability
5. Are all IR and MRB dispositioned and concurred by QA?	X				18. Open PFR on this H/W ☐ Attached ☒ None	Mission Assurance Mgr. 6/17/05
6. Is complete as-built list information included in the build book?	X				19. Open PFR on similar H/W ☐ Attached ☒ None	Project Office
7. Have all required environmental tests & analyses been completed?	X			ETAS attached	20. Handling Document → See Item 11 ☒ Attached ☐ None	PI James J. Bock 6/17/05
8. Is all required assembly and/or subsystem level functional testing complete?	X			Performance Test Data Attached. Also see EIDP in item # 4.	21. Shortage List ☐ Attached ☒ None	
9. Have all piece parts, processes and materials been approved by JPL?	X				22. Requirements Verification Matrix ☒ Attached (See #4, #7, #8) ☐ None	
10. Does this hardware meet all contamination control requirements?	X			Parts, processes and MIUL met all contamination control and out-gassing requirements.	23. Qualification Status ☒ Attached ☐ None	
11. Are all shipping containers, shipping and special handling procedures ready?	X			See Attached Document D-26790	24. Mate / Demate Record ☒ Attached ☐ None	
12. Is additional work required to bring this hardware to flight (flight-spare) readiness?		X			25. Operating Log ☒ Attached (See Item # 24) ☐ None	
13. Is this hardware acceptable for flight?	X				26. MICD ☒ Attached ☐ None	


PWR BOARD 040
SPIRE
10209750
JFET MODULE
S/N016

RAL EIDP Table of Contents Versus JPL HRCR Check List Item Numbers

RAL EIDP Section Number	RAL EIDP Title	JPL HRCR Check List Item Number	Notes
1	Shipping Documents		Shipper and Final IR
2	Transportation, Packing, Handling & Integration Procedures	11	Special Handling Document D-26790
3	Certificate of Conformance / Delivery Review Board MOM		HRCR book is the C of C
4	As Built Configuration Status List	1 & 2	Assembly Drawings
5	List of Waivers	4	RFW (request for waiver) Attached
6	Copies of Waivers	4 & 7	RFW (request for waiver) Attached
7	List of Non-Conformance Reports		See RFW in 4 & 7
8	Copies of Non-Conformance Reports		See RFW in 4 & 7
9	Cleanliness Statement		Final IR QA Inspection
10	Operational Manual		NA
11	Top Level Drawings (inc. Family Tree)	14	Top Assembly Drawing
12	Interface Drawings	26	MICD Drawing
13	Functional, Block & Mechanical Drawings		NA
14	Electrical Circuit Drawings		NA
15	Serialized Components List		In build books – not shipped
16	Mass Properties/ Power Budget	HRCR Check List Page 1	Mass listed in HRCR check list
17	Qualification Status List / Test Matrix	23	Qualification Unit Test Matrix
18	Test Reports	4, 7, 8, 23	
19	Open Work / Deferred Work / Open Tests		NA
20	Calibration Data		NA
21	Historical Record	23	Qualification Unit Test Matrix
22	Manufacturing Logbook(s)		In build books – not shipped
23	Operating Time / Cycle Record	25	
24	Connector Mating Record	24	
25	Age Sensitive Items Record		NA
26	Pressure Vessels – History/Test Record		NA
27	Temporary Installation Record		NA
28	Reference List of EIDPs (Lower level)		NA
29	Other Useful Information		NA

JPL Hardware Requirements Certification Review (HRCR)

Junction Field Effect Transistor (JFET) Flight Module

10209750-1 S/N 016

SPIRE Element
Herschel Space Observatory Project

June 17, 2005

Configuration of Module, Boards & Membranes

Module 10209750-1	S/N 16	S/N 16
PWB 10209760-1	S/N 040	S/N 045
Membrane 10209758-1	J6.16.3	J6.17.1

Attachment of HRCR Items #1
Drawing Release Status

ALL ASSEMBLY & PARTS DRAWINGS ARE RELEASED IN PDMS

Released Drawings:

10209719-1 assembly built per released Rev. A drawing (studlock)

10209722-1 assembly built per released Rev. B drawing (interface drawing)

10209750-1 assembly built per released Rev. B drawing (module assy)

10209751-1 assembly built per released Rev. B drawing (chassis 1)

10209752-1 assembly built per released Rev. A drawing (chassis 2)

10209753-1 assembly built per released Rev. A drawing (chassis 3)

10209754-1 assembly built per released Rev. C drawing (mount)

10209756-1 assembly built per released Rev. B drawing (chassis lid)

10209757-1 assembly built per released Rev. A drawing (membrane)

10209758-1 assembly built per released Rev. A drawing (membrane assy)

10209759-1,-2,-4 redlined Rev. B drawing (gasket)

10209760-1 assembly built per released Rev. C drawing (board assembly)

10209761-1 assembly built per released Rev. C drawing (solder connector)

10209769-1 assembly built per released Rev. A drawing (stiffener)

10209777-1 assembly built per released Rev. B drawing (board)

10209858-2 assembly built per released Rev. A drawing (special fastener)

10217636-1 assembly built per released Rev. A drawing (clip)

Attachment of HRCR Item #4: EIDP (End Item Data Package)

EIDP Coverpage For JFET Testing

Unit Identfication		
Name	:	JFET PFM Module
Part #	:	10209750-1
S/N	:	#016

Environmemtal Testing	Axes Tested	Temp	Duration/# of Cycle	Requirement	Source	Waiver
Random Vibration Test	X, Y, Z	Rm T	1 min/axis	X, Y, Z	SSSD, JFET-DES-07	
High Level Sine Vibe Test	None	NA	NA	X, Y, Z	SSSD, JFET-DES-07	HR-SP-JPL-RFW-005
Bakeout	NA	80 C	24 hrs	> 24 HRS		
Thermal Cycles	NA	RmT to 80 K	2	Minimum 1	D-20549	

Performance Characteristics		Specification		Source	Waiver
Power needed for <11 bad channels (Min Perf.)	6.33 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	HR-SP-JPL-RFW-004
Power needed for <4 bad channels (Design Value)	6.47 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02	
Power needed for 100 % Yield per unit	7.33 mW	NA		NA	
Median Noise at < 11 bad chs.	10.19 nV/rtHz	<15 nV/rtHz Min Performance	<7 nV/rtHz Design Value	SSSD, JFET-PER-01	
Median Noise at < 4 bad chs.	10.08 nV/rtHz			SSSD, JFET-PER-01	
Median Noise at 100 % Yield.	7.53 nV/rtHz			SSSD, JFET-PER-01	
# of Channels over the max. offset voltage	0	< 15 mV		SSSD, BDA-DRCU-27	
Common Mode Rejection Ratio	< -60 dB by design, as measured in EM4 unit			SSSD, BDA-DRCU-11	

Board Level Details		Board SN 040 (JAA-JDD)		Board SN 045 (JAA'-JDD')		Source
# Channels Tested	:	24		24		
Median Noise at 3.5 mW	:	8.47 nV/rtHz		7.63 nV/rtHz		SSSD, JFET-PER-01
# of good channels at 3.5 mW	:	23	95.8% Yield	24	100% Yield	SSSD, JFET-PER-02
Power Needed for 100 % Yield	:	3.80 mW		3.53 mW		SSSD, JFET-PER-02
Median Noise at High Power (w/ 100 % Yield)		7.21 nV/rtHz		7.63 nV/rtHz		SSSD, JFET-PER-01
Median Gain at High Power		0.98		0.98		NA
Heater Resistance, 4K Reference value	:	3.176 kΩ		3.77 kΩ		NA

Definitions		
Good Channels	:	Noise less than a min. performance value of 15 nV/rtHz
Yield	:	# of Good Channels / 24
Filenames		
Noise Measurements	:	JFET_Mod16_brd40,45_Noise_perf.pdf
Source Voltages (RmT, 4K)	:	JFET Module 16, 17 voltage data, 40,45,41,43 040105.pdf

Notes

1) The Base temperature for all performance characterization was 4K
2) All Noise Measurements were made with the inputs shorted to ground
3) Type of membranes: SN040: 41% Overetched; SN045: 43% Overetched

Attachment of HRCR Item #7: RFW (Request For Waiver)

CCLRC Rutherford Appleton Laboratory	REQUEST FOR WAIVER / DEVIATION (RFW/RFD)	PRODUCT ASSURANCE Space Science and Technology Department

RFW/RFD Number:	HR-SP-JPL-RFW-005v1

Spacecraft / Project	Herschel	**Originator's Name**	Kalyani Sukhatme	
System / Experiment / Model	SPIRE	**Signature / Date**		
Sub-System	detectors	**Request Type** (Highlight applicable request)	Waiver (RFW)	Deviation (RFD)
Assembly		**Organisation**	Jet Propulsion Laboratory	
Sub-Assembly		**Ref. Doc. / Drwg No.**	SPIRE-JPL-PRJ-000456	
Item		**References**		
Serial No.				

RFW/RFD Title	**BDA and JFET module sine test deletion**

End Items(s) Affected (Hardware, Software)		
Name	**CI-Number**	**Model(s)**
Bolometric Detector Assemblies JFET Modules		CQM, PFM, FS CQM, PFM, FS

Requirement / Interface Documents Affected				
Specification/Drawing Title	**Number**	**Issue**	**Date**	**App. Paragraph**
BDA-SSSD (SPIRE-JPL-PRJ-000456)		3.2	Jan 7, 2003	BDA-DES-10, JFET-DES-07

Description of Deviation / Discrepancy / Non-Conformance

High Level Sine- Vibe Test is not performed on these units

Other Items or Requirements (Potentially) Affected

Need for RFW/RFD and Rationale for Acceptance

The hardware has to be qualified under a cold vibration test and is installed in the cold vibration facility for the purpose of the test. The high level sine vibration test configuration will put the hardware and the personnel at risk since the cold vibration facility is not structurally capable of withstanding the high levels. Obtaining additional resources (cost and schedule) for developing a new set-up is not feasible at this time.

Up issue RFW to 5v1 with this note added

There is no Requirement to do a high level sine test on previously Qualified units, Only Random Acceptance level test are required.

	Approved	Rejected	Name	Date
Engineering:	REF SPIRE – RAL-MOM-002250		Digitally signed by Eric Clark Date: 2004.12.22 08:57:49 Z	20 December 04
Product Assurance:				20 December 04
CCB-Chairman:				
Principle Investigator				
Product Assurance:				
Co-Investigator				
Prime Contractor				
ESA Project Office				

Attachment of HRCR Item #7: ETAS (Environmental Test Summary)

ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)

AUTHORIZATION SECTION

PROJECT: Herschel		LOG NO.: HS040	
SYSTEM/ASSEMBLY TITLE: JFET Modules S/N 16,17			DATE ISSUED: 4/12/05
REFERENCE DESIGNATION NUMBER	PART NO. (IF MULTIPLE, ATTACH LIST): 10209750-1	REV.	SERIAL NO.: 016,017

HARDWARE TYPE: ☐ EM QUAL ☒ FLIGHT ☐ FLIGHT SPARE ☐ OTHER — PRE-ENVIRONMENTAL INSPECTION REPORT NUMBER (ATTACH IR)

WIRING HARNESS: ☐ EM QUAL ☐ FLIGHT ☐ EM ☐ SE — PART NO. — REV. — SERIAL NO.

TEST DESCRIPTION (CHECK ALL APPLICABLE): ☐ SINE VIBRATION ☒ RANDOM VIBRATION ☐ PYROSHOCK ☒ THERMAL VAC. ☐ ACOUSTIC ☐ EMC ☐ THERMAL ATMOSPHERE ☐ OTHER _____

TYPE OF TEST: ☐ QUALIFICATION ☒ PROTO FLIGHT ☐ FLIGHT ACCEPTANCE ☐ RETEST

WILL ALL TESTS/LEVES/DURATIONS REQUIRED BY THE PROJECT DOCUMENTS BE PERFORMED ON THIS UNIT?
☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) ENTER PROJ. DOC. NO. AND REV. ____

HAS THE UNIT PASSED ALL PRE-ENVIRONMENTAL FUNCTIONAL TESTS?
☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION

HAVE ALL DESIGN ANALYSES BEEN COMPLETED AND REQUIRED CHANGES BEEN IMPLEMENTED?
☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION

IS THE TEST ARTICLE IDENTICAL TO OTHER FLIGHT UNITS?
☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION

ARE ALL PFRs AGAINST THIS UNIT CLOSED?
☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION

HAVE ALL WAIVERS AND ECRs BEEN APPROVED AND ARE THEY INCORPORATED?
☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST) BRIEF EXPLANATION

TEST AUTHORIZED BY

COGNIZANT ENGINEER	DATE	TECHNICAL MGR./INSTR MRG./PI PREP REP	DATE	ENVIRONMENTAL REQUIREMENTS ENG.	DATE
[signature]	4/13/05	[signature]	4/13/05	[signature]	4/13/05

SUMMARY SECTION

TEST AGENCY (IF MULTIPLE, ATTACH SUMMARY AND TEST DATES)	TEST INITIATION DATE	ACCUMULATED OPERATING HOURS PRIOR TO FIRST ENVIRONMENTAL TEST
JPL Building 144	04/15/05	
SERIAL NUMBERS ACTUALLY TESTED: 016 / 017	TEST TERMINATION DATE	OPERATING HOURS DURING ENVIRONMENTAL EXPOSURE

TEST DESCRIPTION

VIBRATION	ACOUSTIC	PYROSHOCK SHOCK	THERMAL VACUUM	TEMPERATURE ATMOSPHERE	OTHER
AXES: X Y Z		AXES: X Y Z	☒ PRESSURE: <10E-5 <77K		
SINE VIBRATION ☐☐☐			NO OF CYCLES: 2<= # <=3	NO OF CYCLES:	____
RANDOM VIBRATION ☒☒☒	☐	SHOCKS/AXIS:			

EMC ☐ COND. SUSC. ☐ COND. EMIS. ☐ ISOLATION
ESD ☐ RAD. SUSC. ☐ RAD. EMIS. ☐ MAGNETICS

TEMP. LEVEL (°c) AND ACCUMULATED DURATION (HRS.)
HOT: ____°c, ____h COLD: ____°c, ____h
HOT: ____°c, ____h COLD: ____°c, ____h

WERE THERE ANY PFRs GENERATED DURING ENVIRONMENTAL TESTS? ☐ YES ☒ NO (IF NO, ATTACH EXCEPTIONS LIST)	LIST PFR NOS. / BRIEF EXPLANATION
ARE THE POST ENVIRONMENTAL DAMAGE INSPECTIONS COMPLETE? ☒ YES ☐ NO (IF YES, ATTACH A COPY OF THE INSPECTION REPORTS. IF NO, ATTACH EXPLANATION)	LIST PFR NOS. / BRIEF EXPLANATION
WERE ALL PLANNED TESTS/LEVELS/DURATIONS ACHIEVED? ☒ YES ☐ NO (IF NO, ATTACH EXCEPTIONS LIST)	LIST PFR NOS. / BRIEF EXPLANATION

☐ TESTS HAVE NOT BEEN SUCCESSFULLY COMPLETED. SEE THE ATTACHED SUMMARY FOR ACTIONS THAT NEED TO BE TAKEN.

COGNIZANT ENGINEER	DATE	TECHNICAL MGR./INSTR MRG./PI PREP REP	DATE	ENVIRONMENTAL REQUIREMENTS ENG.	DATE

HARDWARE HAS SUCCESSFULLY COMPLETED THE ENVIRONMENTAL TESTS LISTED ON THIS FORM OR REMAINING ACTIONS HAVE BEEN TAKEN, INCLUDING RETEST.

COGNIZANT ENGINEER	DATE	TECHNICAL MGR./INSTR MRG./PI PREP REP	DATE	ENVIRONMENTAL REQUIREMENTS ENG.	DATE
[signature]	6/14/05	[signature]	6/14/05	[signature]	6-14-05

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Attachment of HRCR Item #7: ETAS (Environmental Test Summary)

JPL

ENVIRONMENTAL TEST AUTHORIZATION AND SUMMARY (ETAS)

OTHER AUTHORIZATION PROVISIONS AND EXPLANATIONS

(is a 3-axis warm vibration test (room temp) done on the JFET flight modules SN016 and 017. The test will be done with the JFET unit mounted inside a mock-up JFET rack. The unit will be assessed both before and after the test with visual inspections and electrical checkouts. 3 response accelerometers will be mounted onto the JFET rack in order to give response data.

2 to ~~3~~ vacuum thermal cycles will also be completed.

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Attachment of HRCR Item #7: ETAS (Environmental Test Summary)

JPL

ENVIRONMENTAL TES[illegible]UTHORIZATION AND SUMMARY (ETAS)

ENVIRONMENTAL TEST SUMMARY

HARDWARE	S/N	ETAS	TEST ENVIRONMENT LEVELS & DURATION	DATE TEST PERFORMED	TEST AGENCY	PASS/ FAIL	COMMENTS
SPIRE JFET (10209750-1)	016,017	HSO40	**X, Y, and Z** 1 minute Random Vibe Frequency [Hz] / Spec [g^2.Hz] 20 / 0.01 100 / 0.05 300 / 0.05 499 / 0.0214 500 / 0.0214 2000 / 0.00214 Each axis1/4 g sine sweep 20-2000 Hz each axis 2-3 vaccuum thermal cycles. <10E-5 mbar, <70K				

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Attachment of HRCR Item # 8: Test Data - Source Voltage Data

JFET SOURCE VOLTAGE MEASUREMENT

Post bake, Post-vibe, SN16,17

			pwr1 1,2A		pwr2 3,4A		pwr3 1,2 B		pwr4 3,4B		pwr1 1,2A		pwr2 3,4A		pwr3 1,2 B		pwr4 3,4B	
Date			5/24/2005		5/24/2005		5/24/2005		5/24/2005		5/31/2005		5/31/2005		5/31/2005		5/31/2005	
T, plate			4K T		4K T		4K T		4K T		Rm T		Rm T		Rm T		Rm T	
			4K T		4K T		4K T		4K T		Rm T		Rm T		Rm T		Rm T	
Vdd			3		3		3		3		3		3		3		3	
Vss			-1.5		1.5		-1.5		-1.5		-1.5		-1.5		-1.5		-1.5	
Vdd'			2.748		2.779		2.676		2.762		2.721		2.748		2.651		2.736	
Vss'			-1.245		-1.277		-1.174		-1.26		-1.218		-1.246		-1.148		-1.233	
Idd			0.9659		0.8455		1.2443		0.9119		1.0543		0.9504		1.322		0.9966	
Iss			0.9646		0.8443		1.2431		0.9106		1.053		..949		1.3207		0.9953	
SN			40		45		41		43		40		45		41		43	
Channel #				DELTA		DELTA		DELTA		DELTA		DELTA		DELTA		DELTA		DELTA
1	a		0.701	0.002	0.860	0.001	0.276	0.003	0.775	0.005	0.987	0.003	1.158	0	0.553	0	1.057	0.005
	b		0.703		0.859		0.273		0.780		0.990		1.158		0.553		1.062	
2	a		0.716	0.002	0.147	0.006	0.734	0.007	0.699	0.004	1.005	0.001	0.468	0.006	0.997	0.006	0.983	0.002
	b		0.718		0.141		0.727		0.703		1.004		0.462		0.991		0.985	
3	a		0.874	0.006	0.139	0.005	0.697	0.004	0.814	0.005	1.155	0.005	0.461	0.001	0.961	0.004	1.098	0.008
	b		0.880		0.144		0.701		0.809		1.160		0.460		0.965		1.090	
4	a		0.697	0.002	0.356	0.002	0.678	0	0.771	0.001	0.987	0.001	0.670	0.004	0.946	0.002	1.055	0.002
	b		0.699		0.354		0.678		0.772		0.986		0.666		0.944		1.057	
5	a		0.841	0.001	0.912	0.004	0.683	0.002	0.662	0	1.123	0.002	1.213	0.003	0.965	0.004	0.947	0
	b		0.842		0.908		0.685		0.662		1.125		1.210		0.969		0.947	
6	a		0.789	0.003	0.584	0.005	0.729	0.001	0.736	0.004	1.070	0.002	0.889	0.005	0.993	0	1.024	0.003
	b		0.792		0.589		0.728		0.732		1.072		0.894		0.993		1.021	
7	a		0.889	0.009	0.913	0.004	0.753	0.003	0.773	0.002	1.171	0.009	1.216	0.003	1.014	0.002	1.070	0
	b		0.880		0.917		0.756		0.771		1.162		1.219		1.016		1.070	
8	a		0.708	0.002	0.919	0.002	0.770	0.003	0.685	0.004	0.998	0.002	1.216	0.002	1.031	0.002	0.972	0.004
	b		0.710		0.917		0.773		0.689		1.000		1.214		1.033		0.976	
9	a		0.751	0.007	1.074	0.001	0.761	0.002	0.640	0.007	1.039	0.005	1.370	0	1.029	0.003	0.934	0.006
	b		0.758		1.073		0.763		0.647		1.044		1.370		1.032		0.940	
10	a		0.698	0.002	0.118	0.002	0.843	0.002	0.723	0	0.992	0.001	0.456	0.003	1.109	0.001	1.011	0
	b		0.700		0.116		0.845		0.723		0.993		0.453		1.110		1.011	
11	a		0.710	0.002	0.906	0.002	0.668	0.001	0.693	0.002	1.005	0	1.214	0.002	0.945	0	0.993	0.003
	b		0.712		0.908		0.667		0.691		1.005		1.216		0.945		0.990	
12	a		0.704	0.002	0.910	0.001	0.739	0.003	1.162	0.006	0.998	0.003	1.224	0.001	1.010	0.003	1.441	0.006
	b		0.702		0.909		0.742		1.156		0.995		1.225		1.013		1.435	
13	a		0.715	0.001	0.227	0.008	0.448	0.013	0.268	0.01	1.013	0.002	0.559	0.006	0.731	0.014	0.597	0.011
	b		0.716		0.235		0.461		0.278		1.015		0.565		0.745		0.586	
14	a		0.661	0.003	1.108	0.004	0.625	0.005	0.696	0.004	0.962	0.003	1.410	0.001	0.899	0.007	1.002	0.006
	b		0.664		1.104		0.620		0.700		0.965		1.409		0.892		1.008	
15	a		0.681	0.002	0.362	0.009	0.687	0.004	0.722	0.002	0.975	0	0.683	0.009	0.962	0.001	1.011	0.002
	b		0.679		0.371		0.691		0.720		0.975		0.692		0.963		1.009	
16	a		0.708	0.003	0.156	0.005	0.711	0.002	0.654	0.003	1.003	0.002	0.484	0.004	0.976	0	0.947	0.002
	b		0.705		0.151		0.709		0.651		1.001		0.480		0.976		0.945	
17	a		0.739	0.002	0.250	0.008	0.711	0.001	0.678	0.002	1.029	0.002	0.573	0.008	0.980	0.002	0.969	0.002
	b		0.737		0.258		0.710		0.680		1.027		0.581		0.982		0.971	
18	a		0.689	0.004	0.527	0.006	0.729	0.004	0.801	0.001	0.989	0.001	0.839	0.005	0.997	0.004	1.086	0.002
	b		0.685		0.533		0.733		0.802		0.988		0.844		1.001		1.088	
19	a		0.691	0	1.008	0.001	0.695	0.003	0.724	0.005	0.982	0.001	1.326	0	0.963	0.002	1.008	0.005
	b		0.691		1.009		0.692		0.729		0.981		1.326		0.961		1.013	
20	a		0.659	0.003	0.360	0.001	0.728	0.003	0.710	0.004	0.963	0.002	0.691	0.004	0.992	0.003	1.011	0.002
	b		0.656		0.359		0.731		0.714		0.961		0.695		0.995		1.013	
21	a		0.699	0.003	0.344	0.007	1.005	0.003	0.699	0.001	0.991	0.001	0.660	0.007	1.258	0.004	0.988	0.001
	b		0.702		0.337		1.008		0.698		0.992		0.653		1.262		0.989	
22	a		0.687	0.001	0.237	0.011	0.737	0.001	0.726	0.003	0.977	0	0.557	0.01	1.003	0	1.009	0.002
	b		0.688		0.248		0.738		0.729		0.977		0.567		1.003		1.011	
23	a		0.727	0	0.296	0.008	0.696	0.001	0.787	0.002	1.013	0.001	0.614	0.004	0.962	0.002	1.068	0.002
	b		0.727		0.290		0.695		0.785		1.014		0.610		0.960		1.066	
24	a		0.676	0.003	0.436	0.005	0.785	0.003	0.674	0.003	0.966	0.002	0.750	0.003	1.044	0.003	0.958	0.005
	b		0.679		0.441		0.788		0.677		0.968		0.753		1.047		0.963	
25	a			0		0		0		0		0		0		0		0
	b																	
26	a			0		0		0		0		0		0		0		0
	b																	
27	a			0		0		0		0		0		0		0		0
	b																	
28	a			0		0		0		0		0		0		0		0
	b																	
29	a			0		0		0		0		0		0		0		0
	b																	
30	a			0		0		0		0		0		0		0		0
	b																	

Attachment of HRCR Item # 8: Noise Test Data

	Pwr11	Pwr10	Pwr2	Pwr1	Pwr9	Pwr8	Pwr5	Pwr4	Pwr7	Pwr5b	Pwr3
Vdd (V)	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8
Vss (V)	-1.54	-1.52	-1.5	-1.45	-1.4	-1.38	-1.36	-1.34	-1.32	-1.3	-1.2
Vdd' (V)	2.535	2.537	2.54	2.545	2.551	2.554	2.556	2.558	2.561	2.563	2.575
Vss' (V)	-1.281	-1.264	-1.246	-1.202	-1.158	-1.141	-1.123	-1.105	-1.087	-1.07	-0.982
Idd (mA)	1.0144	1.0053	0.9963	0.9735	0.9511	0.9419	0.9324	0.9232	0.9141	0.905	0.8592
Iss (mA)	0.9793	0.9703	0.9613	0.9387	0.9163	0.9072	0.8977	0.8886	0.8795	0.8704	0.8249
I (mA)	0.99685	0.9878	0.9788	0.9561	0.9337	0.92455	0.91505	0.9059	0.8968	0.8877	0.84205
P (mW)	3.8039796	3.7546278	3.7057368	3.5825067	3.4630933	3.41621225	3.36646895	3.3183117	3.2715264	3.2250141	2.99517185
	-12	-12	-12	-12	-12	-12	-12	-12	-12	-12	-12

Channel Num	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz
Channel: 1	8.55	6.68	6.48	8.93	9.22	9.90	10.71	12.58	14.61	16.49	18.05
Channel: 2	6.63	6.44	6.92	8.28	6.73	7.41	8.63	8.54	8.95	13.70	13.76
Channel: 3	8.78	7.35	7.70	7.17	6.99	7.30	7.70	6.71	7.49	11.34	7.53
Channel: 4	6.44	6.78	5.94	5.83	6.25	5.75	5.65	7.10	5.54	11.47	7.47
Channel: 5	6.38	6.82	8.11	8.57	8.93	8.76	10.07	10.54	11.12	13.65	13.75
Channel: 6	9.46	8.37	9.37	11.64	14.53	15.87	22.30	22.46	26.07	27.41	44.91
Channel: 7	8.67	9.12	9.06	8.05	7.73	8.44	7.15	8.71	8.06	10.63	10.20
Channel: 8	8.30	7.66	9.40	10.39	14.17	14.49	16.14	22.84	21.21	28.27	26.77
Channel: 9	6.74	5.83	6.03	6.82	6.58	7.78	7.92	9.20	8.10	12.37	11.00
Channel: 10	6.41	6.32	6.24	5.86	5.56	6.03	5.74	8.54	7.12	10.30	10.13
Channel: 11	6.51	6.41	6.61	7.13	6.19	6.08	6.96	5.93	6.67	8.31	7.43
Channel: 12	7.11	7.22	8.43	10.00	10.43	12.39	12.00	15.98	16.85	19.51	39.82
Channel: 13	6.75	6.64	7.80	7.06	7.95	9.36	11.39	11.60	12.25	15.33	35.83
Channel: 14	10.25	11.89	10.15	12.23	9.84	11.04	11.72	8.64	12.29	9.76	13.98
Channel: 15	6.58	10.02	8.24	8.97	8.02	9.26	10.55	8.96	10.15	10.98	9.38
Channel: 16	8.34	6.83	7.61	7.86	10.09	8.95	10.22	10.67	9.94	9.48	16.13
Channel: 17	8.21	8.15	7.87	6.11	6.65	9.46	7.30	8.22	7.53	7.52	7.64
Channel: 18	7.30	9.95	7.15	8.24	10.38	7.92	10.79	10.65	10.23	9.91	15.87
Channel: 19	12.69	15.71	12.77	15.82	13.68	16.06	14.95	14.60	16.86	14.37	15.33
Channel: 20	7.93	8.26	7.91	8.71	9.79	8.70	11.28	14.59	15.18	17.57	37.20
Channel: 21	6.68	5.55	7.36	8.01	7.80	8.88	8.50	9.16	9.90	9.54	11.16
Channel: 22	14.44	14.30	17.89	16.43	15.26	14.84	14.77	19.81	19.90	21.77	24.09
Channel: 23	6.04	8.48	5.92	7.64	6.00	7.00	6.41	7.64	6.52	6.21	7.15
Channel: 24	6.23	8.99	6.79	8.28	9.29	9.56	10.08	10.06	10.60	10.19	12.56
Median	7.21	7.50	7.75	8.26	8.47	8.91	10.15	9.63	10.19	11.40	13.75
Overall Mean	7.98	8.32	8.24	8.92	9.08	9.63	10.37	11.41	11.80	13.59	17.38
Good Mean	7.98	8.00	7.82	8.26	8.82	9.06	9.57	9.63	9.28	10.57	10.22
MP Reqd							15				
Yield	**0.00**	**0.00**	**0.00**	**0.00**	**0.00**	**0.00**	**0.00**	**0.00**	**0.00**	**0.00**	**0.00**
# Good Ch.	0	0	0	0	0	0	0	0	0	0	0
# Bad Ch.	24	24	24	24	24	24	24	24	24	24	24

JFET_Mod16_brd40_Noise_perf.xls

Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise

	Pwr9	Pwr2	Pwr3	Pwr1	Pwr5	Pwr5b	Pwr7	Pwr4	Pwr8
Vdd (V)	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8
Vss (V)	-1.7	-1.6	-1.55	-1.5	-1.45	-1.42	-1.41	-1.4	-1.3
Vdd' (V)	2.551	2.562	2.568	2.573	2.579	2.582	2.583	2.585	2.596
Vss' (V)	-1.455	-1.367	-1.322	-1.278	-1.233	-1.207	-1.198	-1.189	-1.1
Idd (mA)	0.954	0.911	0.8891	0.8675	0.8458	0.8329	0.8287	0.8243	0.7806
Iss (mA)	0.927	0.8843	0.8624	0.841	0.8193	0.8065	0.8024	0.798	0.7545
I (mA)	0.9405	0.89765	0.87575	0.85425	0.83255	0.8197	0.81555	0.81115	0.76755
P (mW)	3.767643	3.52686685	3.4066675	3.28971675	3.1736806	3.1058433	3.08359455	3.0612801	2.8368648
	-8	-6	-6	-12 (ch 14 is -6)	-6	-6	-6	-6	-8

Channel Num	Vn @150 Hz		Vn @150 Hz		Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz
Channel: 1	8.49	8.39	11.04	12.87	13.97	14.65	12.30	14.35	13.65
Channel: 2	7.00	7.86	9.60	7.48	7.23	7.07	7.16	8.59	8.06
Channel: 3	9.09	7.64	13.36	9.32	10.66	10.93	11.64	13.67	14.16
Channel: 4	8.12	7.43	7.34	7.18	5.09	8.97	7.16	9.16	8.71
Channel: 5	7.77	6.96	6.56	6.59	9.27	7.70	7.22	8.26	11.39
Channel: 6	6.63	12.06	6.94	7.44	8.26	7.49	7.53	6.89	10.28
Channel: 7	7.61	12.34	19.17	22.24	31.56	32.36	43.02	37.50	50.77
Channel: 8	6.31	6.78	6.92	7.18	8.90	7.55	6.49	6.61	7.25
Channel: 9	7.70	10.01	11.30	14.15	16.92	14.89	15.64	17.31	14.41
Channel: 10	7.04	6.83	8.70	6.92	8.35	9.73	8.78	7.36	11.34
Channel: 11	6.43	6.22	7.54	8.48	9.93	9.95	13.50	9.85	9.73
Channel: 12	7.56	9.77	11.98	12.10	12.16	13.46	15.69	10.72	11.34
Channel: 13	6.74	6.29	9.78	8.68	5.91	8.22	12.71	9.02	9.45
Channel: 14	7.94	11.16	14.35	17.03	19.00	19.89	26.02	22.80	19.60
Channel: 15	9.74	7.62	7.71	6.51	8.78	9.23	11.19	7.18	11.49
Channel: 16	6.91	7.79	8.83	6.87	7.37	8.21	7.55	8.55	9.75
Channel: 17	8.29	6.94	6.01	6.70	7.91	7.58	9.59	10.94	15.45
Channel: 18	11.78	6.33	10.65	9.13	8.55	11.21	12.38	11.56	27.68
Channel: 19	7.22	7.06	6.82	8.18	7.62	11.73	11.89	12.75	19.66
Channel: 20	9.01	6.95	7.75	10.31	9.08	11.92	15.24	15.63	24.03
Channel: 21	9.01	7.22	7.51	7.60	9.00	6.59	8.32	6.90	7.72
Channel: 22	6.90	8.61	9.25	12.36	11.92	13.54	16.18	16.34	21.77
Channel: 23	8.58	8.32	14.86	8.58	10.90	12.20	11.91	11.61	12.82
Channel: 24	7.88	9.63	9.20	9.16	11.10	9.47	12.57	9.65	7.81
Median	7.74	7.63	9.02	8.53	9.04	9.84	11.90	10.28	11.44
Overall Mean	7.91	8.18	9.72	9.71	10.81	11.44	12.99	12.22	14.93
Good Mean	7.91	8.18	9.30	8.81	9.14	10.10	9.99	9.66	10.55
MP Reqd					15				
Yield	**1.00**	**1.00**	**0.96**	**0.92**	**0.88**	**0.92**	**0.75**	**0.79**	**0.71**
# Good Ch.	24	24	23	22	21	22	18	19	17
# Bad Ch.	0	0	1	2	3	2	6	5	7

JFET_Mod16_brd45_Noise_perf.xls

Attachment of HRCR Item # 9: SPIRE MIUL Cover Page

MIUL = Material Identification & Utilization List

Declared Materials List's and Processes List are not included in this HRCR

Materials and Processes List

SPIRE

JPL D-25725

REV B
1/05/04

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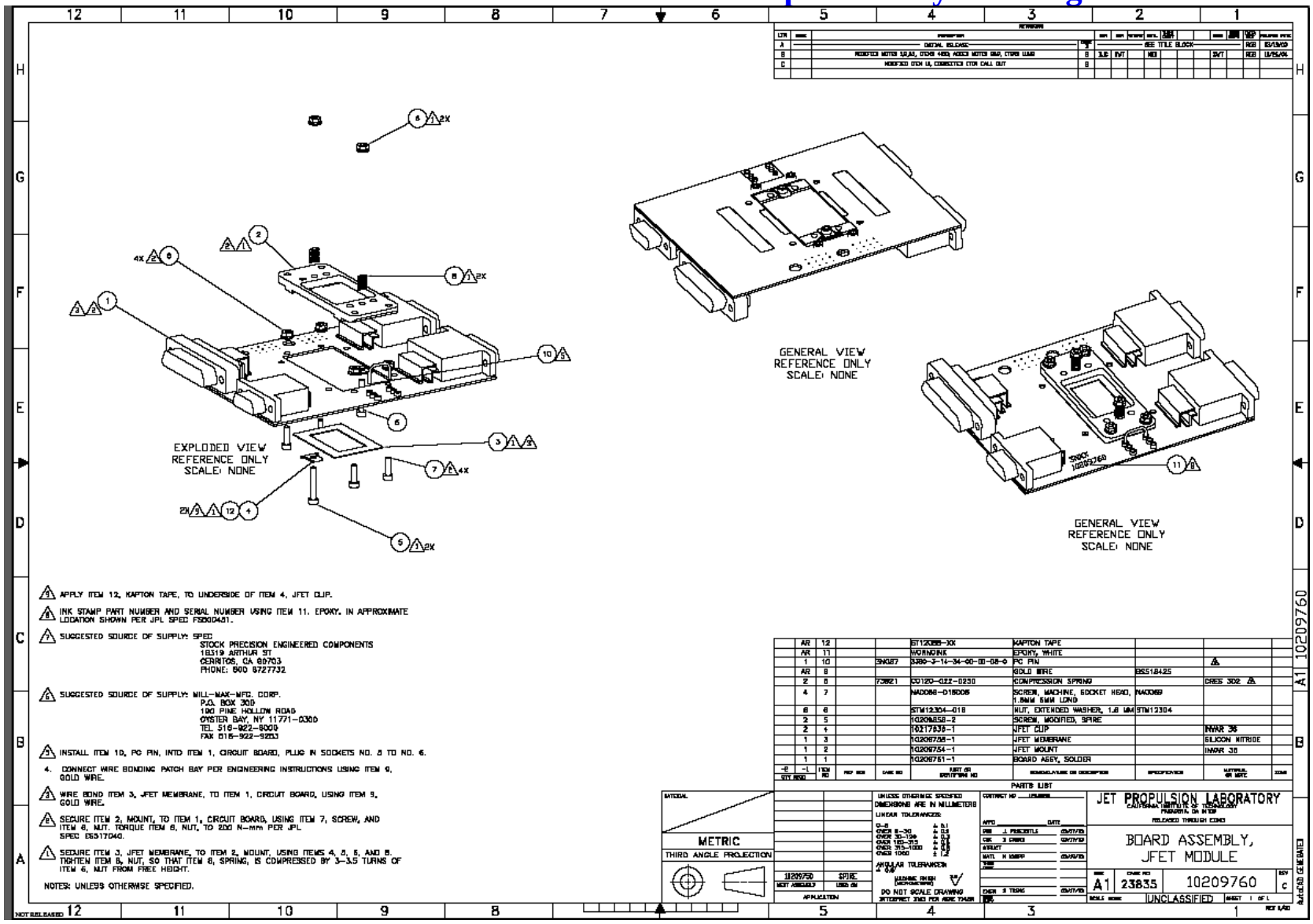
Reviewed by: _____
M. Knopp M&P Engineer

Attachment of HRCR Item # 11:

See End of This HRCR Package for "JFET Module Handling Document"

Attachment of HRCR Item # 14: JFET Module Top Assembly Drawing 10209750-1



Attachment of HRCR Item # 23: Qualification Compliance Test

Qualification Model JFET Module

EIDP Coverpage For JFET Testing

Unit Identification							
Name	:	JFET QM Module					
Part #	:	10209750-1					
S/N	:	#001					

Environmental Testing						
	Axes Tested	**Temperature**	**Duration/# of Cycle**	**Requirement**	**Source**	**Waiver**
Random Vibration Test	X, Y, Z	100 K	2 min/axis	X, Y, Z	SSSD, JFET-DES-07	
High Level Sine Vibe Test	None	NA	NA	X, Y, Z	SSSD, JFET-DES-07	HR-SP-JPL-RFW_005
Bakeout	NA	80 C	72 Hours	80C, 72 Hrs	D-20549	
Thermal Cycles	NA	RmT to 80 K	27	Minimum 15	D-20549	

Performance Characteristics						
		Specification		**Source**		**Waiver**
Power needed for <11 bad channels (Min Perf.)	9.1 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02		RFW in process
Power needed for <4 bad channels (Design Value)	10.8 mW	11 mW for CQM, 7 mW for PFM/FS		SSSD, JFET-TEC-05, JFET-PER-02		
Power needed for 100 % Yield per unit	13.5 mW	NA		NA		
Median Noise at < 11 bad chs.	7.13 nV/rtHz	<15 nV/rtHz Min Performance		SSSD, JFET-PER-01		
Median Noise at < 4 bad chs.	6.1 nV/rtHz		<7 nV/rtHz Design Value	SSSD, JFET-PER-01		
Median Noise at 100 % Yield.	6.97 nV/rtHz			SSSD, JFET-PER-01		
# of Channels over the max. offset voltage	0	< 15 mV for CQM < 15 mV for PFM/FS			SSSD, BDA-DRCU-27	
Common Mode Rejection Ratio	< -60 dB by design, as measured in EM4 unit				SSSD, BDA-DRCU-11	

Board Level Detail						
		Board SN 001			**Source**	
# Channels Tested	:	24				
Median Noise at 3.5 mW	:	18 nV/rtHz			SSSD, JFET-PER-01	
# of good channels at 3.5 mW	:	7	29% Yield		SSSD, JFET-PER-02	
Power Needed for 100 % Yield	:	6.75 mW			SSSD, JFET-PER-02	
Median Noise at High Power (w/ 100 % Yield)		6.97 nV/rtHz			SSSD, JFET-PER-01	
Median Gain at High Power		0.98			NA	

Definitions		
Good Channels	:	Noise less than a min. performance value of 15 nV/rtHz
Yield	:	# of Good Channels / 24
Filenames		
Noise Measurements	:	QualJFETPostVibeNoise_Summary.pdf

Notes	
1)	The Base temperature for all performance characterization was 4K
2)	All Noise Measurements were made with the inputs shorted to ground

Attachment of HRCR Item # 24 & #25: Mate/Demate & Operation Logs

Hardware ID JFET SN 16,17							
Date	Time	AIDS	Power	Mate	Demate	Transport	Notes
1-Apr	8:00 AM	245138				X	103 -> 183
1-Apr	9:00 AM	245138		X			Mate All Connectors
1-Apr	10:00 AM	245138					Measure all resistances
1-Apr	1:00 PM	245138	X				30 min each board, warm S.V. test (green dewar)
12-Apr	8:00 AM	245138					Assemble into CSF
13-Apr	7:30 AM	245138			X		Remove all shorting connectors, close out CSF
15-Apr	8:00 AM	245138				X	183->144
15-Apr	9:00 AM	245138					Pump out
15-Apr	9:30 AM	245138					Run 3-axis warm shake
15-Apr	2:00 PM	245138				X	144->183
16-Apr	8:00 AM	245138		X			Install shorting connectors
16-Apr	9:00 AM	245138				X	Remove JFETs from CSF
18-Apr	9:00 AM	245138		X			Install into blue dewar
18-Apr	10:00 AM	245138	X				Take source voltage measurements
18-Apr	11:00 AM	245138			X		Remove from blue dewar, store in flight cabinet
20-May	8:00 AM	245396		X			Install into green dewar
20-May	9:00 AM	245396					Pump out
20-May	10:00 AM	245396	X				30 min each board, warm S.V. test (green dewar)
23-May	1:00 PM	245396					Transfer LN2
23-May	8:00 PM	245396					Transfer Helium
24-May	8:00 AM	245396	X				30 min each board, cold S.V. test (green dewar)
24-May	10:00 AM	245396	X				8 hours, board 40 noise
24-May	6:00 PM	245396	X				3 hours, board 45 noise
25-May	8:00 AM	245396	X				6 hours, board 45 noise
25-May	2:00 PM	245396	X				6 hours, board 41 noise
26-May	8:00 AM	245396	X				10 hours, board 43 noise
27-May	8:00 AM	245396					warm dewar
31-May	8:00 AM	245396					pump out
31-May	9:00 AM	245396	X				30 min each board, warm S.V. test (green dewar)
31-May	1:00 PM	245396					cool dewar
1-Jun	8:00 AM	245396	X				30 min each board, cold S.V. test (green dewar)
2-Jun	10:00 AM	245396	X				2 hours, board 40, gain and CMRR
2-Jun	12:00 PM	245396	X				2 hours, baord 45, gain and CMRR
2-Jun	2:00 PM	245396	X				2 hours, board 41, gain and CMRR
2-Jun	4:00 PM	245396	X				2 hours, board 43, gain and CMRR
3-Jun	8:00 AM	245396	X				8 hours, board 43 noise
3-Jun	6:00 PM	245396					warm dewar
6-Jun	8:00 AM	245396	X				30 min each board, warm S.V. test (green dewar)
6-Jun	1:00 PM	245396			X	X	Demate, Transport 183->103

Attachment of HRCR Item # 24 & #25: Mate/Demate & Operation Logs (continued)

OPERATION LOG SHEET -- SPIRE JFET BOARDS MODULE

USE THE "NOTE" COLUMN TO DESCRIBE ACTIONS

DEVICE (BRD) S/N: 40 (54) PROJECT: SPIRE/ JFET BOARD

DATE	TIME	TECH	PWR ON	PWR OFF	MATE JAA	MATE JBB	MATE JCC	MATE JDD	DEMATE JAA	DEMATE JBB	DEMATE JCC	DEMATE JDD	TRANSFORT	NOTE
11-01-04	9:30AM	103199			✓	✓	✓	✓	—	—	—	—		SAVERS INSTALLED
11-18-04		103199			—	—	—	—	—	—	—	—		GND & CHASSIS. "
11-16-04	9:30AM	103199			—	—	—	—	—	—	—	—		GND & CHASSIS "
12-16-04	9:30AM	103199	✓	✓	—	—	—	—	—	—	—	—		SOURCE TEST "
2-9-05		103199			-	-	-	-	-	-	-	-		GND & CHASSIS "
2-9-05		103199	✓	✓	-	-	-	-	-	-	-	-		SOURCE TEST "
3-21-05	10:00AM	103199			✓	✓	✓	✓	-	-	✓	✓		GND & CHASSY "
3-21-05		103199	✓	✓	-	-	✓	✓	✓	✓	-	-		SOURCE TEST
3/23/05		103199			✓	✓	✓	✓			✓	✓		GND & CHASSY
3/23/05		103199	✓	✓			✓	✓	✓	✓				SOURCE TEST
3/28/05	ST Rec	103199 PR			✓	✓	✓	✓			✓	✓		GND & CHASSY
3/28/05		ST.	✓	✓			✓	✓	✓	✓				SOURCE
6-17-05		NAN	✓	✓	✓	✓	✓	✓						SHUT PLG / SAVER SOURCE TEST

NOTE: CONNECTOR ARE RE-USED. FROM ASSY # 10209761-1 S/N 031, MDS # 240881, JR# 923860 NAN 3-25-05

Attachment of HRCR Items # 24 & # 25: Mate/Demate & Operation Logs

OPERATION LOG SHEET -- SPIRE JFET BOARDS MODULE

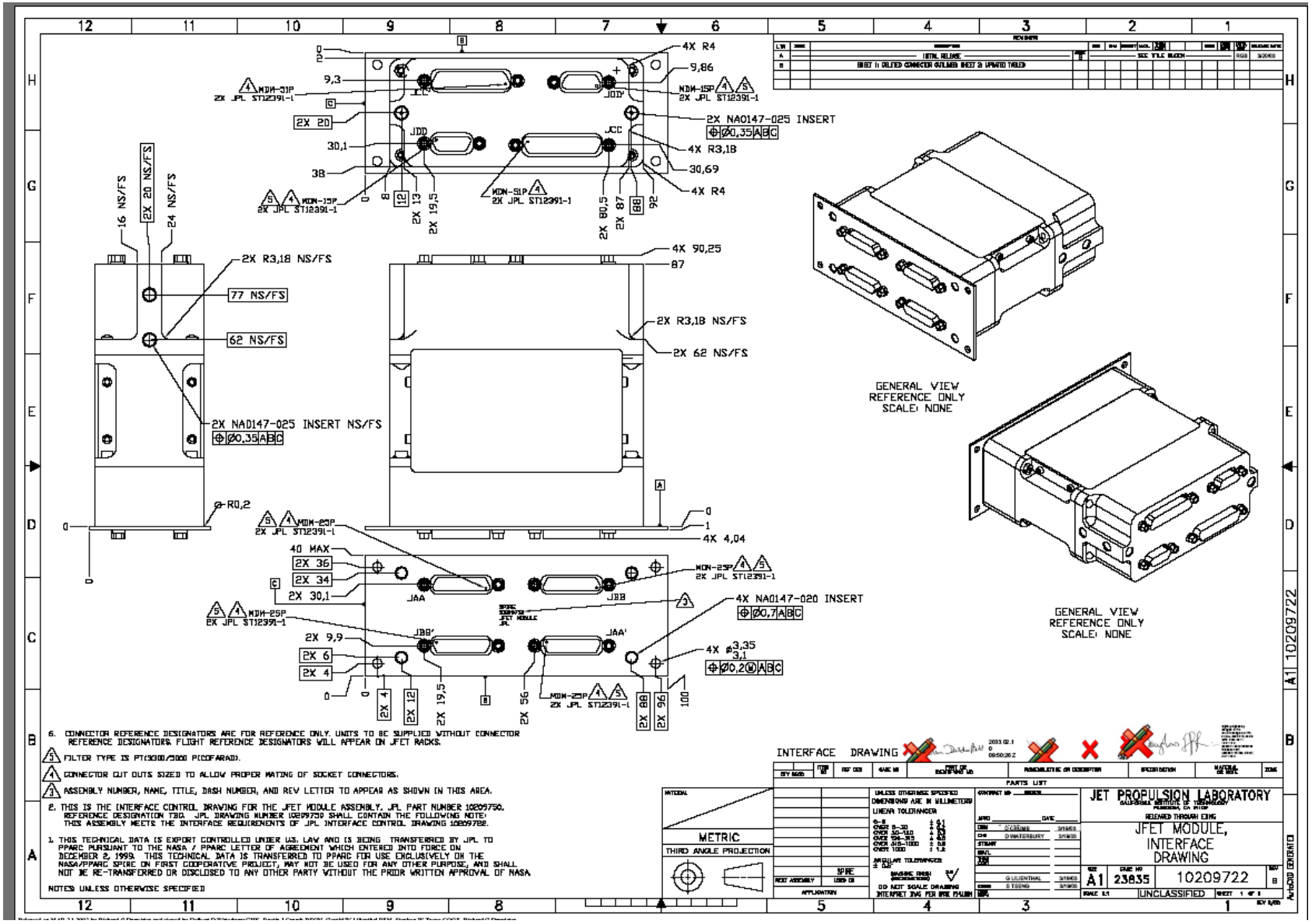
USE THE "NOTE" COLUMN TO DESCRIBE ACTIONS

DEVICE (BRD) S/N: 045 (59) **PROJECT:** SPIRE/ JFET BOARD

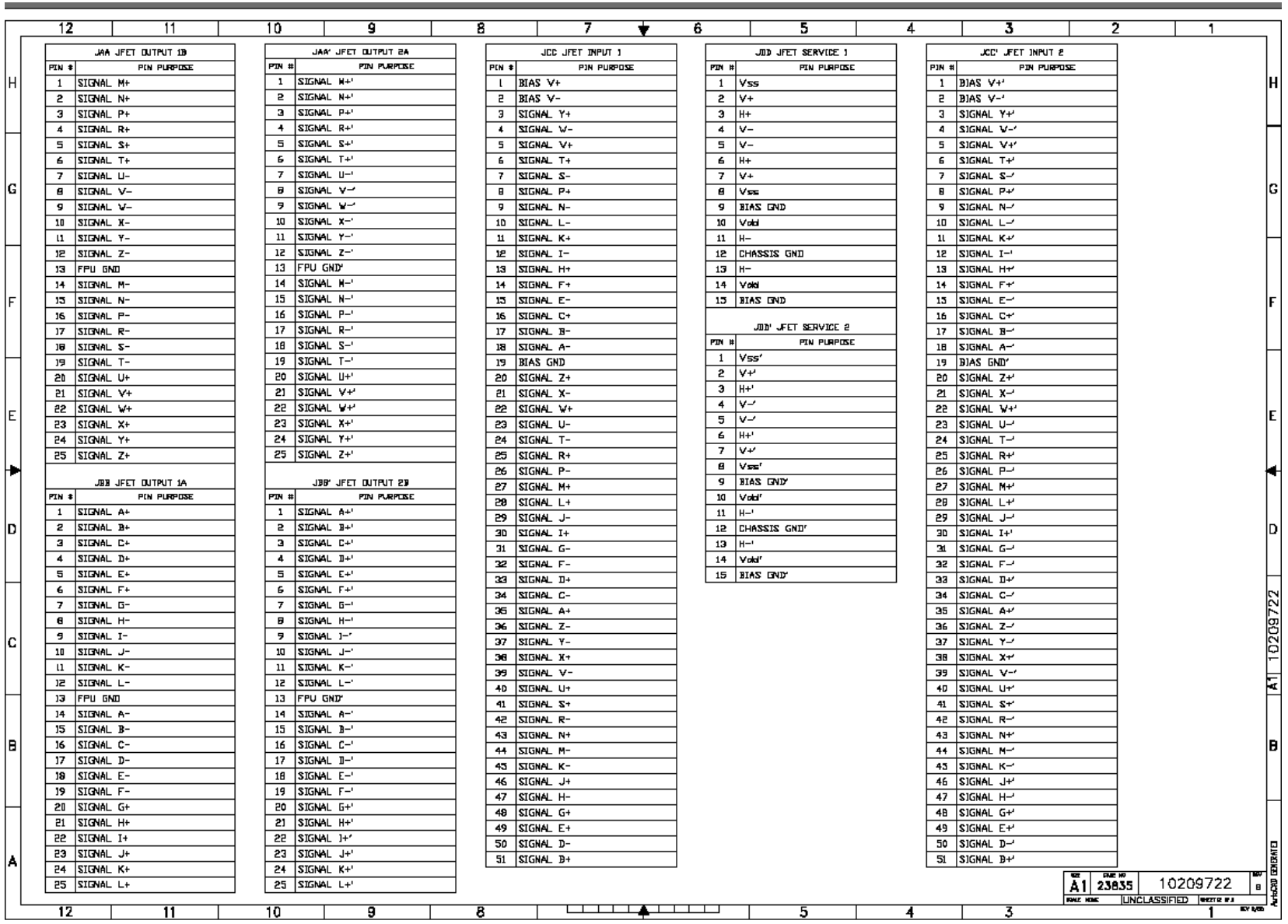
DATE	TIME	TECH	PWR ON	PWR OFF	MATE				DEMATE				TRANSFORT	NOTE
					JAA	JBB	JCC	JDD	JAA	JBB	JCC	JDD		
11/4/04		NAN			✓	✓	✓	✓	—	—	—	—		GND & CHASSIS - SAVER ON
1/12/05		NAN			—	—	—	—	—	—	—	—		GND & CHASSIS - SAVER ON
1-27-05		NAN			–	–	–	–	–	–	–	–		GND & CHASSIS - "
1-27-05		NAN	✓	✓	–	–	–	–	–	–	–	–		SOURCE TEST
2-23-05		NAN			–	–	–	–	–	–	–	–		GND & CHASSIS
2-23-05		NAN	✓	✓	–	–	–	–	–	–	–	–		SOURCE TEST
3-21-05		NAN			–	–	–	–	–	–	–	–		GND & CHASSIS
3-21-05		NAN	✓	✓	–	–	–	–	–	–	–	–		SOURCE TEST
3-23-05		NAN			✓	✓	✓	✓	✓	✓	✓	✓		GND & CHASSIS
3-23-05		NAN	✓	✓	–	–	✓	✓	–	–	✓	✓		SOURCE TEST
3-28-05		ST			✓	✓	✓	✓	✓	✓	✓	✓		GND & CHASSIS
3-28-05		ST	✓	✓	–	–	✓	✓	–	–	✓	✓		SOURCE TEST
6-17-05		NAN	✓	✓	✓	✓	✓	✓						SOURCE TEST SAVER ON

NOTE: CONNECTORS ARE RE-USED FROM ASSY 10207961-1 S/N:028 MDJA 24878 IR# 923892

Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 1 of 2)



Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 2 of 2)



JAA JFET OUTPUT 1B

PIN #	PIN PURPOSE
1	SIGNAL M+
2	SIGNAL N+
3	SIGNAL P+
4	SIGNAL R+
5	SIGNAL S+
6	SIGNAL T+
7	SIGNAL U-
8	SIGNAL V-
9	SIGNAL W-
10	SIGNAL X-
11	SIGNAL Y-
12	SIGNAL Z-
13	FPU GND
14	SIGNAL M-
15	SIGNAL N-
16	SIGNAL P-
17	SIGNAL R-
18	SIGNAL S-
19	SIGNAL T-
20	SIGNAL U+
21	SIGNAL V+
22	SIGNAL W+
23	SIGNAL X+
24	SIGNAL Y+
25	SIGNAL Z+

JBB JFET OUTPUT 1A

PIN #	PIN PURPOSE
1	SIGNAL A+
2	SIGNAL B+
3	SIGNAL C+
4	SIGNAL D+
5	SIGNAL E+
6	SIGNAL F+
7	SIGNAL G-
8	SIGNAL H-
9	SIGNAL I-
10	SIGNAL J-
11	SIGNAL K-
12	SIGNAL L-
13	FPU GND
14	SIGNAL A-
15	SIGNAL B-
16	SIGNAL C-
17	SIGNAL D-
18	SIGNAL E-
19	SIGNAL F-
20	SIGNAL G+
21	SIGNAL H+
22	SIGNAL I+
23	SIGNAL J+
24	SIGNAL K+
25	SIGNAL L+

JAA' JFET OUTPUT 2A

PIN #	PIN PURPOSE
1	SIGNAL M+'
2	SIGNAL N+'
3	SIGNAL P+'
4	SIGNAL R+'
5	SIGNAL S+'
6	SIGNAL T+'
7	SIGNAL U-'
8	SIGNAL V-'
9	SIGNAL W-'
10	SIGNAL X-'
11	SIGNAL Y-'
12	SIGNAL Z-'
13	FPU GND'
14	SIGNAL M-'
15	SIGNAL N-'
16	SIGNAL P-'
17	SIGNAL R-'
18	SIGNAL S-'
19	SIGNAL T-'
20	SIGNAL U+'
21	SIGNAL V+'
22	SIGNAL W+'
23	SIGNAL X+'
24	SIGNAL Y+'
25	SIGNAL Z+'

JBB' JFET OUTPUT 2B

PIN #	PIN PURPOSE
1	SIGNAL A+'
2	SIGNAL B+'
3	SIGNAL C+'
4	SIGNAL D+'
5	SIGNAL E+'
6	SIGNAL F+'
7	SIGNAL G-'
8	SIGNAL H-'
9	SIGNAL I-'
10	SIGNAL J-'
11	SIGNAL K-'
12	SIGNAL L-'
13	FPU GND'
14	SIGNAL A-'
15	SIGNAL B-'
16	SIGNAL C-'
17	SIGNAL D-'
18	SIGNAL E-'
19	SIGNAL F-'
20	SIGNAL G+'
21	SIGNAL H+'
22	SIGNAL I+'
23	SIGNAL J+'
24	SIGNAL K+'
25	SIGNAL L+'

JCC JFET INPUT 1

PIN #	PIN PURPOSE
1	BIAS V+
2	BIAS V-
3	SIGNAL Y+
4	SIGNAL W-
5	SIGNAL V+
6	SIGNAL T+
7	SIGNAL S-
8	SIGNAL P+
9	SIGNAL N-
10	SIGNAL L-
11	SIGNAL K+
12	SIGNAL I-
13	SIGNAL H+
14	SIGNAL F+
15	SIGNAL E-
16	SIGNAL C+
17	SIGNAL B-
18	SIGNAL A-
19	BIAS GND
20	SIGNAL Z+
21	SIGNAL X-
22	SIGNAL W+
23	SIGNAL U-
24	SIGNAL T-
25	SIGNAL R+
26	SIGNAL P-
27	SIGNAL M+
28	SIGNAL L+
29	SIGNAL J-
30	SIGNAL I+
31	SIGNAL G-
32	SIGNAL F-
33	SIGNAL D+
34	SIGNAL C-
35	SIGNAL A+
36	SIGNAL Z-
37	SIGNAL Y-
38	SIGNAL X+
39	SIGNAL V-
40	SIGNAL U+
41	SIGNAL S+
42	SIGNAL R-
43	SIGNAL N+
44	SIGNAL M-
45	SIGNAL K-
46	SIGNAL J+
47	SIGNAL H-
48	SIGNAL G+
49	SIGNAL E+
50	SIGNAL D-
51	SIGNAL B+

JDD JFET SERVICE 1

PIN #	PIN PURPOSE
1	Vss
2	V+
3	H+
4	V-
5	V-
6	H+
7	V+
8	Vss
9	BIAS GND
10	Vdd
11	H-
12	CHASSIS GND
13	H-
14	Vdd
15	BIAS GND

JDD' JFET SERVICE 2

PIN #	PIN PURPOSE
1	Vss'
2	V+'
3	H+'
4	V-'
5	V-'
6	H+'
7	V+'
8	Vss'
9	BIAS GND'
10	Vdd'
11	H-'
12	CHASSIS GND'
13	H-'
14	Vdd'
15	BIAS GND'

JCC' JFET INPUT 2

PIN #	PIN PURPOSE
1	BIAS V+'
2	BIAS V-'
3	SIGNAL Y+'
4	SIGNAL W-'
5	SIGNAL V+'
6	SIGNAL T+'
7	SIGNAL S-'
8	SIGNAL P+'
9	SIGNAL N-'
10	SIGNAL L-'
11	SIGNAL K+'
12	SIGNAL I-'
13	SIGNAL H+'
14	SIGNAL F+'
15	SIGNAL E-'
16	SIGNAL C+'
17	SIGNAL B-'
18	SIGNAL A-'
19	BIAS GND'
20	SIGNAL Z+'
21	SIGNAL X-'
22	SIGNAL W+'
23	SIGNAL U-'
24	SIGNAL T-'
25	SIGNAL R+'
26	SIGNAL P-'
27	SIGNAL M+'
28	SIGNAL L+'
29	SIGNAL J-'
30	SIGNAL I+'
31	SIGNAL G-'
32	SIGNAL F-'
33	SIGNAL D+'
34	SIGNAL C-'
35	SIGNAL A+'
36	SIGNAL Z-'
37	SIGNAL Y-'
38	SIGNAL X+'
39	SIGNAL V-'
40	SIGNAL U+'
41	SIGNAL S+'
42	SIGNAL R-'
43	SIGNAL N+'
44	SIGNAL M-'
45	SIGNAL K-'
46	SIGNAL J+'
47	SIGNAL H-'
48	SIGNAL G+'
49	SIGNAL E+'
50	SIGNAL D-'
51	SIGNAL B+'

Attachment of HRCR Item # 11:

JFET Module

Handling Document D-26790

Field Effect Transistor (JFET) Module 10209750-1

Prepared by: Kalyani Sukhatme 10 September, 2003

Revised by: Roger Welker & Steve Tseng 15 June, 2005

1. Introduction

This document provides guidelines for electrical handling for the SPIRE JFET Module.

1.1 Hardware Description

Each JFET module has two sets of 24 JFET channels. The JFET channels are populated on 1.0 micron thick Silicon Nitride membranes which provides thermal isolation. The operating temperature for these JFETs is ~120 K. The process of powering up the JFETs dissipates heat into the membrane resulting in a temperature increase with respect to the base temperature (4K to 10 K). Higher the power dissipation, higher is the temperature of the JFETs.

Each JFET channel consists of a matched pair of FETs (Figure 1.1-1) with a requirement for the offset voltage of less than **15 mV** between the matched pair. [The characteristic offset voltage is the difference between the source voltages (V_{sa} and V_{sb} with respect to ground) of the two FETs.]

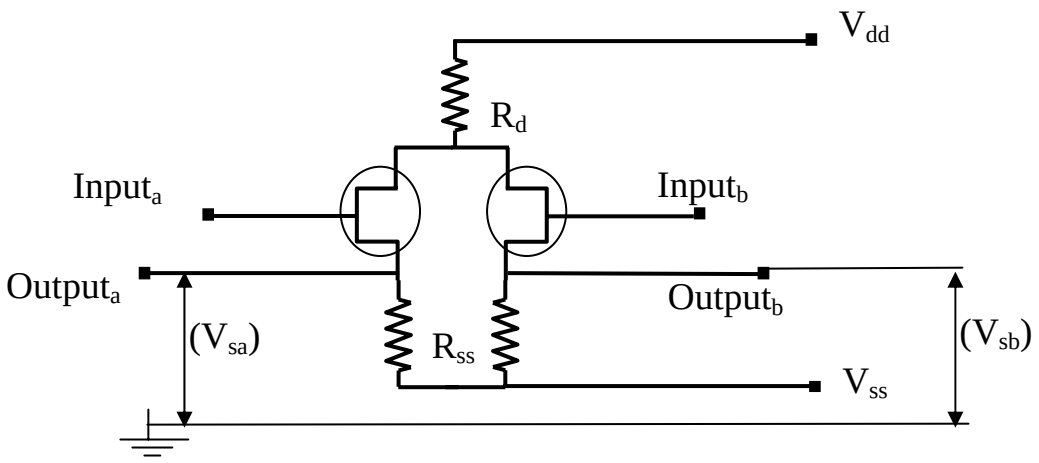


Figure 1.1-1

The Gates of the JFETs are the 'Inputs' of the circuit and the Sources (V_{sa} and V_{sb}) of the JFETs are the outputs, as marked in Figure 1.1-1. Vdd and Vss are the power lines for the circuit.

2. Handling

1. **The JFET Module is Contamination Sensitive**: Open shipment suitcase in an ISO 14644 Class 7 (FED-STD-209 Class 10,000) or cleaner cleanroom. Handle hardware with approved[1] nitrile or polyurethane ESD safe cleanroom gloves.

[1] JPL approved ESD safe cleanroom gloves are:

Nitrile:

Ansell-Edmont Nitrilite	http://www.ansellpro.com/ce/products3.asp?pid=87
Ansell-Edmont Nitrilite Silky	http://www.ansellpro.com/ce/products3.asp?pid=149
Ansell-Edmont Silky Ultra-Clean	http://www.ansellpro.com/ce/products3.asp?pid=150
Safeskin Critical (white)	http://www.safeskin.com/crit_nt_glv.asp

Polyurethane:

Wilshire Technology DuraCLEAN call in US, 323-259-6469 for ordering information

2. **The JFET Module is ESD Sensitive**:

Please handle with appropriate ESD hardware handling procedures. Handle with grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.

ESD: Handle with approved[2] wrist straps, ESD-safe gloves and ESD smocks at an approved ESD protected workstation[3]. All personnel within 1 meter of unprotected ESD sensitive hardware shall be certified for ESD awareness[4]. Maintain shorting plugs on the unit at all times, except when the unit is installed in the final assembly of the SPIRE instrument. JFET modules are shipped with two shorting plugs for ESD protection. Refer to attached electrical handling document for other important safety precautions. Follow all instructions for the use of wrist straps, ESD smocks, static protected work areas, ionizers, packing/unpacking and cable handling per JPL standard D-1348, rev. F (This document is available through the public domain by the following URL: http://acquisition.jpl.nasa.gov/rfp/miri/dewar/DL-2671-584331/JPL_D-1348.pdf).

ESD - Ionizer: Prior to mate or demate of any connector, turn on an ionizer approved[5] for ESD sensitive components in clean room environment at least 5 minutes in advance and place/hold both sides of the connections in front of the ionized air stream for a minimum of 10 seconds before mating/demating operation. Position the ionizer near the hardware within the required distance per manufacturer's manual. Different makes and models of ionizers have different positioning requirements. During the mating/demating operations, it is necessary to follow the requirements for handling ESD sensitive hardware.

ESD - Connection to GSE: It is essential to ensure that all signal and bias lines of the GSE are grounded prior to mating the JFET hardware to the GSE. A save-to-mate check must be performed prior to connecting the JFET to the GSE. No excessive voltages and currents on all signal and bias lines shall be observed while the hardware is connected.

QA Oversight: Quality Assurance personnel should witness all handling, electrical testing, operation and integration of JFET flight hardware. At a minimum, a "two person" rule should be invoked at all times, where oversight by an independent party is provided to ensure hardware safety during handling, test and integration operations.

Humidity Sensitive: Place hardware in a humidity controlled ISO 14644 Class 7 (FED-STD 209 Class 10,000) cleanroom. Maintain humidity level at 35%-50% RH typical, for ESD safety.

3. **The JFET Module is Fragile**: Please do not drop or otherwise shock the unit including the shipping suitcase and container. Do not remove the cover of the JFET Module.

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[2] JPL approved wrist straps are:
Speidel Twist-o-Flex ™ brand metal expansion bracelet wrist straps
3M model 4600 adjustable molded thermoplastic wrist straps

[3] All work areas shall be certified and operated in compliance with the requirements of the following subsections sections of JPL-STD D-1348 rev. F section 2.3: subsections: 6, 8-11, 14-19, 21, 23 – 27, 29 – 36, 38 – 43 and 45.

[4] All personnel shall be trained and certified to the requirements of section 2.3.3 of JPL STD_D-1348 rev. F.

[5] The ionizer performance shall be verified to comply with the requirements of JPL-STD-D-1348 rev. F, Table 1 for devices with human body model ESD sensitivity less than 50 volts. The ionizer shall discharge from ± 1000 volts to less than ± 20 volts in less than 20 seconds and have a float potential of less than ± 20 volts.

3. Power ON Procedure

1. The JFET Module should be powered on **WITH the shorting plugs** (JPL Supplied Protection connectors) in place and with the **inputs shorted to ground.** Pins #9 and #15 on the 15-pin MDM connectors on the JFET Module are the bias grounds on the module. These pins should also be shorted to the power supply ground. The unit may be powered up without the shorting plug only when the inputs are connected to the detector system.

   Under no circumstances the unit should be powered up without the inputs shorted to ground either via the shorting plug (JPL Supplied) or via the detector system.

2. Do not exceed a voltage of +5 V for the Vdd line and –5 V for the Vss line of the JFET Module.

3. When removing the shorting plugs from the unit for installation into the instrument, please use standard ESD precautions including grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.

4. Electrical Check-out Test: Characteristic Offset Voltage Measurement

1) Verify that the gates of the JFET channels (Inputs) are shorted together and grounded.
2) Apply the power supply ground to the bias ground pins on the unit (Pins 9 and 15 on the 15-pin MDM connectors)
3) Power on the JFET modules with Vdd = +3 V and Vss = -1.5 V
4) Verify that the handheld multimeter is in calibration.
5) Connect one side of the handheld multimeter to ground (Power supply ground).
6) And measure the voltage with respect to ground of each side (V_{sa} and V_{sb}) of each channel.
7) Calculate the characteristic offset voltage (V_{offset}) for each channel ($V_{offset}= V_{sa}-V_{sb}$)
8) Compare the values for each of the channels with the specific datasheet provided with the unit. The datasheets accompanying the unit also provides the values for the drain and source currents for a similar test performed at JPL.

REFER TO MEASURED SOURCE VOLTAGE DATA FOR ACTUAL HARDWARE. Here is an example of the source voltage values and the drain and the source currents obtained for such a test at room temperature are given in the Table 4-1

T, JFET	rm T	
Vdd	3 V	
Vss	-1.5 V	
Idd	1.564 mA	
Iss	1.5686 mA	
Channel #	(V)	DELTA (V)
1	1.130	0
	1.130	
2	1.075	0.001
	1.074	
3	0.781	0.001
	0.780	
4	1.088	0.005

	1.093	
5	0.834	0.001
	0.833	
6	1.012	0.003
	1.015	
7	0.785	0.002
	0.787	
8	1.148	0.004
	1.144	
9	0.753	0
	0.753	
10	0.693	0.008
	0.701	
11	1.110	0.004
	1.114	
12	0.758	0.001
	0.759	
13	0.832	0.002
	0.830	
14	1.264	0.001
	1.265	
15	1.206	0
	1.206	
16	0.818	0.001
	0.819	
17	0.526	0.005
	0.521	
18	1.423	0
	1.423	
19	0.773	0.002
	0.775	
20	0.873	0.004
	0.877	
21	1.387	0.006
	1.393	
22	1.417	0.003
	1.420	
23	0.887	0.002
	0.889	
24	0.888	0.003
	0.891	

- END OF -

Attachment of HRCR Item # 11:

“JFET Module Handling Document D-26790”

END OF

HRCR PACKAGE