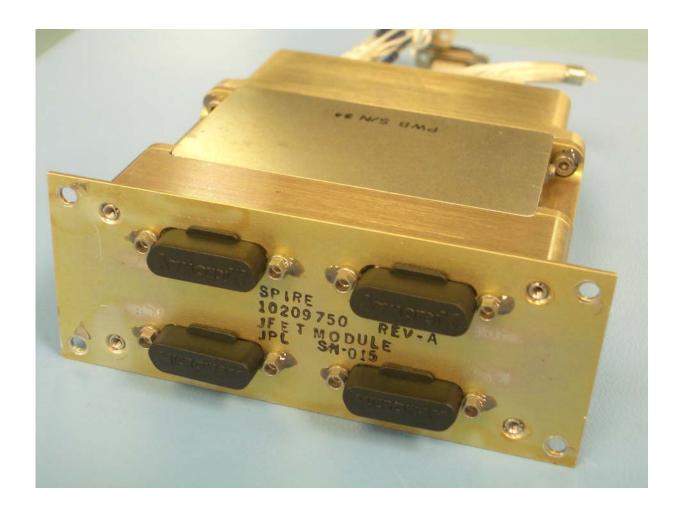
JPL Hardware Requirements Certification Review – SPIRE Element No. D-30476

JPL Hardware Requirements Certification Review – SPIRE Element No. D-30476

Assembly / Subsystem		PEM				Phone		Section		Date
SPIRE		Ма	rtin	Herr	nan	(818) 354-8	541	386		3 February, 2005
Drawing/ Part No.	Dwg. Rev.	No	men	clati	ure	Serial No.	Model	Туре	Final IR No.	Mass (Meas. / Req.)
10209750-1	В	JF	ET N	lodu	le	015	FLIGHT	N/A	923847	276.9 gm / 305 gm
Check applicable answer a explanation in remarks col		Y E S	N O	N A	R e	marks		Data Attachments		Signature & Date
Are all drawings and spec complete, approved, release		Х						14. Latest Top ☑ Attached	Assembly drawings None	Cognizant Engineer
2. Do the released drawings specifications reflect all appr		Х						15. List of open Attached	ECRs None	Mentina 2/18/05
3. Is hardware identical to o delivered? If no, provide diff		Х						16. Waivers (RF ☑ Attached	W request for waiver) ☐ None	QA Engineer 2/18/05
4. Does the hardware meet its functional requirements, specifications, waivers, ICDs?		Х	¥		EIDP attached. Also see item # 8 attachments.		17. Open MRB ☐ Attached ☐ None		Environments/Reliability A — Le 2/18/05	
5. Are all IR and MRB dispo concurred by QA?	sitioned and	Х		,				18. Open PFR o	n this H/W	Mission Assurance Mgr.
6. Is complete as-built list in included in the build book?	formation	Х						19. Open PFR on similar H/W Attached None		Project Office
7. Have all required environ analyses been completed?	mental tests &	Х			ETAS attached			20. Handling Do	cument →See Item 11 ☐ None	A ams . Sol 2/18/05
8. Is all required assembly a subsystem level functional to		Х			Performance Te Also see EIDP in		ied.	21. Shortage Lis Attached	t None	
9. Have all piece parts, proc materials been approved by		Х						22. Requirements Verification Matrix Attached (See #4, #7, #8) None		
10. Does this hardware mee contamination control require		X				es and MIUL met all 23. Quali control and out-gassing Attack			Status None	
11. Are all shipping containe special handling procedures		Х			See Attached Do	ocument D-26	ent D-26790 24. Mate / Demate Record Attached None			
12. Is additional work require hardware to flight readiness?	•		Х					25. Operating Lo		
13. Is this hardware accepta	able for flight?	X						26. MICD	None	



RAL EIDP Table of Contents Versus JPL HRCR Check List Item Numbers

RAL EIDP Section Number	RAL EIDP Title	JPL HRCR Check List Item Number	Notes
1	Shipping Documents		Shipper and Final IR
2	Transportation, Packing, Handling & Integration Procedures	11	Special Handling Document D-26790
3	Certificate of Conformance / Delivery Review Board MOM		HRCR book is the C of C
4	As Built Configuration Status List	1 & 2	Assembly Drawings
5	List of Waivers	4	RFW (request for waiver) Attached
6	Copies of Waivers	4 & 7	RFW (request for waiver) Attached
7	List of Non-Conformance Reports		See RFW in 4 & 7
8	Copies of Non-Conformance Reports		See RFW in 4 & 7
9	Cleanliness Statement		Final IR QA Inspection
10	Operational Manual		NA
11	Top Level Drawings (inc. Family Tree)	14	Top Assembly Drawing
12	Interface Drawings	26	MICD Drawing
13	Functional, Block & Mechanical Drawings		NA
14	Electrical Circuit Drawings		NA
15	Serialized Components List		In build books – not shipped
16	Mass Properties/ Power Budget	HRCR Check List Page 1	Mass listed in HRCR check list
17	Qualification Status List / Test Matrix	23	Qualification Unit Test Matrix
18	Test Reports	4, 7, 8, 23	
19	Open Work / Deferred Work / Open Tests		NA
20	Calibration Data		NA
21	Historical Record	23	Qualification Unit Test Matrix
22	Manufacturing Logbook(s)		In build books – not shipped
23	Operating Time / Cycle Record	25	
24	Connector Mating Record	24	
25	Age Sensitive Items Record		NA
26	Pressure Vessels – History/Test Record		NA
27	Temporary Installation Record		NA
28	Reference List of EIDPs (Lower level)		NA
29	Other Useful Information		NA

JPL Hardware Requirements Certification Review (HRCR)

Junction Field Effect Transistor (JFET) Flight Module

10209750-1 S/N 015

SPIRE Element
Herschel Space Observatory Project

February 3, 2005

Configuration of Module, Boards & Membranes

Module 10209750-1	S/N 15	S/N 15
PWB 10209760-1	S/N 34	S/N 35
Membrane 10209758-1	J6.4.1	J6.4.4

Attachment of HRCR Items #1 Drawing Release Status

ALL ASSEMBLY & PARTS DRAWINGS ARE RELEASED IN PDMS

Released Drawings:

10209719-1	assembly built per released Rev. A drawing (studlock)
10209722-1	assembly built per released Rev. B drawing (interface drawing)
10209750-1	assembly built per released Rev. B drawing (module assy)
10209751-1	assembly built per released Rev. B drawing (chassis 1)
10209752-1	assembly built per released Rev. A drawing (chassis 2)
10209753-1	assembly built per released Rev. A drawing (chassis 3)
10209754-1	assembly built per released Rev. C drawing (mount)
10209756-1	assembly built per released Rev. B drawing (chassis lid)
10209757-1	assembly built per released Rev. A drawing (membrane)
10209758-1	assembly built per released Rev. A drawing (membrane assy)
10209759-1,-2	2,-4 redlined Rev. B drawing (gasket)
10209760-1	assembly built per released Rev. C drawing (board assembly)
10209761-1	assembly built per released Rev. C drawing (solder connector)
10209769-1	assembly built per released Rev. A drawing (stiffener)
10209777-1	assembly built per released Rev. B drawing (board)
10209858-2	assembly built per released Rev. A drawing (special fastener)
10217636-1	assembly built per released Rev. A drawing (clip)

Attachment of HRCR Item #4: EIDP

EIDP Cov	verpage I	For JFET	Testing
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			LIDI	Coverpage	TOI SEE	resung	I	
Г	Unit Identfication							
	Name	:	JFET PFI	M Module				
	Part #	:	10209	750-1				
Г	S/N	:	#0	15				
Ξ								
┖	Environmemtal Testing	_						
		l	Axes	_	Duration/#			
┡		┞	Tested	Temp	of Cycle	Requirement	Source	Waiver
	Random Vibration Test	l	X, Y, Z	Rm T	1 min/axis	v v 7	SSSD, JFET-DES-07	
Н	Random vibration rest	┝	7, 1, 2	RIII I	1 IIIII V d XIS	Λ, Ι, Δ	SSSD.	HR-SP-JPL-
	High Level Sine Vibe Test	l	None	NA	NA	X, Y, Z	JFET-DES-07	RFW-005
Н	Bakeout	t	NA	80 C	26 hrs	> 24 HRS		
Н	Thermal Cycles	H	NA NA	RmT to 80 K	2	Minimum 1	D-20549	
	•						2 223 13	
L	Performance Characteristics	_						
				Specific			Source	Waiver
	Power needed for <11 bad channels		0.44	11 mW fo			SSSD,	HR-SP-JPL-
	(Min Perf.) Power needed for <4 bad channels	-	8.11 mW	7 mW for i		JFE1-TEC	-05, JFET-PER-02 SSSD.	RFW-004
	(Design Value)	l	8.24 mW	7 mW for i		JEET-TEC	-05, JFET-PER-02	
Н	Power needed for 100 %	t				0.2.12		
	Yield per unit	l	9.14 mW	N.A	4		NA	
	Median Noise at < 11 bad chs.		10.17 nV/rtHz	<15 nV/rtHz	<7 nV/rtHz	SSSD,	JFET-PER-01	
	Median Noise at < 4 bad chs.	Γ	8.88 nV/rtHz	Min	Design	SSSD,	JFET-PER-01	
	Median Noise at 100 % Yield.	Γ	7.30 nV/rtHz	Performance	Value	SSSD,	JFET-PER-01	
	# of Channels over the	Γ					SSSD,	
L	max. offset voltage	L	0	< 15 mV			BDA-DRCU-27	
L	Common Mode Rejection Ratio	L	< -80 dB by design, as measured in EM4 unit			nit	SSSD, BDA-DRCU-11	
Н	Board Level Details	_						
		ı		SN 034 -JDD)		rd SN 035 VA'-JDD')	Source	
Н	# Channels Tested		24	-500)	24	VA -200)	Source	
Н	# Charmers resieu	Ė	24		24		SSSD.	
	Median Noise at 3.5 mW	:	19.35	nV/rtHz	15.9	92 nV/rtHz	JFET-PER-01	
	# of good channels	T		37.5%		45.8 %	SSSD,	
	at 3.5 mW	:	9	Yield	11	Yield	JFET-PER-02	
	Power Needed for				4.40		SSSD,	
H	100 % Yield Median Noise at High Power (w/ 100	1	4.72		4.42 mW		JFET-PER-02 SSSD.	
	% Yield)		7.32 n	V/rtHz	7.2	4 nV/rtHz	JFET-PER-01	
	Median Gain at High Power	f		98		0.98	NA NA	
	Heater Resistance, 4K Reference valu		2.92	2 kΩ	3	.01 kΩ	NA	
Г	Definitions	Γ						
	Good Channels	:	Noise less than	n a min. perform	ance value o	f 15 nV/rtHz		
	Yield	:	# of Good Channels / 24					
	Filenames	Γ						
	Noise Measurements	:	JFET_Mod15_	brd34, 35_Nois	e_perf.pdf			
	Source Voltages (RmT, 4K)	:	JFET Module 1	12,15 voltage da	ata.pdf			
	Notes							
1)	The Base temperature for all performa	no	e characterizati	on was 4K				
2)	All Noise Measurements were made w	ith	the inputs shor	ted to ground				
2)	Type of membranes:	Π		veretched Perf	orated	SN035: 31% Out	etched Perforated	
(د	Type of memoranes.		5/4057. 3376 C	veretorieu nem	orateu	514035. 31% OVER	etoried i eriorated	
_		_						

Attachment of HRCR Item #4: RFW (request for waiver)

		RFW/RFD Number:	HR-SP-JPL	RFW-016
Spacecraft / Project	Herschel	Originator's Name	Steve Tseng	
System / Experiment / Model	1.1 SPIRE	Signature / Date		
Sub-System	detectors	Request Type (Highlight applicable request)	Waiver (RFW)	Deviation (RFD)
Assembly	JFET modules	1.1.1.1 Organisation	Jet Propulsion	Laboratory
Sub-Assembly		Ref. Doc. / Drwg No.	SPIRE-JPL-P	RJ-000456
Item		References		
Serial No.		I/GIGIGIICG3		
RFW/RFD Title	JFET Power Dissipation s/n 01	15		

End Items(s) Affected (Hardware, Software)							
Name	CI-N	umber		Model(s)			
JFET Module p/n 10209750 s/n 015			PFI	И			
ı	Requirement / Interface Doc	uments Affect	ed				
Specification/Drawing Title	Number	Issue	Date	App. Paragraph			
BDA-SSSD	SPIRE-JPL-PRJ-0004456	3.2	7/1/03	JFET-PER-01			
BDA-SSSD	SPIRE-JPL-PRJ-0004456	3.2	7/1/03	JFET-PER-01 JFET-PER-02			
BDA-SSSD	SPIRE-JPL-PRJ-0004456	3.2	7/1/03				

Requirement states that dissipation of photometer JFETs is to be less than 7 mW average, while supplying 90% of channels with voltage noise < 15 nV/rtHz according to BDA-SSSD JFET-PER-01, JFET-PER-02, JFET-TEC-05. Measured JFET performance of the JFETs indicates that 8.11 mW of power dissipation will be required to meet the specified yield and noise performance specifications.

Other Items or Requirements (Potentially) Affected

Overall sensitivity of the bolometer sub-system is affected by JFET noise performance. JFET power dissipation impacts the heat sink temperature of the 3He refrigerator and may in turn increase the base detector temperature. Dissipation of JFETs affects power dissipation on cryostat.

Need for RFW/RFD and Rationale for Acceptance

Measured JFET performance of JFETs indicates that 8.11 mW of power dissipation will be required to meet the specified yield and noise performance specifications. JPL is unable to significantly alter the JFET fabrication process in order to meet the power specification without undue risk to the stated PFM/FS delivery dates. Furthermore, JPL requests a full system optimisation to revisit the noise and power requirements on the JFETs. The JFET modules can meet the noise design value with 100 % yield at 9.14 mW.

	Approved	Rejected	Name	Date
Engineering:				
Product Assurance:				
CCB-Chairman:				
Principal Investigator				
Product Assurance:				
Co-Investigator				
Prime Contractor				
ESA Project Office				

Attachment of HRCR Item #7: RFW (request for waiver)

		RFW/RFD Number:			HR-SP-JPL-RFW-005		
Spacecraft / Project	Herschel		Originator's Name	iginator's Name Kalyan		lyani Sukhatme	
System / Experiment / Model	SPIRE		Signature / Date				
Sub-System	detectors		Request Type (Highlight applicable reque	est)	Waiver (RFW)	Deviation (RFD)	
Assembly		Organisation Jet Propulsion		n Laboratory			
Sub-Assembly			Ref. Doc. / Drwg No. SPIRE-JPL-PRJ-00045		RJ-000456		
Item			References				
Serial No.			References				
RFW/RFD Title	BDA and JFET module sine test deletion						

End Items(s) Affected (Hardware, Software)									
Name CI-Number Model(s)									
Bolometric Detector Assemblies CQM, PFM, FS									
JFET Modules				CQM, PFM, FS					
D	anvironant / Interfera Dec	Affaat	- al						
	equirement / Interface Doc	_	1						
Specification/Drawing Title	Number	Issue	Date	App. Paragraph					
BDA-SSSD (SPIRE-JPL-PRJ-		3.2	Jan 7,	BDA-DES-10, JFET-DES-					
000456)			2003	07					
Descript	ion of Deviation / Discrepa	ncy / Non-Conf	ormano	ce					
High Level Sine- Vibe Test is not perfore	med on these units								
Other Items or Persinguents (Petentially) Affected									
Other Items or Requirements (Potentially) Affected									

Need for RFW/RFD and Rationale for Acceptance

The hardware has to be qualified under a cold vibration test and is installed in the cold vibration facility for the purpose of the test. The high level sine vibration test configuration will put the hardware and the personnel at risk since the cold vibration facility is not structurally capable of withstanding the high levels. Obtaining additional resources (cost and schedule) for developing a new set-up is not feasible at this time.

	Approved	Rejected	Name	Date
JPL Engineering:				
JPL Product Assurance:				
CCB-Chairman:				
Principal Investigator				
Product Assurance:				
Co-Investigator				
Prime Contractor				
ESA Project Office				

Attachment of HRCR Item #7: ETAS (environmental test summary)

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 | REP DATE 2/7/03 ON ACCUMULATED OF OPERATING HOUR N RMAL VACUUM RE: <10E-5 RT. C L K K YCLES: 2-1-1-2 TEMP. I S NOS. / BRIEF EXP NOS. / BRIEF EXP TOS. / BRIEF EXP TOS. / BRIEF EXP TOS. / BRIEF EXP TOS. / BRIEF EXP | DERATING HOURS PRISON TEMPERATURE NO OF CYCLES: LEVEL ("c) AND ACCUMOT: "c; HOT: "c; LANATION LANATION TO BE TAKEN ENVIRONMENTAL | MENTAL EXPOSURI THE ATMOSPHERE JIMULATED DURATI | PIRONMENTAL TEST E ON (HRS.) "c, h "c, h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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Attachment of HRCR Item #7: ETAS (environmental test summary)

					E 1 JPL 2683 R 1/98 FF
JPL	ENVIRONMENTAL TE		the state of the s	AND DESCRIPTION OF THE PARTY OF	AS)
and a second second second	OTHER AUTHORIZATION	PHOVISIONS AN	DEXFLANATIO	/N3	
	es will also be completed.				
xis vibe was completed a	and is carried on AIDS#'s	243946 and 2441	64, ETAS#'s	HSO31 nad HSC	32.
E 2 JPL 2683 R 1/98 FF					

Attachment of HRCR Item #7: ETAS (environmental test summary)

	COMMENTS	
Y (ETAS)	PASS/ FAIL	
D SUMMARY	TEST AGENCY	
FAL TES THORIZATION AND SUI	DATE TEST PERFORMED	
ENVIRONMENTAL TES THORIZATION AND SUMMARY (ETAS) ENVIRONMENTAL TEST SUMMARY	TEST ENVIRONMENT LEVELS & DURATION	cycles. <10E-5 mbar, <70K to R.F.
ENVIE	ETAS	HSO37
	N/S	5
4	HARDWARE	SPIRE JFET (10209750-1)

Attachment of HRCR Item # 8: Test Data - Source Voltage & Noise For Module 15

JFET SOURCE VOLTAGE MEASUREMENT

		Post Vibe,	post bake,	SN12,15 m	odule, grn o	dewar, rm T.				PERF TES	T Post Vibe	, post bake	post bake, SN12,15 n		dewar, Hel	lium.	
Date		11/5/	2004	11/5/	2004	11/5/	2004	11/5/	2004	11/9/	2004	11/9/	2004	11/9/	2004	11/9/	2004
T, plate		Rn	n T	Rn	ı T	Rn	ı T	Rn	n T	4	K	4	K	4	K	4	K
		Rn		Rn		Rn		Rn		4			K	41		4	
Vdd Vss		-1		1		-1		-1	5		3		.5	3 -1.		-1	
ldd			288	0.9		1.3			345	0.9		0.9		1.10		1.02	
lss			269	9.0		1.2		1.1			608		258	1.10		1.02	
SN		2	2	2	3	3	4	3	5	2	2	2	3	34	4	3	5
Channel#			DELTA		DELTA		DELTA		DELTA		DELTA		DELTA		DELTA		DELTA
1	a	1.002	0.003	0.973	0.003	0.977	0.001	1.125	0.002	0.691	0.007	0.643	0.004	0.685		0.829	0.003
1	b	0.999	0.003	0.976	0.003	0.978	0.001	1.123	0.002	0.684	0.007	0.647	0.004	0.684	0.001	0.826	0.003
2	a b	1.041	0.002	1.587	0.009	1.039 1.038	0.001	0.746	0.005	0.729	0.005	1.283	0.006	0.749 0.745	0.004	0.434	0.006
<u> </u>	a	1.043		1.516		1.214		1.196		0.725		1.209		0.743		0.901	
3	b	1.042	0.005	1.524	0.008	1.211	0.003	1.196	0	0.730	0.005	1.216	0.007	0.927	0.003	0.901	0
4	a	0.981 0.980	0.001	0.980	0.003	0.894 0.889	0.005	1.149	0	0.662 0.662	0	0.649 0.644	0.005	0.599 0.595	0.004	0.849 0.852	0.003
<u> </u>	b a	1.420		0.977		1.781		0.921		1.102		0.644		1.520		0.852	
5	b	1.429	0.009	0.965	0	1.793	0.012	0.926	0.005	1.109	0.007	0.632	0.002	1.534	0.014	0.624	0.008
6	a	1.745	0.013	1.727	0.013	0.974	0.002	0.960	0.001	1.466	0.011	1.405	0.014	0.661	0	0.657	0
	b a	1.758 0.974		1.714 1.342		0.972 0.996		0.961		1.477 0.651		1.391		0.661		0.657 0.808	
7	b	0.970	0.004	1.335	0.007	1.000	0.004	1.107	0.001	0.648	0.003	1.014	0.007	0.695	0.006	0.805	0.003
8	a	1.000	0.001	0.897	0.002	0.962	0.004	0.820	0.005	0.682	0.002	0.565	0.007	0.666	0.003	0.509	0.006
	b a	0.999 0.964		0.895 1.415		0.966 1.048		0.825 1.286		0.680 0.638		0.558 1.093		0.669		0.515	
9	b	0.965	0.001	1.413	0.007	1.045	0.003	1.279	0.007	0.641	0.003	1.093	0.006	0.748	0.005	0.984	0.008
10	a	0.973	0.001	1.058	0	0.981	0.003	1.314	0.005	0.649	0.002	0.727	0.001	0.683	0.002	1.020	0.003
	b	0.972	0.001	1.058		0.978		1.319	0.000	0.647	0.002	0.726	0.001	0.681	0.002	1.023	0.000
11	a b	0.969 0.972	0.003	0.527 0.515	0.012	1.157 1.155	0.002	0.970	0.002	0.637 0.642	0.005	0.168 0.156	0.012	0.856 0.857	0.001	0.651	0.001
12	a	0.971	0.002	0.918	0.009	1.311	0.007	0.950	0.003	0.641	0.003	0.573	0.009	1.024	0.006	0.639	0.004
12	b	0.973	0.002	0.927	0.009	1.318	0.007	0.947	0.003	0.644	0.003	0.582	0.008	1.030	0.000	0.635	0.004
13	a b	0.970	0.002	1.414	0.009	1.011	0	0.971	0.003	0.645 0.649	0.004	1.097	0.008	0.708 0.708	0	0.653	0.003
14	a	1.246	0.006	0.961	0.002	1.061	0.003	0.987	0.001	0.933	0.004	0.622	0.003	0.754	0.003	0.673	0.002
17	b	1.240	0.000	0.963	0.002	1.064	0.003	0.986	0.001	0.929	0.004	0.625	0.003	0.757	0.003	0.671	0.002
15	a b	1.307	0.015	0.962 0.962	0	1.172 1.176	0.004	0.847 0.845	0.002	0.992 0.982	0.01	0.613 0.615	0.002	0.877 0.882	0.005	0.519 0.516	0.003
16	a	1.534		1.749		0.745		1.113		1.242		1.451		0.422		0.805	
16	b	1.540	0.006	1.759	0.01	0.757	0.012	1.114	0.001	1.246	0.004	1.461	0.01	0.434	0.012	0.804	0.001
17	a b	1.116	0.007	1.002	0.006	1.145	0.001	0.991	0.003	0.806 0.813	0.007	0.675	0.005	0.851	0.002	0.682	0.003
<u> </u>	a	0.961		1.008		1.144		1.067		0.646		0.769		0.856		0.762	
18	b	0.960	0.001	1.094	0.001	1.152	0.006	1.064	0.003	0.641	0.005	0.770	0.001	0.861	0.005	0.756	0.006
19	a	0.931	0.003	0.970	0	0.889	0.001	0.506	0.008	0.619	0.003	0.641	0.001	0.594	0.003	0.181	0.008
L	b a	0.934 0.963		0.970 0.846		0.888 1.119		0.498		0.622 0.633		0.642 0.515		0.591 0.824		0.173 0.652	
20	b	0.964	0.001	0.849	0.003	1.116	0.003	0.976	0.004	0.636	0.003	0.519	0.004	0.824	0	0.649	0.003
21	a	0.965	0.001	1.641	0.01	1.164	0.005	1.358	0.001	0.650	0.002	1.341	0.01	0.874	0.006	1.071	0
	b a	0.964 1.022		1.631 1.672		1.169 1.256		1.359		0.648 0.712		1.331		0.880		1.071 0.743	
22	b	1.022	0.004	1.667	0.005	1.255	0.001	1.044	0.001	0.712	0.002	1.373	0.003	0.970	0.002	0.743	0
23	a	1.007	0	0.961	0.001	1.700	0.011	0.963	0.003	0.694	0.002	0.639	0.006	1.437	0.012	0.657	0.002
	b	1.007 0.982		0.960 1.706		1.711 1.058		0.960		0.696 0.668		0.633		1.449 0.769		0.655 0.670	
24	a b	0.983	0.001	1.695	0.011	1.055	0.003	0.981	0	0.668	0	1.407	0.011	0.767	0.002	0.674	0.004

Attachment of HRCR Item #8: Test Data - Source Voltage & Noise

Board S/N 034 in Module S/N 015

		Pwr1	Pwr2	Pwr3	Pwr4	Pwr5	Pwr5b	Pwr7	Pwr8	Pwr9	Pwr10	Pwr11	Pwr12	Pwr13	Pwr14
	Vdd (V)	2.5	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.82	2.84	2.87	2.8
	Vss (V)	-1.5	-1.7	-1.6	-1.5	-1.4	-1.45	-1.47	-1.46	-1.48	-1.25	-1.45	-1.45	-1.45	-1.45
	Vdď (V)	2.205	2.477	2.49	2.503	2.516	2.51	2.507	2.508	2.505	2.535	2.529	2.549	2.578	2.509
	Vss' (V)	-1.212	-1.385	-1.298	-1.21	-1.124	-1.1667	-1.1841	-1.1754	-1.1926	-0.9929	-1.1667	-1.1664	-1.1664	-1.1665
	Idd (mA)	1.1353	1.2431	1.1935	1.1431	1.0929	1.118	1.128	1.123	1.133	1.0169	1.1185	1.1189	1.1197	1.1179
	Iss (mA)	1.0967	1.2032	1.1538	1.1034	1.0534	1.0784	1.0884	1.0834	1.0934	0.9778	1.0788	1.0792	1.08	1.0783
	I (mA)	1.116	1.22315	1.17365	1.12325	1.07315	1.0982	1.1082	1.1032	1.1132	0.99735	1.09865	1.09905	1.09985	1.0981
	P (mW)	3.813372	4.7238053	4.4457862	4.17062725	3.906266	4.03775194	4.09047702	4.06352688	4.11616832	3.518551065	4.060280805	4.08341037	4.11827834	4.03606655
	Channel Num	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz	Vn @150 Hz
15	Channel: 1	7.25	6.63	7.29	7.36	6.89	7.51	5.51	6.60	6.67	7.70	6.85	7.19	6.57	5.61
14	Channel: 2	20.95	9.40	12.63	11.83	17.29	14.91	13.23	15.81	12.17	25.80	12.55	12.05	10.74	13.46
13	Channel: 3	23.13	8.25	9.89		22.89	17.25	14.94	14.44	15.32	25.46	15.32	15.41	14.39	19.17
12	Channel: 4	7.80	7.33	6.39		7.56	6.04	6.77	7.89	6.77	15.64	5.14	6.65	7.55	7.09
10	Channel: 5	7.68	7.04	5.61	6.01	5.18		7.29	5.27	6.34	8.07	5.63	5.93	8.12	5.66
9	Channel: 6	15.19	9.70		14.51	13.97		14.72	12.66	14.04	22.84	14.75		12.73	15.07
8	Channel: 7	15.87	7.61	8.00	9.57	12.75		9.67	9.21	10.78	31.31	11.88	10.21	10.09	11.43
7	Channel: 8	6.29	6.58	7.97	7.43	7.24		7.10	5.97	4.94	7.94	5.46	7.63	7.67	5.90
6	Channel: 9	7.67	12.84	11.56	9.10	6.99		8.86	8.51	7.28	7.68	8.82	9.92	9.74	8.18
5	Channel: 10	22.10	12.23	11.88			16.95	16.15	15.55	14.87	17.78	15.40	16.86	17.30	14.61
4	Channel: 11	9.71	8.34	8.46		9.79		9.06	7.31	7.37	20.65	8.58	8.16	11.04	8.61
3	Channel: 12	16.51	7.30	9.97	11.97	16.15	15.03	14.53	13.22	13.96	28.38	12.45	12.67	16.23	14.49
28	Channel: 13	12.36	7.67	8.43		9.26		9.65	9.93	9.10	11.17	10.04	10.56	9.59	8.60
27	Channel: 14	20.74	7.23	7.49			12.30	11.28	11.54	9.54	36.05	12.63	12.71	13.36	11.37
26	Channel: 15	17.70	7.27	8.27	9.50	12.71	10.23	8.98	9.49	8.36	47.45	9.02	10.20	9.71	10.18
25	Channel: 16	10.90	5.99		7.98	9.10		7.78	7.74	7.57	20.12	7.64	8.80	7.25	7.26
24 23	Channel: 17 Channel: 18	18.85 18.03	7.31 6.52	6.81 9.33	14.41 12.51	15.27 16.97	15.19 15.04	12.55 11.38	15.24 14.87	14.26 13.02	20.66 32.09	14.27 12.63	14.82 12.14	16.84 12.12	14.41 14.07
22	Channel: 19	14.11	7.85	7.67	9.69	11.52	10.61	9.01	9.41	9.47	18.59	10.39	10.01	9.57	12.52
21	Channel: 20	6.79	5.56	7.62	6.40	7.64		6.28	6.92	6.39	11.92	5.56	7.60	6.82	6.15
19	Channel: 21	55.55	14.67	19.34	33.31	51.83	40.98	38.62	44.99	41.44	64.83	41.75	36.89	37.97	50.45
18	Channel: 22	8.85	7.38	6.37		6.88			6.31	6.58	9.12	7.24	6.55	6.22	6.81
17	Channel: 23	7.57	5.71	6.12		5.66		6.67	5.85	6.72	11.12	6.16	6.53	5.50	6.58
16	Channel: 24	8.09	6.59			8.12			7.23	7.03	11.33	8.11	8.17	9.02	9.37
	Median	13.24		8.13		10.66		9.03	9.31	8.73	19.35	9.53	10.11	9.73	9.78
	Overall Mean	14.99		9.04	10.71	13.25			11.33	10.83	21.40	11.18	11.33	11.51	11.96
	Good Mean	8.85		8.59		8.83			9.02	9.24	9.56	9.32		9.39	9.64
	MP Regd			3,00		15									
	Yield	0.54	1.00	0.96	0.96	0.67	0.71	0.92	0.83	0.92	0.38	0.88	0.88	0.83	0.88
	# Good Ch.	13		23		16			20	22		21	21	20	21
	# Bad Ch.	11	0	1	1	8	7		4	2		3		4	3

Attachment of HRCR Item #8: Test Data - Source Voltage & Noise

Board S/N 035 in Module S/N 015

	Pwr1	Pwr2	Pwr3	Pwr4	Pwr5	Pwr5b	Pwr7
Vdd (V)	2.8	2.8	2.8	2.8	2.8	2.8	2.8
Vss (V)	-1.5	-1.6	-1.55	-1.7	-1.57	-1.65	-1.35
Vdd' (V)	2.527	2.515	2.521	2.5016	2.518	2.508	2.545
Vss' (V)	-1.2319		-1.276	-1.407	-1.293	-1.363	-1.1
Idd (mA)	1.051	1.0653	1.075	1.1478	1.0847	1.1236	0.9772
Iss (mA)	1.0168	1.0994	1.0407	1.1133	1.0502	1.0891	0.9434
I (mA)	1.0339	1.08235	1.05785	1.13055	1.06745	1.10635	0.9603
P (mW)	3.88632671	4.15081225	4.01665645	4.41886773	4.06805195	4.28268085	3.5002935

Channel Num			Vn @150 Hz				
Channel: 1	7.94	9.94	15.60	8.06	8.43		12.88
Channel: 2	8.24	5.46	8.12	6.59	7.09	6.79	15.02
Channel: 3	6.89	5.30	6.94	6.83	6.02	5.77	9.37
Channel: 4	7.49	7.69	6.85	8.81	7.94	8.80	9.02
Channel: 5	12.47	7.91	9.43	7.24	9.49	6.72	
Channel: 6	6.06	5.38	6.67	6.40	5.82	6.53	
Channel: 7	15.84	7.73	10.69	6.92	10.17	6.93	23.09
Channel: 8	6.97	5.83	7.55	5.47	6.70	6.77	8.81
Channel: 9	26.80	19.64	23.86	11.78	20.62	13.92	33.02
Channel: 10	10.17	8.70	8.25	6.78	7.95	9.20	12.89
Channel: 11	10.08	9.20	7.49	10.40	9.65	9.61	9.91
Channel: 12	19.74	12.38	13.89	7.24	13.37	8.14	
Channel: 13	11.07	8.13	11.67	8.42	10.74	9.03	
Channel: 14	18.31	14.19	16.04	10.49	16.92	12.86	36.78
Channel: 15	45.18	24.40	30.21	10.93	27.32	15.37	85.29
Channel: 16	9.51	8.23	8.43	5.82	7.50	7.61	17.77
Channel: 17	14.61	8.89	10.56	5.82	9.23	7.74	27.82
Channel: 18	12.53	11.62	11.47	9.09	11.20	9.60	
Channel: 19	8.63	8.50	7.25	7.14	6.84	7.28	14.23
Channel: 20	12.03	11.06	10.94	13.11	12.17	13.23	
Channel: 21	20.04	14.62	16.68	7.37	16.08	9.97	24.00
Channel: 22	5.30	6.66	5.01	6.34	5.71	6.35	
Channel: 23	6.76	6.05	6.35	5.70	8.42	6.61	16.82
Channel: 24	6.51	8.58	6.88	7.63	7.31	6.38	8.98
Median	10.12	8.54	8.93	7.24	8.83	7.94	15.92
Overall Mean	12.88	9.84	11.12	7.93	10.53	8.74	21.04
Good Mean	9.07	8.73	8.65	7.93	8.59	8.45	10.29
MP Reqd					15		
Yield	0.75	0.92	0.79	1.00	0.83	0.96	0.46
# Good Ch.	18	22	19	24	20	23	11
# Bad Ch.	6	2	5	0	4	1	13

Attachment of HRCR Item # 9: SPIRE MIUL Cover Page

MIUL = Material Identification & Utilization List

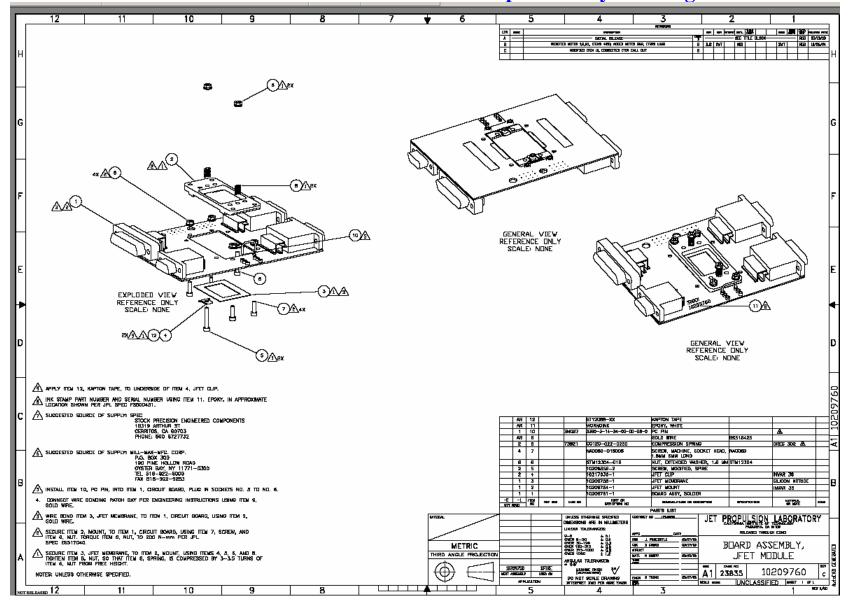
Declared Materials List's and Processes List are not included in this HRCR

Materials and Processes List
SPIRE
or me
JPL D-25725
REV B
Management of the second of th
1/05/04
This technical data is export controlled under U.S. law and is being transferred by JPL to ESA
for use exclusively so the Herschell Disaster The information of the Property
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Reviewed by:
M. Knopp M&P Engineer
W. Khopp War Engineer
9

Attachment of HRCR Item #11:

See End of This HRCR Package for "JFET Module Handling Document"

Attachment of HRCR Item # 14: JFET Module Top Assembly Drawing 10209750-1



Attachment of HRCR Item #23: Qualification Compliance Test

Qualification Model JFET Module

		EID	P Coverpage	For JFET Te	sting		
Unit Identfication						1	
Name	T-	JEET O	M Module				
Part #	-		9750-1				
S/N	-		001				
5/14	-	77	001				
Environmemtal Testing							
	Π	Axes		Duration/# of			
	┖	Tested	Temperature	Cycle	Requirement	Source	Waiver
						SSSD,	
Random Vibration Test	╄	X, Y, Z	100 K	2 min/axis	X, Y, Z	JFET-DES-07	
l						SSSD,	HR-SP-JP
High Level Sine Vibe Test	⊢	None	NA	NA	X, Y, Z	JFET-DES-07	RFW_005
Bakeout	╄	NA	80 C	72 Hours	80C, 72 Hrs	D-20549	
Thermal Cycles		NA	RmT to 80 K	27	Minimum 15	D-20549	
Performance Characteristics	;						
	Т		Specif	ication	s	ource	Waiver
Power needed for <11 bad	T			or CQM.		SSD.	RFW in
channels (Min Perf.)		9.1 mW		PFM/FS	· -	550, 5, JFET-PER-02	process
Power needed for <4 bad	\vdash	e. i ilivv		or CQM.		SSD.	process
channels (Design Value)		10.8 mW		PFM/FS	I -	5, JFET-PER-02	
Power needed for 100 %	T	10.0 1111	7 11177 101		0.2200	0,012112102	
Yield per unit	13.5 mW NA					NA	
Median Noise at < 11 bad chs.	T	7.13 nV/rtHz			SSSD. J	FET-PER-01	
Median Noise at < 4 bad chs.	T	6.1 nV/rtHz	Min	<7 nV/rtHz	FET-PER-01		
Median Noise at 100 % Yield.	\vdash	6.97 nV/rtHz		Design Value		FET-PER-01	
# of Channels over the	\vdash		< 15 mV for C0			SSSD.	
max. offset voltage		0	< 15 mV for PF	M/FS		BDA-DRCU-27	
	П					SSSD,	
Common Mode Rejection Ratio		< -60 dB by d	esign, as meas	ured in EM4 un	it	BDA-DRCU-11	
Board Level Detail							
		Board	SN 001			Source	
# Channels Tested	:	24					
						SSSD,	
Median Noise at 3.5 mW	:	18 n	V/rtHz			JFET-PER-01	
# of good channels				1		SSSD,	
at 3.5 mW	:	7	29% Yield	_		JFET-PER-02	
Power Needed for		0.75 14				SSSD,	
100 % Yield Median Noise at High Power (w/	:	6.75 mW		-		JFET-PER-02 SSSD.	
100 % Yield)		8.07	nV/rtHz			JFET-PER-01	
Median Gain at High Power	+		.98	-		NA	
mestali cali at riigii i owei	+	, ·	.00	 		150	
	+					L	
Definitions	۲			I		I	
Good Channels		Noise loss than	a min. performar	l see value of 15 ml	//etil=	l .	1
Yield		# of Good Char		ice value or 10 h	инп4		
Filenames	-	or Good Char	iiieis / 24			1	
	+	OwellECTO: "	Chablaine Com				
Noise Measurements	H	Qualife i Post	/ibeNoise_Summ	ary.pur			
Notes	+						
The Base temperature for all performa	l nno-	obarantorization	n was AV				
All Noise Measurements were made v	vitri	the inputs shorte	ea to grouna				+

Attachment of HRCR Item # 24 & #25: Mate/Demate & Operation Logs

Date	Time	AIDS	Power	Mate	Demate	Transport	Notes
1/5/04		244299		×		×	103 -> 183
1/5/04		~	X				.5 hr each board, wrm S.V.
15/04	1	~					prop ort
19/04		-					transfer LN2 (77K)
19/04		~					transfer holim (4K)
19/04			×				11 12 12 12 12
110/04		<i>(t)</i>					4 hours, bond 34, mise data
		<u> </u>	χ.				8 hrs , " "
111/04			× ×				11 11 11
112/04		-	_×				8 hrs, board 35, noise data
112104		-	×				2 hrs, board 34, gain duta, CMR
112/04	<u> </u>		_×				, Jan , J.N-
/16/04		 	s.	N:			beah warn up
/16/09		· · · ·		λ .	×		switch connector to fix goob w/ SNI
117104	<u> </u>						go to LNZ helium
119/04		ď	×				
(19/04		0	×	:			(6 hrs , band 22 , noise data
122/04		c	X				2 hrs, board 22, noise data
122/04		~					6 hrs board 23, poised data
123 /04	:	"	Υ X	.			2 hr
123 /04		4	×				3 WS " GAIN, CMRR
123104		(-	x				3 ks, boad 22 gain, CMRC
130/04		"	×				. 5 hr each board, wm s.V.
11/04					*	*	183 - 103
						1.	
·							

Attachment of HRCR Item # 24 & #25: Mate/Demate & Operation Logs (continued)

Date	Time	AIDS	Power	Mate	Demate	Transport	Notes
125/04	9 A	244163				×	103 → 158
126104		**					Pump out, Stort Rakent to 80
128/04	10 A					×	Pump out, Stort Bakent to 80
季10/29	30	244164	×				.5 hr each board wim s.
/1	1030 A	re				X	183 -> 144
(1	_	11					3 axis worm shake
12	Afternoon	1/	_	_	-	- 1	Transfer to ESD bags
14	9:00 am.						Install into Green Dewar
(4		"	×				.5 hr each board , win S.V.
14						×	183 -> 103 (Mod 14 bad S.V.)
			N 7				PFR 284 924
			:				
					<u> </u>		
<u> </u>							
				:			
			:				
				er.			
						,	
			3 B				

Attachment of HRCR Items # 24 & # 25: Mate/Demate & Operation Logs (PWB S/N 034)

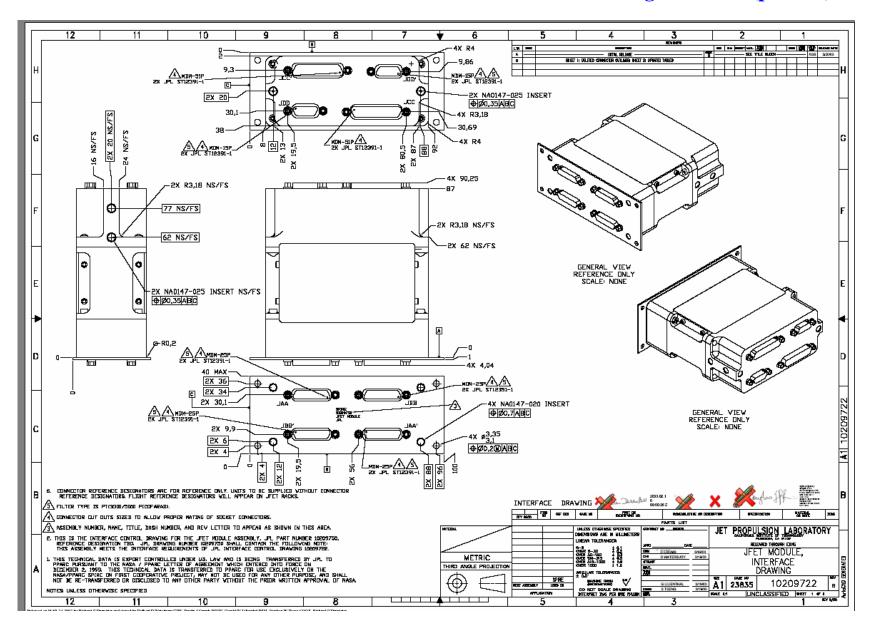
DEVICE (BRD) S/N: 3	4 (48		OJECT:	SE THI SPIRE/	JFET I	BOARD)	TOBE			0110		
DATE	TIME	TECH	PWR ON	PWR OFF	JAA	JBB	JCC	JDD	JAA	JBB	JCC	JDD	TRANSFORT	NOTE
1-15-4	7:00AM	103199			-	V	V	-		-	_	-		GND & CHASSIS - SAVER-ON
7-19-4		103199			-	-	-	-	-	-	-	~	1	GND OHACEIS - 11
-16-4		103199			1	1	-	-	-	-	-	_		GND & CHASSIS "
-16-4		103199		v	~	~	0	har	Arm	-	-	-		SOURCE TEST "
3-19-4	,	103199			-	-	-	-	-	-	-	-		GNP & CHASSIS
-19-4		103199	V	V	-	-	-	-	-	-	-	-		SOUPCE TEST
0-18-4		ST MAN			~	-	V	-		V.	V	V		GND & CHASMS
0-18-4		ST NA	1	V			~	~	1	V				SOURCE TEST
0-21-4)	ST NOW			V	V	V	V			V	V		GIND & CHASSIS
0-21-4		ST NOW	V	V			V	V	V	V				SOURCE TEST
0-25-4		ST- N/W			V	V	V	V			V	V		GND 9 OHUSSIS
0-25-4		ST-NAW	1	V			V	V	V	U				SOURCETEST
				2										
				17		T. VI								
												-		
			-						-					
	-													
														
	-													
	age of the same of													

Attachment of HRCR Items # 24 & # 25: Mate/Demate & Operation Logs (PWB S/N 035)

OPERATION LOG SHEET -- SPIRE JFET BOARDS MODULE

DATE	TIME	TECH	PWR	PWR OFF	JAA	MA		IDD	100	DEM	ATE			NOTE	
-15-04	7-0044	103199	ON	OFF	V		JCC		JAA	JBB	JCC	JDD	TRANSFORT		
-19-04	7.004	103199			1	V	V	L		_				GND & CHASSY - SAVE	RON
16-04		103199			-									GND & GMASSIS T.	*/
16-04		103119				entine.				1				GND YOHASANS TO STURGE - SOURCE TEST	EST
10.00		103199				-								STURGE -	SWER
19-11		103199	C	-				-						GND 9 OHAS815	- 11
-18-00		102149	-		-	/								SOURCE TEST	"
19-04		ST NIW	V	V	0	D'	V	1		/	V	V		GN113 (1775)	
-21-04		OT NEW		-		./	V	V	V	0				SOUPCE TEST EIND & CHASENS	
-21-04		ST NIN	~	1	-	V		-			V	V		GND & CHASSIS	
-25-04		ST NOW	· · ·		16		V	0			V	V		SDUPCE TEST GND & CHASGIS SDUPLE TEST	
1000		7/ 10/0			V	0	V	V			0	U		GND & CHASSIS	
						_	0		V	0				SOUPLE TEST	
				-		_									
		-	<u> </u>												
		-													
		-										11			
									0.45 s s / 0.55						
		N 12	-												
			t.												
				A. 177. San											

Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 1 of 2)



Attachment of HRCR Item # 26: MICD - JFET Interface Drawing 10209722 (p 2 of 2)

	12 11	10 9	8	7 ★	6	5	4	3	2	1
	JAA JEET DUTPUT 139	JAAY JEET OUTPUT 2A		JET INPUT 1	1 [JID JET SERVICE 1		JCC' JEET INPUT	,	
	PIN # PUN PURPUSE	PIN # PIN PURPLEE	PIN #	PIN PURPOSE	PIN		_	PIN # PIN PUR		
l _H	1 SIGNAL M+	1 SIGNAL H+'	l BIAS V		1 1			1 BIAS V+'		
11	2 SIGNAL N+	2 SIGNAL N+'	2 BIAS V		2	V+		5 BIAS A-,		
	3 SIGNAL P+	3 SIGNAL P+1	3 SIGNAL		3	H+		3 SIGNAL Y+		
	4 SIGNAL R+	4 SIGNAL R+1	4 SIGNAL		4	V-		4 SIGNAL V-'		
	5 SIGNAL S+	5 SIGNAL S+'	5 SIGNAL		5	V-		5 SIGNAL V+'		
	6 SIGNAL T+	6 SIGNAL T+'	6 SIGNAL	T+	6	H+		6 SIGNAL T+'		
	7 SIGNAL U-	7 SIGNAL U-'	7 SIGNAL	-2	7	V+		7 SIGNAL S-/		
G	8 SIGNAL V-	B SIGNAL V-	B SIGNAL	P+	8	Vss		B SIGNAL P+'		
	9 SIGNAL V-	9 SIGNAL W-	9 SIGNAL	N-	9	DIAS CAIE		9 SIGNAL N-/		
	10 SIGNAL X-	10 SIGNAL X-	1D SIGNAL	L-	10	Vald		10 SIGNAL L-/		
	II SIGNAL Y-	11 SIGNAL Y-'	11 SIGNAL	K+	11	H-		1L SIGNAL K+'		
П	12 SIGNAL Z-	12 SIGNAL Z-'	12 SIGNAL	I-	12	CHASSIS GNII		12 SIGNAL I-'		
	13 FPU GND	13 FPU GND	13 SIGNAL	H+	13	H-		13 SIGNAL H+		
	14 SIGNAL M-	14 SIGNAL H-'	14 SIGNAL	F+	14	Yoki		14 SIGNAL F+'		
F	15 SIGNAL N-	15 SIGNAL N-'	15 SIGNAL	E-	15	BIAS GND		13 SIGNAL E-		
	16 SIGNAL P-	16 SIGNAL P-'	16 STGNAL	C+				16 SIGNAL C+*		
	17 SIGNAL R-	17 SIGNAL R-'	17 SIGNAL	B-]	JUDY JEET SERVICE 2		17 SIGNAL B-		
	18 SIGNAL S-	18 SIGNAL S-'	18 SIGNAL		PIN			18 SIGNAL A-		
\Box	19 SIGNAL T-	19 SIGNAL T-'	19 BIAS GI] 1			19 BIAS GND'		
	20 SIGNAL U+	20 SIGNAL U+'	20 SIGNAL	Z+	2	V+'		20 SIGNAL Z+'		
	21 SIGNAL V+	21 SIGNAL V+'	21 SIGNAL	X-	3	H+'		21 SIGNAL X-		
-	22 SIGNAL W+	22 SIGNAL V+'	22 SIGNAL	∀ +] 4	V-		22 SIGNAL W+1		
-	23 SIGNAL X+	23 SIGNAL X+'	23 SIGNAL		5	V-2		23 SIGNAL U-		
	24 SIGNAL Y+	24 SIGNAL Y+'	24 SIGNAL	T-		H+'		24 SIGNAL T-		
	25 SIGNAL Z+	25 SIGNAL Z+'	25 SIGNAL	R+] 7	V+/		25 SIGNAL R+		
-			26 SIGNAL	P-] <u>e</u>	Vss'		26 SIGNAL P-		
	JEE JFET DUTPUT 1A	JBB' JFET DUTPUT 20	27 SIGNAL	M+	9	YIND ZAIE		27 SIGNAL M+1		
	PIN # PIN PURPUSE	PIN # PIN PURPOSE 1 SIGNAL A+'	28 SIGNAL		10	Vald'		28 SIGNAL L+'		
	1 SIGNAL A+ 2 SIGNAL B+		29 SIGNAL		11	H-'		29 SIGNAL J-		
U		3 SIGNAL E+'	3D SIGNAL		12	CHASSIS GND		'+I JANDI2 DE		
		4 SIGNAL I+'	31 SIGNAL		13	H-'		2d Signal G→		
			32 SIGNAL		14	Yokl'		32 SIGNAL F-		
Н		5 SIGNAL E+' 6 SIGNAL F+'	33 SIGNAL	□ +	15	BIAS GND.		33 SIGNAL D+/		
	6 SIGNAL F+ 7 SIGNAL G-		34 SIGNAL					34 SIGNAL C-/		
	7 SIGNAL G- 6 SIGNAL H-	7 SIGNAL 5-' 8 SIGNAL H-'	35 SIGNAL					35 SIGNAL A+'		
	9 SIGNAL I-	9 SIGNAL 1-'	36 SIGNAL		1			36 SIGNAL Z-		
C	10 SIGNAL J-	10 SIGNAL I-	37 SIGNAL		1			37 SIGNAL Y-		
	II SIGNAL K-	11 ZIGNAL K-	38 SIGNAL		1			YX JANDIZ BE		
	12 SIGNAL L-	15 ZIGNAL F-,	39 SIGNAL		1			39 ZIGNAL V-'		
Н	13 FPU GND	13 FPU GND	4D SIGNAL		1			4D SIGNAL U+*		
	14 SIGNAL A-	14 ZIGNAL 4	41 SIGNAL		1			41 SIGNAL S+*		
	15 SIGNAL B-	15 SIGNAL B-'	42 SIGNAL					42 SIGNAL R-		
	16 SIGNAL C-	16 SIGNAL C-'	43 SIGNAL					43 SIGNAL N+		
	17 SIGNAL D-	17 SIGNAL II-'	44 SIGNAL					44 SIGNAL M-		
	18 SIGNAL E-	18 SIGNAL E-'	45 SIGNAL					45 SIGNAL K-		
	19 SIGNAL F-	19 SIGNAL F-'	46 SIGNAL		1			46 SIGNAL J+'		
\Box	20 SIGNAL G+	20 SIGNAL F+'	47 SIGNAL		1			47 SIGNAL H-		
	21 SIGNAL H+	21 SIGNAL H+'	48 SIGNAL		1			4B SIGNAL G+		
	22 SIGNAL I+	22 SIGNAL 1+'	49 SIGNAL		1			49 SIGNAL E+		
	23 SIGNAL J+	23 SIGNAL J+'	50 SIGNAL		1			50 SIGNAL D-		
A	24 SIGNAL K+	24 SIGNAL K+'	51 SIGNAL	B+	_			51 SIGNAL B+		
	25 SIGNAL L+	25 SIGNAL L+'							42 RE H	
	ES STUTTE LT	Ed STRIME LT.							A1 2383	UNCLASSIFIED HEZER F.J.
	12 11	10 9	8			5	4	3	,-m. na.	1 50
		, -								<u> </u>

Attachment of HRCR Item #11:

SPIRE

Handling Document

Field Effect Transistor (JFET) Module

10209750-1

Prepared by: Kalyani Sukhatme

10 September, 2003

Hardware Handling Guidelines

Contamination: Open shipment suitcase in a FED-STD-209 Class 10,000 clean room (ISO 14644-1 class 7) or better. Handle hardware with gloves.

ESD: Handle with grounding straps, ESD-safe gloves and ESD smocks at an ESD-safe workstation. Maintain shorting plugs on the unit whenever ESD is a concern. Refer to attached electrical handling document for other important safety precautions.

Fragile: Do not drop or otherwise shock the hardware including the shipping suitcase and container.

Humidity Sensitive: Place hardware in a humidity controlled Class 10,000 clean room. Maintain humidity level at 35%-50% RH typical, for ESD safety.

SPIRE JFET Electrical Handling Document

1	Int	troduction	.1
	1.1	Hardware Description	.1
2	На	andling	.2
3	Po	ower ON Procedure	.2
4	Ele	ectrical Check-out Test: Characteristic Offset Voltage Measurement	.3

1. Introduction

This document provides guidelines for electrical handling for the SPIRE JFET Module.

1.1 Hardware Description

Each JFET module has two sets of 24 JFET channels. The JFET channels are populated on 1.0 micron thick Silicon Nitride membranes which provides thermal isolation. The operating temperature for these JFETs is ~120 K. The process of powering up the JFETs dissipates heat into the membrane resulting in a temperature increase with respect to the base temperature (4K to 10 K). Higher the power dissipation, higher is the temperature of the JFETs.

Each JFET channel consists of a matched pair of FETs (Figure 1.1-1) with a requirement for the offset voltage of less than **15 mV** between the matched pair. [The characteristic offset voltage is the difference between the source voltages $(V_{sa} \text{ and } V_{sb} \text{ with respect to ground})$ of the two FETs.]

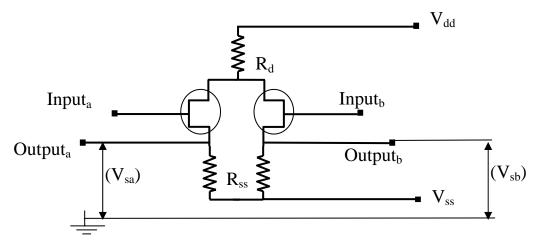


Figure 1.1-1

The Gates of the JFETs are the 'Inputs' of the circuit and the Sources (V_{sa} and V_{sb}) of the JFETs are the outputs, as marked in Figure 1.1-1. Vdd and Vss are the power lines for the circuit.

Handling

- 1. **The JFET Module is Contamination Sensitive**: Handle the unit with Gloves only in a FED-STD-209 Class 100000 clean room (ISO 14644-1 class 7) or better.
- 2. **The JFET Module is ESD Sensitive**: Please handle with appropriate ESD hardware handling procedures. Handle with grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.
- 3. **The JFET Module is Fragile**: Please do not drop or otherwise shock the unit. Please DO NOT remove the cover of the JFET Module.

Power ON Procedure

1. The JFET Module should be powered on **WITH the shorting plugs** (JPL Supplied Protection connectors) in place and with the **inputs shorted to ground.** Pins #9 and #15 on the 15-pin MDM connectors on the JFET Module are the bias grounds on the module. These pins should also be shorted to the power supply ground. The unit may be powered up without the shorting plug only when the inputs are connected to the detector system.

Under no circumstances the unit should be powered up without the inputs shorted to ground either via the shorting plug (JPL Supplied) or via the detector system.

- 2. Do not exceed a voltage of +5 V for the Vdd line and -5 V for the Vss line of the JFET Module.
- 3. When removing the shorting plugs from the unit for installation into the instrument, please use standard ESD precautions including grounding straps, ESD-safe gloves, ESD smocks at an ESD-safe workstation.

Electrical Check-out Test: Characteristic Offset Voltage Measurement

- 1) Verify that the gates of the JFET channels (Inputs) are shorted together and grounded.
- 2) Apply the power supply ground to the bias ground pins on the unit (Pins 9 and 15 on the 15-pin MDM connectors)
- 3) Power on the JFET modules with Vdd = +3 V and Vss = -1.5 V
- 4) Verify that the handheld multimeter is in calibration.
- 5) Connect one side of the handheld multimeter to ground (Power supply ground).
- 6) And measure the voltage with respect to ground of each side (V_{sa} and V_{sb}) of each channel.
- 7) Calculate the characteristic offset voltage (V_{offset}) for each channel ($V_{offset} = V_{sa} V_{sb}$)
- 8) Compare the values for each of the channels with the specific datasheet provided with the unit. The datasheets accompanying the unit also provides the values for the drain and source currents for a similar test performed at JPL.

REFER TO MEASURED SOURCE VOLTAGE DATA FOR ACTUAL HARDWARE. Here is an example of the source voltage values and the drain and the source currents obtained for such a test at room temperature are given in the Table 4-1

T, JFET	rm T					
Vdd	3 V					
Vss	-1.5 V					
ldd	1.564 mA					
lss	1.5686 mA					
Channel #	(V)	DELTA (V)				
1	1.130	0				
1	1.130	U				
2	1.075	0.001				
2	1.074	0.001				
2	0.781	0.001				
3	0.780	0.001				
4	1.088	0.005				
4	1.093	0.005				
5	0.834	0.001				
3	0.833	0.001				
6	1.012	0.003				
0	1.015	0.003				
7	0.785	0.002				
/	0.787	0.002				
8	1.148	0.004				
0	1.144	0.004				
9	0.753	0				
9	0.753	U				

_	_	
10	0.693	0.008
	0.701	0.000
11	1.110	0.004
11	1.114	0.004
12	0.758	0.001
12	0.759	0.001
13	0.832	0.002
- 10	0.830	0.002
14	1.264	0.001
1.	1.265	0.001
15	1.206	0
	1.206	
16	0.818	0.001
	0.819	0.001
17	0.526	0.005
	0.521	0.000
18	1.423	0
	1.423	
19	0.773	0.002
	0.775	0.002
20	0.873	0.004
-	0.877	
21	1.387	0.006
	1.393	
22	1.417	0.003
	1.420	
23	0.887	0.002
	0.889	
24	0.888	0.003
	0.891	

- END OF Attachment of HRCR Item # 11: JFET Module Handling Document

END OF HRCR PACKAGE