CCLRC Rutherford Appleton Laboratory	MINUTES OF MEETINGS (MoM)	PRODUCT ASSURANCE Space Science and Technology Department

Subject / Title:	CQM JFET grounding anomaly NRB	Document No:	SPIRE-RAL-MoM-002243 Issue 1.0	Date	6 Dec 04	Page 1 of 3

Spacecraft / Project	Herschel / SPIRE	Meeting Place	Telecon ES Office
Instrument / Model	CQM	Subsystem	JFET

Participants		Agenda
Print Name & Company	***Signature Required***	Discussion of JFET anomaly **Ref NCR No.HR-SP-RAL-NCR-092 (attached)**
Chairman Eric Sawyer		
Secretary		
ESA		
ESA JanRautakoski		
ESA Carsten Scharmberg		
RAL		
Astrium Siegmund.Idler		
Alcatel Guy Doubrovik		
Company		**Additional Distribution** **Jim Newell JPL** **Marty Herman JPL** **SPIRE Project Office Judy Long)**
Company		

No	Discussion
	Outline of problem given by Eric. Short to chassis on the non functioning thermal dummy JFETS This could affect the EMC test at EQM level. Possible solutions identified: 1 Saver on cold side with ground connections broken as described in NCR. 2 Saver on warm end Option 1 is preferred by SPIRE because option 2 would leave an antenna that could cause EMC problem. Savers likely to be a minimum of 40mm long. ASED need to asses if there is room for the proposed saver. CAD model needs to be loaded to do this assessment. Connectors are mounted on brackets on the JFETS, can these be moved to provide more clearance? SPIRE response is no because the back harness is very stiff and there is little room for this. An alternative solution may be to make savers longer to allow some bend. ASED assessment to

	consider this. Timing of Harness integration is TBD, ASED to investigate. To be discussed at the IRR. ASED propose that all effort is made to fit at the cold end, if this is not possible them go to option 2 at a later stage.

CCLRC Rutherford Appleton Laboratory	**NON-CONFORMANCE REPORT (NCR)**	**PRODUCT ASSURANCE Space Science and Technology Department**

NCR Number:	HR-SP-RAL-NCR-092

Spacecraft / Project	**HERSCHEL**	**Originator's Name**	Doug Griffin	
Experiment / Model	**SPIRE**	**Signature**		
Sub-System	**FPU/JFP/JFS**	**Date**	30 November 2004	
Assembly		**Level (Highlight if applicable)**	Major	**Minor**
Sub-Assembly				
Item		**NRB Reference**		
Serial Number				

NCR Occurred During (Highlight if applicable)	Manufacture	Inspection	Test	Integration	Other

NCR Title	SPIRE EQM Electrical Interface Bench Test Anomalies

NCR Description
See Attachment One
Cause of NCR
To be determined.
Disposition / Corrective Action

Document or Drawing Affected (Title, Number & Issue)	**Estimated COST OF NCR (cost of : correction, Materials, Resource, and delay to Project etc.)**

NCR CLOSED	**Name**	**Sign & Date**	
		Approved	**Rejected**
Engineering:			
Product Assurance:			
CCB-Chairman:			
Principle Investigator			
Product Assurance:			
Co-Investigator			
Prime Contractor			
ESA Project Office			

Attachment One: NCR Description/Cause

The bench test of the FPU/JFP/JFS carried out during the incoming inspection of CQM SPIRE for the satellite level EQM test campaign revealed several anomalies. The test procedure and test results are listed in SPIRE-RAL-NOT-002216, Issue 3.0. The anomalies are listed and described in Table 1.

Table 1 - Summary of issues found during SPIRE CQM bench test

Number	Comment / Description
1	▪ Pins 3 and 22 on JFP J26 (redundant PSW JFET Bias 2) are open circuit. The corresponding pins on the prime Backharness are not open circuit. ▪ This function is not used during the test campaign. The fault could either be in the internal wiring within the **STM** JFET module or within the back harness. ▪ No meaningful diagnostic can be carried out with the JFP mated to the FPU. The problem is to be reviewed when the instrument is returned to RAL at the conclusion of the EQM programme.
2	▪ PSW analogue ground is shorted via 53.2kΩ to the chassis of the JFP. This can be seen in Figure 1 which illustrates the part of the bench test which verifies isolation between FPU Faraday Shield and analogue ground. This violates the SPIRE grounding scheme.
3	▪ SLW and SSW analogue grounds are shorted to chassis of JFS via approximately 1.0 Ω.

The error in the grounding scheme (Numbers 2 and 3 above) can be corrected by inserting MWDM37 way adaptors on JFP J27, JFP J28, JFS J09 and JFS J10. These adaptors would break the ground links for the PSW and JFP/JFS and are specified in Table 2 and Table 3. The adaptors would have the same physical envelope as a connector saver.

Table 2 Ground scheme correcting connector for JFS J09 and JFS J10

Pin	Function	Implemented
1	PTC Bias +ve	Yes
2	PTC Ground	No
3	PTC JFETV Bias -ve	Yes
4	SLW_BIAS-ve	Yes
5	SLW_BIAS +ve	Yes
6	SLW GND WIRE	No
7	SLW_JFETV -ve	Yes
8	SLW_JFETV +ve	Yes
9	SSW_BIAS1 shld	No
10	SSW_BIAS1 –ve	Yes
11	SSW_JFETV1 +ve	Yes
12	SSW GND WIRE	No
13	SSW_BIAS2 +ve	Yes
14	SSW_JFETV2 shld	No
15	SSW_JFETV2 -ve	Yes
16	PTC_JFET_HEATER +ve	Yes
17	SLW_JFET_HEATER +ve	Yes
18	SLW_JFET_HEATER shld	No
19	SSW_JFET_HEATER -ve	Yes
20	PTC Bias –ve	Yes
21	PTC JFETV Bias +ve	Yes
22	SLW_BIAS+ve	Yes
23	SLW_BIAS shld	No

Pin	Function	Implemented
24	SLW_BIAS -ve	Yes
25	SLW_JFETV +ve	Yes
26	SLW_JFETV shld	No
27	SLW_JFETV -ve	Yes
28	SSW_BIAS1 +ve	Yes
29	SSW_JFETV1 shld	No
30	SSW_JFETV1 -ve	Yes
31	SSW_BIAS2 shld	No
32	SSW_BIAS2 –ve	Yes
33	SSW_JFETV2 +ve	Yes
34	None	No
35	PTC_JFET_HEATER -ve	Yes
36	SLW_JFET_HEATER -ve	Yes
37	SSW_JFET_HEATER +ve	Yes

Table 3 - Ground scheme correcting connector for JFP J27 and JFP J28

Pin	Funtion	Implemented
1	PSW_JFETV1 shld	No
2	PSW_JFETV1 -	Yes
3	PSW_JFETV2 +	Yes
4	PSW_JFETV3 shld	No
5	PSW_JFETV3 -	Yes
6	PSW_JFETV4 +	Yes
7	PSW_JFETV5 shld	No
8	PSW_JFETV5 -	Yes
9	PSW_JFETV6 +	Yes
10	PSW GRND	No
11	PSW_BIAS1/2 +	Yes
12	PSW_BIAS3/4 -	Yes
13	PSW_BIAS3/4 shld	No
14	PSW_BIAS5/6 +	Yes
15	PSW_HEATER -	Yes
16	PSW_HEATER shld	No
17	PSW_HEATER +	Yes
18	PSW_HEATER -	Yes
20	PSW_JFETV1 +	Yes
21	PSW_JFETV2 shld	No
22	PSW_JFETV2 -	Yes
23	PSW_JFETV3 +	Yes
24	PSW_JFETV4 shld	No
25	PSW_JFETV4 -	Yes
26	PSW_JFETV5 +	Yes
27	PSW_JFETV6 shld	No
28	PSW_JFETV6 -	Yes
29	PSW_BIAS1/2 -	Yes
30	PSW_BIAS1/2 shld	No
31	PSW_BIAS3/4 +	Yes
32	PSW_BIAS5/6 -	Yes
33	PSW_BIAS5/6 shld	No
34	PSW_HEATER +	Yes
35	PSW_HEATER -	Yes
36	PSW_HEATER shld	No
36	PSW_HEATER shld	No
37	PSW_HEATER +	Yes

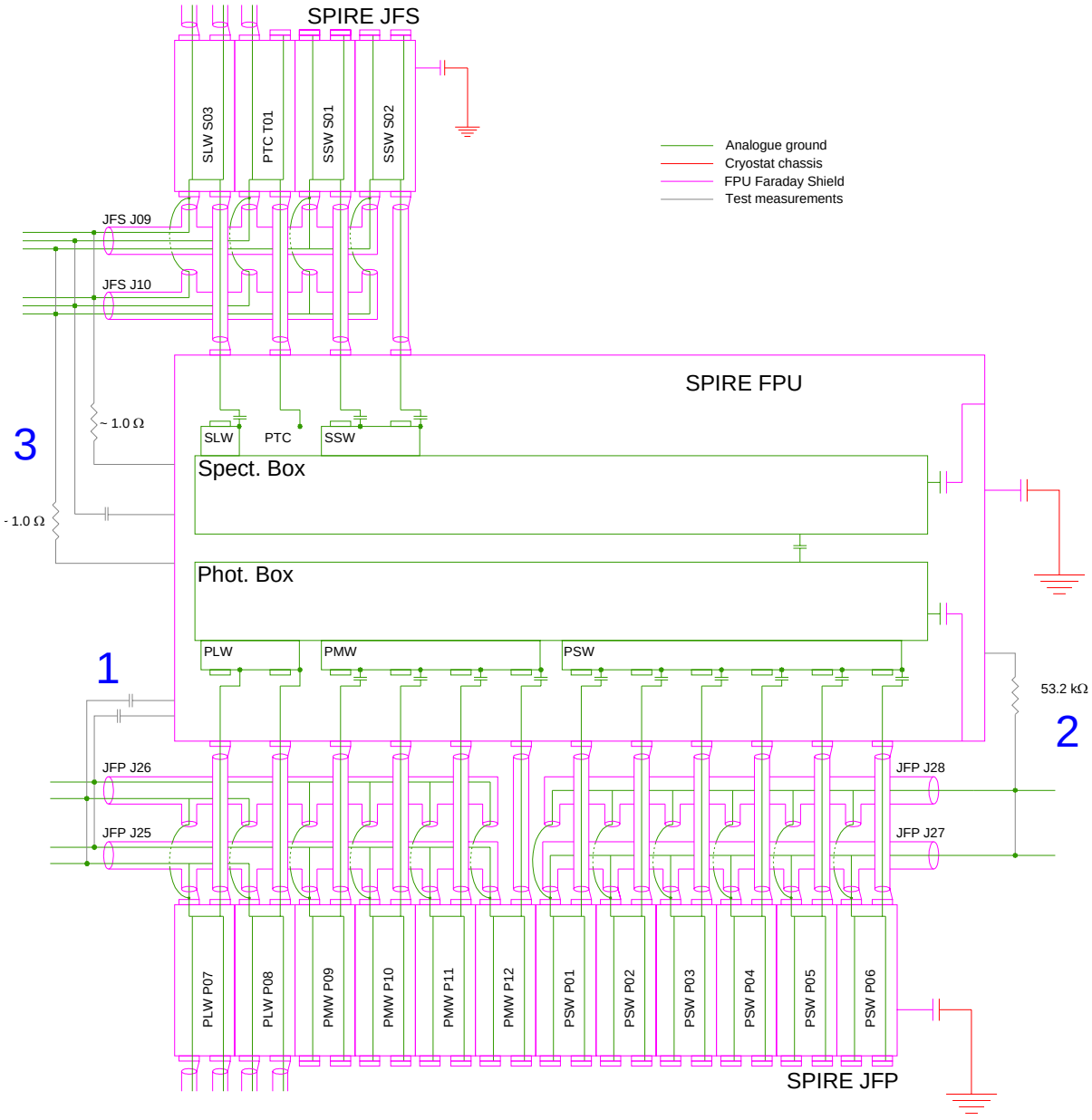

Figure 1 - Schematic illustration of the SPIRE grounding scheme within the cold plane units. Signal wires are not shown. For description, see Table 1. The PLW and PMW grounds (1) are correctly isolated. PSW ground (2) is connected to FPU Chassis by 53.2k Ω. SSW and SLW grounds (3) are hard shorted to ground via ~1.0Ω and PTC ground is correctly isolated.