



CARLO GAVAZZI SPACE SpA

# HSO/FIRST-DPU

Tipo Doc.: Doc. Type:	REPORT	SPIRE-IFS-REP-002196	N° DRD: DRD N°:	N.A.
N° Doc.: Doc. N°:	<b>DPU-RP-CGS-030</b>	Ediz.: Issue:	<b>1</b>	Data: Date:
			<b>5/04/2002</b>	Pagin a
				<b>1</b> Di Of
				<b>95</b>
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CARLO GAVAZZI SPACE SpA

# HSO/FIRST-DPU

HSO/FIRST DPU BASIC S/W TEST REPORT

N° Doc: **DPU-RP-CGS-030**

Doc N°:

Ediz.: **1**

Issue:

Data: **5/04/2002**

Date:

Pagina **2**  
Page

di **95**  
of

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CARLO GAVAZZI SPACE SpA

# HSO/FIRST-DPU

HSO/FIRST DPU BASIC S/W TEST REPORT

N° Doc: **DPU-RP-CGS-030**  
Doc N°:

Ediz.: **1**      Data: **5/04/2002**  
Issue:              Date:

Pagina **3**      di **95**  
Page              of

## LISTA DELLE PAGINE VALIDE / LIST OF VALID PAGES

PAGINA PAGE	EDIZIONE ISSUE	PAGINA PAGE	EDIZIONE ISSUE	PAGINA PAGE	EDIZIONE ISSUE	PAGINA PAGE	EDIZIONE ISSUE	PAGINA PAGE	EDIZIONE ISSUE
1 - 92	1								



CARLO GAVAZZI SPACE SpA

# HSO/FIRST-DPU

## HSO/FIRST DPU BASIC S/W TEST REPORT

N° Doc:	DPU-RP-CGS-030		
Doc N°:			
Ediz.:	1	Data:	5/04/2002
Issue:		Date:	
Pagina	4	di	95
Page		of	

### TABLE OF CONTENT

<b>1. SCOPE.....</b>	<b>8</b>
<b>2. DOCUMENTS .....</b>	<b>9</b>
2.1 APPLICABLE DOCUMENTS .....	9
2.2 REFERENCE DOCUMENTS .....	9
<b>3. ACRONYMS .....</b>	<b>10</b>
<b>4. PARTICIPANTS REQUIRED .....</b>	<b>11</b>
4.1 GENERAL.....	11
4.2 RESPONSIBILITY .....	11
4.3 QA WITNESS OF TEST AND SIGN-OFF .....	11
<b>5. TEST ARTICLE.....</b>	<b>12</b>
5.1 ITEMS DESCRIPTION .....	12
<b>6. TEST CONFIGURATION.....</b>	<b>13</b>
6.1 CROSS REFERENCE MATRIX.....	14
<b>7. INSTRUMENTATION AND TEST EQUIPMENT.....</b>	<b>18</b>
<b>8. TEST PROCEDURES.....</b>	<b>19</b>
8.1 DPU BOOT SW TEST PROCEDURES.....	19
8.1.1 BOOT SW TEST PROCEDURE.....	19
8.1.2 DM TEST PROCEDURE.....	21
8.1.3 PM TEST PROCEDURE.....	22
8.1.4 EEPROM TEST PROCEDURE.....	23
8.1.5 EEPROM TO PM LOAD TEST PROCEDURE.....	26
8.1.6 DM TO PM LOAD TEST PROCEDURE.....	27
8.2 1355 DRIVER TEST PROCEDURE.....	29
8.2.1 1355 POWER ON TEST PROCEDURE.....	29
8.2.2 1355 RESET LINK TEST PROCEDURE.....	30
8.2.3 1355 TIME-OUT TEST PROCEDURE.....	31
8.2.4 1355 OPEN LINK TEST PROCEDURE.....	32
8.2.5 1355 CLOSE LINK TEST PROCEDURE.....	33
8.2.6 1355 START LINK AS MASTER TEST PROCEDURE.....	34
8.2.7 1355 START LINK AS SLAVE TEST PROCEDURE.....	35
8.2.8 1355 STOP LINK TEST PROCEDURE.....	36
8.2.9 1355 GET STATUS REGISTER TEST PROCEDURE.....	37
8.2.10 1355 WRITE LINK TEST PROCEDURE.....	38
8.2.11 1355 READ LINK TEST PROCEDURE.....	39
8.2.12 1355 GET LINK STATUS TEST PROCEDURE.....	40
8.2.13 1355 READ PACKET TEST PROCEDURE.....	41
8.2.14 1355 GET LAST READ SIZE TEST PROCEDURE.....	42
8.2.15 1355 GET LAST READ WRITE SIZE TEST PROCEDURE.....	43
8.2.16 1355 GET LAST PACKET NUMBER TEST PROCEDURE.....	44
8.2.17 1355 WRITE TO BOARD MEMORY TEST PROCEDURE.....	45
8.2.18 1355 READ FROM BOARD MEMORY TEST PROCEDURE.....	46
8.2.19 1355 WRITE REGISTER TEST PROCEDURE.....	47
8.2.20 1355 READ REGISTER TEST PROCEDURE.....	48
8.3 WATCHDOG TEST PROCEDURE.....	49
8.3.1 DELAY SETTING TEST PROCEDURE.....	49




CARLO GAVAZZI SPACE SpA

# HSO/FIRST-DPU

## HSO/FIRST DPU BASIC S/W TEST REPORT


N° Doc:	<b>DPU-RP-CGS-030</b>		
Doc N°:			
Ediz.:	<b>1</b>	Data:	<b>5/04/2002</b>
Issue:		Date:	
Pagina	<b>5</b>	di	<b>95</b>
Page		of	

8.3.2	DELAY PROGRAMMING TEST PROCEDURE .....	50
8.3.3	WATCHDOG REFRESH TEST PROCEDURE.....	51
8.3.4	WATCHDOG STATUS TEST PROCEDURE.....	52
8.4	MIL-STD 1553 SW DRIVER TEST PROCEDURE .....	53
8.4.1	OPEN MIL-STD 1553 CHANNEL.....	53
8.4.2	TXMIL-STD 1553 MESSAGE .....	55
8.4.3	RXMIL-STD 1553 MESSAGE .....	56
8.4.4	CLOSE MIL-STD CHANNEL .....	57
8.5	EEPROM DRIVER TEST PROCEDURE.....	58
8.5.1	DELETE EEPROM SEGMENT .....	58
8.5.2	WRITE EEPROM CELL.....	59
8.5.3	DELETE EEPROM CELL .....	61
8.5.4	WRITE EEPROM SEGMENT.....	63
8.5.5	ENABLE/DISABLE EEPROM PROTECTION.....	65
8.5.6	COPY PROGRAM IN EEPROM .....	66
<b>ANNEX A : 1553 RETURNED PACKETS FORMAT AFTER 1355 COMMAND.....</b>		<b>69</b>
:	LEGENDA.....	69
ANNEX A2 :	POWER-ON, OPEN LINK AND CLOSE LINK RETURNED PACKET.....	69
ANNEX A3 :	WRITE REGISTERS RETURNED PACKET.....	70
ANNEX A4 :	READ REGISTERS RETURNED PACKET.....	70
ANNEX A5 :	START LINK MASTER AND SLAVE, STOP LINK AND RESET LINK RETURNED PACKETS.....	71
ANNEX A6 :	WRITE LINK RETURNED PACKET.....	73
ANNEX A7 :	READ LINK RETURNED PACKET.....	76
ANNEX A8 :	READ PACKET RETURNED PACKET.....	79
ANNEX A9 :	PACKET NUM, GET_W_SIZE AND GET_R_SIZE RETURNED PACKETS.....	83
ANNEX A10 :	GET STATUS RETURNED PACKET.....	83
ANNEX A11 :	GET_IDSTATE AND GET_IDSTATUS RETURNED PACKET.....	83
ANNEX A12 :	SET TIMEOUT RETURNED PACKET.....	85
ANNEX A13 :	EXIT STUB RETURNED PACKET.....	85
ANNEX A14 :	ERROR ON SELECT NUMBER OF FUCTION RETURNED PACKET.....	85
ANNEX A15 :	WRITE TO BOARD MEMORY RETURNED PACKET.....	86
ANNEX A16 :	READ FROM BOARD MEMORY RETURNED PACKET.....	88
ANNEX A17 :	WATCHDOG DELAY RETURNED PACKET.....	89
ANNEX A18 :	WATCHDOG DELAY FAILED RETURNED PACKET.....	90
ANNEX A19 :	WATCHDOG REFRESH RETURNED PACKET.....	90
ANNEX A20 :	WATCHDOG STATUS RETURNED PACKET.....	90
ANNEX A21 :	ERROR CODE RETURNED PACKET.....	90
ANNEX A22 :	EXIT STUB RETURNED PACKET.....	90
<b>ANNEX A1 : RETURNED MIL-STD-1553 PACKETS FORMAT AFTER A EEPROM COMMAND.....</b>		<b>91</b>
<b>ANNEX C : 1355 DRIVERS RETURNED ERRORS CODE .....</b>		<b>91</b>

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>6</b> di <b>95</b> Page              of


## LIST OF FIGURES

figure 6-1:Test Configuration Environment..... 13

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>7</b> di Page              of <b>95</b>

## LIST OF TABLES

table 6-1: Cross reference table .....	17
table 7-1: Instrumentation and Test Equipment Table .....	18


 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>8</b> di <b>95</b> Page              of

## 1. SCOPE

The aim of the present document is to provide a detailed test report of HSO/First-DPU BASIC S/W to be installed on the Data Processing Units developed in the framework of the HSO/FIRST program.

The test to be performed according to the Test Procedure as defined in [AD 6] are to demonstrate the compliance of the above item to the requirements specified in the applicable document [AD 7] as part of the overall verification program.



 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>9</b> di Page              of <b>95</b>


## 2. DOCUMENTS

### 2.1 APPLICABLE DOCUMENTS

- [AD1]: CNR.IFSI.2000TR01 "Documento di Specifiche Tecniche per il Contratto delle Data Processing Uniste del Satellite First dell'ESA" IFSI (Issue: 1 - 15/09/2000)
- [AD2]: Technical proposal CGS (Ref. S9-030 November 99)
- [AD3]: "Allegato Tecnico al Contratto ASI"
- [AD4]: Product Assurance Plan for the FIRST DPU (DPU-PL-CGS-001 Issue 1 Jan. 2001)
- [AD5]: DPU-PL-CGS-002 Dpu-Sw Verification And Validation Plan/Acceptance TEST (issue 1)
- [AD6]: SCI-PT-ICD-07527 Packet Structure Interface Control Document (Issue 1, 1 September 2000)
- [AD7]: DPU-SQ-CGS-001 Dpu-Bsw Software Requirements Document (July 12, 2001).
- [AD8]: CNR.IFSI.2001 TR01 DPU/ICU issue Draft 3 Switch On Procedure DPU SWITCH ON Procedure


### 2.2 REFERENCE DOCUMENTS

- [RD 1]: ACE/Mini ACE Series BC/RT/MT DDC user's guide
- [RD 2]: SMCS 332 user's guide

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>10</b> di <b>95</b> Page              of

### 3. ACRONYMS

AD	Applicable Document Number
BB	Broadband
CE	Conducted Emission
C.I.	Configuration Item. Also called Part Number (P/N)
CGS	Carlo Gavazzi Space
CS	Conducted Susceptibility
DPU	Data Processing Unit
DM	Data Memory
FIRST	Far Infra-Red and Sub-millimeter Telescope
FPU	Focal Plane Unit
FCS	Frame Check Sequence
GND	Ground
HIFI	Heterodyne Instrument for First
HK	House Keeping
ICD	Interface Control Document
ICU	Instrument Control Unit
IID	Instrument Interface Document
I/F	Interface
LCL	Latching Current Limiter
NA	Not Applicable
NB	Narrowband
OCP	Over-Current Protection
OVP	Over-Voltage Protection
P/N	Part Number. Also called Configuration Item C.I.
PA	Product Assurance
PACS	Photoconductor Array Camera and Spectrometer
PM	Program Memory
PL	Payload
PVS	Procedure Variation Sheet
QA	Quality Assurance
RD#	Reference Document Number
RE	Radiated Emission
RS	Radiated Susceptibility
RTN	Return Line
S/C	Spacecraft
S/W	Software
SPIRE	Spectral and Photometric Imaging receiver
TBC	To Be Confirmed
TBD	To Be Determined
TM/TC	Telemetry & Tele-command
UUT	Unit Under Test

 CARLO GAVAZZI SPACE SpA	<b>HSO/FIRST-DPU</b>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>11</b> di <b>95</b> Page              of

## 4. PARTICIPANTS REQUIRED

### 4.1 GENERAL

All test will be performed under QA surveillance in accordance with, and following detailed procedure of applicable PA Plan. Start of the Test shall be notified to Prime Contractor and/or Customer as applicable.


### 4.2 RESPONSIBILITY

The technical responsibility for testing and test results is up to the Software department.

QA is responsible for ensuring that all the agreed procedures are carefully observed, that test equipment and instrumentation used during testing is calibrated and within validity date: that the test data sheets are recorded in the Test Report and signed by the operators and QA witnesses, that all non conforming condition and test results are properly documented and notified to the Prime Contractor, and that all requirements of applicable PA Plan, specification and Statement of Work pertaining to the acceptance tests, are fully satisfied.

### 4.3 QA WITNESS OF TEST AND SIGN-OFF

QA inspector, or its delegate, shall witness the tests described in this procedure for the EM model in accordance to the requirement specified in the applicable PA Plans. For the EM QA or its delegate will check the test report sheets only.

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>12</b> di <b>95</b> Page              of

## 5. TEST ARTICLE

The test article consists of the HSO/DPU FIRST BASIC SW. It is composed of the following items

- BOOT SW
- DRIVERS SW
  - 1355 Drivers
  - 1553 Drivers
  - Watchdog Drivers
  - EEPROM Drivers

### 5.1 ITEMS DESCRIPTION

**The BOOT SW** is that will be resident in the PROM memory and it will allow the copy of the EEPROM program in Program Memory for the execution. The program is able to detect Data memory errors, Program memory errors, EEPROM memory errors, Application Program instruction errors by means of the Frame Check sequence checking. The Program signals the errors by means of the MIL-STD-1553 sending a Telemetry Packet to Computer Data management System according to the [AD 6] document. The BOOT SW program allows to upload a new version of the "Application Program" from Computer Data Management System via MIL-STD-1553. The CMDS will send adequate TC in order to upload the Data Memory of the Board and then it will move all the page in Program memory adjusting the Instruction parallelism.

**The 1355 Drivers** allow to command the Spacewire interface. A suite of the basic (Data Link layer) and High level (Transport Layer) functions are provided in order to allow an easy interface to the Application Software.

**The 1553 Drivers** allow to program and command the DDC chip for the MIL-STD-1553 management. A suite of elementary and High level function is provided in order to allow an easy interface to the Application Software. The users can choose the level more adequate interfacing the Application Software.

**The Watchdog Drivers** allow to command the Watchdog. Essential functions are provided in order to program the watchdog board.

**The EEPROM Drivers** allow to read and write the EEPROM. High level functions are provided for programming the EEPROM. The EEPROM is shared in page and the first 7 words of each page are reserved for page Header. Each page contains the PM check sequence and DM check sequence. When a cell of the page is written the FCS are automatically computed. The EEPROM Drives includes a high level function which allows to transfer a program in Program memory in EEPROM specifying the start address and the end address. The Interrupt vectors table is automatically included.

## 6. TEST CONFIGURATION

The following picture shows the Test environment configuration (figure 6-1).

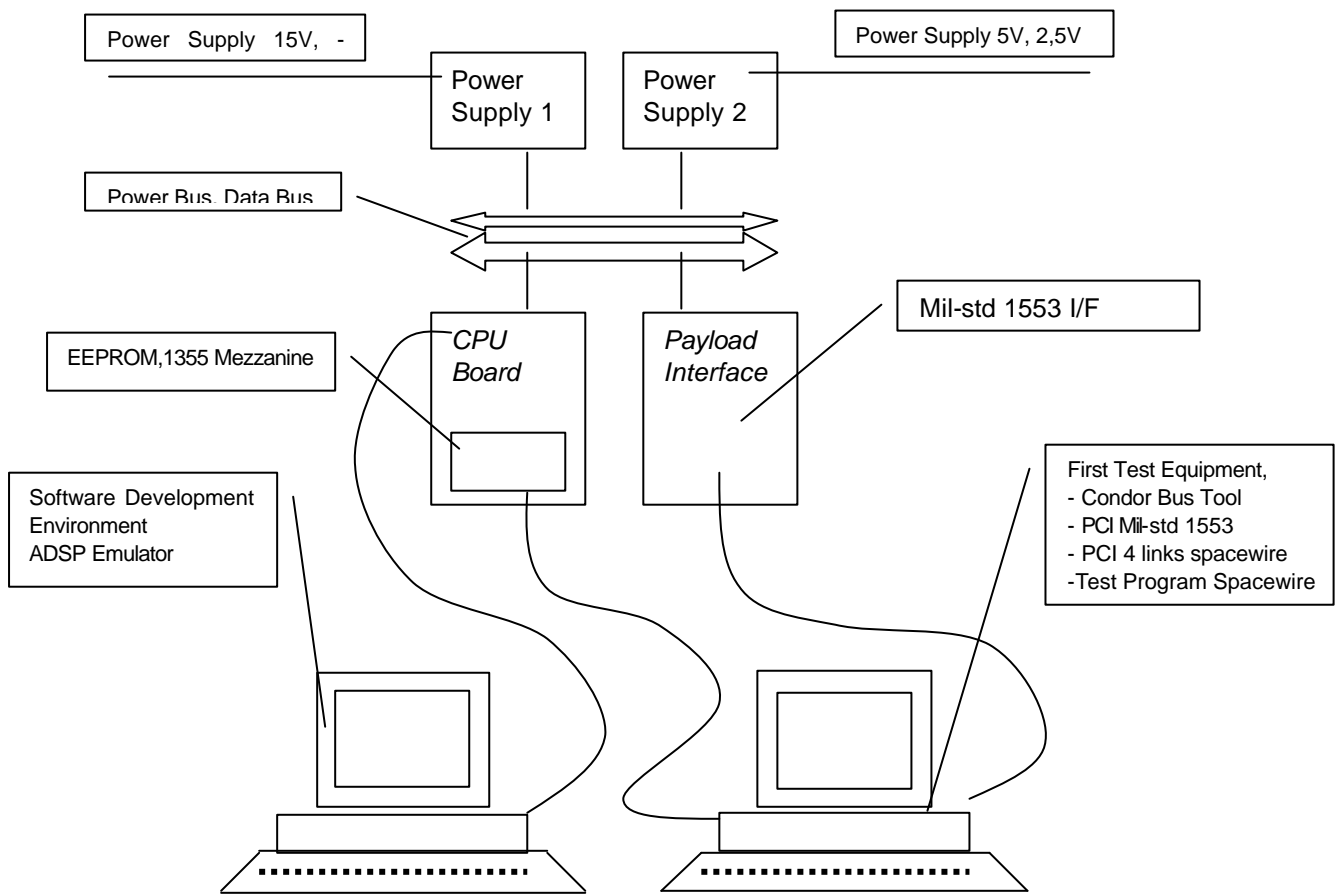


figure 6-1: Test Configuration Environment



CARLO GAVAZZI SPACE SpA

# HSO/FIRST-DPU

## HSO/FIRST DPU BASIC S/W TEST REPORT

N° Doc: **DPU-RP-CGS-030**

Doc N°:

Ediz.: **1**  
Issue:

Data: **5/04/2002**  
Date:

Pagina **14**  
Page

di **95**  
of

### 6.1 CROSS REFERENCE MATRIX

Cross reference among requirements and procedure steps is provided in the following table (table 6-1).

Requirements	Procedure Step
SRD-3.1.1.0-000	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-010	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-020	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-040	<b>SEL-R</b>
SRD-3.1.1.0-050	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-060	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-070	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-080	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-090	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-100	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-110	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-120	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-130	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-140	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-150	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-160	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-170	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-180	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-190	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-200	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-210	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-220	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-230	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-240	<b>SEL-R</b>
SRD-3.1.1.0-250	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-260	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-270	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-280	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-290	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-300	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-310	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-320	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-330	<b>SEL-R</b>
SRD-3.1.1.0-340	<b>SEL-R</b>
SRD-3.1.1.0-350	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-360	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.1.0-370	TR-BOOTSW -010, -20, -25, -30, -40, -50
SRD-3.1.2.0-000	<b>SEL-R</b>
SRD-3.1.2.0-005	<b>SEL-R</b>
SRD-3.1.2.0-010	<b>SEL-R</b>
SRD-3.1.2.0-020	<b>SEL-R</b>
SRD-3.1.3.0-000	<b>SEL-R</b>
SRD-3.1.4.0-000	TR-BOOTSW -20
SRD-3.1.4.0-010	TR-BOOTSW -20
SRD-3.1.4.0-020	TR-BOOTSW -20
SRD-3.1.4.0-030	TR-BOOTSW -20
SRD-3.1.4.0-040	TR-BOOTSW -20



CARLO GAVAZZI SPACE SpA

# HSO/FIRST-DPU

HSO/FIRST DPU BASIC S/W TEST REPORT

N° Doc: **DPU-RP-CGS-030**  
Doc N°:  
Ediz.: **1**      Data: **5/04/2002**  
Issue:              Date:  
Pagina **15**      di **95**  
Page              of

SRD-3.1.5.0-000	TR-BOOTSW -25
SRD-3.1.5.0-010	TR-BOOTSW -25
SRD-3.1.5.0-020	TR-BOOTSW -25
SRD-3.1.5.0-030	TR-BOOTSW -25
SRD-3.1.5.0-040	TR-BOOTSW -25
SRD-3.1.6.0-000	TR-BOOTSW -30
SRD-3.1.6.0-010	TR-BOOTSW -30
SRD-3.1.6.0-020	TR-BOOTSW -30
SRD-3.1.6.0-030	TR-BOOTSW -30
SRD-3.1.6.0-040	TR-BOOTSW -30
SRD-3.1.6.0-050	TR-BOOTSW -30
SRD-3.1.6.0-060	TR-BOOTSW -30
SRD-3.1.6.0-070	TR-BOOTSW -30
SRD-3.1.7.0-000	TR-BOOTSW -40
SRD-3.1.7.0-010	TR-BOOTSW -40
SRD-3.1.7.0-020	TR-BOOTSW -40
SRD-3.1.7.0-030	TR-BOOTSW -40
SRD-3.1.7.0-040	TR-BOOTSW -40
SRD-3.1.8.0-000	TR-BOOTSW -50
SRD-3.1.8.0-010	TR-BOOTSW, -50
SRD-3.1.8.0-020	TR-BOOTSW, -50
SRD-3.1.8.0-030	TR-BOOTSW, -50
SRD-3.1.8.0-040	TR-BOOTS, -50
SRD-3.2.0.0-000	TR-DRV1355 -010
SRD-3.2.0.0-010	TR-DRV1355 -010
SRD-3.2.0.0-020	TR-DRV1355 -020
SRD-3.2.0.0-025	TR-DRV1355 -030
SRD-3.2.0.0-030	TR-DRV1355 -040
SRD-3.2.0.0-040	TR-DRV1355 -050
SRD-3.2.0.0-050	TR-DRV1355 -060
SRD-3.2.0.0-060	TR-DRV1355 -070
SRD-3.2.0.0-070	TR-DRV1355 -080
SRD-3.2.0.0-080	TR-DRV1355 -090
SRD-3.2.0.0-090	TR-DRV1355 -100
SRD-3.2.0.0-100	TR-DRV1355 -100
SRD-3.2.0.0-110	TR-DRV1355 -010
SRD-3.2.0.0-120	TR-DRV1355 -110
SRD-3.2.0.0-130	TR-DRV1355 -110
SRD-3.2.0.0-140	TR-DRV1355 -120
SRD-3.2.0.0-150	TR-DRV1355 -120
SRD-3.2.0.0-160	TR-DRV1355 -140, -130
SRD-3.2.0.0-170	TR-DRV1355 -140
SRD-3.2.0.0-180	TR-DRV1355 -160
SRD-3.2.0.0-190	TR-DRV1355 -150
SRD-3.2.0.0-200	TR-DRV1355 -200, -190
SRD-3.2.0.0-210	TR-DRV1355 -180, 170
SRD-3.3.2.0-000	TR-DRV1553 -010
SRD-3.3.2.0-010	TR-DRV1553 -010
SRD-3.3.3.1-000	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.1-010	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.1-020	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.1-030	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.1-040	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.1-050	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.1-060	TR-DRV1553 -010, -20, -30, -40

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CARLO GAVAZZI SPACE SpA

# HSO/FIRST-DPU


## HSO/FIRST DPU BASIC S/W TEST REPORT

N° Doc: **DPU-RP-CGS-030**  
 Doc N°:  
 Ediz.: **1**      Data: **5/04/2002**  
 Issue:              Date:  
 Pagina **16**      di **95**  
 Page              of

SRD-3.3.3.2-000	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.2-010	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.2-020	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.2-030	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.2-040	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.2-050	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.2-060	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.3-000	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.3-010	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.3-020	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.3-030	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.3-040	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.3-050	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.3-060	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.3-070	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.3-080	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.3-090	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.3-100	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.3-110	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.3-120	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.3-130	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.3-140	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.3-150	TR-DRV1553 -010, -20, -30, -40
SRD-3.3.3.3-160	TR-DRV1553 -010, -20, -30, -40
SRD-3.5.0.0-000	TR-DRVEPRM -10, -50
SRD-3.5.0.0-010	TR-DRVEPRM -10, -50
SRD-3.5.0.0-020	TR-DRVEPRM -20, -50
SRD-3.5.0.0-030	TR-DRVEPRM -30, -50
SRD-3.5.0.0-040	TR-DRVEPRM -40, -50
SRD-3.6.0.0-000	TR-DRVWD -10
SRD-3.6.0.0-010	TR-DRVWD -20
SRD-3.6.0.0-020	TR-DRVWD -30
SRD-4.1.1.0-000	SEL-R
SRD-4.1.2.0-000	SEL-R
SRD-4.1.2.0-010	SEL-R
SRD-4.1.2.0-020	SEL-R
SRD-4.1.2.0-030	SEL-R
SRD-5.1.0.0-000	SEL-R
SRD-5.1.0.0-010	SEL-R
SRD-5.1.0.0-020	SEL-R
SRD-5.1.0.0-030	SEL-R
SRD-5.1.0.0-040	SEL-R
SRD-5.1.0.0-050	SEL-R
SRD-5.1.0.0-060	SEL-R
SRD-5.1.0.0-070	SEL-R
SRD-5.1.0.0-080	SEL-R
SRD-5.1.0.0-090	SEL-R
SRD-5.2.0.0-000	SEL-R
SRD-5.2.0.0-010	SEL-R
SRD-5.3.0.0-000	SEL-R
SRD-5.3.0.0-010	SEL-R
SRD-5.3.0.0-020	SEL-R
SRD-6.1.0.0-000	SEL-R
SRD-6.2.0.0-000	SEL-R
SRD-6.3.0.0-000	SEL-R


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	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>17</b> di <b>95</b> Page              of

<i>SRD-6.4.0.0-000</i>	<b>SEL-R</b>
<i>SRD-7.0.0.0-000</i>	<b>SEL-R</b>
<i>SRD-7.0.0.0-010</i>	<b>SEL-R</b>
<i>SRD-8.0.0.0-000</i>	<b>SEL-R</b>
<i>SRD-9.0.0.0-000</i>	<b>SEL-R</b>

*table 6-1: Cross reference table*

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	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>18</b> di <b>95</b> Page                of

## 7. INSTRUMENTATION AND TEST EQUIPMENT

The complete list of the instrumentation used during the test shall be recorded in table (table 7-1).

N.	EQUIPMENT
1	Power Supply 2 outputs (5V, 2,5V)
2	Power Supply 2 outputs (15V, -15V)
3	ADSP Emulator
4	Personal Computer with ADSP 21020 SDE tool
5	Personal Computer with 1355 PCI board, 1553 PCI board and Test equipment tools
6	Cable connecting Mil-Std-1553
7	Cable connecting Spacewire interface

*table 7-1: Instrumentation and Test Equipment Table*

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	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>19</b> di <b>95</b> Page                of

## 8. TEST PROCEDURES.

### 8.1 DPU BOOT SW TEST PROCEDURES.

#### 8.1.1 BOOT SW TEST PROCEDURE.

Step	Test Procedure Identifier	TR-BOOTSW -010	Results	Remarks
	Purpose	Verify the uploading of an Application Program from EEPROM.		
	Special Requirement	For this operation is requested an Open Box condition to connect the DSP emulator.		
Procedure steps				
1	Program the EEPROM mezzanine using the SW Test drivers. Dump the EEPROM contained from 0x80000000 to 0x800017ff. Insert a programmed EPROM (FIRST DPU BOOT SW ver 2.0.) on the HSO/FIRST DPU board. Power On. Connect the ADSP Emulator Reset the Board. Open the Program Window.  Verify that the BOOTSW program has been uploaded in the first 1555 cells in program memory.		OK	
2	Perform a chip reset by emulator Start program Set breakpoint before of jumping to "Application Program"  Verify that the program has been uploaded dumping the PM area from 0 to 0x100 cells and from 0x4000 to 0x4acc cell and comparing it with the instruction inside the EXE file.		OK	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>20</b> di <b>95</b> Page              of

3	Set a new breakpoint before of reprogramming the EEPROM Start the program  Verify that the EEPROM has been cleaned and the first six pages are blanks.	OK	
4	Start the program Wait until the end of program  Verify that the program has been correctly performed comparing the new programmed EEPROM with the values previously dumped	OK	
Date 28/04/2002		Test Conductor A. Bertoli	
		P. Assurance S. Legramandi	

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	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>21</b> di <b>95</b> Page                of

## 8.1.2 DM TEST PROCEDURE.

Step	Test Procedure Identifier	TR-BOOTSW -020	Results	Remarks
	Purpose	Verify DM errors detection during initialization		
	Special Requirement	For this operation is requested an Open Box condition to connect the DSP emulator.		
Procedure steps				
1	Insert a programmed EPROM (FIRST DPU BOOT SW ver 2.0.) on the HSO/FIRST DPU board. Power On. Connect the ADSP Emulator Reset the Board. Open the Program Window and Data Window  Verify that the BOOTSW program has been uploaded in the first 1555 cells in program memory.		OK	
2	Perform a chip reset by emulator Start program Set breakpoint before of reading the data from Data memory Write the 0xFFFFFFFF data in the DM cell Start program  Verify that the Boot SW detects the DM error verifying that a TM error message is sent to the FIRST TE containing the incorrect DM page address.		OK	
3	Verify that the BOOT SW is waiting a TC from FIRST TE checking that the "Application Program" has not been also uploaded ( from 0x4000 to 0x4acc the PM contains spurious data)		OK	
Date 28/04/2002		Test Conductor A. Bertoli	P. Assurance S. Legramandi	

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	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>22</b> di <b>95</b> Page                of

### 8.1.3 PM TEST PROCEDURE.

Step	Test Procedure Identifier	TR-BOOTSW -025	Results	Remarks
	Purpose	Verify possible PM error detection during initialization		
	Special Requirement	For this operation is requested an Open Box condition to connect the DSP emulator.		
Procedure steps				
1	Insert a programmed EPROM (FIRST DPU BOOT SW ver 2.0.) on the HSO/FIRST DPU board. Detach the Emulator and reconnect in order to erase previous value in PM. Power On. Connect the ADSP Emulator Reset the Board. Open the Program Window and Data Window  Verify that the BOOTSW program has been uploaded in the first 1555 cells in program memory.		OK	
2	Perform a chip reset by emulator Start program Set breakpoint before of reading the data from Program memory Write the 0xFFFFFFFF data in the PM cell Start program  Verify that the Boot SW detects the PM error verifying that a TM error message is sent to the FIRST TE containing the incorrect PM page address.		OK	
3	Verify that the BOOT SW is waiting a TC from FIRST TE checking that the "Application Program" has not been also uploaded ( from 0x4000 to 0x4acc the PM contains spurious data)		OK	
Date 28/04/2002		Test Conductor A. Bertoli	P. Assurance S. Legramandi	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>23</b> di <b>95</b> Page                of

## 8.1.4 EEPROM TEST PROCEDURE.

Step	Test Procedure Identifier	TR-BOOTSW -030	Results	Remarks
	Purpose	Verify that the "Application Software" is uploaded when an error in the first partition is found.		
	Special Requirement	For this operation is requested an Open Box condition to connect the DSP emulator.		
Procedure steps				
1	Program the EEPROM mezzanine using the SW Test drivers. Dump the EEPROM contained from 0x80000000 to 0x800017ff. Insert a programmed EPROM (FIRST DPU BOOT SW ver 2.0.) on the HSO/FIRST DPU board. Detach the Emulator and reconnect in order to erase previous value in PM. Power On. Connect the ADSP Emulator Reset the Board. Open the Program Window and Data Window  Verify that the BOOTSW program has been uploaded in the first 1555 cells in program memory.	OK		
2	Perform a chip reset by emulator Read the value at the EEPROM address 0x80000020 Write a different value (i.e 0xFFFFAAAA) at the EEPROM address 0x80000020 Set a break point before of jumping to the "Application Program" execution. Start program  Verify that the program has been uploaded, dumping the PM area from 0 to 0x100 cells and from 0x4000 to 0x4acc cell and comparing it with the instruction inside the EXE file.	OK		

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	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>24</b> di <b>95</b> Page                of

3	<p>Set a new breakpoint before of reprogramming the EEPROM Start the program</p> <p>Verify that the EEPROM has been cleaned and the first six pages are blanks.</p>	OK	
4	<p>Start the program Wait until the end of program</p> <p>Verify that the program has been correctly performed comparing the new programmed EEPROM with the values previously dumped Verify that the values 0xFFFFAAAA at the 0x80000020 is equal to the value read at step 2</p>	OK	
5	<p>Restart the system (power off) Insert a programmed EPROM (FIRST DPU BOOT SW ver 2.0.) on the HSO/FIRST DPU board. Detach the Emulator and reconnect in order to erase previous value in PM. Power On. Connect the ADSP Emulator Reset the Board. Open the Program Window and Data Window</p> <p>Verify that the BOOTSW program has been uploaded in the first 1555 cells in program memory.</p>	OK	
6	<p>Perform a chip reset by emulator Read the value at the EEPROM address 0x8003fc20 Write a different value (i.e 0xFFFFAAAA) at the EEPROM address 0x8003fc20 Set a break point before of jumping to the "Application Program" execution. Start program</p> <p>Verify that the program has been uploaded, dumping the PM area from 0 to 0x100 cells and from 0x4000 to 0x4acc cell and comparing it with the instruction inside the EXE file.</p>	OK	



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	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>25</b> di <b>95</b> Page                of

7	Set a new breakpoint before of reprogramming the EEPROM Start the program  Verify that the EEPROM has been cleaned and the first six pages are blanks.	OK	
8	Start the program Wait until the end of program  Verify that the program has been correctly performed comparing the new programmed EEPROM with the values previously dumped Verify that the values 0xFFFFAAAA at the 0x8003fc20 is equal to the value read at step 5	OK	
9	Restart the test procedure (Power off) Detach the Emulator and reconnect in order to erase previous value in PM. Power On. Connect the ADSP Emulator Reset the Board. Open the Program Window and Data Window  Verify that the BOOTSW program has been uploaded in the first 1555 cells in program memory.	OK	
10	Perform a chip reset by emulator Read the value at the EEPROM address 0x80000060 and 0x8003fcAA Write a different value (i.e 0xFFFFAAAA) at the EEPROM address 0x80000060 and 0x8003fcAA Set a break point before of jumping to the "Application Program" execution. Start program  Verify that the program has not been uploaded, and the "Application Program" has not been copied in the 0x4000 to 0x4acc cells. Verify that a TM error message is generated indicating the EEPROM page address failed And the Checksum expected and computed..	OK	
Date 28/04/2002		Test Conductor A. Bertoli	P. Assurance S. Legramandi

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>26</b> di <b>95</b> Page                of

### 8.1.5 EEPROM TO PM LOAD TEST PROCEDURE.

Step	Test Procedure Identifier	TR-BOOTSW -040	Results	Remarks
	Purpose	Verify an error is detected during the uploading of an Application Program from EEPROM to PM.		
	Special Requirement	For this operation is requested an Open Box condition to connect the DSP emulator.		
Procedure steps				
1	Program the EEPROM mezzanine using the SW Test drivers Insert a programmed EPROM (FIRST DPU BOOT SW ver 2.0.) on the HSO/FIRST DPU board. Power On. Connect the ADSP Emulator Reset the Board. Open the Program Window.  Verify that the BOOTSW program has been uploaded in the first 1555 cells in program memory.		OK	
2	Perform a chip reset by emulator Set breakpoint before of starting the EEPROM to PM upload Start program  No checks is requested		OK	
3	Write at the EEPROM address 0x80000820 the value 0xFFFFFFFF Stat program  Stop program and Verify that a TM error message is sent by means of MIL1553 to FIRST TE indicating the failed PM page upload. Verify that the "Application Program" has been partially uploaded: page 1,2 are ok page 3 is failed checking the PM content.		OK	
Date 28/04/2002	Test Conductor A. Bertoli	P. Assurance S. Legramandi		

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>27</b> di <b>95</b> Page              of

## 8.1.6 DM TO PM LOAD TEST PROCEDURE.

Step	Test Procedure Identifier	TR-BOOTSW -050	Results	Remarks
	Purpose	Verify an error is detected during the uploading of an Application Program from DM to PM.		
	Special Requirement	For this operation is requested an Open Box condition to connect the DSP emulator.		
Procedure steps				
1	Reset the EEPROM content Generate using Tcgen program the DM pages that will be uploaded Insert a programmed EPROM (FIRST DPU BOOT SW ver 2.0.) on the HSO/FIRST DPU board. Power On. Connect the ADSP Emulator Reset the Board. Open the Program Window and Data Window.  Verify that the BOOTSW program has been uploaded in the first 1555 cells in program memory.		OK	
2	Perform a chip reset by emulator Upload the DM pages in Data Memory starting from 0x00004000 Set breakpoint before of the DM test Start program  No check is required		OK	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>28</b> di <b>95</b> Page                of

3	Change the value in the memory cell in order to fail the DM test Start the program  Verify that a TM message is sent to FIRST TE	OK	
4	Send a TC in order to force the DM to PM program copy Set a breakpoint before of jumping to "Application Program" execution  Verify that the "Application Program" is correctly copied at the following address: Pm 0x0 to 0x100 Pm 0x4000 to 0x4acc Dumping the PM content and comparing it with the Application program exe file	OK	
5	Start Program  Verify that the EEPROM has been reprogrammed by means of the "Application Program" uploaded	OK	
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	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>29</b> di <b>95</b> Page              of

## 8.2 1355 DRIVER TEST PROCEDURE.

### 8.2.1 1355 POWER ON TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 -010	Results	Remarks
	Purpose	Verify the correct functioning of 1355 Power On.		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On. Load on Bus Tools Software the file Power-On.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal. Off-line verification: Check in the log file Power-On-log.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A2.		OK	
Date 28/04/2002	Test Conductor A. Bertoli	P. Assurance S. Legramandi		

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>30</b> di <b>95</b> Page              of

## 8.2.2 1355 RESET LINK TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 -020	Results	Remarks
	Purpose	Verify the possibility to reset the SMCS332 link.		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Load on Bus Tools Software the file Reset-link.btd Run on Bus Tools the network Wait to receive the last packet from remote terminal Off-line verification: Check in the log file Reset-link.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A5.		OK	
Date 28/04/2002	Test Conductor A. Bertoli	P. Assurance S. Legramandi		

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	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>31</b> di <b>95</b> Page              of

### 8.2.3 1355 TIME-OUT TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV/1355 -030	Results	Remarks
	Purpose	Verify the possibility to set time-out value for the SMCS332		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On Load on Bus Tools Software the file Time-out.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal. Off-line verification: Check in the log file Time-out.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A12.		OK	
Date 28/04/2002		Test Conductor A. Bertoli	P. Assurance S. Legramandi	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>32</b> di <b>95</b> Page              of

## 8.2.4 1355 OPEN LINK TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 -040	Results	Remarks
	Purpose	Verify the correct functioning of 1355 Power On.		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On Load on Bus Tools Software the file Open-link.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal. Off-line verification: Check in the log file Open-link.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A2.		OK	
Date 28/04/2002	Test Conductor A. Bertoli	P. Assurance S. Legramandi		



 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>33</b> di <b>95</b> Page              of

## 8.2.5 1355 CLOSE LINK TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 -050	Results	Remarks
	Purpose	Verify the possibility to close each of the three SMCS links		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On Load on Bus Tools Software the file Close-link.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal Off-line verification: Check in the log file Close-link.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A2.		OK	
Date 28/04/2002	Test Conductor A. Bertoli	P. Assurance S. Legramandi		

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>34</b> di <b>95</b> Page              of

## 8.2.6 1355 START LINK AS MASTER TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 -060	Results	Remarks
	Purpose	Verify the possibility to start, as master, each of the three SMCS links using different speed values.		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On Load on Bus Tools Software the file Start-Link-as Master.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal. Off-line verification: Check in the log file Start-Link-as Master.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A5.		OK	
Date 28/04/2002		Test Conductor A. Bertoli	P. Assurance S. Legramandi	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>35</b> di <b>95</b> Page              of

## 8.2.7 1355 START LINK AS SLAVE TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 -070	Results	Remarks
	Purpose	Verify the possibility to start, as slave, each of the three SMCS links using different speed values.		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On. Load on Bus Tools Software the file Start-Link-as-slave.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal Off-line verification: Check in the log file Start-Link-as-slave.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A5		OK	
Date 28/04/2002		Test Conductor A. Bertoli	P. Assurance S. Legramandi	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>36</b> di <b>95</b> Page              of

## 8.2.8 1355 STOP LINK TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 -080	Results	Remarks
	Purpose	Verify the possibility to start, as slave, each of the three SMCS links using different speed values.		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On. Load on Bus Tools Software the file Start-Link-as-slave.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal Off-line verification: Check in the log file Start-Link-as-slave.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A5.		OK	
Date 28/04/2002		Test Conductor A. Bertoli	P. Assurance S. Legramandi	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>37</b> di <b>95</b> Page              of

## 8.2.9 1355 GET STATUS REGISTER TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 -090	Results	Remarks
	Purpose	Verify the possibility to get the status of register for each of the three SMCS links.		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On Load on Bus Tools Software the file Get-Status-Register.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal Off-line verification: Check in the log file file Get-Status-Register.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A10.		OK	
Date 28/04/2002	Test Conductor A. Bertoli	P. Assurance S. Legramandi		

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>38</b> di <b>95</b> Page              of

## 8.2.10 1355 WRITE LINK TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 –100	Results	Remarks
	Purpose	Verify the possibility to transmit data over each of the three SMCS links		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On. Load on Bus Tools Software the file Write-Link.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal Off-line verification: Check in the log file Write-Link.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A6.		OK	
Date 28/04/2002	Test Conductor A. Bertoli	P. Assurance S. Legramandi		

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>39</b> di <b>95</b> Page              of

## 8.2.11 1355 READ LINK TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 –110	Results	Remarks
	Purpose	Verify the possibility to receive data over each of the three SMCS links		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On. Load on Bus Tools Software the file Read-Link.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal. Off-line verification: Check in the log file Read-Link.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A7.		OK	
Date 28/04/2002	Test Conductor A. Bertoli	P. Assurance S. Legramandi		

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>40</b> di <b>95</b> Page              of

## 8.2.12 1355 GET LINK STATUS TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 –120	Results	Remarks
	Purpose	Verify the possibility to return the current transmit/receive link status for each of the three SMCS links.		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On. Load on Bus Tools Software the file Get-Link-Status.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal. Off-line verification: Check in the log file Get-Link-Status.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A11.		OK	
Date 28/04/2002		Test Conductor A. Bertoli	P. Assurance S. Legramandi	



 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>41</b> di <b>95</b> Page              of

### 8.2.13 1355 READ PACKET TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 –130	Results	Remarks
	Purpose	Verify the possibility to receive data over each of the three SMCS links		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On. Load on Bus Tools Software the file Read-packet.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal. Off-line verification: Check in the log file Read-packet.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A8		OK	
Date 28/04/2002	Test Conductor A. Bertoli	P. Assurance S. Legramandi		

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>42</b> di <b>95</b> Page              of

## 8.2.14 1355 GET LAST READ SIZE TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 –140	Results	Remarks
	Purpose	Verify the possibility to get the number of received data over each of the three SMCS links.		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On. Load on Bus Tools Software the file Get-Last-Read-Size.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal. Off-line verification: Check in the log file Get-Last-Read-Size.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A9.		OK	
Date 28/04/2002		Test Conductor A. Bertoli	P. Assurance S. Legramandi	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>43</b> di <b>95</b> Page              of

## 8.2.15 1355 GET LAST READ WRITE SIZE TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 –150	Results	Remarks
	Purpose	Verify the possibility to get the number of transmitted data over each of the three SMCS links.		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On. Load on Bus Tools Software the file Get-Last-Write-Size.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal. Off-line verification: Check in the log file Get-Last-Write-Size.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A9.		OK	
Date 28/04/2002		Test Conductor A. Bertoli	P. Assurance S. Legramandi	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>44</b> di <b>95</b> Page              of

## 8.2.16 1355 GET LAST PACKET NUMBER TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 –160	Results	Remarks
	Purpose	Verify the possibility to get the number of received packet over each of the three SMCS links		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On. Load on Bus Tools Software the file Get-Last-Packet-Num.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal. Off-line verification: Check in the log file Get-Last-Packet-Num.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A9		OK	
Date 28/04/2002	Test Conductor A. Bertoli	P. Assurance S. Legramandi		

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>45</b> di <b>95</b> Page              of

## 8.2.17 1355 WRITE TO BOARD MEMORY TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 –170	Results	Remarks
	Purpose	Verify the possibility to write in DPRAM for each of the three SMCS links.		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On. Load on Bus Tools Software the file Write-to-board Mem.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal. Off-line verification: Check in the log file Write-to-board Mem.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A15.		OK	
Date 28/04/2002		Test Conductor A. Bertoli	P. Assurance S. Legramandi	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>46</b> di <b>95</b> Page              of

## 8.2.18 1355 READ FROM BOARD MEMORY TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 –180	Results	Remarks
	Purpose	Verify the possibility to read from DPRAM of SMCS device		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On. Load on Bus Tools Software the file Write-to-board Mem.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal. Off-line verification: Check in the log file Write-to-board Mem.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A16		OK	
Date 28/04/2002	Test Conductor A. Bertoli	P. Assurance S. Legramandi		

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>47</b> di <b>95</b> Page              of

## 8.2.19 1355 WRITE REGISTER TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 –190	Results	Remarks
	Purpose	Verify the possibility to write in a generic register of SMCS device		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On. Load on Bus Tools Software the file Write-to-board Mem.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal. Off-line verification: Check in the log file Write-to-board Mem.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A3.		OK	
Date 28/04/2002		Test Conductor A. Bertoli	P. Assurance S. Legramandi	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>48</b> di <b>95</b> Page              of

## 8.2.20 1355 READ REGISTER TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRV1355 -200	Results	Remarks
	Purpose	Verify the possibility to read the value contained in a generic register of SMCS device		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On. Load on Bus Tools Software the file Read-Reg.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal. Off-line verification: Check in the log file Read-Reg.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A4.		OK	
Date 28/04/2002	Test Conductor A. Bertoli	P. Assurance S. Legramandi		




 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>49</b> di <b>95</b> Page              of

### 8.3 WATCHDOG TEST PROCEDURE.

#### 8.3.1 DELAY SETTING TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRVWD -010	Results	Remarks
	Purpose	Verify the correct functioning of Watchdog Delay Setting.		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment		
Procedure steps				
1	Power On. Load on Bus Tools Software the file WD-Delay.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal. Off-line verification: Check in the log file WD-Delay.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A17.		OK	
Date 28/04/2002	Test Conductor A. Bertoli	P. Assurance S. Legramandi		

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>50</b> di <b>95</b> Page              of

### 8.3.2 DELAY PROGRAMMING TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRVWD -020	Results	Remarks
	Purpose	Verify the correct functioning of Watchdog Delay Programming.		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment.		
Procedure steps				
1	Power On. Load on Bus Tools Software the file WD-Delay-fail.btd Run on Bus Tools the network. Wait to receive the last packet from remote terminal. Off-line verification: Check in the log file WD-Delay-fail.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A18.		OK	
Date 28/04/2002		Test Conductor A. Bertoli	P. Assurance S. Legramandi	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>51</b> di <b>95</b> Page              of

### 8.3.3 WATCHDOG REFRESH TEST PROCEDURE.

Step	Test Procedure Identifier	TR-DRVWD -030	Results	Remarks
	Purpose	Verify the correct functioning of Watchdog refresh		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment.		
Procedure steps				
1	Power On Load on Bus Tools Software the file WD-Refresh.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal. Off-line verification: Check in the log file WD-Refresh.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A19		OK	
Date 28/04/2002		Test Conductor A. Bertoli	P. Assurance S. Legramandi	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>52</b> di <b>95</b> Page                of

### 8.3.4 WATCHDOG STATUS TEST PROCEDURE.


Step	Test Procedure Identifier	TR-DRVWD -040	Results	Remarks
	Purpose	Verify the correct functioning of Watchdog status		
	Special Requirement	For this operation is requested the use of S/W Stub and Test Equipment.		
Procedure steps				
1	Power On. Load on Bus Tools Software the file WD-Status.btd. Run on Bus Tools the network. Wait to receive the last packet from remote terminal. Off-line verification:  Check in the log file WD-Status.bmd the following: 1) at what function the packet answer are shown in ID field. 2) the success are shown in Error Code field. If Error Code is different from zero, the function is failed. To find error condition see Annex C. 3) the packet size is shown in third word of packet. For several information about the other packet's word see Annex A20.		OK	
Date 28/04/2002	Test Conductor A. Bertoli	P. Assurance S. Legramandi		

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>53</b> di <b>95</b> Page              of

## 8.4 MIL-STD 1553 SW DRIVER TEST PROCEDURE

### 8.4.1 OPEN MIL-STD 1553 CHANNEL

Step	Test Procedure Identifier	TR-DRV1553 -010	Results	Remarks
	Purpose	Verify the configuration of the MIL register and look up table		
	Special Requirement	.		
Procedure steps				
1	Upload the MIL-STD-1553 SW test using the ADSP emulator Connect the MIL1553 between board and Test Equipment and start the CONDOR BUS TOOL Program Set Remote terminal = 7 Set breakpoint after the Open procedure Start the program  Verify that the Mil registers are configured as defined in the specification The DDC chip is configured as Remote Terminal		OK	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>54</b> di <b>95</b> Page                of

2	<p>Set a new breakpoint after the mil configuration procedure</p> <p>Verify that the Mil registers are configured as defined in the specification</p> <p>The Look Up Table as the following configuration</p> <ul style="list-style-type: none"> <li>- The SA 10, 11-14, 27 Rx message has been configured pointing to Mil1553 memory free</li> <li>- The SA 10,11-26,27 Tx message has been configured pointing to Mil1553 memory free</li> <li>- The related SACW has been configured the message are configured in buffer message mode/or single buffer mode</li> </ul> <p>Verify that the pointed memory space are not overlapped but they are correctly allocated</p> <p>Verify that the Interrupt on Broadcast synchronize message mode code with data is enabled</p> <p>Verify that the memory configuration of the MIL follows the Mil DDC specification.</p>	OK	
3	<p>Set breakpoint after the Rtrun procedure</p> <p>Verify that the Mil Stack memory is cleared 0x8F000000 0x80000100</p>	OK	
Date 28/04/2002		Test Conductor A. Bertoli	
		P. Assurance S. Legramandi	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>55</b> di <b>95</b> Page              of

## 8.4.2 TX MIL-STD 1553 MESSAGE

Step	Test Procedure Identifier	TR-DRV1553 -020	Results	Remarks
	Purpose	Verify the Tx messages transmission		
	Special Requirement	.		
Procedure steps				
1	Upload the MIL-STD-1553 SW test using the ADSP emulator Connect the MIL1553 between board and Test Equipment and start the CONDOR BUS TOOL Program Set Remote terminal = 7 Set breakpoint after the Open procedure Start the program Set the CONDOR BUS TOOL Tx messages in order to acquire the SA 10, 11-26, 27 message  Verify that the messages are correctly received (no random value are acquired) Verify that the messages in the SA 11- 26 are composed of 32 words Verify that the messages in the SA 10, 27 are composed of 2 words		OK	
2	Acquire Tx messages by means of the CONDOR BUS TOOLS  Verify that the messages are correctly received (the value are incremented with respect to the Previous acquisition) Verify that the messages in the SA 11- 26 are composed of 32 words Verify that the messages in the SA 10, 27 are composed of 2 words Verify stopping the emulator that MIL1553 Stack memory contains the block message words		OK	
Date 28/04/2002		Test Conductor A. Bertoli	P. Assurance S. Legramandi	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>56</b> di <b>95</b> Page              of

### 8.4.3 RX MIL-STD 1553 MESSAGE

Step	Test Procedure Identifier	TR-DRV1553 -030	Results	Remarks
	Purpose	Verify the Rx messages reception		
	Special Requirement	.		
Procedure steps				
1	Upload the MIL-STD-1553 SW test using the ADSP emulator Connect the MIL1553 between board and Test Equipment and start the CONDOR BUS TOOL Program Set Remote terminal = 7 Set breakpoint after the Open procedure Start the program Set the CONDOR BUS TOOL Rx messages in order to acquire the SA 10, 11-24, 27 message  Verify that the messages are correctly transmitted to the ADSP Board checking the MIL DDC memory Verify that the messages in the SA 11- 26 are composed of 32 words Verify that the messages in the SA 10, 27 are composed of 2 words		OK	
2	Transmit Rx messages by means of the CONDOR BUS TOOLS  Verify that the messages are correctly transmitted to the ADSP Board checking the MIL DDC memory Verify that the messages in the SA 11- 26 are composed of 32 words Verify that the messages in the SA 10, 27 are composed of 2 words Verify stopping the emulator that MIL1553 Stack memory contains the block message words		OK	
Date 28/04/2002		Test Conductor A. Bertoli	P. Assurance S. Legramandi	



 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>57</b> di <b>95</b> Page                of

#### 8.4.4 CLOSE MIL-STD CHANNEL

Step	Test Procedure Identifier	TR-DRV1553 -040	Results	Remarks
	Purpose	Verify the Rx messages reception		
	Special Requirement	.		
Procedure steps				
1	Upload the MIL-STD-1553 SW test using the ADSP emulator Connect the MIL1553 between board and Test Equipment and start the CONDOR BUS TOOL Program Set Remote terminal = 7 Set breakpoint after the Open procedure Start the program Send and Acquire Rx and Tx MIL messages  Verify that all the messages are received - SA Rx 10,11-14,27 - SA Tx 10,11,26,27		OK	
2	Exit the program  Verify that the Mil register are reset		OK	
Date 28/04/2002		Test Conductor A. Bertoli	P. Assurance S. Legramandi	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>58</b> di <b>95</b> Page              of

## 8.5 EEPROM DRIVER TEST PROCEDURE

### 8.5.1 DELETE EEPROM SEGMENT

Step	Test Procedure Identifier	TR-DRVEPRM -010	Results	Remarks
	Purpose	Deleting of EEPROM segment		
	Special Requirement	.		
Procedure steps				
1	Upload the EEPROM test program using the ADSP emulator Set a breakpoint after a Delete Segment function call Write 10 times the 0xFFFFFFFF value beginning from the 0x80000000 address Start the program  Verify (when the breakpoint is stricken ) that the segment beginning at 0x80000000 until 0x800003FF address is cleaned		OK	
Date	Test Conductor	P. Assurance		
28/04/2002	A. Bertoli	S. Legramandi		

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>59</b> di <b>95</b> Page                of

## 8.5.2 WRITE EEPROM CELL

Step	Test Procedure Identifier	TR-DRVEPRM -020	Results	Remarks
	Purpose	Write EEPROM single cell inside the segment		
	Special Requirement	.		
Procedure steps				
1	Upload the EEPROM test program using the ADSP emulator Set a breakpoint after a write segment cell function call Start the program	Verify (when the breakpoint is stricken ) that the segment beginning at 0x80000C00 until 0x80000FFF address is written register the frame check sequence at the 0x80000C06 address and the value at 0x8000C17	OK	
2	Set a breakpoint after the "write eeprom cell" function call Start program	Verify that the 0xFFFFFFFF value is written at 0x80000C17 address and the DM Frame Check Sequence and PM Frame Check Sequence are changed with respect to the previous value	OK	
3	Set a Breakpoint after the "write eeprom cell" function call The original value of the segment is written at 0x80000c17 address Start program	Verify that the 0x00000010 value is written at 0x80000C17 Verify the DM Frame Check sequence and PM Frame sequence are the same of the step 1	OK	


 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>60</b> di <b>95</b> Page                of

4	Set a breakpoint before the "write eeprom cell" function call which writes the value 0xFFFFFFFF at the 0x80000C06 Read the value in 0x80000c06 Start Program  No check is required	OK	
5	Set breakpoint after the "write eeprom cell" function call  Verify that the 0xFFFFFFFF is written at 0x80000c06 address; Verify that the DM frame check sequence is changed with respect to value reported in step 4 Verify that the PM check sequence is equal to the value reported in Step 4	OK	
6	Write the original value at the 0x80000C06  Verify that DM FCS is equal to value reported in step 4 Verify that PM FCS is equal to the value reported in step 4	OK	
Date 28/04/2002		Test Conductor A. Bertoli	
		P. Assurance S. Legramandi	


 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>61</b> di Page                of <b>95</b>

### 8.5.3 DELETE EEPROM CELL

Step	Test Procedure Identifier	TR-DRVEPRM -020	Results	Remarks
	Purpose	Deleting of EEPROM single cell inside a segment		
	Special Requirement	.		
Procedure steps				
1	Upload the EEPROM test program using the ADSP emulator Set a breakpoint after a write segment cell function call Start the program  Verify that the segment beginning at 0x80000C00 until 0x80000FFF address is written register the frame check sequence at the 0x80000C06 address and the value at 0x8000C17		OK	
2	Set a breakpoint after the "delete eeprom cell" function call Start program  Verify that the 0x00000000 value is written at 0x80000C17 address and the DM Frame Check Sequence and PM Frame Check Sequence are changed with respect to the previous value		OK	
3	Set a Breakpoint after the "write eeprom cell" function call The original value of the segment is written at 0x80000c17 address Start program  Verify that the 0x00000010 value is written at 0x80000C17 Verify the DM Frame Check sequence and PM Frame sequence are the same of the step 1		OK	


 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>62</b> di <b>95</b> Page                of

4	Set a breakpoint before the "delete eeprom cell" function call which writes the value 0x00000000 at the 0x80000C06 Read the value in 0x80000c06 Start Program  No check is required	OK	
5	Set breakpoint after the "delete eeprom cell" function call  Verify that the 0x00000000 is written at 0x80000c06 address; Verify that the DM frame check sequence is changed with respect to value reported in step 4 Verify that the PM check sequence is equal to the value reported in Step 4	OK	
6	Write the original value at the 0x80000C06  Verify that DM FCS is equal to value reported in step 4 Verify that PM FCS is equal to the value reported in step 4	OK	
Date 28/04/2002		Test Conductor A. Bertoli	
P. Assurance S. Legramandi			

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>63</b> di <b>95</b> Page                of

#### 8.5.4 WRITE EEPROM SEGMENT

Step	Test Procedure Identifier	TR-DRVEPRM –030	Results	Remarks
	Purpose	Verify the EEPROM segment write		
	Special Requirement	.		
Procedure steps				
1	Upload the EEPROM test program using the ADSP emulator Set a breakpoint after a Delete Segment function call Start the program	Verify that the segment beginning at 0x80000C00 until 0x80000FFF address is cleaned	OK	
2	Set breakpoint after "write segment function" Start Program	Verify that a EEPROM segment is written at 0x80000C00 until xù0x80000FFF Verify that value of the segment are incremented by one starting from 0x8000C07 Verify that the first six word are the same defined inside the header	OK	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>64</b> di <b>95</b> Page              of

	Verify that in the header are included the field as follow <ul style="list-style-type: none"> <li>- current page</li> <li>- Total Page</li> <li>- NextPage in EEPROM</li> <li>- Application S/W start address</li> <li>- Application S/W Frame Check Sequence</li> <li>- PM start address</li> <li>- PM length</li> <li>- DM FCS</li> <li>- PM FCS</li> <li>- Boot Option</li> </ul> Verify that the word at 0x80000C05 address is the PM FCS (MSB 16 bits) and DM FCS (LSB 16 bits)	OK	
Date 28/04/2002	Test Conductor A. Bertoli	P. Assurance S. Legramandi	



 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>65</b> di <b>95</b> Page              of

### 8.5.5 ENABLE/DISABLE EEPROM PROTECTION

Step	Test Procedure Identifier	TR-DRVEPRM -040	Results	Remarks
	Purpose	Verify Enable/Disable EEPROM protection		
	Special Requirement	.		
Procedure steps				
1	Upload the EEPROM test program using the ADSP emulator Set a breakpoint after the "Enable Protection EEPROM" function call Verify that is possible to write a random data in EEPROM using the emulator Start the program  Verify that is no more possible to write a data in EEPROM (EEPROM is protected)		OK	
2	Set breakpoint after the "Disable Protection" function call  Verify that is possible to write in EEPROM the data		OK	
Date 28/04/2002		Test Conductor A. Bertoli	P. Assurance S. Legramandi	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date:
		Pagina <b>66</b> di <b>95</b> Page              of

## 8.5.6 COPY PROGRAM IN EEPROM

Step	Test Procedure Identifier	TR-DRVEPRM -050	Results	Remarks
	Purpose	Uploading in EEPROM of a generic program in Program Memory		
	Special Requirement	.		
Procedure steps				
1	Upload the EEPROM test program using the ADSP emulator Start the program  Wait the end of program		OK	
2	Verify that the first EEPROM page is written starting from 0x80000000 address Verify that the header has the following values <ul style="list-style-type: none"> <li>- PM address = 0000</li> <li>- PM length = 0x100</li> <li>- Current Eeprom page = 1</li> <li>- Total Eeprom pages = 6</li> <li>- Next Eeprom page = 0x80000400</li> </ul> Verify that in the segment are recorded the first 256 instructions (interrupt table) (Primary boot)		OK	
3	Verify that the Last EEPROM page is written starting from 0x8003FC00 address and the content is the same of the page in step 2 Verify that the header has the following values <ul style="list-style-type: none"> <li>- PM address = 0000</li> <li>- PM length = 0x100</li> <li>- Current Eeprom page = 1</li> <li>- Total Eeprom pages = 6</li> <li>- Next Eeprom page = 0x80000400</li> </ul> Verify that in the segment are recorded the first 256 instructions (interrupt table) (secondary Boot)		OK	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>67</b> di <b>95</b> Page                of

4	Verify that the EEPROM page is written starting from 0x8003FC00 address Verify that the header has the following values <ul style="list-style-type: none"> <li>- PM address = 4000</li> <li>- PM length = 0x2A6</li> <li>- Current Eeprom page = 2</li> <li>- Total Eeprom pages = 6</li> <li>- Next Eeprom page = 0x80000800</li> </ul> Verify that in the segment are recorded 0x2A6 instruction starting from PM address 0x4000	OK	
5	Verify that the EEPROM page is written starting from 0x8003FC00 address Verify that the header has the following values <ul style="list-style-type: none"> <li>- PM address = 42A6</li> <li>- PM length = 0x2A6</li> <li>- Current Eeprom page = 3</li> <li>- Total Eeprom pages = 6</li> <li>- Next Eeprom page = 0x80000C00</li> </ul> Verify that in the segment are recorded 0x2A6 instruction starting from PM address 0x42A6	OK	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>68</b> di <b>95</b> Page                of

6	Verify that the EEPROM page is written starting from 0x8003FC00 address Verify that the header has the following values <ul style="list-style-type: none"> <li>- PM address = 454C</li> <li>- PM length = 0x2A6</li> <li>- Current Eeprom page = 4</li> <li>- Total Eeprom pages = 6</li> <li>- Next Eeprom page = 0x80001000</li> </ul> Verify that in the segment are recorded 0x2A6 instruction starting from PM address 0x454C	OK	
7	Verify that the EEPROM page is written starting from 0x8003FC00 address Verify that the header has the following values <ul style="list-style-type: none"> <li>- PM address = 47F2</li> <li>- PM length = 0x2A6</li> <li>- Current Eeprom page = 5</li> <li>- Total Eeprom pages = 6</li> <li>- Next Eeprom page = 0x80000C00</li> </ul> Verify that in the segment are recorded 0x2A6 instruction starting from PM address 0x47F2	OK	
Date 28/04/2002		Test Conductor A. Bertoli	
P. Assurance S. Legramandi			

**ANNEX A : 1553 RETURNED PACKETS FORMAT AFTER 1355 COMMAND.**

**ANNEX A1: LEGENDA.**

Color	Memory zone
	Data memory
	General Registers
	Link Registers
	Software architecture
	DPRAM

**ANNEX A2: POWER-ON, OPEN LINK AND CLOSE LINK RETURNED PACKET.**

Functions	Word	Packets format	Memdump Zone	
Power-on	1	ID		
Open	2	Error Code		
Close	3	Packet_Size		
	4	Start Addr High		
	5	Start Addr Low		
	6	End Addr High		
	7	End Addr Low		
	8	i_status		Start SW_Architecture
	9	i_state		
	10	li_ByteSize_TX H		
	11	li_ByteSize_TX L		
	12	li_ByteSize_RX H		
	13	li_ByteSize_RX L		
	14	li_packets H		
	15	li_packets L		
	16	d_Flag		
	17	j_Timeout		
	18	None	End SW_Architecture	
	19	Start Addr High		
	20	Start Addr Low		
	21	End Addr High		
	22	End Addr Low		
	23	SICR high		Start: General Registers
	24	SICR Low		
	25	TRS_CTRL H		
	26	TRS_CTRL L		
	27	RT_CTRL H		
	28	RT_CTRL L		
	29	ISR H		
	30	ISR L		
	31	IMR H		
	32	IMR L		
	33	COMI_CS0R H		

	34	COMI_CS0R L	End: General Registers
	35	COMI_ACR H	
	36	COMI_ACR L	
	37	PRCIR H	
	38	PRCIR L	

**ANNEX A3: WRITE REGISTERS RETURNED PACKET.**

<i>Functions</i>	<i>Word</i>	<i>Packets format</i>	<i>Memdump Zone</i>
<b>WriteReg</b>	1	ID	
	2	Error Code	
	3	Packet_Size	
	4	Start Addr High	
	5	Start Addr Low	
	6	End Addr High	
	7	End Addr Low	
	8	CH1_COMICFG H	Start: Registers
	9	CH1_COMICFG L	End: Registers

**ANNEX A4: READ REGISTERS RETURNED PACKET.**

<i>Functions</i>	<i>Word</i>	<i>Packets format</i>	<i>Memdump Zone</i>
<b>ReadReg</b>	1	ID	
	2	Error Code	
	3	Packet_Size	
	4	Value Read H	Start: read
	5	Value Read L	End: read
	6	Start Addr High	
	7	Start Addr Low	
	8	End Addr High	
	9	End Addr Low	
	10	CH1_COMICFG H	Start: Registers
	11	CH1_COMICFG L	End: Registers



CARLO GAVAZZI SPACE SpA

# HSO/FIRST-DPU

HSO/FIRST DPU BASIC SW TEST REPORT

N° Doc: **DPU-RP-CGS-030**  
 Doc N°:  
 Ediz.: **1**      Data: **5/04/2002**  
 Issue:            Date:  
 Pagina **71**      di **95**  
 Page              of

## ANNEX A5: START LINK MASTER AND SLAVE, STOP LINK AND RESET LINK RETURNED PACKETS.

Functions	Word	Packets format	Memdump Zone	
Start link Master	1	ID		
	2	Error Code		
Start link Slave	3	Packet_Size		
	4	Start Addr High		
Stop link	5	Start Addr Low		
	6	End Addr High		
Reset link	7	End Addr Low		
	8	i_status	Start SW_Architecture	
9	i_state			
10	li_ByteSize_TX H			
11	li_ByteSize_TX L			
12	li_ByteSize_RX H			
13	li_ByteSize_RX L			
14	li_packets H			
15	li_packets L			
16	d_Flag			
17	j_Timeout			
18	None	End SW_Architecture		
	19	Start Addr High		
	20	Start Addr Low		
	21	End Addr High		
	22	End Addr Low		
	23	SICR high		Start: Registers
	24	SICR Low		
	25	TRS_CTRL H		
	26	TRS_CTRL L		
	27	RT_CTRL H		
	28	RT_CTRL L		
	29	ISR H		
	30	ISR L		
	31	IMR H		
	32	IMR L		
	33	COMI_CS0R H		
	34	COMI_CS0R L		
	35	COMI_ACR H		
	36	COMI_ACR L		
	37	PRCIR H		
	38	PRCIR L	End: Registers	
	39	Start Addr High		
	40	Start Addr Low		
	41	End Addr High		
	42	End Addr Low		
	43	CHx_DSM_MODR H		Start Link Registers
	44	CHx_DSM_MODR L		
	45	CHx_DSM_CMDR H		
	46	CHx_DSM_CMDR L		



CARLO GAVAZZI SPACE SpA

# HSO/FIRST-DPU

## HSO/FIRST DPU BASIC S/W TEST REPORT

N° Doc: **DPU-RP-CGS-030**  
Doc N°:  
Ediz.: **1**      Data: **5/04/2002**  
Issue:              Date:  
Pagina **72**      di **95**  
Page              of

47	CHx_DSM_STAR H	
48	CHx_DSM_STAR L	
49	CHx_DSM_TSTR H	
50	CHx_DSM_TSTR L	
51	CHx_ADDR H	
52	CHx_ADDR L	
53	CHx_RT_ADDR H	End Link Registers
54	CHx_RT_ADDR L	
55	CHx_PR_STAR H	
56	CHx_PR_STAR L	
57	CHx_CNTRL1 H	
58	CHx_CNTRL1 L	
59	CHx_CNTRL2 H	
60	CHx_CNTRL2 L	
61	CHx_HTID H	
62	CHx_HTID L	
63	CHx_HCNTRL H	
64	CHx_HCNTRL L	
65	CHx_ESR1 H	
66	CHx_ESR1 L	
67	CHx_ESR2 H	
68	CHx_ESR2 L	
69	CHx_COMICFG H	
70	CHx_COMICFG L	
71	CHx_TX_SAR H	
72	CHx_TX_SAR L	
73	CHx_TX_EAR H	
74	CHx_TX_EAR L	
75	CHx_TX_CAR H	
76	CHx_TX_CAR L	
77	CHx_TX_FIFO H	
78	CHx_TX_FIFO L	
79	CHx_TX_EOPB H	
80	CHx_TX_EOPB L	
81	CHx_RX_SAR H	
82	CHx_RX_SAR L	
83	CHx_RX_EAR H	
84	CHx_RX_EAR L	
85	CHx_RX_CAR H	
86	CHx_RX_CAR L	
87	CHx_RX_FIFO H	
88	CHx_RX_FIFO L	
89	CHx_STAR H	
90	CHx_STAR L	





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HSO/FIRST DPU BASIC SW TEST REPORT

N° Doc: **DPU-RP-CGS-030**  
 Doc N°:  
 Ediz.: **1**      Data: **5/04/2002**  
 Issue:              Date:  
 Pagina **73**      di **95**  
 Page              of

## ANNEX A6: WRITE LINK RETURNED PACKET.

Functions	Word	Packets format	Memdump Zone
<b>Write link</b>	1	ID	
	2	Error Code	
	3	Packets_Size	
	4	Start Addr High	
	5	Start Addr Low	
	6	End Addr High	
	7	End Addr Low	
	8	i_status	Start SW_Architecture
	9	i_state	
	10	li_ByteSize_TX H	
	11	li_ByteSize_TX L	
	12	li_ByteSize_RX H	
	13	li_ByteSize_RX L	
	14	li_packets H	
	15	li_packets L	
	16	d_Flag	
	17	j_Timeout	
	18	None	End SW_Architecture
	19	Start Addr High	
	20	Start Addr Low	
	21	End Addr High	
	22	End Addr Low	
	23	SICR high	Start: General Registers
	24	SICR Low	
	25	TRS_CTRL H	
	26	TRS_CTRL L	
	27	RT_CTRL H	
	28	RT_CTRL L	
	29	ISR H	
	30	ISR L	
	31	IMR H	
	32	IMR L	
	33	COMI_CS0R H	
	34	COMI_CS0R L	
	35	COMI_ACR H	
	36	COMI_ACR L	
	37	PRCIR H	
	38	PRCIR L	End: General Registers
	39	Start Addr High	
	40	Start Addr Low	
	41	End Addr High	
	42	End Addr Low	



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N° Doc: **DPU-RP-CGS-030**  
Doc N°:  
Ediz.: **1**      Data: **5/04/2002**  
Issue:              Date:  
Pagina **74**      di **95**  
Page              of

43	CHx_DSM_MODR H
44	CHx_DSM_MODR L
45	CHx_DSM_CMDR H
46	CHx_DSM_CMDR L
47	CHx_DSM_STAR H
48	CHx_DSM_STAR L
49	CHx_DSM_TSTR H
50	CHx_DSM_TSTR L
51	CHx_ADDR H
52	CHx_ADDR L
53	CHx_RT_ADDR H
54	CHx_RT_ADDR L
55	CHx_PR_STAR H
56	CHx_PR_STAR L
57	CHx_CNTRL1 H
58	CHx_CNTRL1 L
59	CHx_CNTRL2 H
60	CHx_CNTRL2 L
61	CHx_HTID H
62	CHx_HTID L
63	CHx_HCNTRL H
64	CHx_HCNTRL L
65	CHx_ESR1 H
66	CHx_ESR1 L
67	CHx_ESR2 H
68	CHx_ESR2 L
69	CHx_COMICFG H
70	CHx_COMICFG L
71	CHx_TX_SAR H
72	CHx_TX_SAR L
73	CHx_TX_EAR H
74	CHx_TX_EAR L
75	CHx_TX_CAR H
76	CHx_TX_CAR L
77	CHx_TX_FIFO H
78	CHx_TX_FIFO L
79	CHx_TX_EOPB H
80	CHx_TX_EOPB L
81	CHx_RX_SAR H
82	CHx_RX_SAR L
83	CHx_RX_EAR H
84	CHx_RX_EAR L
85	CHx_RX_CAR H
86	CHx_RX_CAR L
87	CHx_RX_FIFO H

Start: Link Registers



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N° Doc: **DPU-RP-CGS-030**  
Doc N°:  
Ediz.: **1**      Data: **5/04/2002**  
Issue:              Date:  
Pagina **75**      di  
Page              of **95**

88	CHx_RX_FIFO L	End: Link Registers
89	CHx_STAR H	
90	CHx_STAR L	
91	Start Addr High	
92	Start Addr Low	
93	End Addr High	
94	End Addr Low	Start DPRAM channel
95	DPRAM	
.....	DPRAM	
132	DPRAM	End DPRAM channel



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HSO/FIRST DPU BASIC SW TEST REPORT

N° Doc: **DPU-RP-CGS-030**  
 Doc N°:  
 Ediz.: **1**      Data: **5/04/2002**  
 Issue:            Date:  
 Pagina **76**      di **95**  
 Page              of

## ANNEX A7: READ LINK RETURNED PACKET.

Functions	Word	Packets format	Memdump Zone
<b>Read link</b>	1	ID	
	2	Error Code	
	3	Packets_Size	
	4	Start Addr High	
	5	Start Addr Low	
	6	End Addr High	
	7	End Addr Low	
	8	i_status	
	9	i_state	
	10	li_ByteSize_TX H	
	11	li_ByteSize_TX L	
	12	li_ByteSize_RX H	
	13	li_ByteSize_RX L	
	14	li_packets H	
	15	li_packets L	
	16	d_Flag	
	17	j_Timeout	
	18	None	End SW_Architecture
	19	Start Addr High	
	20	Start Addr Low	
	21	End Addr High	
	22	End Addr Low	
	23	SICR high	Start: Registers
	24	SICR Low	
	25	TRS_CTRL H	
	26	TRS_CTRL L	
	27	RT_CTRL H	
	28	RT_CTRL L	
	29	ISR H	
	30	ISR L	
	31	IMR H	
	32	IMR L	
	33	COMI_CS0R H	
	34	COMI_CS0R L	
	35	COMI_ACR H	
	36	COMI_ACR L	
	37	PRCIR H	
	38	PRCIR L	End: Registers
	39	Start Addr High	
	40	Start Addr Low	
	41	End Addr High	
	42	End Addr Low	



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N° Doc: **DPU-RP-CGS-030**  
Doc N°:  
Ediz.: **1**      Data: **5/04/2002**  
Issue:              Date:  
Pagina **77**      di **95**  
Page              of

43	CHx_DSM_MODR H
44	CHx_DSM_MODR L
45	CHx_DSM_CMDR H
46	CHx_DSM_CMDR L
47	CHx_DSM_STAR H
48	CHx_DSM_STAR L
49	CHx_DSM_TSTR H
50	CHx_DSM_TSTR L
51	CHx_ADDR H
52	CHx_ADDR L
53	CHx_RT_ADDR H
54	CHx_RT_ADDR L
55	CHx_PR_STAR H
56	CHx_PR_STAR L
57	CHx_CNTRL1 H
58	CHx_CNTRL1 L
59	CHx_CNTRL2 H
60	CHx_CNTRL2 L
61	CHx_HTID H
62	CHx_HTID L
63	CHx_HCNTRL H
64	CHx_HCNTRL L
65	CHx_ESR1 H
66	CHx_ESR1 L
67	CHx_ESR2 H
68	CHx_ESR2 L
69	CHx_COMICFG H
70	CHx_COMICFG L
71	CHx_TX_SAR H
72	CHx_TX_SAR L
73	CHx_TX_EAR H
74	CHx_TX_EAR L
75	CHx_TX_CAR H
76	CHx_TX_CAR L
77	CHx_TX_FIFO H
78	CHx_TX_FIFO L
79	CHx_TX_EOPB H
80	CHx_TX_EOPB L
81	CHx_RX_SAR H
82	CHx_RX_SAR L
83	CHx_RX_EAR H
84	CHx_RX_EAR L
85	CHx_RX_CAR H
86	CHx_RX_CAR L
87	CHx_RX_FIFO H

Start Link Registers



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N° Doc: **DPU-RP-CGS-030**  
 Doc N°:  
 Ediz.: **1**      Data: **5/04/2002**  
 Issue:            Date:  
 Pagina **78**      di  
 Page              of **95**

88	CHx_RX_FIFO L	End Link Registers
89	CHx_STAR H	
90	CHx_STAR L	
91	Start Addr High	
92	Start Addr Low	
93	End Addr High	
94	End Addr Low	Start DPRAM channel
95	DPRAM	
.....	DPRAM	
132	DPRAM	End DPRAM channel



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HSO/FIRST DPU BASIC SW TEST REPORT

N° Doc: **DPU-RP-CGS-030**  
 Doc N°:  
 Ediz.: **1**      Data: **5/04/2002**  
 Issue:              Date:  
 Pagina **79**      di **95**  
 Page              of

## ANNEX A8: READ PACKET RETURNED PACKET.

Functions	Word	Packets format	Memdump Zone	Note		
Read packets	1	ID		Packets number = 3		
	2	Error Code				
	3	Packets_Size				
	4	Start Addr High				
	5	Start Addr Low				
	6	End Addr High				
	7	End Addr Low				
	8	i_status			Start SW_Architecture	
	9	i_state				
	10	li_ByteSize_TX H				
	11	li_ByteSize_TX L				
	12	li_ByteSize_RX H				
	13	li_ByteSize_RX L				
	14	li_packets H				
	15	li_packets L				
	16	d_Flag				
	17	j_Timeout				
	18	None				End SW_Architecture
	19	Start Addr High				
	20	Start Addr Low				
	21	End Addr High				
	22	End Addr Low				
	23	SICR high			Start: Registers	
	24	SICR Low				
	25	TRS_CTRL H				
	26	TRS_CTRL L				
	27	RT_CTRL H				
	28	RT_CTRL L				
	29	ISR H				
	30	ISR L				
	31	IMR H				
	32	IMR L				
	33	COMI_CS0R H				
	34	COMI_CS0R L				
	35	COMI_ACR H				
	36	COMI_ACR L				
	37	PRCIR H				
	38	PRCIR L				End: Registers
	39	Start Addr High				
	40	Start Addr Low				
	41	End Addr High				
	42	End Addr Low				



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## HSO/FIRST DPU BASIC SW TEST REPORT

N° Doc:  
Doc N°:

**DPU-RP-CGS-030**

Ediz.:  
Issue:

**1**

Data:  
Date:

**5/04/2002**

Pagina  
Page

**80**

di  
of

**95**

43	CHx_DSM_MODR H	Start Link Registers	
44	CHx_DSM_MODR L		
45	CHx_DSM_CMDR H		
46	CHx_DSM_CMDR L		
47	CHx_DSM_STAR H		
48	CHx_DSM_STAR L		
49	CHx_DSM_TSTR H		
50	CHx_DSM_TSTR L		
51	CHx_ADDR H		
52	CHx_ADDR L		
53	CHx_RT_ADDR H		
54	CHx_RT_ADDR L		
55	CHx_PR_STAR H		
56	CHx_PR_STAR L		
57	CHx_CNTRL1 H		
58	CHx_CNTRL1 L		
59	CHx_CNTRL2 H		
60	CHx_CNTRL2 L		
61	CHx_HTID H		
62	CHx_HTID L		
63	CHx_HCNTRL H		
64	CHx_HCNTRL L		
65	CHx_ESR1 H		
66	CHx_ESR1 L		
67	CHx_ESR2 H		
68	CHx_ESR2 L		
69	CHx_COMICFG H		
70	CHx_COMICFG L		
71	CHx_TX_SAR H		
72	CHx_TX_SAR L		
73	CHx_TX_EAR H		
74	CHx_TX_EAR L		
75	CHx_TX_CAR H		
76	CHx_TX_CAR L		
77	CHx_TX_FIFO H		
78	CHx_TX_FIFO L		
79	CHx_TX_EOPB H		
80	CHx_TX_EOPB L		
81	CHx_RX_SAR H		
82	CHx_RX_SAR L		
83	CHx_RX_EAR H		
84	CHx_RX_EAR L		
85	CHx_RX_CAR H		
86	CHx_RX_CAR L		
87	CHx_RX_FIFO H		
88	CHx_RX_FIFO L		
89	CHx_STAR H		
90	CHx_STAR L		End Link Registers





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# HSO/FIRST-DPU

## HSO/FIRST DPU BASIC SW TEST REPORT

N° Doc: **DPU-RP-CGS-030**  
Doc N°:  
Ediz.: **1**      Data: **5/04/2002**  
Issue:              Date:  
Pagina **81**      di **95**  
Page              of

91	Start Addr High	
92	Start Addr Low	
93	End Addr High	
94	End Addr Low	
95	rx_pbuffer	Start rx_pbuffer
96	rx_pbuffer	
97	rx_pbuffer	
98	rx_pbuffer	
99	rx_pbuffer	
100	rx_pbuffer	
101	rx_pbuffer	
102	rx_pbuffer	
103	rx_pbuffer	
104	rx_pbuffer	
105	rx_pbuffer	
106	rx_pbuffer	
107	rx_pbuffer	
108	rx_pbuffer	
109	rx_pbuffer	
110	rx_pbuffer	
111	rx_pbuffer	
112	rx_pbuffer	
113	rx_pbuffer	
114	rx_pbuffer	
115	rx_pbuffer	
116	rx_pbuffer	
117	rx_pbuffer	
118	rx_pbuffer	
119	rx_pbuffer	
120	rx_pbuffer	
121	rx_pbuffer	
122	rx_pbuffer	
123	rx_pbuffer	
124	rx_pbuffer	
125	rx_pbuffer	
126	rx_pbuffer	
127	rx_pbuffer	
128	rx_pbuffer	
129	rx_pbuffer	
130	rx_pbuffer	
131	rx_pbuffer	
132	rx_pbuffer	
133	rx_pbuffer	
134	rx_pbuffer	
135	rx_pbuffer	
136	rx_pbuffer	
137	rx_pbuffer	
138	rx_pbuffer	



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## HSO/FIRST DPU BASIC S/W TEST REPORT

N° Doc: **DPU-RP-CGS-030**  
Doc N°:  
Ediz.: **1**      Data: **5/04/2002**  
Issue:              Date:  
Pagina **82**      di **95**  
Page              of

139	rx_pbuffer
140	rx_pbuffer
141	rx_pbuffer
142	rx_pbuffer
143	rx_pbuffer
144	rx_pbuffer
145	rx_pbuffer
146	rx_pbuffer
147	rx_pbuffer
148	rx_pbuffer
149	rx_pbuffer
150	rx_pbuffer
151	rx_pbuffer
152	rx_pbuffer
153	rx_pbuffer
154	rx_pbuffer
155	rx_pbuffer
156	rx_pbuffer
157	rx_pbuffer
158	rx_pbuffer
159	rx_pbuffer
160	rx_pbuffer
161	rx_pbuffer
162	rx_pbuffer
163	rx_pbuffer
164	rx_pbuffer
165	rx_pbuffer
166	rx_pbuffer
167	rx_pbuffer
168	rx_pbuffer
169	rx_pbuffer
170	rx_pbuffer
171	rx_pbuffer
172	rx_pbuffer
173	rx_pbuffer
174	rx_pbuffer
175	rx_pbuffer
176	rx_pbuffer
177	rx_pbuffer
178	rx_pbuffer
179	rx_pbuffer
180	rx_pbuffer
181	rx_pbuffer
182	rx_pbuffer
183	rx_pbuffer
184	rx_pbuffer
185	rx_pbuffer
186	rx_pbuffer

187	rx_pbuffer	End rx_pbuffer
188	rx_pbuffer	
189	rx_pbuffer	
190	rx_pbuffer	
191	rx_pbuffer	
192	rx_pbuffer	
193	rx_pbuffer	
194	rx_pbuffer	
195	rx_pbuffer	
196	rx_pbuffer	
197	rx_pbuffer	
198	rx_pbuffer	

### ANNEX A9: PACKET NUM, GET\_W\_SIZE AND GET\_R\_SIZE RETURNED PACKETS.

Functions	Word	Packets format	Memdump Zone
<b>Get_W_SIZE</b>	1	ID	
<b>Get_R_SIZE</b>	2	Error Code	
<b>Packet Num</b>	3	Packets_Size	
	4	li_value high	Start data read
	5	li_value low	End data read
	6	Start Addr High	
	7	Start Addr Low	
	8	End Addr High	
	9	End Addr Low	
	10	byte H SW arch	Start SW_Architecture
	11	byte L SW arch	End SW_Architecture

### ANNEX A10: GET STATUS RETURNED PACKET.

Functions	Word	Packets format	Memdump Zone
<b>Status</b>	1	ID	
	2	Error Code	
	3	Packet_Size	
	4	Li_value read H	Start data read
	5	Li_value read L	End data read
	6	Start Addr High	
	7	Start Addr Low	
	8	End Addr High	
	9	End Addr Low	
	10	byte H register	Start: Status Register
	11	byte L register	End: Status Register

### ANNEX A11: GET\_IDSTATE AND GET\_IDSTATUS RETURNED PACKET.

Functions	Word	Packets format	Memdump Zone
<b>IDStatus</b>	1	ID	
<b>IDState</b>	2	Error Code	

	3	Packet_Size	
	4	li_value_read	Data read
	5	Start Addr High	
	6	Start Addr Low	
	7	End Addr High	
	8	End Addr Low	
	9	byte SW arch	SW_Architecture

**ANNEX A12: SET TIMEOUT RETURNED PACKET.**

<i>Functions</i>	<i>Word</i>	<i>Packets format</i>	<i>Memdump Zone</i>
<b>Set Timeout</b>	1	ID	
	2	Error Code	
	3	Packet_Size	
	4	Start Addr High	
	5	Start Addr Low	
	6	End Addr High	
	7	End Addr Low	
	8	byte SW arch	
	9	Start Addr High	Start: Registers
	10	Start Addr Low	
	11	End Addr High	
	12	End Addr Low	
	13	SICR high	
	14	SICR Low	
	15	TRS_CTRL H	
	16	TRS_CTRL L	
	17	RT_CTRL H	
	18	RT_CTRL L	
	19	ISR H	
	20	ISR L	
	21	IMR H	
	22	IMR L	
	23	COMI_CS0R H	
	24	COMI_CS0R L	
	25	COMI_ACR H	
	26	COMI_ACR L	
	27	PRCIR H	
	28	PRCIR L	End: Registers

**ANNEX A13: EXIT STUB RETURNED PACKET.**

<i>Functions</i>	<i>Word</i>	<i>Packets format</i>	<i>Memdump Zone</i>
<b>Exit_Stub</b>	1	ID	
	2	Error Code	
	3	Packet_Size	

**ANNEX A14: ERROR ON SELECT NUMBER OF FUCTION RETURNED PACKET.**

<i>Functions</i>	<i>Word</i>	<i>Packets format</i>	<i>Memdump Zone</i>
<b>None</b>	1	ID	
	2	Error Code	
	3	Packet_Size	



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# HSO/FIRST-DPU

HSO/FIRST DPU BASIC S/W TEST REPORT

N° Doc: **DPU-RP-CGS-030**  
 Doc N°:  
 Ediz.: **1**      Data: **5/04/2002**  
 Issue:            Date:  
 Pagina **86**      di  
 Page              of **95**

## ANNEX A15: WRITE TO BOARD MEMORY RETURNED PACKET.

Functions	Word	Packets format	Memdump Zone	
Write to Board Memory	1	ID	Start tx_pbuffer	
	2	Error Code		
	3	Packet_size		
	4	Buffer size		
	5	Tx_pbuffer		
	6	Tx_pbuffer		
	7	Tx_pbuffer		
	8	Tx_pbuffer		
	9	Tx_pbuffer		
	10	Tx_pbuffer		
	11	Tx_pbuffer		
	12	Tx_pbuffer		
	13	Tx_pbuffer		
	14	Tx_pbuffer		
	15	Tx_pbuffer		
	16	Tx_pbuffer		
	17	Tx_pbuffer		
	18	Tx_pbuffer		
	19	Tx_pbuffer		
	20	Tx_pbuffer		
	21	Tx_pbuffer		
	22	Tx_pbuffer		
	23	Tx_pbuffer		
	24	Tx_pbuffer		
	25	Tx_pbuffer		
	26	Tx_pbuffer		
	27	Tx_pbuffer		
	28	Tx_pbuffer		
	29	Tx_pbuffer		
	30	Tx_pbuffer		
	31	Tx_pbuffer		
	32	Tx_pbuffer		
	33	Tx_pbuffer		
	34	Tx_pbuffer		
	35	Tx_pbuffer		
	36	Tx_pbuffer		
	37	Tx_pbuffer		
	38	Tx_pbuffer		
	39	Tx_pbuffer		
	40	Start Addr High		End tx_pbuffer
	41	Start Addr Low		
	42	End Addr High		
	43	End Addr Low		
	44	DPRAM		
		Start DPRAM channel		



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## HSO/FIRST DPU BASIC S/W TEST REPORT

N° Doc: **DPU-RP-CGS-030**  
Doc N°:  
Ediz.: **1**      Data: **5/04/2002**  
Issue:              Date:  
Pagina **87**      di  
Page              of **95**

45	DPRAM	
46	DPRAM	
47	DPRAM	
48	DPRAM	
49	DPRAM	
50	DPRAM	
51	DPRAM	
52	DPRAM	
53	DPRAM	
54	DPRAM	
55	DPRAM	
56	DPRAM	
57	DPRAM	
58	DPRAM	
59	DPRAM	
60	DPRAM	
61	DPRAM	
62	DPRAM	
63	DPRAM	
64	DPRAM	
65	DPRAM	
66	DPRAM	
67	DPRAM	
68	DPRAM	
69	DPRAM	
70	DPRAM	
71	DPRAM	
72	DPRAM	
73	DPRAM	
74	DPRAM	
75	DPRAM	
76	DPRAM	
77	DPRAM	
78	DPRAM	
79	DPRAM	
80	DPRAM	
81	DPRAM	
82	DPRAM	



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# HSO/FIRST-DPU

HSO/FIRST DPU BASIC S/W TEST REPORT

N° Doc: **DPU-RP-CGS-030**  
 Doc N°:  
 Ediz.: **1**      Data: **5/04/2002**  
 Issue:              Date:  
 Pagina **88**      di **95**  
 Page              of

## ANNEX A16: READ FROM BOARD MEMORY RETURNED PACKET.

Functions	Word	Packets format	Memdump Zone	
Read from Board Memory	1	ID	Start rx_pbuffer	
	2	Error Code		
	3	Packet_size		
	4	Buffer size		
	5	Rx_pbuffer		
	6	Rx_pbuffer		
	7	Rx_pbuffer		
	8	Rx_pbuffer		
	9	Rx_pbuffer		
	10	Rx_pbuffer		
	11	Rx_pbuffer		
	12	Rx_pbuffer		
	13	Rx_pbuffer		
	14	Rx_pbuffer		
	15	Rx_pbuffer		
	16	Rx_pbuffer		
	17	Rx_pbuffer		
	18	Rx_pbuffer		
	19	Rx_pbuffer		
	20	Rx_pbuffer		
	21	Rx_pbuffer		
	22	Rx_pbuffer		
	23	Rx_pbuffer		
	24	Rx_pbuffer		
	25	Rx_pbuffer		
	26	Rx_pbuffer		
	27	Rx_pbuffer		
	28	Rx_pbuffer		
	29	Rx_pbuffer		
	30	Rx_pbuffer		
	31	Rx_pbuffer		
	32	Rx_pbuffer		
	33	Rx_pbuffer		
	34	Rx_pbuffer		
	35	Rx_pbuffer		
	36	Rx_pbuffer		
	37	Rx_pbuffer		
	38	Rx_pbuffer		
	39	Rx_pbuffer		
	40	Start Addr High		End rx_pbuffer
	41	Start Addr Low		
	42	End Addr High		
	43	End Addr Low		
	44	DPRAM		
		Start DPRAM channel		





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# HSO/FIRST-DPU


## HSO/FIRST DPU BASIC S/W TEST REPORT

N° Doc: **DPU-RP-CGS-030**  
 Doc N°:  
 Ediz.: **1**      Data: **5/04/2002**  
 Issue:              Date:  
 Pagina **89**      di  
 Page              of **95**

45	DPRAM	
46	DPRAM	
47	DPRAM	
48	DPRAM	
49	DPRAM	
50	DPRAM	
51	DPRAM	
52	DPRAM	
53	DPRAM	
54	DPRAM	
55	DPRAM	
56	DPRAM	
57	DPRAM	
58	DPRAM	
59	DPRAM	
60	DPRAM	
61	DPRAM	
62	DPRAM	
63	DPRAM	
64	DPRAM	
65	DPRAM	
66	DPRAM	
67	DPRAM	
68	DPRAM	
69	DPRAM	
70	DPRAM	
71	DPRAM	
72	DPRAM	
73	DPRAM	
74	DPRAM	
75	DPRAM	
76	DPRAM	
77	DPRAM	
78	DPRAM	
79	DPRAM	
80	DPRAM	
81	DPRAM	
82	DPRAM	

### ANNEX A17: WATCHDOG DELAY RETURNED PACKET.

Functions	Word	Packets format	Memdump Zone
WD_Delay	1	ID	
	2	Error Code	
	3	Packet_Size	
	4	Watchdog Timer	

 CARLO GAVAZZI SPACE SpA	<h1>HSO/FIRST-DPU</h1>	N° Doc: <b>DPU-RP-CGS-030</b> Doc N°:
	<b>HSO/FIRST DPU BASIC S/W TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>90</b> di Page              of <b>95</b>

**ANNEX A18: WATCHDOG DELAY FAILED RETURNED PACKET.**

<i>Functions</i>	<i>Word</i>	<i>Packets format</i>	<i>Memdump Zone</i>
<b>WD_Delay_Fail</b>	1	ID	
	2	Error Code	
	3	Packet_Size	
	4	Watchdog Timer	

**ANNEX A19: WATCHDOG REFRESH RETURNED PACKET.**

<i>Functions</i>	<i>Word</i>	<i>Packets format</i>	<i>Memdump Zone</i>
<b>WD_Refresh</b>	1	ID	
	2	Error Code	
	3	Packet_Size	

**ANNEX A20: WATCHDOG STATUS RETURNED PACKET.**

<i>Functions</i>	<i>Word</i>	<i>Packets format</i>	<i>Memdump Zone</i>
<b>WD_Status</b>	1	ID	
	2	Error Code	
	3	Packet_Size	
	4	Watchdog Status	

**ANNEX A21: ERROR CODE RETURNED PACKET.**

<i>Functions</i>	<i>Word</i>	<i>Packets format</i>	<i>Memdump Zone</i>
<b>None</b>	1	ID	
	2	Error Code	
	3	Packet_Size	

**ANNEX A22: EXIT STUB RETURNED PACKET.**

<i>Functions</i>	<i>Word</i>	<i>Packets format</i>	<i>Memdump Zone</i>
<b>Exit_Stub</b>	1	ID	
	2	Error Code	
	3	Packet_Size	



CARLO GAVAZZI SPACE SpA

# HSO/FIRST-DPU

HSO/FIRST DPU BASIC S/W TEST REPORT

N° Doc: **DPU-RP-CGS-030**  
 Doc N°:  
 Ediz.: **1**      Data: **5/04/2002**  
 Issue:              Date:  
 Pagina **91**      di **95**  
 Page              of

## ANNEX A1: RETURNED MIL-STD-1553 PACKETS FORMAT AFTER A EEPROM COMMAND

N/A

## ANNEX C : 1355 DRIVERS RETURNED ERRORS CODE

Flag	Function	Type of error
0	FOR ALL	OK
1	FOR ALL	NOT-OK
2	WRITE TO BOARD MEMORY	OVERFLOW ON TRANSMISSION ON DPRAM
3	WRITE TO BOARD MEMORY	UNDERFLOW ON TRANSMISSION ON DPRAM
4		
9		
10	READ FROM BOARD MEMORY	OVERFLOW ON RECEPTION ON DPRAM
11	READ FROM BOARD MEMORY	UNDERFLOW ON RECEPTION ON DPRAM
12		
19		
20	OPEN LINK	ERROR: NUM OF LINK > MAX NUM OF LINK
21	OPEN LINK	LINK CH1 ALREADY OPEN
22	OPEN LINK	LINK CH2 ALREADY OPEN
23	OPEN LINK	LINK CH3 ALREADY OPEN
24		
29		
30	CLOSE LINK	ERROR: NUM OF LINK > MAX NUM OF LINK
31	CLOSE LINK	LINK CH1 ALREADY CLOSE
32	CLOSE LINK	LINK CH2 ALREADY CLOSE
33	CLOSE LINK	LINK CH3 ALREADY CLOSE
34		
39		
40	START LINK MASTER	ERROR: NUM OF LINK > MAX NUM OF LINK
41	START LINK MASTER	LINK CH1 CLOSE
42	START LINK MASTER	LINK CH2 CLOSE
43	START LINK MASTER	LINK CH3 CLOSE
44	START LINK MASTER	SPEED NOT AUTHORIZED ON LINK CH1
45	START LINK MASTER	SPEED NOT AUTHORIZED ON LINK CH2
46	START LINK MASTER	SPEED NOT AUTHORIZED ON LINK CH3
47	START LINK MASTER	ERROR ON WRITE REGISTER CH1_DSM_MODR
48	START LINK MASTER	ERROR ON WRITE REGISTER CH2_DSM_MODR
49	START LINK MASTER	ERROR ON WRITE REGISTER CH3_DSM_MODR
50	START LINK MASTER	ERROR ON WRITE REGISTER CH1_COMICFG
51	START LINK MASTER	ERROR ON WRITE REGISTER CH2_COMICFG
52	START LINK MASTER	ERROR ON WRITE REGISTER CH3_COMICFG
53	START LINK MASTER	ERROR ON WRITE REGISTER CH1_CNTRL1
54	START LINK MASTER	ERROR ON WRITE REGISTER CH2_CNTRL1
55	START LINK MASTER	ERROR ON WRITE REGISTER CH3_CNTRL1

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## HSO/FIRST DPU BASIC S/W TEST REPORT

N° Doc: **DPU-RP-CGS-030**  
Doc N°:  
Ediz.: **1**      Data: **5/04/2002**  
Issue:              Date:  
Pagina **92**      di **95**  
Page              of

56	START LINK MASTER	ERROR ON WRITE REGISTER CH1_DSM_CMDR
57	START LINK MASTER	ERROR ON WRITE REGISTER CH2_DSM_CMDR
58	START LINK MASTER	ERROR ON WRITE REGISTER CH3_DSM_CMDR
59	START LINK MASTER	STARTING ERROR: LINK CH1 IS BLOCKED
60	START LINK MASTER	STARTING ERROR: LINK CH1 IS BLOCKED
61	START LINK MASTER	STARTING ERROR: LINK CH1 IS BLOCKED
62		
63		
64		
65	SET TIMEOUT	ERROR TIMEOUT ISN'T AUTHORIZED ON LINK CH1
66	SET TIMEOUT	ERROR TIMEOUT ISN'T AUTHORIZED ON LINK CH2
67	SET TIMEOUT	ERROR TIMEOUT ISN'T AUTHORIZED ON LINK CH3
68		
69		
70	STOP LINK	ERROR: NUM OF LINK > MAX NUM OF LINK
71	STOP LINK	LINK CH1 ALREADY CLOSE
72	STOP LINK	LINK CH2 ALREADY CLOSE
73	STOP LINK	LINK CH3 ALREADY CLOSE
74	STOP LINK	ERROR ON WRITE REGISTER CH1_DSM_CMDR
75	STOP LINK	ERROR ON WRITE REGISTER CH2_DSM_CMDR
76	STOP LINK	ERROR ON WRITE REGISTER CH3_DSM_CMDR
77		
89		
90	READ PACKET	ERROR: NUM OF LINK > MAX NUM OF LINK
91	READ PACKET	ERROR OVERFLOW ON DPRAM ON LINK CH1
92	READ PACKET	ERROR OVERFLOW ON DPRAM ON LINK CH2
93	READ PACKET	ERROR OVERFLOW ON DPRAM ON LINK CH3
94	READ PACKET	LINK CH1 CLOSE
95	READ PACKET	LINK CH2 CLOSE
96	READ PACKET	LINK CH3 CLOSE
97	READ PACKET	LINK CH1 PARITY OR DISCONNECT ERROR DETECTED
98	READ PACKET	LINK CH2 PARITY OR DISCONNECT ERROR DETECTED
99	READ PACKET	LINK CH3 PARITY OR DISCONNECT ERROR DETECTED
100	READ PACKET	LINK CH1 NOT STARTED OR NOT DONE
101	READ PACKET	LINK CH2 NOT STARTED OR NOT DONE
102	READ PACKET	LINK CH3 NOT STARTED OR NOT DONE
103		
109		
110	RESET LINK	ERROR: NUM OF LINK > MAX NUM OF LINK
111	RESET LINK	LINK CH1 CLOSE: RESET IMPOSSIBLE
112	RESET LINK	LINK CH2 CLOSE: RESET IMPOSSIBLE
113	RESET LINK	LINK CH3 CLOSE: RESET IMPOSSIBLE
114	RESET LINK	ERROR ON WRITE REGISTER CH1_DSM_CMDR
115	RESET LINK	ERROR ON WRITE REGISTER CH2_DSM_CMDR
116	RESET LINK	ERROR ON WRITE REGISTER CH3_DSM_CMDR
117		
129		
130	READ LINK	ERROR: NUM OF LINK > MAX NUM OF LINK



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# HSO/FIRST-DPU

## HSO/FIRST DPU BASIC S/W TEST REPORT

N° Doc: **DPU-RP-CGS-030**  
Doc N°:  
Ediz.: **1**      Data: **5/04/2002**  
Issue:              Date:  
Pagina **93**      di **95**  
Page              of

131	READ LINK	READ BYTE OVERFLOW ON LINK CH1
132	READ LINK	READ BYTE OVERFLOW ON LINK CH2
133	READ LINK	READ BYTE OVERFLOW ON LINK CH3
134	READ LINK	LINK CH1 CLOSE
135	READ LINK	LINK CH2 CLOSE
136	READ LINK	LINK CH3 CLOSE
137	READ LINK	LINK CH1 PARITY OR DISCONNECT ERROR DETECTED
138	READ LINK	LINK CH2 PARITY OR DISCONNECT ERROR DETECTED
139	READ LINK	LINK CH3 PARITY OR DISCONNECT ERROR DETECTED
140	READ LINK	READ ERROR ON CH1_DSM_STAR
141	READ LINK	READ ERROR ON CH2_DSM_STAR
142	READ LINK	READ ERROR ON CH3_DSM_STAR
143	READ LINK	ERROR WRITE ON CH1_RX_SAR
144	READ LINK	ERROR WRITE ON CH2_RX_SAR
145	READ LINK	ERROR WRITE ON CH3_RX_SAR
146	READ LINK	ERROR WRITE ON CH1_RX_EAR
147	READ LINK	ERROR WRITE ON CH2_RX_EAR
148	READ LINK	ERROR WRITE ON CH3_RX_EAR
149	READ LINK	TIMEOUT ERROR: LINK CH1 NOT STARTED
150	READ LINK	TIMEOUT ERROR: LINK CH2 NOT STARTED
151	READ LINK	TIMEOUT ERROR: LINK CH3 NOT STARTED
152	READ LINK	TRANSFER IN PROGRESS ON LINK CH1
153	READ LINK	TRANSFER IN PROGRESS ON LINK CH2
154	READ LINK	TRANSFER IN PROGRESS ON LINK CH3
155	READ LINK	NULL NOT FOUND ON LINK CH1
156	READ LINK	NULL NOT FOUND ON LINK CH2
157	READ LINK	NULL NOT FOUND ON LINK CH3
158	READ LINK	ERROR PARITY ON LINK CH1
159	READ LINK	ERROR PARITY ON LINK CH2
160	READ LINK	ERROR PARITY ON LINK CH3
161	READ LINK	ERROR DISCONNECT ON LINK CH1
162	READ LINK	ERROR DISCONNECT ON LINK CH2
163	READ LINK	ERROR DISCONNECT ON LINK CH3
164		
169		
170	WRITE LINK	ERROR: NUM OF LINK > MAX NUM OF LINK
171	WRITE LINK	OVERFLOW ON WRITE ON CH1
172	WRITE LINK	OVERFLOW ON WRITE ON CH2
173	WRITE LINK	OVERFLOW ON WRITE ON CH3
174	WRITE LINK	LINK CH1 CLOSE
175	WRITE LINK	LINK CH2 CLOSE
176	WRITE LINK	LINK CH3 CLOSE
177	WRITE LINK	LINK CH1 PARITY OR DISCONNECT ERROR DETECTED
178	WRITE LINK	LINK CH2 PARITY OR DISCONNECT ERROR DETECTED
179	WRITE LINK	LINK CH3 PARITY OR DISCONNECT ERROR DETECTED
180	WRITE LINK	ERROR WRITE ON CH1_TX_SAR
181	WRITE LINK	ERROR WRITE ON CH2_TX_SAR
182	WRITE LINK	ERROR WRITE ON CH3_TX_SAR




CARLO GAVAZZI SPACE SpA

# HSO/FIRST-DPU

## HSO/FIRST DPU BASIC S/W TEST REPORT

N° Doc: **DPU-RP-CGS-030**  
Doc N°:  
Ediz.: **1**      Data: **5/04/2002**  
Issue:              Date:  
Pagina **94**      di **95**  
Page              of

183	WRITE LINK	ERROR WRITE ON CH1_TX_EAR
184	WRITE LINK	ERROR WRITE ON CH2_TX_EAR
185	WRITE LINK	ERROR WRITE ON CH3_TX_EAR
186	WRITE LINK	TIMEOUT ERROR ON CH1
187	WRITE LINK	TIMEOUT ERROR ON CH2
188	WRITE LINK	TIMEOUT ERROR ON CH3
189	WRITE LINK	TRANSFER IN PROGRESS ON LINK CH1
190	WRITE LINK	TRANSFER IN PROGRESS ON LINK CH2
191	WRITE LINK	TRANSFER IN PROGRESS ON LINK CH3
192	WRITE LINK	NULL NOT FOUND ON LINK CH1
193	WRITE LINK	NULL NOT FOUND ON LINK CH2
194	WRITE LINK	NULL NOT FOUND ON LINK CH3
195		
199		
200	START LINK SLAVE	ERROR: NUM OF LINK > MAX NUM OF LINK
201	START LINK SLAVE	LINK CH1 CLOSE
202	START LINK SLAVE	LINK CH2 CLOSE
203	START LINK SLAVE	LINK CH3 CLOSE
204	START LINK SLAVE	SPEED ERROR ON LINK CH1
205	START LINK SLAVE	SPEED ERROR ON LINK CH2
206	START LINK SLAVE	SPEED ERROR ON LINK CH3
207	START LINK SLAVE	ERROR ON READ REGISTER CH1_DSM_STAR
208	START LINK SLAVE	ERROR ON READ REGISTER CH2_DSM_STAR
209	START LINK SLAVE	ERROR ON READ REGISTER CH3_DSM_STAR
210	START LINK SLAVE	ERROR ON WRITE REGISTER CH1_DSM_MODR
211	START LINK SLAVE	ERROR ON WRITE REGISTER CH2_DSM_MODR
212	START LINK SLAVE	ERROR ON WRITE REGISTER CH3_DSM_MODR
213	START LINK SLAVE	ERROR ON WRITE REGISTER CH1_COMICFG
214	START LINK SLAVE	ERROR ON WRITE REGISTER CH2_COMICFG
215	START LINK SLAVE	ERROR ON WRITE REGISTER CH3_COMICFG
216	START LINK SLAVE	ERROR ON WRITE REGISTER CH1_CNTRL1
217	START LINK SLAVE	ERROR ON WRITE REGISTER CH2_CNTRL1
218	START LINK SLAVE	ERROR ON WRITE REGISTER CH3_CNTRL1
219	START LINK SLAVE	ERROR ON WRITE REGISTER CH1_DSM_CMDR
220	START LINK SLAVE	ERROR ON WRITE REGISTER CH2_DSM_CMDR
221	START LINK SLAVE	ERROR ON WRITE REGISTER CH3_DSM_CMDR
222	START LINK SLAVE	TRANSFER ERROR TIMEOUT CH1
223	START LINK SLAVE	TRANSFER ERROR TIMEOUT CH2
224	START LINK SLAVE	TRANSFER ERROR TIMEOUT CH3
225		
239		
240	STUB	VALUE ERROR
241	STUB	POWER ON FAILED: NO SW ARCHITETTURE PRODUCED
242	STUB	WRITE REGISTER FAILED
243	STUB	READ REGISTER FAILED
244	STUB	WRITE ON WATCHDOG REGISTER FAILED
245	STUB	ERROR TO ACCESS AT SW ARCHITECTURE
246	STUB	ERROR TO GET LINK STATUS

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	<b>HSO/FIRST DPU BASIC SW TEST REPORT</b>	Ediz.: <b>1</b> Data: <b>5/04/2002</b> Issue:              Date: Pagina <b>95</b> di Page              of <b>95</b>