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Reference Documents 1
Document Issue Record 1
1. Introduction 1
2. Spacecraft AIT Flow 2
2.1. Annotated EQM AIT flow 2
2.2. Annotated PFM AIT Flow 3
3. Termination connectors to make SPIRE ESD safe ..... **Error! Bookmark not defined.**
4. Specification of termination connectors 12
5. Comments on the integration procedure 16

Reference Documents

RD-1 HP-2-ASED-PL-0021 Issue 2
RD-2 Astrium HP-2-ASED-PL-0031 Issue 1

Document Issue Record

Issue Number	Date	Changes
0.1 Draft	Friday, 11 June 2004	Initial release for comment

1. Introduction

This note outlines the precautions to be taken to protect the focal plane units of SPIRE from ESD damage during AIT when they are not connected to the DRCU. Particular attention is paid to the spacecraft EQM and PFM AIT phases.

Section 2 of this note outlines the AIT sequence of the Spacecraft for both the EQM and PFM AIT programmes. The AIT flow charts are taken from RD-1 and RD-2 and are included for information only. The flowcharts are annotated to indicate the particular configuration of ESD protection hardware required at different stages of the EQM and PFM programmes.

Section 3 specifies the configuration that the instrument will be in to keep the focal plane units from being damaged by ESD events. These instrument configurations have been annotated on the flow charts in section 2.

Section 4 specifies the main details of the hardware identified in section 4 .

As some new hardware has been specified in this document, various procedures will need to be revised and possibly updated to reflect this new information. Comments on the existing procedures are included in section 5.

2. Spacecraft AIT Flow

2.1. Annotated EQM AIT flow

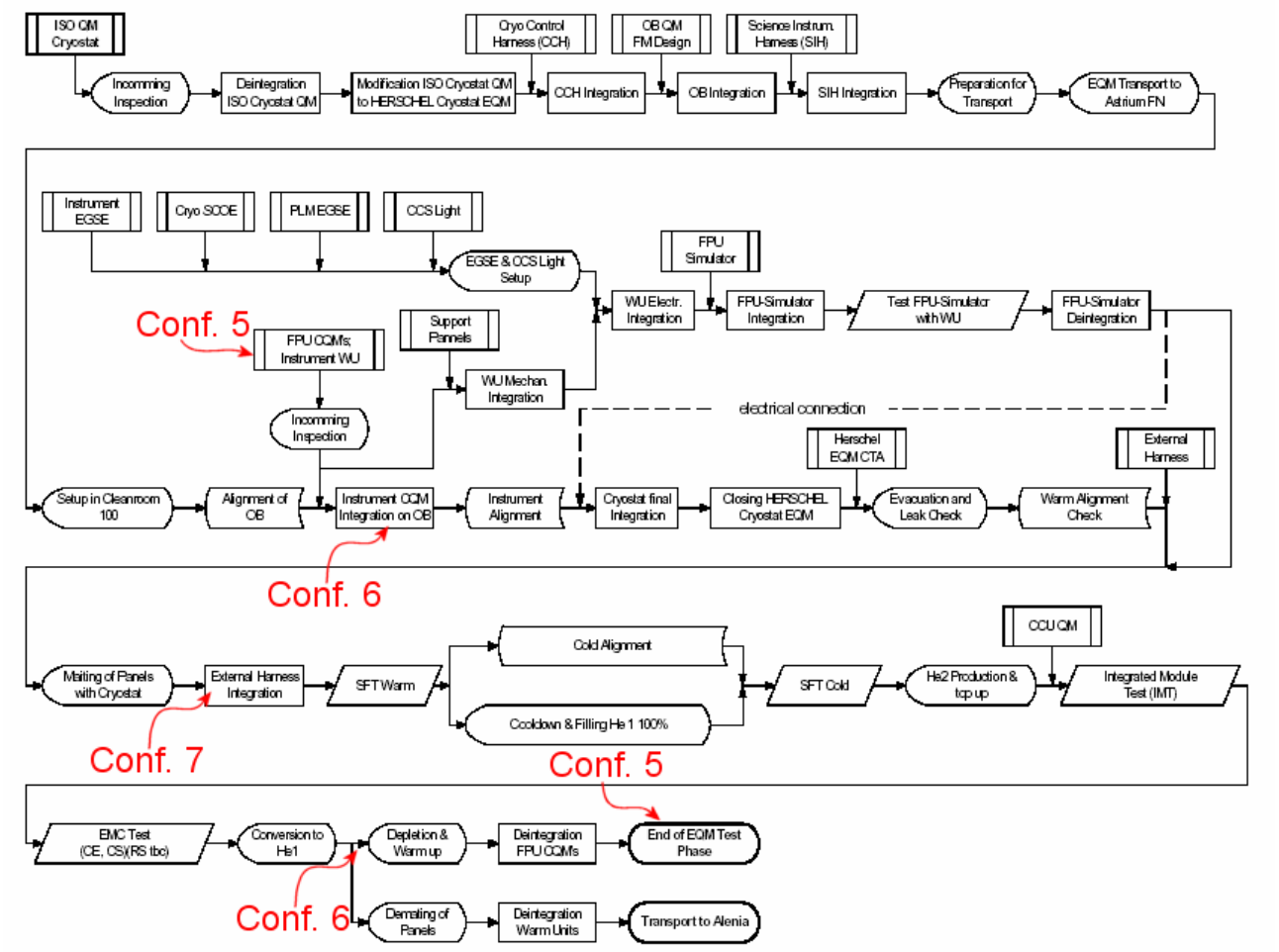


Figure 1 – Annotated EQM AIT Flow chart. Un-marked-up chart *for reference only*, from Astrium HP-2-ASED-PL-0021 Issue 2

2.2. Annotated PFM AIT Flow

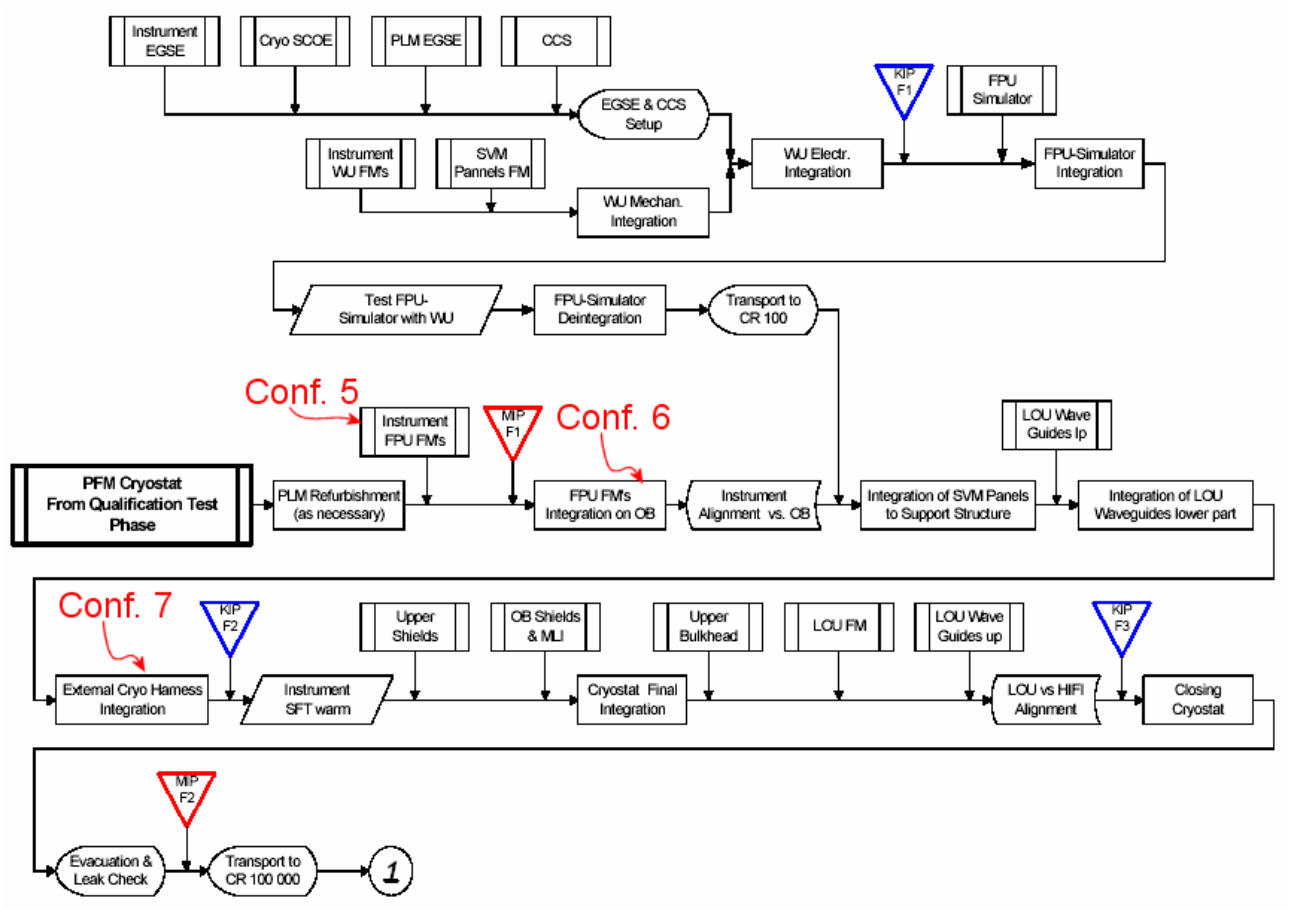


Figure 2 – Annotated PFM AIT Flow chart Un-marked-up chart *for reference only*, from Astrium HP-2-ASED-PL-0031 Issue 1

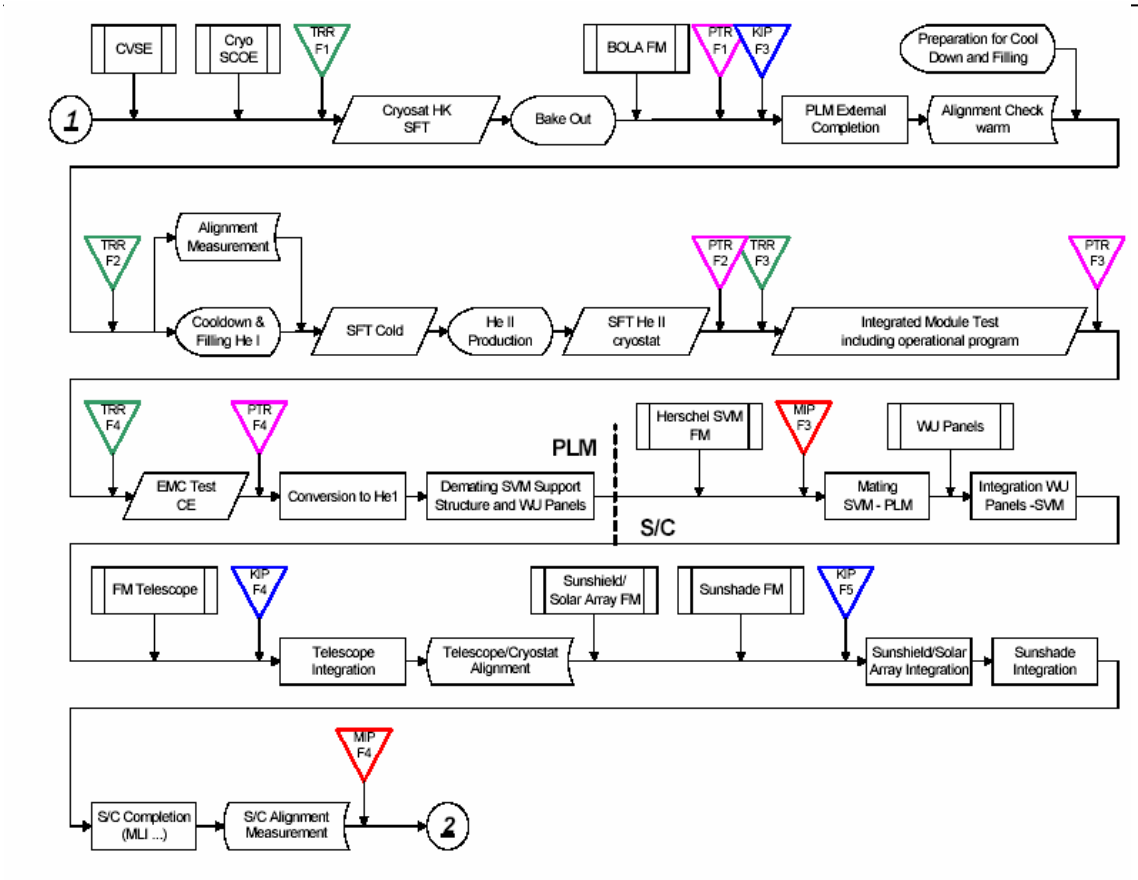
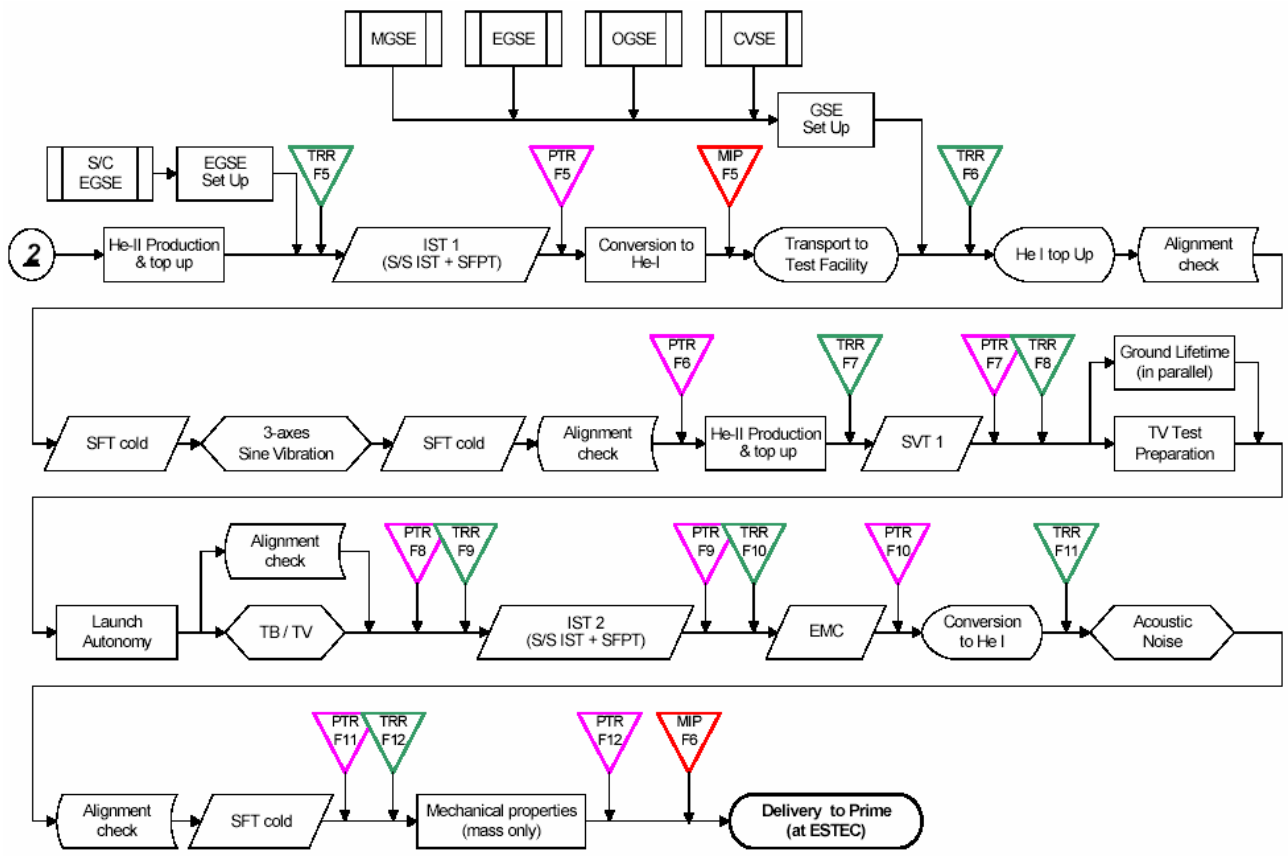
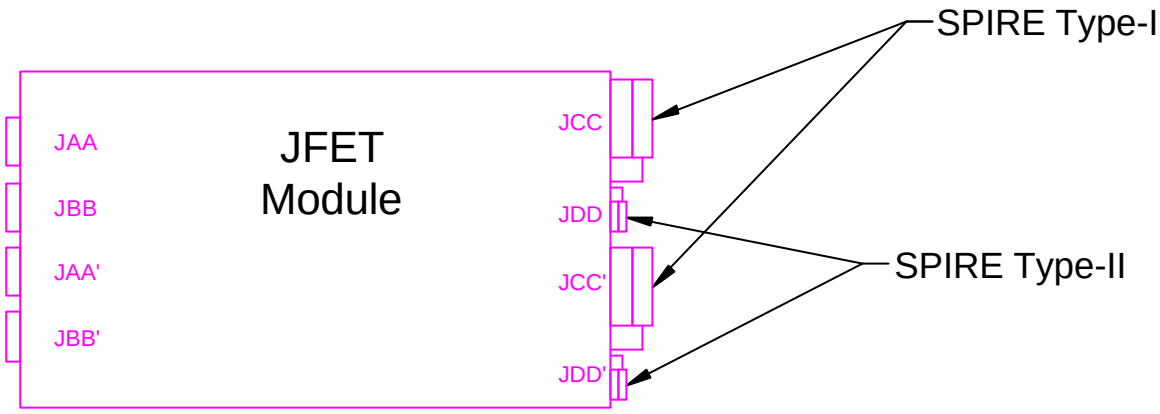
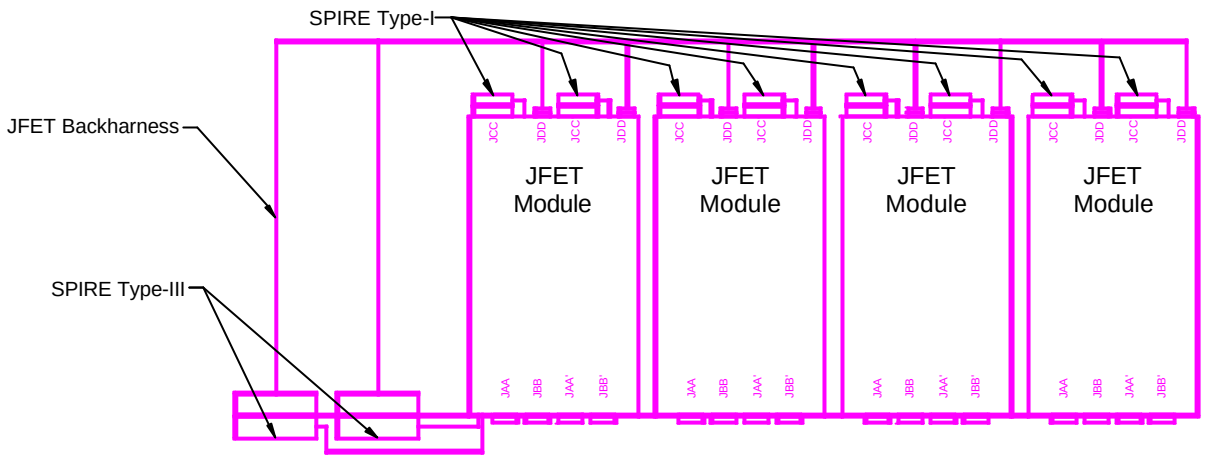


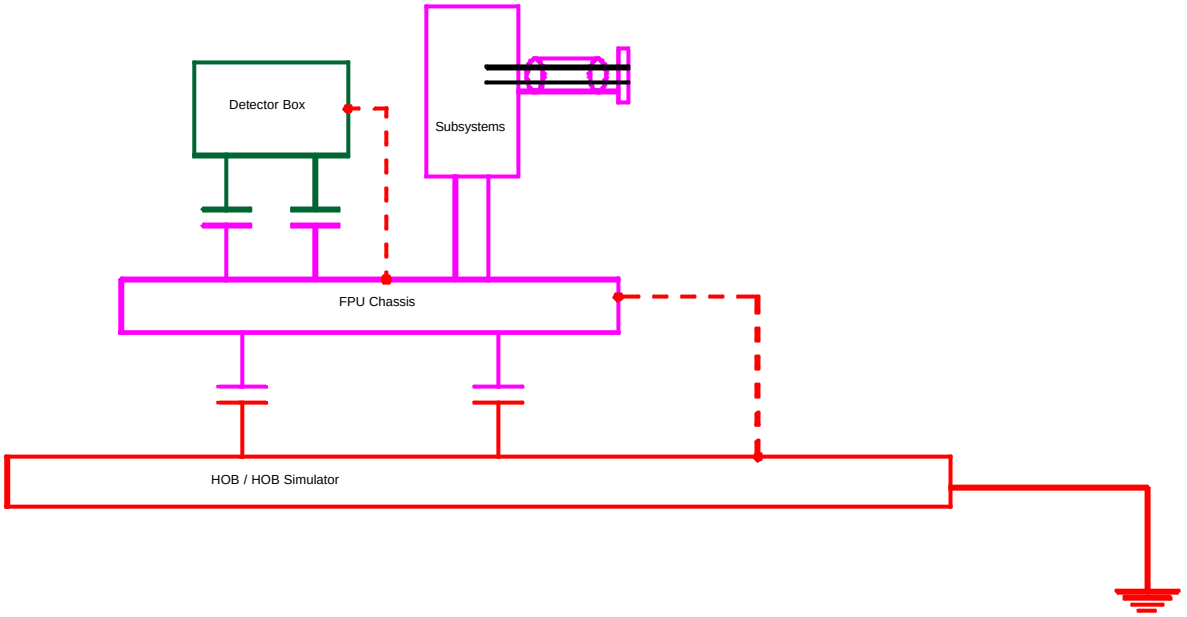
Figure 3 - PFM AIT Flow (*for reference only,* from Astrium HP-2-ASED-PL-0031 Issue 1)

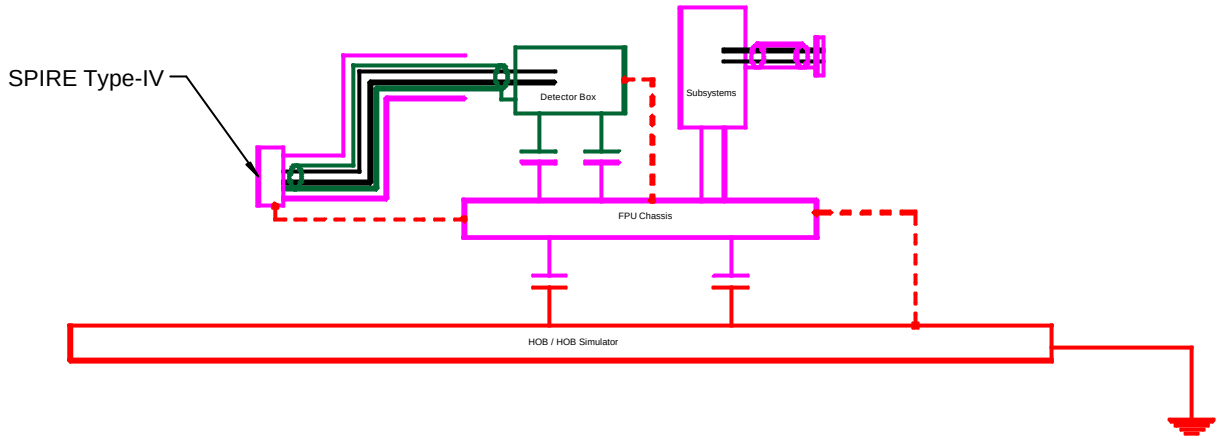


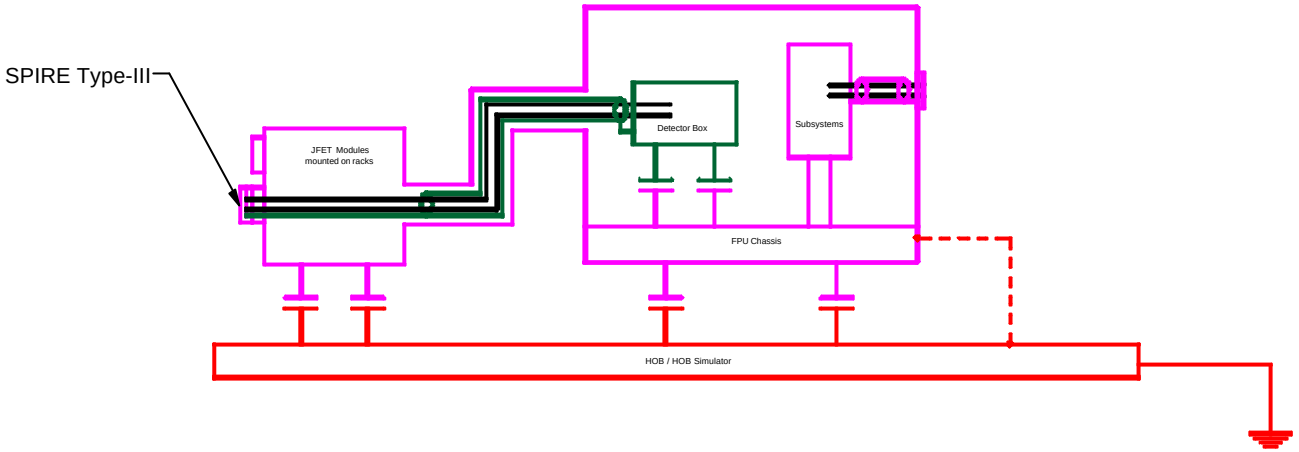
3. ESD Protected Instrument Configurations

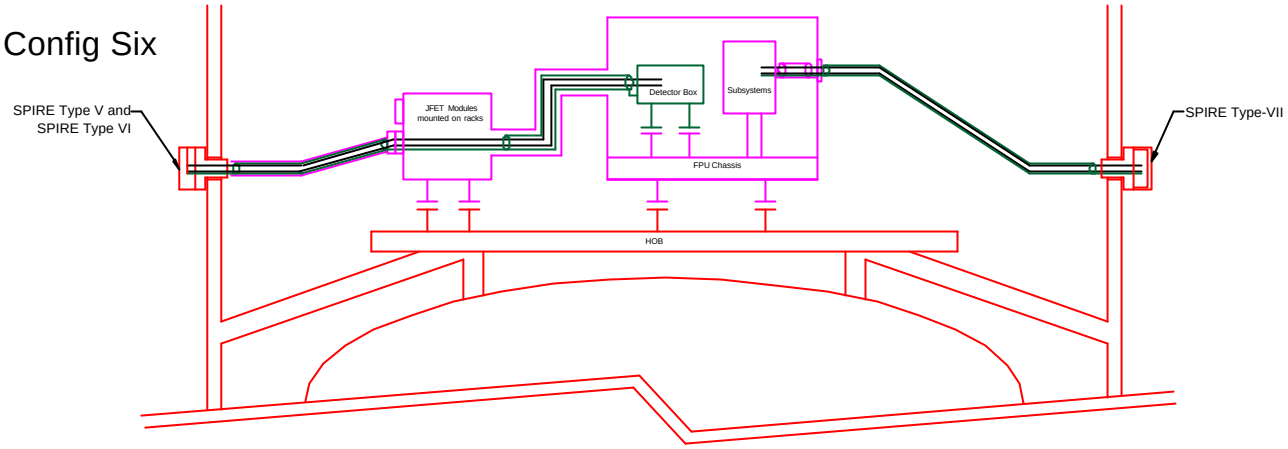
Instrument Configuration	Location/State of Instrument	ESD Protection Details
Config. 1	• JFET modules as delivered and not integrated into JFET racks	 • SPIRE termination plugs Type-I used to protect gates of JFETs • SPIRE termination plugs Type-II used to protect drain and sources of JFETs **Comments** • The outputs of the JFETs are left open (JAA, JBB, JAA' and JBB'); a discharge to these could damage the devices

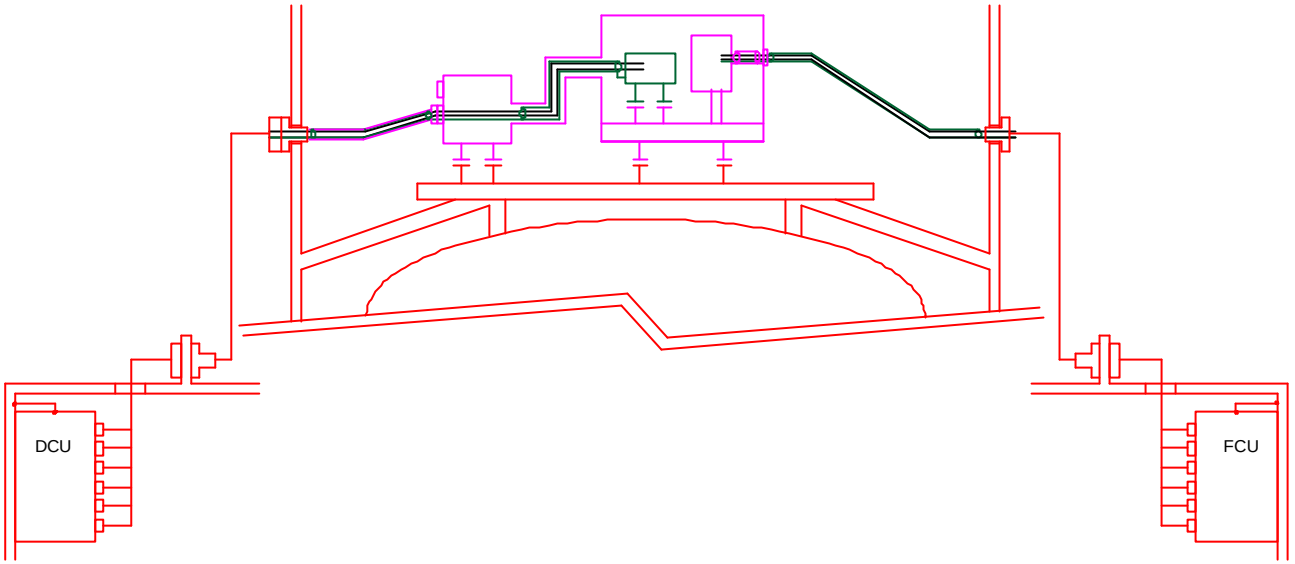
Instrument Configuration	Location/State of Instrument	ESD Protection Details
Config. 2	• JFET Modules integrated into JFET racks • JFET Backharnesses installed • No external harness connected to JFETS	 • SPIRE termination plugs Type-I used to protect gates of JFETs • SPIRE termination plugs Type-III used to protect drain and sources of JFETs **Comments** • The outputs of the JFETs are left open (JAA, JBB, JAA' and JBB'); a discharge to these could damage the devices

Instrument Configuration	Location/State of Instrument	ESD Protection Details
Config. 3	• During integration • Covers off • JFETs not connected • BDA Harnesses not connected	 • Red Tag grounding strap connecting the Photometer Detector Box to FPU Chassis • Red Tag grounding strap connecting the Spectrometer Detector Box to FPU Chassis • Red Tag grounding strap connecting FPU Chassis to Optical Bench • Lumalloy film covering exposed BDA connectors. • No termination plugs on the subsystem connectors **Comments** • A discharge to the BDA connector pins could damage the detectors and/or the bias resistors • The subsystem are left unprotected (except for the protection afforded by the Cristek filters)

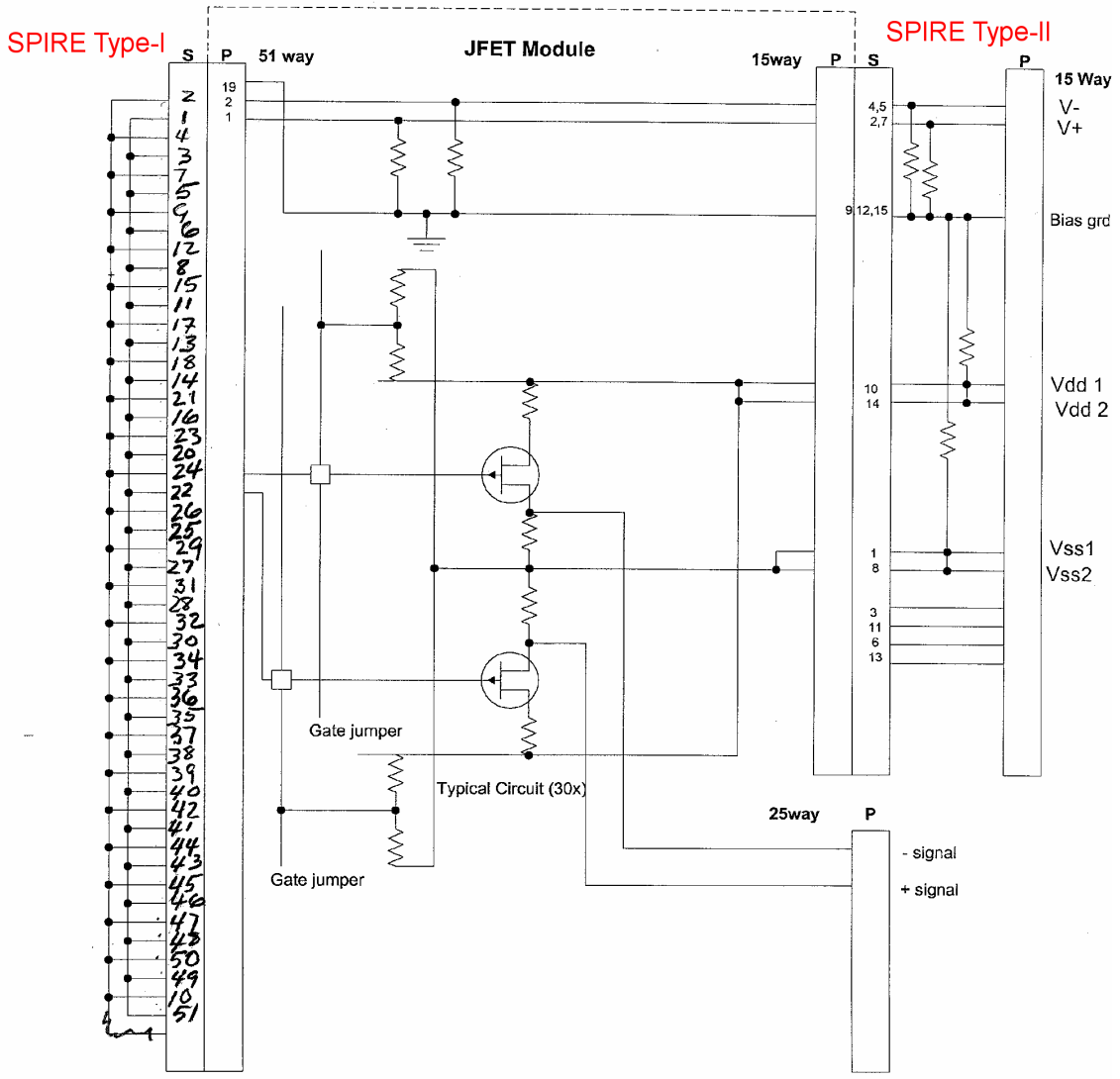
Instrument Configuration	Location/State of Instrument	ESD Protection Details
Config. 4	• During integration • Covers off • JFETs not connected • BDA Harnesses connected	 • Red Tag grounding strap connecting the Photometer Detector Box to FPU Chassis • Red Tag grounding strap connecting the Spectrometer Detector Box to FPU Chassis • Red Tag grounding strap connecting FPU Chassis to Optical Bench • One MDM51P shorting plug SPIRE-Type IV protecting Photometer BDAs • One MDM51P shorting plug SPIRE-Type IV protecting Spectrometer BDAs • Exposed, un-terminated MDM51 connectors stowed inside Lumalloy bags

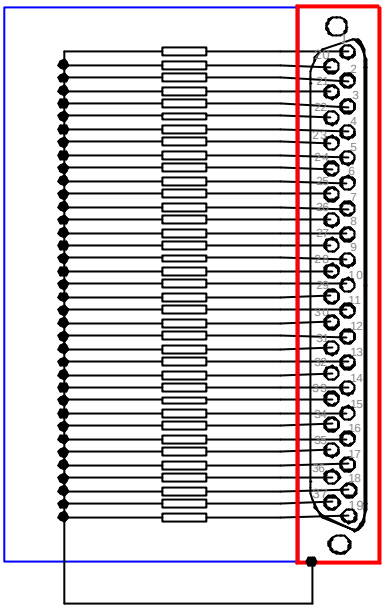
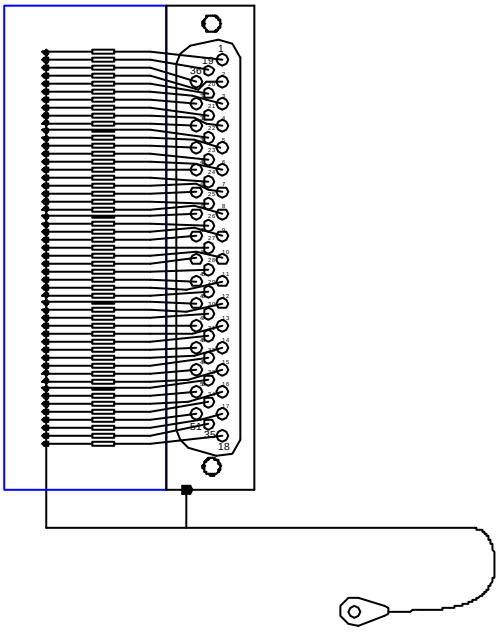
Instrument Configuration	Location/State of Instrument	ESD Protection Details
Config. 5	• Covers ON • BDA - JFETs harnesses connected • JFET backharnesses pre-installed on JFETs	 • Red Tag grounding strap connecting FPU Chassis to Optical Bench • Four MDM 37S shorting plugs (SPIRE Type-V) on Photometer Bias connectors (JFP J25, J26, J27 and J28) • Two MDM 37S shorting plugs (SPIRE Type-V) on Spectrometer Bias connectors (JFS J09 and J10) • Lumalloy covering exposed MDM25P connectors **Comments** • This is the configuration used for transport of the cold plane units.

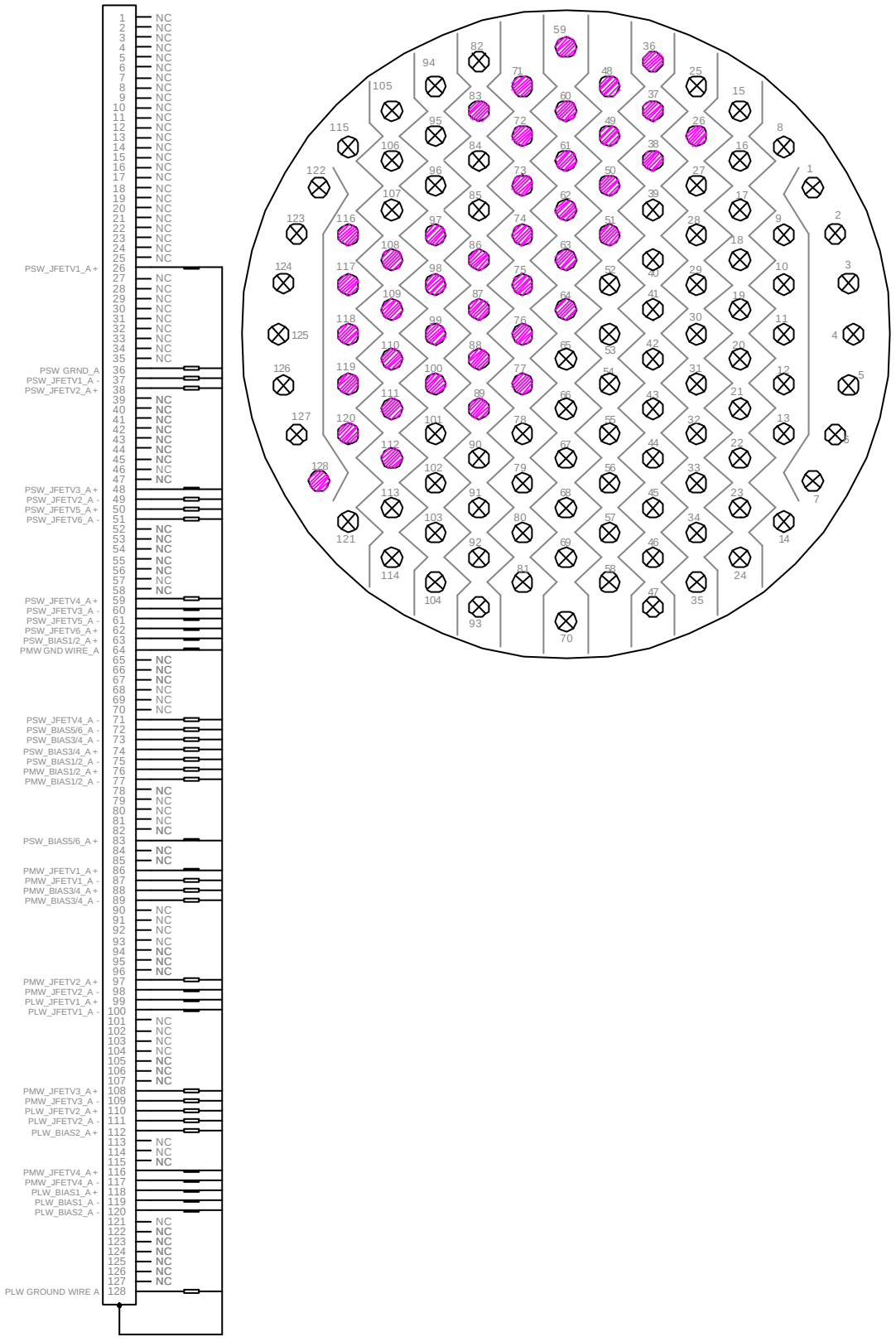
Instrument Configuration	Location/State of Instrument	ESD Protection Details
Config. 6	• Covers ON • BDA - JFETs harnesses connected • JFET backharnesses pre-installed on JFETs • Internal SIH installed (i.e. Cryoharness) • Cryostat closed and therefore no further access to PFUs possible! • SIH not connecting WE to cold plane units.	 • Shorting plug (SPIRE Type-IV) on Photometer bias • Shorting plug (SPIRE Type-V) on Spectrometer bias • EMC Backshell (SPIRE Type-VIII) on other active exposed harnesses **Comments** **A. For EQM (only PLW BDA/JFET active):** • If the external SIH between the CVV-CB wall and the SVM I/F-CB **is not installed**, then SPIRE termination plug Type-IV to be used to substitute CVV-CB 210000 P26 • If the external SIH between the CVV-CB and the SVM I/F-CB **is installed** then SPIRE termination plug Type-IV to be used on SVM I/F-CB 312000 P04 • EMI plug backshell to cover exposed receptacles on C6, C10 and C11 with no mating plug contacts will provide adequate protection. **B. For PFM (all Phot and Spect. BDAs active):** • If the external SIH between the CVV-CB and the SVM I/F-CB **is not installed**, then SPIRE termination plug Type-IV to be used to substitute CVV-CB 210000 P26 and Type-V to be used to substitute CVV-CB 210000 P32 • If the external SIH between the CVV-CB and the SVM I/F-CB **is not installed**, then SPIRE termination plug Type-IV to be used to substitute CVV-CB 210000 P26 and Type-V to be used to substitute CVV-CB 210000 P32312000 P04 • EMI plug backshell to cover exposed receptacles on C2, C4, C5, C6, C7, C8, C9, C10, C11, C13 with no mating plug contacts will provide adequate protection.

Instrument Configuration	Location/State of Instrument	ESD Protection Details
Config. 7	• FPU/JFETs integrated on optics bench • Cryoharness fully integrated • DRCU fully integrated	 **Comments** **A. For EQM:** • Only Phot Bias (C3), PLW Detector harness (C6) and prime S/S harnesses (C10/C11) connected. • Backshell covers C6 **B. For PFM:** • All detector and subsystem harnesses used

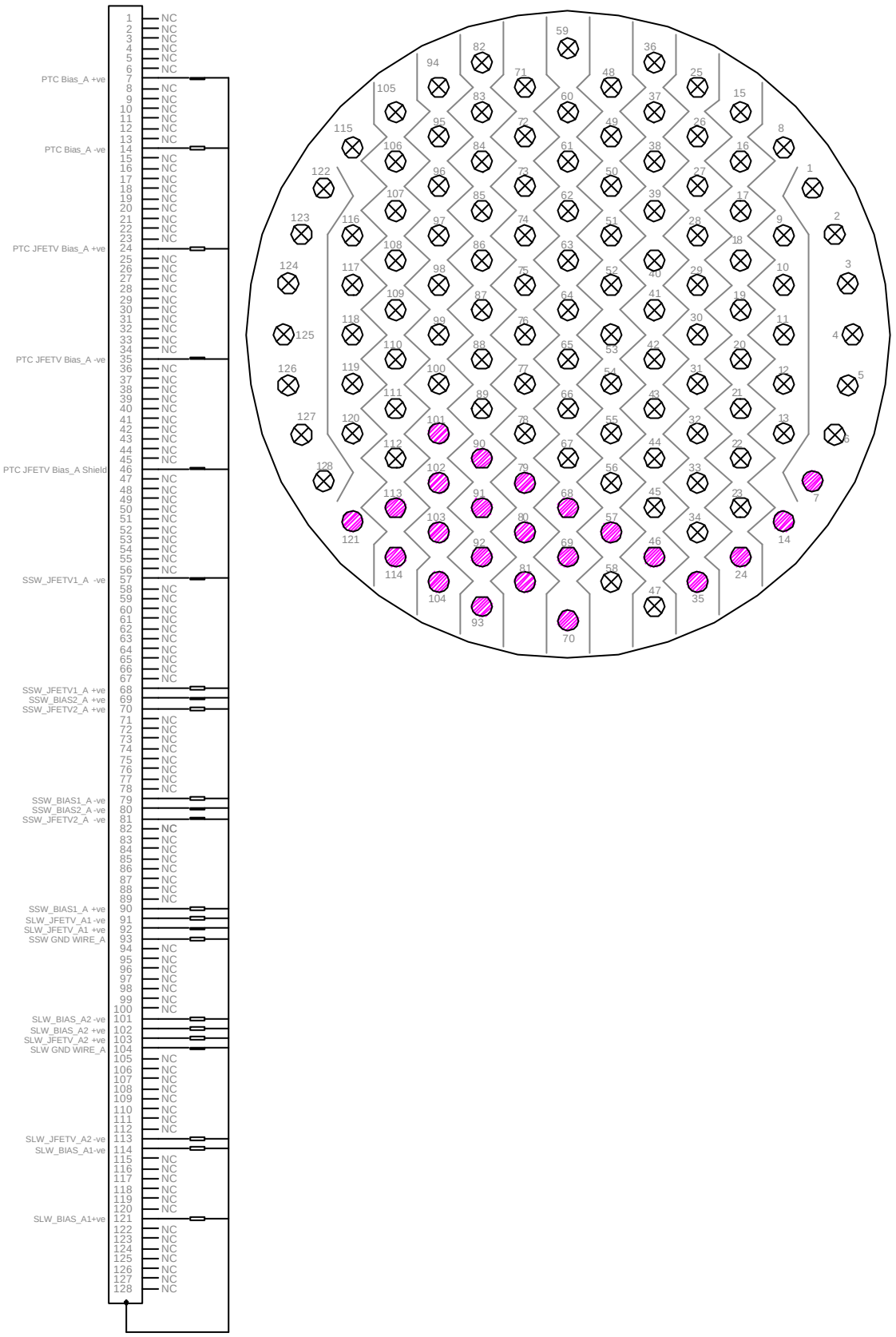
4. Specification of termination connectors

Name	Details
SPIRE Types I and II	 • Type-I used on JFET inputs JCC and JCC' • Type-II used on JFET bias input JDD and JDD' • SPIRE Provided

Name	Details
SPIRE Type-III	MDM 37S  • 37 x 1Meg Ohm resistors to chassis of connector • Mates with Phot JFET Backharness JFP J25, J26, J27 and J28. Four required. • Mates with Spect. JFET Backharness JFS J09 and J10 • SPIRE Provided
SPIRE Type -IV	MDM 51S  • 51 x 1Meg Ohm resistors to chassis of connector • Solder tab to connect backshell to chassis of FPU/Detector box approximately 400mm long • One required for photometer side of instrument. • One required for spectrometer side of instrument • SPIRE Provided

Name	Details
SPIRE Type-V	

- For cryoharness C3
- 41 x 1Meg Ohm resistors to chassis of connector
- ESA (Industry) Provided

Name	Details
SPIRE Type-VI	

- 128-Way termination plug for Spectrometer JFETs and BDAs
- 23 x 1Meg Ohm resistors to chassis of connector
- ESA (Industry) provided

Name	Details
SPIRE Type-VI	• ESA (Industry) provided • EMC Backshell providing a 360° electrically conductive barrier over the exposed contacts

5. Comments on the integration procedure

1	Integration of JFET modules into JFET racks	To be written 1
2	Integration of BDAs into FPU	To be written 2
3	Integration of JFET-BDA harnesses to BDAs	To be written
4	Integration of JFET-BDA harnesses to JFET racks	To be written
5	Integration of FPU and JFETs into cryostat	To be written
6	Integration of cryoharness to DRCU	To be written
7	De-integration of cryoharness to DRCU	To be written
8	De-integration of FPU and JFETs De-into cryostat	To be written
9	De-integration of JFET-BDA harnesses to JFET racks	To be written
10	De-integration of JFET-BDA harnesses to BDAs	To be written
11	De-integration of BDAs De-into FPU	To be written
12	De-integration of JFET modules De-into JFET racks	To be written