Doug Griffin - Tuesday, 06 April 2004

Attachments:

1. Jamie's email
2. Relationship between total cooler load and cooler temperature
3. Extract from SPIRE-JPL-NOT-000623 - Temperature Stability Requirements for SPIRE

Comments

- The total (internal parasitics + useful coolth) cooler load cannot be more than **approximately** [1] 30uW to achieve a hold time of 48 hours. A maximum of 10uW seems very high.
- From attachment Two, it can be seen that the first order linearised function of cold tip temperature vs. total cooler load at the operating point is **0.63mK/uW**
- Previous thermal analysis has shown that the maximum temperature drift of the 300-mK system without the PTC should be better than 0.125 mK/hour several hours after recycle.
- To minimise the load on the cooler due to I^2R heating on the PTC, the PTC can be set to control the temperature in a series of short stabilisation periods rather than over a single long period. In this scenario, the PTC would be set to control the 300-mK system for a period of (lets say three hours), after which the set point would be re-adjusted and the transients left to die out and the next three hour stabilisation period would commence.
    - From discussions with Lionel, it takes roughly 15 minutes for the temperature to stabilise to within a couple of percent of the steady state value after a step change in the gross heat load on the cooler[2].
    - The time constant of the BDAs is roughly 100 seconds.
- Three hours of stabilisation followed by would require a maximum of (3 hours x 0.125mK/hour / 0.63mK/uW = 0.59uW) I^2R dissipation. It would be prudent to double this, so that the set point is 50% of the total range; i.e. max dissipation of 1.19uW.
- The DAC currently implemented on the SCU is **12-bit**
- The PTC heater drive is configured as a current source and not a power source. Therefore, $V_{drive} = V_{max}$ x DAC value / $2^{\text{DAC bits}}$. This means that $P_{drive} = P_{max}$ x (DAC value / $2^{\text{DAC bits}}$)^2 . This means that the dP corresponding to one LSB is not linear. One LSB steps near the bottom of the ACD range produce a very small increment in power, while one LSB steps at the top of the ACD range yield a proportionately coarse step.
    - Table 1 gives the corresponding cold tip dissipation and temperature rise for various numbers of bits over and above 12-bits with 1.19uW maximum.

[1] This is dependant on the temperature of the evaporator at the end of the condensation phase of recycle. This temperature is a function of the strap design and the performance of the ^{2}He cryostat.
[2] Lionel also pointed out that the system is non-linear. It takes longer for the cooler to reach steady state with a small change in the total load than if it is an incremental change.

Table 1- Relation between current commanding precision and DAC output

bits	quanta	dQ 1 LSB		dT 1 LSB	
		Max	Min	Max	Min
12	4096	5.8E-4 uW	7.1E-8 uW	366.2 nK	0.0447 nK
13	8192	2.9E-4 uW	3.5E-8 uW	183.1 nK	0.0224 nK
14	16384	1.4E-4 uW	1.8E-8 uW	91.5 nK	0.0112 nK
15	32768	7.2E-5 uW	8.8E-9 uW	45.8 nK	0.0056 nK
16	65536	3.6E-5 uW	4.4E-9 uW	22.9 nK	0.0028 nK
17	131072	1.8E-5 uW	2.2E-9 uW	11.4 nK	0.0014 nK
18	262144	9.0E-6 uW	1.1E-9 uW	5.7 nK	0.0007 nK
19	524288	4.5E-6 uW	5.5E-10 uW	2.9 nK	0.0003 nK

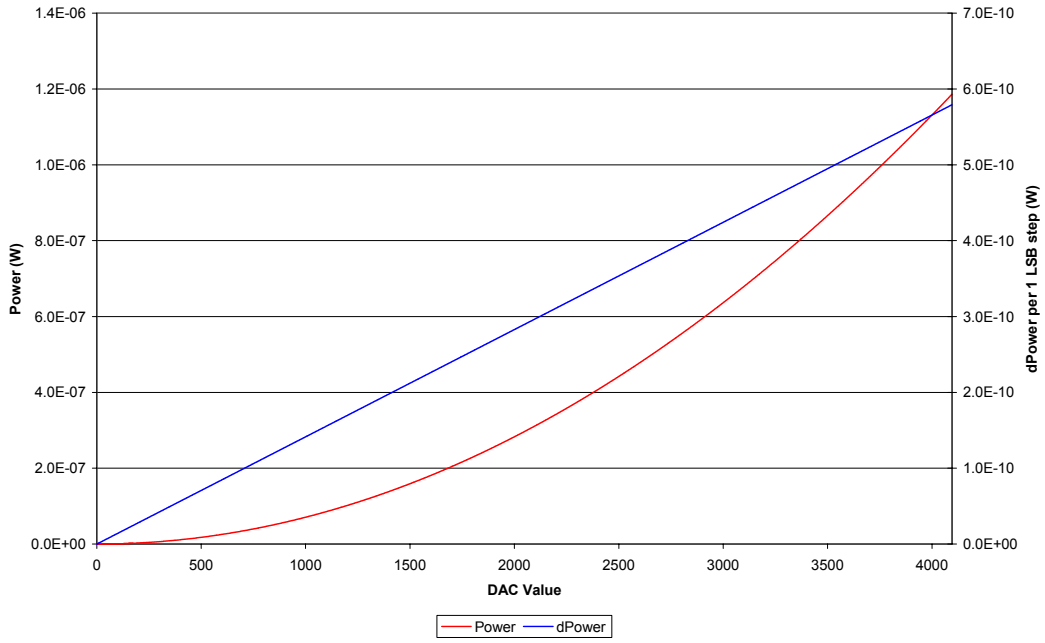

Figure 1 - Power and change in power corresponding to one LSB change vs. DAC value for a 12-bit DAC and 1.19uW maximum power.

- According to Jamie's email, the control precision is insufficient with a 12-bit ADC.
- There are two possible means by which the extra precision on the heat dissipated in the PTC can be achieved. They both involve using a duty cycle on the DAC setting for the PTC heater drive as indicated in Figure 2. This could be carried out in one of two ways;
  - Use the DPU to send commands to the DPU to switch between two ADC values. This would use the LSL and one of the Virtual Machines.
  - Use the FPGA in the SCU to switch between the two DAC settings.
- The DPU is capable of sending commands to the SCU using the Virtual Machine on the Low Speed Link with an estimated jitter of 0-5mS at a maximum frequency of around 10 commands/per second. The jitter on the implementation of the command would limit the number of extra bits of precision that could be achieved. The commanding speed would limit the temperature ripple induced by switching between the two DAC states.
  - If a cycle is taken to be 250mS long, then 5mS jitter represents about 5 or 6 extra bits of precision.

- If the FPGA was used, then presumably even more precision could be achieved (in terms of less jitter and faster switching and consequently less temperature ripple). The cost of this is the time and difficulty of re-programming the FPGA. Availability of system resources on the FPGA is also an unknown.
- If we are to embark on a procedure whereby the ADC is switched between two values to achieve extra precision on the PTC heater commanding, then I would opt for DPU commanding.

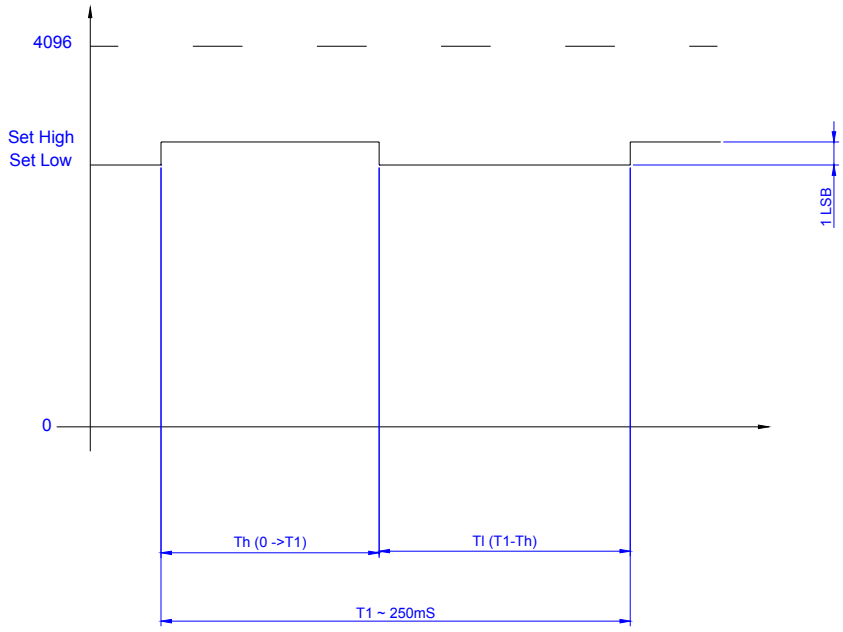

Figure 2 - Schematic for achieving greater than 12-bit precision on PTC heater commanding.

Attachment One: Jamie's email

From: Jamie Bock [jjb@astro.caltech.edu]
Sent: 13 March 2004 00:06
To: "Bruce Swinyard" <"Bruce Swinyard"
Cc: Matt Griffin; Doug Griffin; A.Goizel@rl.ac.uk; Viktor Hristov
Subject: TC heater control requirements

Hi Bruce,

I need to make the requirements on the temperature control heater drive. In order to do this I need to know:

1. What is the maximum power you want to build in? 10 uW seems reasonable to me, although it depends how quickly the cooler drifts while we are making observations, especially near the start where transients are settling down.
2. What is a reasonable control setting for quiescent operation? 2 uW? 3. An estimate as to how many mK rise we get at the control point per uW of input power.

Suppose we get 1 mK / uW with 10 uW max, with a resistor range of 0.5 to 1.5 MOhms. That means the heater circuit must supply 4 V max. If we control at 2 uW with a nominal 1 MOhm resistor, we get V = 1.4 V and a 2 mK temperature rise. Setting the LSB to 20 nK (half the nominal readout sensitivity of 40 nK/rtHz), we get a required accuracy of 7 uV. That is 4 / 7u = 19 bits and a nominal stability of 1.4 / 7u = 5 ppm.

I'm concerned that 19 bits is not going to go over very well. We could back off on the precision of course although the most demanding requirement, drift scanned observations using the entire focal plane, is 100 nK/rtHz at 10 mHz, where the BDA thermal filtering is not effective.

Jamie

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Attachment Two: Relationship between total cooler load and cooler temp.

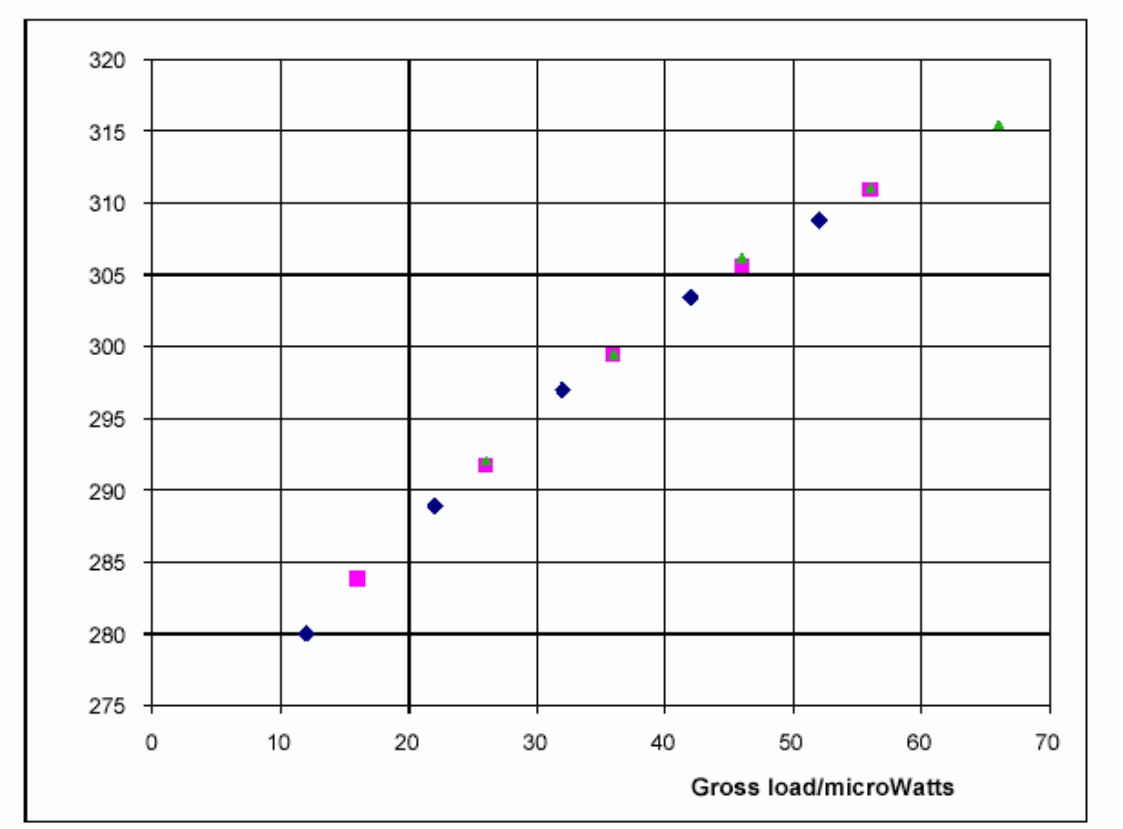

Figure 3 - To achieve a 48 hour hold time, the total load needs to be around 30uW (depending on the L0 temperature during recycle).

Attachment Three: Extract from SPIRE-JPL-NOT-000623

Mode	dT(^{3}He)/dt (mK/hr)	dT(BDA)/dt (mK/hr)	$T_{n,req}$ (nK/√Hz)	$\square_c$ (Hz)
Chopping	50	0.9	1200	1
Spectroscopy	9000	4.8	670	3
DS / point sources	3.9	0.06	1200	0.1
DS / extended emission	3e-3	5e-4	100	0.01