Setting up Vdd for the Flight JFETS
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Scope
This note sets out a procedure for setting the output voltage of the JFET V_{dd} supply for the flight DCU and JFETs.

Background
The requirement set on the DCU JFET power supply in the BDA SSSD (SPIRE-JPL-PRJ-000456 iss 3.2)

"BDA-DRCU-07 – V_{dd} shall be adjustable from 1.5 to 4 V"

This has been interpreted in the DCU as "shall be adjustable by design". That is, it is fixed by a resistor network and not changeable once the unit has been manufactured. This causes a problem in that, because the impedance of the cable is not well known, the voltage actually appearing at the JFET unit may not be the optimum for lowest noise and power dissipation.

It is proposed that the V_{dd} for the flight unit is set by fitting resistors on the power supply at a late stage in the build after the required output voltage has been specified for the actual flight JFET units. We therefore need to predict what the actual voltage at the DCU needs to be for the flight configuration in order to set the resistor values. It is proposed that a combination of tests at instrument and Herschel payload module level could be used to do this.

Measurements at Instrument Level
That there is a voltage drop was confirmed during the CQM test where a 200 mV drop was measured using the method outlined in this section.

The measurement set up used for the CQM PLW JFETs was as shown in figure 1. We take advantage of the fact that the prime and redundant sides of the DCU bias supplies are connected together at the cold end, as there are no redundant cold units, to make a four wire measurement using a high impedance DVM.

The procedure to check the voltage drop is then as follows:

Starts from fully integrated instrument in cryostat either warm or cold

1) Before starting check V_{dd} output value for this unit has been measured and recorded – refer to EIDP.
2) Connect prime side bias harness S1 and S3 into DCU J31 and J29
3) Connect redundant side S1 and S3 P32 and P30 into breakout box
4) Connect DVM across ground and V_{dd} for JFET unit to be tested – see HDD for details
5) Power on DCU
6) Record voltage for this JFET unit.
7) Power down DCU
8) Change DVM to next JFET unit – repeat for each unit to be checked.

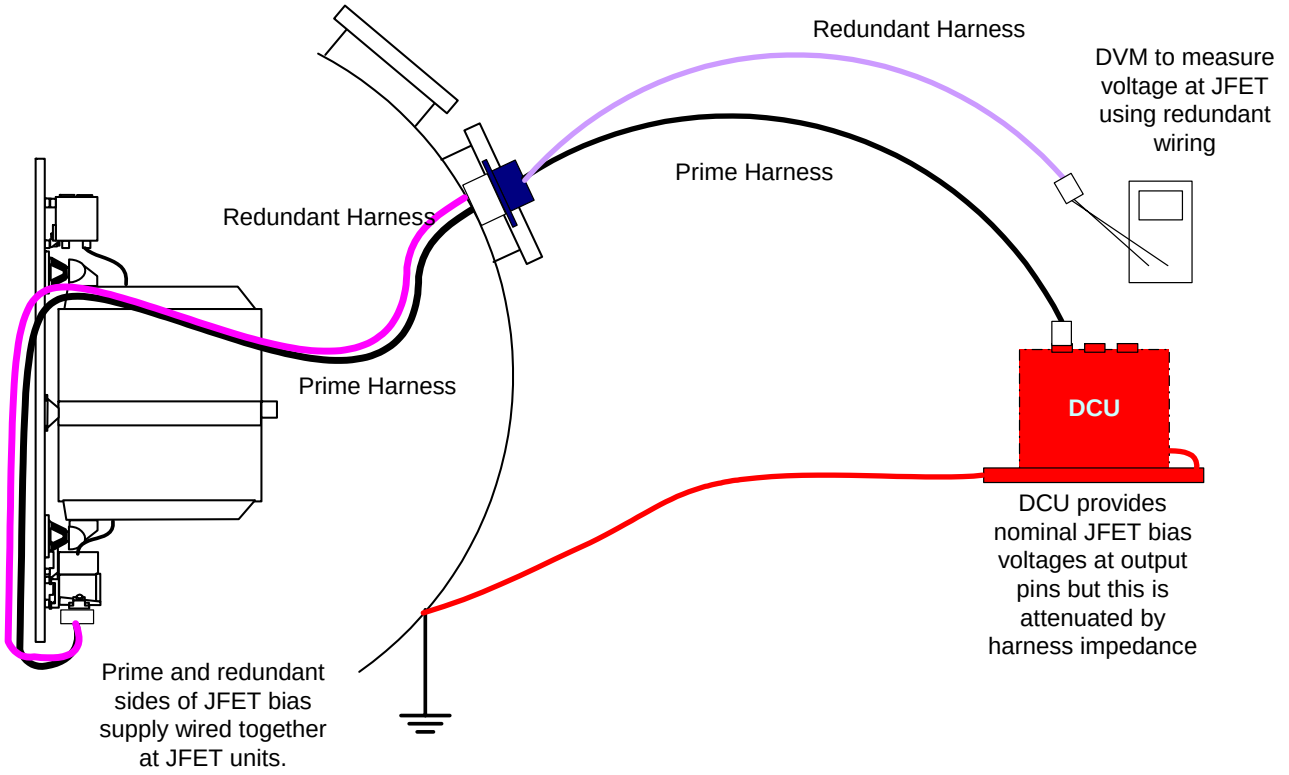

Figure 1: Test configuration used for measuring the voltage at the JFETs during instrument level tests.

We have now checked what the actual V_{dd} is for each JFET unit.

We now have two alternatives:

a) We can use the knowledge of the JFET units as tested at JPL to specify the optimum V_{dd}/V_{ss} combination and, knowing the voltage drop due to the harness, predict what the DCU output should be.

b) We could make measurements of the JFET noise as a function of V_{dd} and, by command, V_{ss} to see what the optimum voltage setting should be for power vs noise. This would have to be done either by using an external supply for V_{dd}, or using an external resistor network.

The only problem with option (b) is that it might take quite sometime to do this measurement. A further alternative would be to do just one or two units like this and use these to verify the measurements made at JPL.

All this testing can be done at RAL during the PFM test campaign using the QM2 DRCU to be delivered in the fourth quarter of 2004. We may be able to start the procedure on the spectrometer side using the QM1 DRCU. In either case, this will give us time to assess the results and propose the value of the resistors to be used in the FM electronics.

Measurements at Payload Module Level

Although the test cryoharness at RAL is designed to accurately simulate the flight harness (in particular with respect to the static impedance), the flight harness may have a different performance

especially when the external part of the harness is at its flight operating temperature. To check this we will request warm and cold impedance tests on the payload harness from Astrium and will compare these to the test conditions at RAL. Ultimately we could also request that we test the voltage drop down the Astrium harness during the EQM testing (albeit with a warm external section) using the redundant part of the harness in the same way as we do at instrument level.

The issue of the actual impedance we will see in flight remains – we can only predict this using a model plus the isothermal testing of the external harness. During the satellite thermal vacuum test we will have the harness at near its flight temperature and will be able to make noise measurements as a function of V_{ss}; this ought to confirm that the V_{dd} is set about right.