Herschel SPIRE

CEA/SAp June 2003 Status and Progress Report

DSM - DAPNIA
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Management & System

Meetings	
12/06	SPIRE PSU Kick off meeting
20/06	DRCU development plan meeting at RAL
26/06	CEA/CNRS/CNES meeting on Herschel development issues
27/06	Internal meeting SPIRE LTU progress meeting
Management act.	
Project control	➢ SPIRE QM1 master schedule update ➢ DCU EM QM1 detailed schedule update ➢ SPIRE FPU simulator detailed schedule update. ➢ SCU detailed schedule update ➢ Action list update. ➢ Documentation management ➢ SPIRE reporting.

Problem Areas	Remedial Actions
Change on the SPIRE development plan leading to a drastic descoping of the CQM functionality is no longer consistent with the DRCU development plan. In particular the validation of the DRCU QM1 design cannot be carried out as foreseen with the CQM model. Change in the DRCU development plan and especially of the DRCU model policy has to be accepted by the CEA and the CNES. Main points have been pointed out in a mail sent on May 28 by JLA to SPIRE Project (excerpt below): a) How to validate the DRCU design? b) When and by what means will CEA get the feedback to start the realisation of the next model. c) Which model will be the next? - 2nd QM1? - QM2: Do CEA still have the time to develop and qualify it before starting the FM development. - PFM: Who takes the risk and the responsibility? Who is paying in case major modifications are needed?	➢ A SPIRE project/CEA/CNRS/CNES meeting took place at RAL on June 20th. ➢ A CEA/CNRS/CNES meeting took place at CNES HQ on June 26th. ➢ A note presents 3 scenarios together with their respective schedules. Respective DRCU FM delivery dates are: - Near nominal: October 05 - Secured PFM: May 05 - PFM: Dec. 04 to Feb. 05 (depending on MCU availability) ➢ SPIRE Project/CEA/CNES telecom planned on July 4th. ➢ DRCU development scenarios will be presented at IHDR.
Availability of the MCU QM0 from LAM in question.	➢ The latest date for the MCU QM0 delivery from LAM to SAp is July 31st. If this date cannot be met, the MCU will not be integrated in the FCU QM1 box.
Concern about the current mechanical and thermal PSU-S/C I/F (base of the FCU box). Preliminary calculation show the current I/F (12 M4 feet) could not meet the dynamical requirement. Heat flow should have to be improved as well. Given the PSU STM development schedule, a decision is to be take at very short notice (PSU STM development is currently on hold).	➢ The current I/F was based on Alcatel agreement (based on static conditions). ➢ It is asked to Alcatel to check again the mechanical constraints. ➢ Possible improvements (if necessary): 1. Replacement of M4 by M5 (M5 was the CEA initial proposal which was rejected by Alcatel). Minor change. 2. Increasing of the number of feet. Major change. 3. Both (1 & 2). 4. The thermal aspect could likely be sorted out by the above mechanical improvement. In case it is not enough, a flat bottom could be added (estimated additional mass 500 g).

Project Milestones

Main Delivery Milestones	*Resp.*	*Baseline*	*Current*
DRCU QM1 delivery to RAL	SAp	09/2003	10/09/2003
FPU Simulator (version 1) delivery to RAL	SAp	09/2003	10/09/2003
DRCU QM2 delivery to RAL	SAp	05/01/2004	**(*)**
DRCU FM delivery to RAL	SAp	30/07/2004	**(*)**

(*) These dates depends on the chosen development scenario (see above "problem area" and the DRCU development scenario note for more details)

DRCU	
DCU EM / QM1	**Status**

- **DAQ IF**
  - 2 test boards available with test completed.
  - DAQ IF upgrade achieved (New xilinx & patch AMP02 replaced by OP400, then by OP484 as needed)
  - New patch fabrication on going.
- **BIAS**
  - Available, test performed
- **LIA-P**
  - LIA-P#1 & #2: Available, test performed
- **LIA-S**
  - LIA-S #1 & 2 : Available, test performed
  - LIA-S #3 : board fabrication, wiring in progress
- **Back-Planes**
  - Functional test backplane available.
  - Performance test backplane available
- **Test plan**
  - Test plans available: LIA-P, LIA-S, BIAS, DAQ-IF.
  - Functional test plan: available.
- **Integration & Test**
  - I/F DPU (FPGA) board validation achieved
  - DAQ-IF + LIA-P#1 + LIA-S#1 + back plane integrated in DCU box , functional & reduced performances test completed
  - First test DCU (DAQ-IF) ←→ LTU done (see AIV) and successful

Progress during the month

- LIA-S # 3 wiring in progress , need more time than scheduled
- DAQ-IF: new patch fabrication on going
- New FPGA to correct some bugs which appeared during the DCU-LTU test.

SCU

Status

- **Documentation**
  - Draft DPU/SCU ICD issued.
  - Test plan writing and data analysis finalisation
- **Test equipments**
  - Simplified test bench: available.
  - Test S/W finalised.
  - FSE development on going
- **DPU VHDL I/F**
  - Available
  - Logic updating without impact on the I/F
- **QM1**
  - Board CCHK + IF
    - board available, preliminary manual test successful,
    - Communication CCHKIF board ↔LTU tested
  - Board Temp + Heat
    - board available, preliminary manual test on analogic parts successful.
  - Back plane:
    - available
  - Test & Integration
    - Integration done
    - Test finalisation
    - Data analysis finalisation
    - Delivery to SAp scheduled 08/07

Progress during the month

- **Documentation**
  - Test plan writing and data analysis finalisation.
- **DPU VHDL I/F**
  - Logic updating without impact on the I/F
- **QM1**
  - Data analysis
  - Delivery to SAp scheduled 08/07

MCU

Status

- Software issue 3 implemented.
- QM0 available at LAM. Test done at SAp with LTU during 3 days: good results, BSM integration at LAM.
- MCU QM0 delivery to SAp scheduled 30/07
- QM2 and FM Sub-contractor selected.
- Delivery scheduled:
  QM1 11/2003
  QM2 05/2004
  FM 12/2004

Progress during the month

- QM0 test done at SAp with LTU during 3 days: good results.
- QM0 back to LAM for BSM integration
- Delivery to SAp scheduled 30/07

PSU	**Status** ➢ Specification available. ➢ Company selected and kick off meeting done on June 12, 2003-07-04 ➢ PSU model delivery dates are: - STM: Nov. 03 - EM: Jan. 04 - PFM: Sept. 04 **Progress during the month** ➢ Kick off meeting. ➢ See Problem area.
DRCU Boxes	**Status** ➢ DCU & FCU box thermal & dynamic studies achieved ➢ **DCU.** • STM: Thermal test performed. • QM1: available at SAp. I/F drawing started. • QM2 & FM: I/F available. ➢ **FCU.** • STM: detailed design achieved, fabrication finalisation • QM1: Available at SAp. I/F drawing updated • QM2 & FM: I/F available **Progress during the month** ➢ FCU STM fabrication on going, delivery scheduled mid-July

Test Equipments & others	
LTU #1	**Status** ➢ LTU SPIRE #1 available ➢ Software development on going ➢ LTU ←→ FPU simulator : good test results ➢ LTU ←→ DCU: first test conducted with DAC-IF board, good results ➢ LTU ←→ SCU CCHKIF board: first communication test conducted, good results ➢ LTU ←→ MCU first test, good results. ➢ Transport container fabrication started **Progress during the month** ➢ 3 Hermes boards received ➢ Software and Hermes boards debugging ➢ Rack I/F received after being updated ➢ LTU ←→ MCU test, good results. ➢ Transport container fabrication started
Power Bench	**Status** ➢ Available at SAp. ➢ Transport equipment fabrication started **Progress during the month** ➢ Delivery to SAp ➢ One bug solving ➢ Weight problem, 45kg instead of 20: transport equipment fabrication started
JPL Bolometer test facility	**Status** ➢ SAp people trained to the use of the JPL Bolometer test facility (including Bacus cryostat) ➢ Bacus Cryostat, mechanical parts, HKL connectors, Electronic & detectors available at SAp. ➢ Focal plane mounting on going **Progress during the month** ➢ Electronic & detectors received from JPL ➢ Focal plane mounting ➢ Electronic problems solving on going.
FPU Simulator #1	**Status** ➢ SPIRE FPU simulator delivered to SAp 26/02/2003 with user manual and log book

FPU Simulator #2	**Status** ➢ **PXI TRIG IO** • 2 units available and maintenance unit available. Test done ➢ **PXI Cernox** • PXI Cernox: test done, technical performances report writing ➢ Orders placed for the second simulator except PXI BOLO SPIRE ➢ VHDL program writing ➢ Supervision software updated taking into account the test results **Progress during the month** ➢ VHDL program writing ➢ Supervision software update taking into account the test results
Part procurement	**Status** ➢ **DCL**: edition 14 ➢ Harnesses connector estimation carried out. ➢ ATP update with Tecnologica **Progress during the month** ➢ Routine work ➢ Work on QM2 passive part procurement (self procured parts).
QM1 Harness	**Status** ➢ DCU-LTU-FPU simulator QM1: available. ➢ SCU harness fabrication on going ➢ MCU power bench harness fabrication on going **Progress during the month** ➢ SCU harness fabrication on going, delivery schedules beginning of July ➢ MCU power bench harness fabrication on going

AIV	**Status** ➢ **Plan** • DRCU development tree available (last version 30/11/2001) • DRCU AIV plan available. • DCU EM/QM1 test plan available (Configuration tests sequences LTU + FPU_sim + DCU QM1) ➢ **QM1 Test** • Test SCU CCHKIF board ↔LTU: good results • Test DCU DAQ-IF board ↔LTU: good results • Test MCU ↔ LTU: good results • Test DCU↔ LTU↔ FPU_sim: functional test on command & acknowledge parts • JPL cryostat handling (see section above) **Progress during the month** ➢ JPL cryostat handling (see section above) ➢ DCU-LTU-FPU_sim: functional test on command & acknowledge parts ➢ LTU bug solving ➢ Help on SCU test plan writing ➢ DCU test equipment preparation
FSE	**Status** ➢ Specification writing: 3 FSE will be built for DCU boards testing: respectively for DACQ/IF, BIAS & LIA boards. **Progress during the month** ➢ Specification writing for 3 FSEs on going
PA/QA	**Status** ➢ DML, DPL, DMPL available. ➢ Reference documentation list update on going ➢ ADP SPIRE , routine work ➢ Non conformity management ➢ Derating & Reliability SCU achieved ➢ Configuration control data base available **Progress during the month** ➢ Non conformity management ➢ Information research about PCB technologies (QM2 & FM) ➢ Contact with firms which are qualified to work in Spatial domain (QM2 & FM) ➢ Information research at CNES & ESA about harnesses ➢ Information research on MIL quality standards about wires. ➢ SPIRE synoptic test configuration writing ➢ Derating & Reliability DCU-BIAS & SCU achieved ➢ Data base creation to ensure configuration control

Milestones	Scheduled	Status
SPIRE FPU simulator #1 delivery to SAp	02/2003	Available
DCU test harness	04/2003	Available
DRCU QM1 harnesses need date	05/2003	Available
LTU DRCU available	04/2003	Available
Detector test cryostat delivery to SAp by JPL	04/2003	Available
MCU QM0 + simulator delivery to SAp	04/2003	**07/2003**
MCU QM1 delivery to RAL		**11/2003**
SCU QM1 delivery by SEDI	05/2002	**08/07/2003**
DRCU QM1 delivery to RAL	**12/05/2003**	**10/09/2003**
Warning: hereafter date correspond to the nominal DRCU development scenarion (see problem area)		
SPIRE FPU simulator #2	*02/2004*	*On schedule*
SCU QM2 delivery to SAp	*05/2004*	*On schedule*
MCU QM2 delivery to SAp	*05/2004*	*On schedule*
DRCU QM2 delivery to RAL	***09/2004***	*On schedule*
MCU FM delivery to SAp	*12/2004*	*On schedule*
SCU FM delivery to SAp	*12/2004*	*On schedule*
PSU delivery to SAp	*09/2004*	*On schedule*
DRCU FM ready for delivery to RAL	***02/2005***	*On schedule*

Documentation progress this month		
Title	**Reference**	**Progress / issue**
Procédure vibrations HSDCU & BOLC STM	SAp-PACS-TT-0162-03	1.0
PV essais VTC DCU STM	SAp-SPIRE-TT-0113-03	1.0
Up screening and lot acceptance test specification for UCC1802 Texas Instrument	BCE1054	1.0
SPIRE QM1 MCU T2	SAp-SPIRE-LD-0115-03	0.2
SPIRE-QM1 SCU T2	SAp-SPIRE-LD-0114-03	0.3
SPIRE & PACS Sorption coolers ICD	HSO-SBT-ICD-012	1.4

Documentation List		
Title	**Reference**	**Version, date**
Reference documentation (documents not coming from SAp, SIS, SEDI…)		
➢ SPIRE Instrument Development Plan IIDR	SPIRE-RAL-PRJ-000035	1.1 draft 12/04/2001
➢ SPIRE Major Milestone List issue 1.3 IIDR	SPIRE-RAL-PRJ-0000455	1.3 31/01/2002
➢ SPIRE Instrument Requirements	SPIRE-RAL-PRJ-000034	1.1 10/01/2002
➢ ICD cooler	HSO-SBT-ICD-012	1.3 07/12/2001
➢ Instrument Interface Document part A	SCI-PT-IIDA-04624	3.0 01/07/2002
➢ Instrument Interface Document part B SPIRE	SCI-PT-IIDB/SPIRE-02124	2.0 31/07/2001
➢ SPIRE Data ICD	SPIRE-RAL-DOC-001078	1.0 draft1 15/01/2002
➢ SPIRE instrument AIV plan	SPIRE-RAL-PRJ-000410	2.1 29/03/2001
➢ SPIRE harness definition	SPIRE-RAL-PRJ-000608	1.1 05/03/2003
➢ Herschel frequency plan	H-P-1-ASPI-PL-0201	1.0 03/05/2002
➢ Radiation requirements	H-P-1-ASPI-SP-0017	1.0 11/06/2001
➢ EMC specification	H-P-1-ASPI-SP-0037	3.0 14/06/2002
➢ Random environment analyses	H-P-2-ASPI-AN-0112	2.0 15/03/2002
➢ Cleanliness requirements specifications	H-P-1-ASPI-SP-0035	2.0 28/06/2002
➢ Herschel general design and interface requirements	H-P-1-ASPI-SP-0027	3.2 15/02/2002
➢ PA requirements for FIRST scientific instruments	PT-RQ-04410	2.0 01/08/2000
➢ Filters - subsystem specification document	SPIRE-QMW-PRJ-000454	2.0 07/09/2001
➢ SPIRE CQM performance test specification	SPIRE-RAL-DOC-001123	0.4 29/05/2002
➢ DPU ICD	SPIRE-IFS-PRJ-000650	1.0 02/04/2001
➢ Calibrator SSSD : SCAL	HSO-CDF-SP-001	1.0 10/09/2001
➢ Calibrator SSSD : PCAL	HSO-CDF-SP-003	1.0 11/09/2001
➢ Environment & tests requirements	H-P-1-ASPI-SP-0030	3.2 18/02/2002
➢ SPIRE instrument AIV plan	SPIRE-RAL-PRJ-000410	2.1 29/03/2001
➢ SPIRE harness definition	SPIRE-RAL-PRJ-000608	1.0 08/07/2002
➢ SPIRE grounding and screening philosophy	SPIRE-RAL-PRJ-00624	1.0 01/10/2002
➢ Note on SPIRE Models Philosophy	None, Bruce Swinyard	1.0 12/07/2000
➢ SPIRE configuration management plan	SPIRE-RAL-PRJ-000626	1.3 28/01/2002
➢ SPIRE product assurance plan	SPIRE-RAL-PRJ-000017	1.1 14/05/2003
➢ DPU ICD	SPIRE-IFS-PRJ-000650	1.4 24/03/2003

Management			
➢ Management plan for the Herschel project.	SAp-FIRST-JLA-0038-01	4.0	23/01/2003
➢ Actions list	SAp-FIRST-DR-0050-01		
➢ DRCU & WIH Development Plan	SAp-SPIRE-JLA-0047-01	4.0	29/01/2003
➢ SPIRE development tree	H0030		30/11/2001
➢ SPIRE product tree	SAp-SPIRE-DR-0094-03	1.0	21/01/2003
➢ WBS Herschel	SAp-FIRST-DR-0043-01	2.1	
➢ WBS SPIRE	SAP-FIRST-DR-0045-01	2.1	
➢ DRCU QM1 master schedule	SAp-SPIRE-DR-0105-03	1.9	26/06/2003
➢ More documentation on the SAp intranet website			
DRCU			
➢ DRCU Specifications document	SAp-SPIRE-Cca-0025-00	1.0	14/02/2003
➢ DRCU Development Tree	H0030		30/11/2001
➢ DRCU ICD	SAp-SPIRE-Cca-0075-02	1.0	14/02/2003
➢ DRCU DPU ICD	SAp-SPIRE-Cca-0076-02	1.0	14/02/2003
➢ DCU design document	SAp-SPIRE-FP-0063-02	0.3	18/02/2003
➢ Test plan DAQ IF	SAp-SPIRE-FP-0067-02	0.1	18/02/2003
➢ Test plan BIAS	SAp-SPIRE-FP-0066-02	0.1	18/02/2003
➢ Test plan LIA P	SAp-SPIRE-FP-0064-02	0.1	18/02/2003
➢ Test plan LIA S	SAp-SPIRE-FP-0065-02	0.1	18/02/2003
➢ SPIRE test configuration,	SAp-SPIRE-LD-0015-01	3.0	08/2001
➢ FPU simulator specifications for DCU / SCU test	SIG-SPIRE-PdA-0030-01	3.0	14/02/2003
➢ SPIRE LTU specifications	SAp-SPIRE-FD-0071-02	1.0	22/04/2002
➢ DRCU AIV Plan	SAp-SPIRE-HT-0082-02	1.3	05/11/2002
➢ DCU EM QM1 Preliminary test plan	SAp-SPIRE-HT-0088-02	1.0	14/02/2003
➢ SCU design document	SEDI-SCU-MM-2002-1	0.7	17/02/2003
➢ PSU SPIRE specification	SAp-SPIRE-DS-012-02	1.1	11/12/2002
➢ More documentation on the SAp intranet website			
QA			
➢ Standard product assurance plan	SAp-GERES-Flo-436-00	1.0	09/11/2000
➢ SPIRE liste des documents à produire	SAp-SPIRE-Flo-0028-00	0.2	15/12/2000
➢ Organisation de la gestion documentaire sur Herschel au SAp	SAp-FIRST-DR-0053-01	1.1	06/12/2001
➢ Gestion des documents sur la base Herschel	SAp-FIRST-DR-0072-02	1.3	15/04/2002
➢ Procédures de contrôle projet sur Herschel	SAp-FIRST-DR-0125-02	1.4	05/09/2002
➢ DRCU processor board PA specification	SAp-SPIRE-Flo-0020-00		10/01/2001
➢ Plan d'action de AP du projet Herschel	SAp-FIRST-Abx-0137-02	1.1	18/06/2002
➢ Evaluation report for test plan of DCU boards	SAp-SPIRE-JF-0079-02	1.0	
➢ DRCU architecture and reliability analysis report	SAp-SPIRE-Flo-0039-01		21/08/2001
➢ DRCU FMEA reliability	SAp-SPIRE-JF-0099-03	0.1	10/02/2003
➢ DRCU preliminary DMPL	SAp-SPIRE-NC-0100-03	1.0	11/02/2003
➢ DRCU preliminary DPL	SAp-SPIRE-NC-0061-02	1.0	13/02/2003
➢ DRCU DML	SAp-SPIRE-NC-0060-02	1.1	24/03/2003
➢ More documentation on the SAp intranet website			