



CEA/SAp
May 2003
Status and Progress Report

SAp-FIRST-DR-0314-03
 H0739
 28/05/2003
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Management & System	
Meetings	
06/05	Internal meeting with SCU team: progress meeting
07/05	SAP – SPIRE Project Telecon
16/05	Internal meeting with SCU team manager: actions plan to ensure the QM model delivery in June
28/05	SAP – SPIRE Project Telecon
Management act.	
Project control	<ul style="list-style-type: none"> ➤ SPIRE QM1 master schedule update ➤ DCU EM QM1 detailed schedule update ➤ SPIRE FPU simulator detailed schedule update. ➤ SCU detailed schedule update ➤ Action list update. ➤ Documentation management ➤ SPIRE reporting.

Problem Areas	Remedial Actions
Test Bolometer and driving/readout electronics still missing for DCU cold testing. On the critical path.	<ul style="list-style-type: none"> ➤ In principle the shipment from JPL should take place week 23 and awaited at SAP week 24. ➤ Consequence on the QM1 delivery dates to be assessed
Change on the SPIRE development plan leading to a drastic descoping of the CQM functionality is no longer consistent with the DRCU development plan. In particular the validation of the DRCU QM1 design cannot be carried out as foreseen with the CQM model. Change in the DRCU development plan and especially of the DRCU model policy has to be accepted by the CEA and the CNES. Main points have been pointed out in a mail sent on May 28 by JLA to SPIRE Project (excerpt below): a) How to validate the DRCU design? b) When and by what means will CEA get the feedback to start the realisation of the next model. c) Which model will be the next? - 2nd QM1? - QM2: Do CEA still have the time to develop and qualify it before starting the FM development. - PFM: Who takes the risk and the responsibility? Who is paying in case major modification are needed?	<ul style="list-style-type: none"> ➤ A meeting is to be arranged between SPIRE Project, CEA and CNES to discuss this issue to take the relevant decisions.

Project Milestones			
<i>Main Delivery Milestones</i>	<i>Resp.</i>	<i>Baseline</i>	<i>Current</i>
DRCU QM1 delivery to RAL	SAp	12/05/2003	08/08/2003 (*)
FPU Simulator (version 1) delivery to RAL	SAp	12/05/2003	08/08/2003
DRCU QM2 delivery to RAL	SAp	05/01/2004	07/04
DRCU FM delivery to RAL	SAp	30/07/2004	12/04 (**)

(*) : Likely postponed due to the late availability of the JPL test means.

(**) : Earliest date.

DRCU	
DCU EM / QM1	<p>Status</p> <ul style="list-style-type: none"> ➤ DAQ IF <ul style="list-style-type: none"> • 2 test boards available with test completed. • DAQ IF upgrade achieved (New xilinx & patch AMP02 replaced by OP400, then by OP484 as needed) • New patch fabrication on going. ➤ BIAS <ul style="list-style-type: none"> • Available, test performed ➤ LIA-P <ul style="list-style-type: none"> • LIA-P#1: Available, test performed • LIA-P #2: Available, test performed ➤ LIA-S <ul style="list-style-type: none"> • LIA-S #1: Available, test performed • LIA-S #2: Available • LIA-S #3 : board fabrication, wiring in progress ➤ Back-Planes <ul style="list-style-type: none"> • Functional test backplane available. • Performance test backplane available ➤ Test plan <ul style="list-style-type: none"> • Test plans available: LIA-P, LIA-S, BIAS, DAQ-IF. • Functional test plan: available. ➤ Integration & Test <ul style="list-style-type: none"> • I/F DPU (FPGA) board validation achieved • DAQ-IF tested on 1 channel, good results • LIA-P#1 & LIA-S#1 connected and tested with LTU. • DAQ-IF + LIA-P#1 + LIA-S#1 + back plane integrated in DCU box , functional & reduced performances test completed • First test DCU (DAQ-IF) ↔ LTU started (see AIV) and successful
	<p>Progress during the month</p> <ul style="list-style-type: none"> ➤ LIA-S # 2 delivered to SAp ➤ LIA-S # 3 wiring in progress ➤ DAQ-IF: new patch fabrication ➤ LIA-P #2 test post fabrication performed ➤ DCU (DAQ-IF) ↔ LTU test: successful

SCU	Status
	<ul style="list-style-type: none"> ➤ Documentation <ul style="list-style-type: none"> • Draft Specification and preliminary (H/W & VHDL) design available. • Draft DPU/SCU ICD issued. • Test plan writing in progress ➤ Test equipments <ul style="list-style-type: none"> • Simplified test bench: available. • Test S/W finalised. • FSE development on going ➤ DPU VHDL I/F <ul style="list-style-type: none"> • Available but not yet integrated ➤ QM1 <ul style="list-style-type: none"> • Board CCHK + IF <ul style="list-style-type: none"> - board available, preliminary manual test successful, - Communication CCHKIF board ↔LTU tested • Board Temp + Heat <ul style="list-style-type: none"> - board available, preliminary manual test on analogic parts successful. • Back plane: <ul style="list-style-type: none"> - available • Test & Integration <ul style="list-style-type: none"> -not started ➤ QM2 <ul style="list-style-type: none"> •
	Progress during the month
	<ul style="list-style-type: none"> ➤ Documentation <ul style="list-style-type: none"> • None ➤ Test equipments <ul style="list-style-type: none"> • Simplified test bench: finalisation ➤ DPU VHDL I/F <ul style="list-style-type: none"> • None ➤ QM1 <ul style="list-style-type: none"> • Communication test CCHKIF board ↔LTU: good results ➤ QM2 <ul style="list-style-type: none"> • None

MCU	Status	
	<ul style="list-style-type: none"> ➤ Design available at LAM & SAp ➤ Software issue 3 implemented ➤ QM0 available and under test. ➤ QM2 and FM Sub-contractor selected. <p>MCU Deliveries from LAM to CEA: QM0 (LAM): End of June 2003 QM1 (SAp): June 2003 QM2: 01/04 (2 months behind schedule at least) PFM: 07/04</p>	
	Progress during the month	
	<ul style="list-style-type: none"> ➤ QM0 test in progress 	
PSU	Status	
	<ul style="list-style-type: none"> ➤ Specification available. ➤ Company selected. 	
	Progress during the month	
	<ul style="list-style-type: none"> ➤ Call for tender report writing ➤ Kick off meeting scheduled beginning of June 	
DRCU Boxes	Status	
	<ul style="list-style-type: none"> ➤ DCU & FCU box thermal & dynamic studies achieved ➤ DCU. <ul style="list-style-type: none"> • <u>STM</u>: box available at SAp. Board front panel & Rack available. Thermal test performed. • <u>QM1</u>: available at SAp. I/F drawing started. • <u>QM2 & FM</u>: I/F available. ➤ FCU. <ul style="list-style-type: none"> • <u>STM</u>: detailed design achieved, fabrication on going • <u>QM1</u>: Available at SAp. I/F drawing updated • <u>QM2 & FM</u>: I/F available 	
	Progress during the month	
	<ul style="list-style-type: none"> ➤ FCU QM1 drawings updated. ➤ FCU STM fabrication on going ➤ DCU STM thermal test performed 	

Test Equipments & others	
LTU #1	Status <ul style="list-style-type: none"> ➤ LTU SPIRE #1 available ➤ Software development: first version available ➤ LTU ↔ FPU simulator : good test results ➤ LTU ↔ DCU: first test conducted with DAC-IF board, good results ➤ LTU ↔ SCU CCHKIF board: first communication test conducted, good results
	Progress during the month
	<ul style="list-style-type: none"> ➤ First communication test LTU ↔ SCU CCHKIF board: success, ➤ Software debugging ➤ Problems solving: a couple of Hermes Boards were sent back to manufacturer
Power Bench	Status <ul style="list-style-type: none"> ➤ Specification available. ➤ Development at sub-contractor on going
	Progress during the month
	<ul style="list-style-type: none"> ➤ Delivery scheduled beginning of June
JPL Bolometer test facility	Status <ul style="list-style-type: none"> ➤ SAp people trained to the use of the JPL Bolometer test facility (including Bacus cryostat) ➤ Bacus Cryostat received at SAp. ➤ Mechanical parts and HKL connectors available
	Progress during the month
	<ul style="list-style-type: none"> ➤ None: waiting for detectors & electronics to perform full testing.
FPU Simulator #1	Status <ul style="list-style-type: none"> ➤ SPIRE FPU simulator delivered to SAp 26/02/2003 with user manual and log book
FPU Simulator #2	Status <ul style="list-style-type: none"> ➤ PXI TRIG IO <ul style="list-style-type: none"> • 2 units available and maintenance unit available. Test done ➤ PXI Cernox <ul style="list-style-type: none"> • PXI Cernox: test done, technical performances report writing ➤ Orders placed for the second simulator except PXI BOLO SPIRE
	Progress during the month
	<ul style="list-style-type: none"> ➤ None (vacation)

Part procurement	Status
	<ul style="list-style-type: none"> ➤ DCL: edition 14 ➤ Harnesses connector estimation carried out. ➤ ATP update with Tecnologica
	Progress during the month
	<ul style="list-style-type: none"> ➤ Routine work ➤ Work on QM2 passive part procurement (self procured parts).
Harness	Status
	<ul style="list-style-type: none"> ➤ Test harness DCU-LTU-FPU simulator QM1 : available.
	Progress during the month
	<ul style="list-style-type: none"> ➤ Test harness DCU-LTU-FPU_simulator delivered to SAp
Containers	Status
	<ul style="list-style-type: none"> ➤ Specification available.
	Progress during the month
	None
AIV	Status
	<ul style="list-style-type: none"> ➤ Plan <ul style="list-style-type: none"> • DRCU development tree available (last version 30/11/2001) • DRCU AIV plan available. • DCU EM/QM1 test plan available (Configuration tests sequences LTU + FPU_sim + DCU QM1) ➤ QM1 Test <ul style="list-style-type: none"> • Test SCU CCHKIF board ↔LTU: good results • Test DCU DAQ-IF board ↔LTU: good results • Test on the LTU Scientific data channel : good results
	Progress during the month
	<ul style="list-style-type: none"> ➤ Configuration tests sequences writing (LTU + FPU_sim + DCU QM1) achievement ➤ Communication test SCU CCHKIF board ↔LTU: good results ➤ Communication test DCU DAQ-IF board ↔LTU: good results ➤ Test on the LTU Scientific data channel, good results
FSE	Status
	<ul style="list-style-type: none"> ➤ Specification writing: 3 FSE will be built for DCU boards testing: respectively for DACQ/IF, BIAS & LIA boards.
	Progress during the month
	<ul style="list-style-type: none"> ➤ Specification writing for 3 FSEs on going

PA/QA	Status	
	<ul style="list-style-type: none"> ➤ DML, DPL, DMPL available. ➤ Reference documentation list update on going ➤ ADP SPIRE , routine work ➤ Non conformity management ➤ Derating & Reliability SCU achieved ➤ Configuration control data base available 	
	Progress during the month	
	<ul style="list-style-type: none"> ➤ Non conformity management ➤ Information research about PCB technologies (QM2 & FM) ➤ Contact with firms which are qualified to work in Spatial domain (QM2 & FM) ➤ Information research at CNES & ESA about harnesses ➤ Information research on MIL quality standards about wires. ➤ SPIRE synoptic test configuration writing ➤ Derating & Reliability DCU-BIAS & SCU achieved ➤ Data base creation to ensure configuration control 	

Milestones		Status
SPIRE FPU simulator #1 delivery to SAp	26/02/2003	Available
DCU test harness	04/2003	Available
DRCU QM1 harnesses need date	05/2003	Available
LTU DRCU available	04/2003	Available
Detector test cryostat delivery to SAp by JPL	04/2003	Available, wait for bolometers
MCU QM1 + simulator delivery to SAp	04/2003	06/2003
SCU QM1 delivery by SEDI	05/2002	06/2003
DRCU QM1 delivery to RAL	12/05/2003	08/08/2003 if JPL bolometers received in time.
SPIRE FPU simulator #2	10/2003	On schedule
SCU QM2 need date	11/2003	On schedule
MCU QM2 delivery to SAp need date	09/2003	11/03
DRCU QM2 delivery to RAL	05/01/2004	07/04
MCU FM delivery to SAp need date	30/04/2004	On schedule
SCU FM need date	30/04/2004	06/04
PSU delivery		10/04
DRCU FM ready for delivery to RAL	30/07/2004	12/04

Documentation progress this month		
Title	Reference	Progress
Note: description des modifications pour mise à niveau des cartes DCU-QM1	SAp-SPIRE-JF-0111-03	0.1
Power supply, analyse des réponses à l'appel d'offre	SAp-PACS-JF-0129-03	0.1
SPIRE configuration management plan	SPIRE-RAL-PRJ-000626	1.3
SPIRE product assurance plan	SPIRE-RAL-PRJ-000017	1.1
DPU ICD	SPIRE-IFS-PRJ-000650	1.4
DCU QM1 plan de test en configuration LTU-DCU-FPU sim	SAp-SPIRE-HT-0112-03	1.0

Documentation List			
Title	Reference	Version, date	
Reference documentation (documents not coming from SAp, SIS, SEDI...)			
➤ SPIRE Instrument Development Plan IIDR	SPIRE-RAL-PRJ-000035	1.1 draft	12/04/2001
➤ SPIRE Major Milestone List issue 1.3 IIDR	SPIRE-RAL-PRJ-0000455	1.3	31/01/2002
➤ SPIRE Instrument Requirements	SPIRE-RAL-PRJ-000034	1.1	10/01/2002
➤ ICD cooler	HSO-SBT-ICD-012	1.3	07/12/2001
➤ Instrument Interface Document part A	SCI-PT-IIDA-04624	3.0	01/07/2002
➤ Instrument Interface Document part B SPIRE	SCI-PT-IIDB/SPIRE-02124	2.0	31/07/2001
➤ SPIRE Data ICD	SPIRE-RAL-DOC-001078	1.0 draft1	15/01/2002
➤ SPIRE instrument AIV plan	SPIRE-RAL-PRJ-000410	2.1	29/03/2001
➤ SPIRE harness definition	SPIRE-RAL-PRJ-000608	1.1	05/03/2003
➤ Herschel frequency plan	H-P-1-ASPI-PL-0201	1.0	03/05/2002
➤ Radiation requirements	H-P-1-ASPI-SP-0017	1.0	11/06/2001
➤ EMC specification	H-P-1-ASPI-SP-0037	3.0	14/06/2002
➤ Random environment analyses	H-P-2-ASPI-AN-0112	2.0	15/03/2002
➤ Cleanliness requirements specifications	H-P-1-ASPI-SP-0035	2.0	28/06/2002
➤ Herschel general design and interface requirements	H-P-1-ASPI-SP-0027	3.2	15/02/2002
➤ PA requirements for FIRST scientific instruments	PT-RQ-04410	2.0	01/08/2000
➤ Filters - subsystem specification document	SPIRE-QMW-PRJ-000454	2.0	07/09/2001
➤ SPIRE CQM performance test specification	SPIRE-RAL-DOC-001123	0.4	29/05/2002
➤ DPU ICD	SPIRE-IFS-PRJ-000650	1.0	02/04/2001
➤ Calibrator SSSD : SCAL	HSO-CDF-SP-001	1.0	10/09/2001
➤ Calibrator SSSD : PCAL	HSO-CDF-SP-003	1.0	11/09/2001
➤ Environment & tests requirements	H-P-1-ASPI-SP-0030	3.2	18/02/2002
➤ SPIRE instrument AIV plan	SPIRE-RAL-PRJ-000410	2.1	29/03/2001
➤ SPIRE harness definition	SPIRE-RAL-PRJ-000608	1.0	08/07/2002
➤ SPIRE grounding and screening philosophy	SPIRE-RAL-PRJ-00624	1.0	01/10/2002
➤ Note on SPIRE Models Philosophy	None, Bruce Swinyard	1.0	12/07/2000
➤ SPIRE configuration management plan	SPIRE-RAL-PRJ-000626	1.3	28/01/2002
➤ SPIRE product assurance plan	SPIRE-RAL-PRJ-000017	1.1	14/05/2003
➤ DPU ICD	SPIRE-IFS-PRJ-000650	1.4	24/03/2003

Management				
➤	Management plan for the Herschel project.	SAp-FIRST-JLA-0038-01	4.0	23/01/2003
➤	Actions list	SAp-FIRST-DR-0050-01		
➤	DRCU & WIH Development Plan	SAp-SPIRE-JLA-0047-01	4.0	29/01/2003
➤	SPIRE development tree	H0030		30/11/2001
➤	SPIRE product tree	SAp-SPIRE-DR-0094-03	1.0	21/01/2003
➤	WBS Herschel	SAp-FIRST-DR-0043-01	2.1	
➤	WBS SPIRE	SAp-FIRST-DR-0045-01	2.1	
➤	DRCU QM1 master schedule	SAp-SPIRE-DR-0105-03	1.5	28/05/2003
➤	DCU EM QM1 at JPL detailed schedule	SAp-FIRST-DR-0050-01	6.2	28/05/2003
➤	SCU QM1 detailed schedule	SEI-SPIRE-MM-0049-01	16.0	28/05/2003
➤	More documentation on the SAp intranet website			
DRCU				
➤	DRCU Specifications document	SAp-SPIRE-Cca-0025-00	1.0	14/02/2003
➤	DRCU Development Tree	H0030		30/11/2001
➤	DRCU ICD	SAp-SPIRE-Cca-0075-02	1.0	14/02/2003
➤	DRCU DPU ICD	SAp-SPIRE-Cca-0076-02	1.0	14/02/2003
➤	DCU design document	SAp-SPIRE-FP-0063-02	0.3	18/02/2003
➤	Test plan DAQ IF	SAp-SPIRE-FP-0067-02	0.1	18/02/2003
➤	Test plan BIAS	SAp-SPIRE-FP-0066-02	0.1	18/02/2003
➤	Test plan LIA P	SAp-SPIRE-FP-0064-02	0.1	18/02/2003
➤	Test plan LIA S	SAp-SPIRE-FP-0065-02	0.1	18/02/2003
➤	SPIRE test configuration,	SAp-SPIRE-LD-0015-01	3.0	08/2001
➤	FPU simulator specifications for DCU / SCU test	SIG-SPIRE-PdA-0030-01	3.0	14/02/2003
➤	SPIRE LTU specifications	SAp-SPIRE-FD-0071-02	1.0	22/04/2002
➤	DRCU AIV Plan	SAp-SPIRE-HT-0082-02	1.3	05/11/2002
➤	DCU EM QM1 Preliminary test plan	SAp-SPIRE-HT-0088-02	1.0	14/02/2003
➤	SCU design document	SEDI-SCU-MM-2002-1	0.7	17/02/2003
➤	PSU SPIRE specification	SAp-SPIRE-DS-012-02	1.1	11/12/2002
➤	More documentation on the SAp intranet website			
QA				
➤	Standard product assurance plan	SAp-GERES-Flo-436-00	1.0	09/11/2000
➤	SPIRE liste des documents à produire	SAp-SPIRE-Flo-0028-00	0.2	15/12/2000
➤	Organisation de la gestion documentaire sur Herschel au SAp	SAp-FIRST-DR-0053-01	1.1	06/12/2001
➤	Gestion des documents sur la base Herschel	SAp-FIRST-DR-0072-02	1.3	15/04/2002
➤	Procédures de contrôle projet sur Herschel	SAp-FIRST-DR-0125-02	1.4	05/09/2002
➤	DRCU processor board PA specification	SAp-SPIRE-Flo-0020-00		10/01/2001
➤	Plan d'action de AP du projet Herschel	SAp-FIRST-Abx-0137-02	1.1	18/06/2002
➤	Evaluation report for test plan of DCU boards	SAp-SPIRE-JF-0079-02	1.0	
➤	DRCU architecture and reliability analysis report	SAp-SPIRE-Flo-0039-01		21/08/2001
➤	DRCU FMEA reliability	SAp-SPIRE-JF-0099-03	0.1	10/02/2003
➤	DRCU preliminary DMPL	SAp-SPIRE-NC-0100-03	1.0	11/02/2003
➤	DRCU preliminary DPL	SAp-SPIRE-NC-0061-02	1.0	13/02/2003
➤	DRCU DML	SAp-SPIRE-NC-0060-02	1.1	24/03/2003
➤	More documentation on the SAp intranet website			