CEA/SAp
April 2003
Status and Progress Report

Management & System	
Meetings	
01/04	Internal meeting: Herschel FSE development
14/04	Meeting with harness sub-contractor
Management act.	
Project control	➢ SPIRE QM1 master schedule update ➢ DCU EM QM1 detailed schedule update ➢ SPIRE FPU simulator detailed schedule update. ➢ SCU detailed schedule update ➢ LTU detailed schedule update ➢ Action list update. ➢ Documentation management ➢ SPIRE reporting.

Problem Areas	Remedial Actions
Test Bolometer and driving/readout electronics still missing for DCU cold testing	➢ E-mail sent to JPL ➢ SPIRE Project to chase JPL
Cost of the QM2 passive parts beyond what we can afford	➢ QM2 will be built with "low cost" commercial parts as far as possible.
No information from LAM on MCU QM1 development progress.	➢
MCU QM2 and PFM delivery by LAM to CEA on the critical path (respectively scheduled 12/03 & 07/04).	➢ The realisation of the MCU QM2 & PFM is fully sub-contracted. There is little hope to have an earlier delivery. No solution yet.
SCU QM1 development does not progress as expected.	➢ Internal disposition to be taken.

Project Milestones			
Main Delivery Milestones	***Resp.***	***Baseline***	***Current***
DRCU QM1 delivery to RAL	SAp	12/05/2003	**08/08/2003**
FPU Simulator (version 1) delivery to RAL	SAp	12/05/2003	**08/08/2003**
DRCU QM2 delivery to RAL	SAp	05/01/2004	07/04
DRCU FM delivery to RAL	SAp	30/07/2004	12/04 (*)

(*) : Earliest date.

DRCU	
DCU EM / QM1	**Status**

- **DAQ IF**
  - 2 test boards available with test completed.
  - DAQ IF upgrade achieved (New xilinx & patch AMP02 replaced by OP400, OP484 replace OP400 as needed)
- **BIAS**
  - Available, test performed
- **LIA-P**
  - LIA-P#1: Available, test performed
  - LIA-P #2: Available
- **LIA-S**
  - LIA-S #1: Available, test performed
  - LIA-S #2-3 : board fabrication, wiring in progress
- **Back-Planes**
  - Functional test backplane available.
  - Performance test backplane available
- **Test plan**
  - Test plans available: LIA-P, LIA-S, BIAS, DAQ-IF.
  - Functional test plan: writing finalisation.
- **Integration & Test**
  - I/F DPU (FPGA) board validation achieved
  - DAQ-IF tested on 1 channel, good results
  - LIA-P#1 & LIA-S#1 connected and tested with LTU.
  - DAQ-IF + LIA-P#1 + LIA-S#1 + back plane integrated in DCU box , functional & reduced performances test completed
  - First test DCU ←→ LTU started

Progress during the month

- DAQ-IF Test equipment finalisation.
- DAQ-IF modified with new OP484. Test on 1 channel: good results
- LIA-P #1 & LIA-S#1 connected with LTU: good results
- LIA-P # 2 wiring achievement, delivered to SAp 09/04
- LIA-S #2 & 3 wiring in progress
- Boards available were pre-integrated in the DCU QM1 Box
- First test DCU←→ LTU. Results encouraging: DCU & LTU communication is satisfactory

SCU

Status

- **Documentation**
  - Draft Specification and preliminary (H/W & VHDL) design available.
  - Draft DPU/SCU ICD issued.
  - Test plan writing in progress
- **Test equipments**
  - Simplified test bench: available.
  - Test S/W finalised.
  - FSE development on going
- **DPU VHDL I/F**
  - Available but not yet integrated
- **QM1**
  - Board CCHK + IF
    - board available, preliminary manual test successful
  - Board Temp + Heat
    - board available, preliminary manual test on analogic parts successful.
  - Back plane:
    - available
  - Test & Integration
    -not started
- **QM2**
  -

Progress during the month

- **Documentation**
  - None
- **Test equipments**
  - Simplified test bench: finalisation
- **DPU VHDL I/F**
  - None
- **QM1**
  - None
- **QM2**
  - None

MCU

Status

- Design available at LAM & SAp
- Software issue 3 implemented
- QM2 and FM Sub-contractor selected.

MCU Deliveries from LAM to CEA:
QM1 (LAM): March 2003
QM1 (SAp): **June 2003**
QM2: 01/04 (2 months behind schedule at least)
PFM: 07/04

Progress during the month

- No reporting from LAM

PSU	**Status** ➢ Specification available. ➢ Call for tender process ongoing: a company has been pre-selected. **Progress during the month** ➢ Bid received. ➢ Pre-selection of a company.
DRCU Boxes	**Status** ➢ DCU & FCU box thermal & dynamic studies achieved ➢ **DCU.** • STM: box available at SAp. Board front panel & Rack available. • QM1: available at SAp. I/F drawing started. • QM2 & FM: I/F available. ➢ **FCU.** • STM: detailed design achieved, fabrication started • QM1: Available at SAp. I/F drawing updated • QM2 & FM: I/F available **Progress during the month** ➢ FCU QM1 drawings updated. ➢ FCU STM fabrication started

Test Equipments & others	
LTU #1	**Status** ➢ LTU SPIRE #1 available ➢ Software development: on going ➢ LTU ←→ FPU simulator : good test results ➢ LTU←→ DCU: first test conducted with DAC/IF board **Progress during the month** ➢ Test LTU SPIRE → FPU simulator ➢ Software development ➢ Test with DACQ/IF board.
Power Bench	**Status** ➢ Specification available. ➢ Study at sub-contractor on going **Progress during the month** ➢ Development at sub-contractor ➢ Meeting with the sub-contractor to ensure the good development of the power bench
JPL Bolometer test facility	**Status** ➢ SAp people trained to the use of the JPL Bolometer test facility (including Bacus cryostat) ➢ Bacus Cryostat received at SAp. ➢ Mechanical parts and HKL connectors available **Progress during the month** ➢ Mechanical parts received. Installation ➢ HK Connectors received ➢ Cryostat seems functional, ➢ Waiting for detectors & electronics to perform full testing.
FPU Simulator #1	**Status** ➢ SPIRE FPU simulator delivered to SAp 26/02/2003 with user manual and log book
FPU Simulator #2	**Status** ➢ **PXI TRIG IO** • 2 units available and maintenance unit available. Test done ➢ **PXI Cernox** • PXI Cernox: test done, technical performances report writing ➢ Orders placed for the second simulator except PXI BOLO SPIRE **Progress during the month** ➢ None

Part procurement	**Status**	
	➢ **DCL**: edition 14 ➢ **OP400** qualification review 12/02/02. Fabrication on going. Precap first package (1000 items) in Oct 2002. Selection FM / QM January 2003 ➢ Harnesses connector estimation carried out. ➢ ATP update with Tecnologica	
	Progress during the month	
	➢ Routine work ➢ Work on QM2 passive part procurement (self procured parts).	
Harness	**Status**	
	➢ Connectors available ➢ Test harness DCU-LTU-FPU simulator: fabrication on going.	
	Progress during the month	
	➢ Test harness DCU-LTU-FPU_simulator fabrication	
Containers	**Status**	
	➢ Specification available.	
	Progress during the month	
	None	
AIV	**Status**	
	➢ DRCU development tree available (last version 30/11/2001) ➢ DRCU AIV plan available. ➢ DCU EM/QM1 test plan writing ongoing (Configuration tests sequences writing (LTU + FPU_sim + DCU QM1)	
	Progress during the month	
	➢ Configuration tests sequences writing (LTU + FPU_sim + DCU QM1)	
SPIRE FSE	**Status**	
	➢ Specification writing: 3 FSE will be built for DCU boards testing: respectively for DACQ/IF, BIAS & LIA boards.	
	Progress during the month	
	➢ Specification writing for 3 FSEs started	

PA/QA	**Status** ➢ DML, DPL, DMPL available. ➢ Reference documentation list update on going ➢ ADP SPIRE , routine work ➢ Non conformity management ➢ Derating & Reliability SCU achieved **Progress during the month** ➢ Non conformity management ➢ Information research about PCB technologies (QM2 & FM) ➢ Contact with firms which are qualified to work in Spatial domain (QM2 & FM) ➢ Information research at CNES & ESA about harnesses ➢ Information research on MIL quality standards about wires. ➢ SPIRE synoptic test configuration writing ➢ Derating & Reliability DCU-BIAS & SCU achieved ➢ DML + DPL + DMPL SPIRE finalisation

Problem Areas	Remedial Actions
DCU performances specifications are hard to reach	➢ Op. amp. Change. ➢ Specification more in line with real JPL Bolometer performance.
DPU-DRCU I/F: problems encountered during integration of the DPU and DRCU simulator	➢ Wait for DPU information

Milestones		Status
SPIRE FPU simulator #1 delivery to SAp	26/02/2003	Available
DCU test harness	04/2003	Available
DRCU QM1 harnesses need date	05/2003	On schedule
LTU DRCU available	04/2003	Available
Detector test cryostat delivery to SAp by JPL	04/2003	Available
MCU QM1 + simulator delivery to SAp	04/2003	06/2003
SCU QM1 delivery by SEDI	05/2002	On schedule
DRCU QM1 delivery to RAL	**12/05/2003**	**08/08/2003**
SPIRE FPU simulator #2	10/2003	On schedule
SCU QM2 need date	11/2003	On schedule
MCU QM2 delivery to SAp need date	09/2003	11/03
DRCU QM2 delivery to RAL	**05/01/2004**	**07/04**
MCU FM delivery to SAp need date	30/04/2004	On schedule
SCU FM need date	30/04/2004	06/04
PSU delivery		**10/04**
DRCU FM ready for delivery to RAL	**30/07/2004**	**12/04**

Documentation progress this month		
Title	**Reference**	**Progress**
None this month		

Documentation List		
Title	**Reference**	**Version, date**
Reference documentation (documents not coming from SAp, SIS, SEDI…)		
➢ SPIRE Instrument Development Plan IIDR	SPIRE-RAL-PRJ-000035	1.1 draft 12/04/2001
➢ SPIRE Major Milestone List issue 1.3 IIDR	SPIRE-RAL-PRJ-0000455	1.3 31/01/2002
➢ SPIRE Instrument Requirements	SPIRE-RAL-PRJ-000034	1.1 10/01/2002
➢ ICD cooler	HSO-SBT-ICD-012	1.3 07/12/2001
➢ Instrument Interface Document part A	SCI-PT-IIDA-04624	3.0 01/07/2002
➢ Instrument Interface Document part B SPIRE	SCI-PT-IIDB/SPIRE-02124	2.0 31/07/2001
➢ SPIRE Data ICD	SPIRE-RAL-DOC-001078	1.0 draft1 15/01/2002
➢ SPIRE instrument AIV plan	SPIRE-RAL-PRJ-000410	2.1 29/03/2001
➢ SPIRE harness definition	SPIRE-RAL-PRJ-000608	1.1 05/03/2003
➢ Herschel frequency plan	H-P-1-ASPI-PL-0201	1.0 03/05/2002
➢ Radiation requirements	H-P-1-ASPI-SP-0017	1.0 11/06/2001
➢ EMC specification	H-P-1-ASPI-SP-0037	3.0 14/06/2002
➢ Random environment analyses	H-P-2-ASPI-AN-0112	2.0 15/03/2002
➢ Cleanliness requirements specifications	H-P-1-ASPI-SP-0035	2.0 28/06/2002
➢ Herschel general design and interface requirements	H-P-1-ASPI-SP-0027	3.2 15/02/2002
➢ PA requirements for FIRST scientific instruments	PT-RQ-04410	2.0 01/08/2000
➢ Filters - subsystem specification document	SPIRE-QMW-PRJ-000454	2.0 07/09/2001
➢ SPIRE CQM performance test specification	SPIRE-RAL-DOC-001123	0.4 29/05/2002
➢ DPU ICD	SPIRE-IFS-PRJ-000650	1.0 02/04/2001
➢ Calibrator SSSD : SCAL	HSO-CDF-SP-001	1.0 10/09/2001
➢ Calibrator SSSD : PCAL	HSO-CDF-SP-003	1.0 11/09/2001
➢ Environment & tests requirements	H-P-1-ASPI-SP-0030	3.2 18/02/2002
➢ SPIRE instrument AIV plan	SPIRE-RAL-PRJ-000410	2.1 29/03/2001
➢ SPIRE harness definition	SPIRE-RAL-PRJ-000608	1.0 08/07/2002
➢ SPIRE grounding and screening philosophy	SPIRE-RAL-PRJ-00624	1.0 01/10/2002
➢ Note on SPIRE Models Philosophy	None, Bruce Swinyard	1.0 12/07/2000

Management			
➢ Management plan for the Herschel project.	SAp-FIRST-JLA-0038-01	4.0	23/01/2003
➢ Actions list	SAp-FIRST-DR-0050-01		
➢ DRCU & WIH Development Plan	SAp-SPIRE-JLA-0047-01	4.0	29/01/2003
➢ SPIRE development tree	H0030		30/11/2001
➢ SPIRE product tree	SAp-SPIRE-DR-0094-03	1.0	21/01/2003
➢ WBS Herschel	SAP-FIRST-DR-0043-01	2.1	
➢ WBS SPIRE	SAP-FIRST-DR-0045-01	2.1	
➢ DRCU QM1 master schedule	SAp-SPIRE-DR-0105-03	1.3	29/04/2003
➢ DCU EM QM1 at JPL detailed schedule	SAP-FIRST-DR-0050-01	6.1	22/04/2003
➢ SPIRE FPU simulator detailed schedule	SIG-FIRST-PdA-0052-01	19	28/04/2003
➢ SCU QM1 detailed schedule	SEI-SPIRE-MM-0049-01	15	31/03/2003
➢ LTU & power bench detailed schedule	SAp-FIRST-DR-0069-02	3.7	31/03/2003
➢ More documentation on the SAp intranet website			
DRCU			
➢ DRCU Specifications document	SAp-SPIRE-Cca-0025-00	1.0	14/02/2003
➢ DRCU Development Tree	H0030		30/11/2001
➢ DRCU ICD	SAp-SPIRE-Cca-0075-02	1.0	14/02/2003
➢ DRCU DPU ICD	SAp-SPIRE-Cca-0076-02	1.0	14/02/2003
➢ DCU design document	SAp-SPIRE-FP-0063-02	0.3	18/02/2003
➢ Test plan DAQ IF	SAp-SPIRE-FP-0067-02	0.1	18/02/2003
➢ Test plan BIAS	SAp-SPIRE-FP-0066-02	0.1	18/02/2003
➢ Test plan LIA P	SAp-SPIRE-FP-0064-02	0.1	18/02/2003
➢ Test plan LIA S	SAp-SPIRE-FP-0065-02	0.1	18/02/2003
➢ SPIRE test configuration,	SAp-SPIRE-LD-0015-01	3.0	08/2001
➢ FPU simulator specifications for DCU / SCU test	SIG-SPIRE-PdA-0030-01	3.0	14/02/2003
➢ SPIRE LTU specifications	SAp-SPIRE-FD-0071-02	1.0	22/04/2002
➢ DRCU AIV Plan	SAp-SPIRE-HT-0082-02	1.3	05/11/2002
➢ DCU EM QM1 Preliminary test plan	SAp-SPIRE-HT-0088-02	1.0	14/02/2003
➢ SCU design document	SEDI-SCU-MM-2002-1	0.7	17/02/2003
➢ PSU SPIRE specification	SAp-SPIRE-DS-012-02	1.1	11/12/2002
➢ More documentation on the SAp intranet website			
QA			
➢ Standard product assurance plan	SAp-GERES-Flo-436-00	1.0	09/11/2000
➢ SPIRE liste des documents à produire	SAp-SPIRE-Flo-0028-00	0.2	15/12/2000
➢ Organisation de la gestion documentaire sur Herschel au SAp	SAp-FIRST-DR-0053-01	1.1	06/12/2001
➢ Gestion des documents sur la base Herschel	SAp-FIRST-DR-0072-02	1.3	15/04/2002
➢ Procédures de contrôle projet sur Herschel	SAp-FIRST-DR-0125-02	1.4	05/09/2002
➢ DRCU processor board PA specification	SAp-SPIRE-Flo-0020-00		10/01/2001
➢ Plan d'action de AP du projet Herschel	SAp-FIRST-Abx-0137-02	1.1	18/06/2002
➢ Evaluation report for test plan of DCU boards	SAp-SPIRE-JF-0079-02	1.0	
➢ DRCU architecture and reliability analysis report	SAp-SPIRE-Flo-0039-01		21/08/2001
➢ DRCU FMEA reliability	SAp-SPIRE-JF-0099-03	0.1	10/02/2003
➢ DRCU preliminary DMPL	SAp-SPIRE-NC-0100-03	1.0	11/02/2003
➢ DRCU preliminary DPL	SAp-SPIRE-NC-0061-02	1.0	13/02/2003
➢ DRCU DML	SAp-SPIRE-NC-0060-02	1.1	24/03/2003
➢ More documentation on the SAp intranet website			