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Management & System				
Meetings				
27/11	Internal Meeting SAp-SEDI : SCU boards reviews			
19/11	Internal Meeting: FSE development: global sub-contracting is a dead end. Other solution to be investigated.			
06/11	Internal meeting: Re-assessment about DCU electronics development & test schedule, preliminary evaluation of the lab equipment			
12/11	Project Telecon: I/F spec., QM1 schedule, Next Detector Summit at CEA on Dec. 12-13			
Management act.				
Project control	<ul style="list-style-type: none"> ➤ SPIRE master schedule updated. ➤ DCU EM QM1 detailed schedule. ➤ SPIRE FPU simulator detailed schedule update. ➤ Action list update. ➤ SPIRE reporting. 			
SAP / JPL / Caltech	<ul style="list-style-type: none"> ➤ F. Pinsard stay: <ul style="list-style-type: none"> • 1/04 to 10/06: DAQ IF + board test • 24/06 to 12/07: BIAS board test • 29/07 to 15/08: LIA-P • 02/09 to 30/09: LIA-S test board + functional system test • 06/01/2003 to 17/01 performances test JPL • 20/01 to 24/01: JPL to Boulder • 27/01 to 03/02: performances test at Boulder ➤ Future stays depending on the evolution of the DCU QM1 development plan. 			
Problem Areas		Remedial Actions		
Late availability of the PSU. FM Schedule impact will be known only at the end of the call for tender process (minimum development time starting from the contract sign off: 14 months)		<ul style="list-style-type: none"> ➤ FM will be powered by a power-bench as long as the PSU FM is not available. ➤ FM delivery likely delayed. 		
Funding issue for the cold tests at Boulder due to the schedule shift.		➤ Under discussion.		
DRCU I/F Definition of the MCU tele-commanding still not frozen.		➤ A dedicated meeting has to be organised (discussion will take place during the forthcoming Detector Summit)		
MCU QM1 and MCU simulator deliveries not secure due to lack of resources at LAM		➤ LAM & CNES are investigating solutions.		
MCU QM2 and PFM delivery by LAM to CEA on the critical path (respectively scheduled 12/03 & 07/04).		➤ The realisation of the MCU QM2 & PFM is fully sub-contracted. There is little hope to have an earlier delivery. No solution yet.		
Actions				
Still Opened				
<i>Ref.</i>	<i>Meeting</i>	<i>Actionnee</i>	<i>Due date</i>	<i>Action</i>
/	/	/	/	/
Closed				
<i>Ref.</i>	<i>Meeting</i>	<i>Actionnee</i>	<i>Due date</i>	<i>Action</i>
/	/	/	/	/
Project Milestones				
<i>Main Delivery Milestones</i>				
		<i>Resp.</i>	<i>Baseline</i>	<i>Current</i>
DRCU QM1 delivery to RAL		SAP	12/05/2003	23/06/2003
FPU Simulator (version 1) delivery to RAL		SAP	12/05/2003	23/06/2003
DRCU QM2 delivery to RAL		SAP	05/01/2004	On schedule (*)
DRCU FM delivery to RAL		SAP	30/07/2004	On schedule (*)

(*): MCU QM2 & PFM as well as PSU FM delivery dates not taken into account.

DRCU	
DCU/QM1	<p>Status</p> <ul style="list-style-type: none"> ➤ DAQ IF <ul style="list-style-type: none"> • 2 test boards available at JPL • Test completed. • DAQ IF upgrade achieved (New xilinx & patch AMP02 mounting) ➤ BIAS <ul style="list-style-type: none"> • Board assembly achieved 29/05 • Board test performed ➤ LIA-P <ul style="list-style-type: none"> • PCB fabrication achieved • Board test performed ➤ LIA-S <ul style="list-style-type: none"> • Board assembly achieved • Board test performed ➤ Back-Planes <ul style="list-style-type: none"> • Functional test backplane available. • Performance test backplane available, test achieved ➤ Test plan <ul style="list-style-type: none"> • Test plans: LIA-P, LIA-S, BIAS, DAQ-IF available in draft form. Update in progress. • Functional test plan: writing finalisation. ➤ Test <ul style="list-style-type: none"> • Functional test achieved • Test on DAQ IF achieved • I/F DPU (FPGA) board validation achieved • DPU I/F: FPGA achieved
	<p>Progress during the month</p>
	<p>Functional test plan writing Boards test plan upgrade</p> <p>Performance test backplane fabrication achievement, test achievement</p> <p>DAQ IF upgrade achievement (New xilinx & patch AMP02 mounting) DAQ IF test achievement</p> <p>DPU I/F: FPGA achievement</p> <p>LIA-P & LIA-S boards delivered to Sap for control and integration in DCU box.</p>

SCU/QM1	Status
	<ul style="list-style-type: none"> ➤ Heaters: prototype test achieved. ➤ Temperature sensors: test successful ➤ DPU I/F command and data I/F achieved. ➤ Analog port study achievement, software preliminary study in progress. ➤ Test board analog port: board test design & studies achieved. ➤ Test software: development started ➤ SCU Documentation <ul style="list-style-type: none"> • Draft Specification and preliminary (H/W & VHDL) design available. • Draft DPU/SCU ICD issued. • Test plan writing in progress ➤ Functions <ul style="list-style-type: none"> • <u>Heater & temperature</u>: implementation achieved • <u>Calibrator</u>: implementation achieved. • <u>HSK</u>: prototype board in fabrication, 2 people were added for a few month's to study it, the test software and a FPGA to convert different communication protocols. • <u>SCU logic (pinout)</u>: study achieved • <u>SCU logic (logic)</u>: study in finalisation, logic finalisation on FPGA ➤ Boards <ul style="list-style-type: none"> • <u>Temperature</u>: design PCB achieved. PCB layout achieved. • <u>Cchkif</u>: design PCB achieved. Board scheme finalisation on going. • <u>Back plane</u>: PCB design & layout achieved.
	Progress during the month
	<p>SCU logic function: upgrade, logic finalisation on FPGA Cchkif: board scheme finalisation Test board analog port: board test design & studies achievement Test software: development started</p>
MCU	Status
	<ul style="list-style-type: none"> ➤ Design available at LAM & Sap ➤ QM2 and FM Sub-contractor selected. MCU Deliveries from LAM to CEA: QM1: 03/03/2003 QM2: 12/03 (2 months behind schedule at least) PFM: 07/04
	Progress during the month
PSU	Status
	<ul style="list-style-type: none"> ➤ Separate power bench will be used for QM1 and QM2 and FM. ➤ Draft Specification available. ➤ Call for tender process started ➤ Contractual specification writing
	Progress during the month
	<p>SPIRE PSU Contractual specification finalisation</p>

DRCU Boxes	Status	
	<ul style="list-style-type: none"> ➤ Modeling completed. ➤ DCU STM board front panel design & fabrication achieved. Mounting achieved ➤ DCU STM rack available ➤ FCU box thermal & dynamic studies achieved ➤ DCU Box. <ul style="list-style-type: none"> • <u>STM</u>: box available at SAp. • <u>QM1</u>: available at SAp. I/F drawing started. • <u>QM2 & FM</u>: I/F available. ➤ FCU Box. <ul style="list-style-type: none"> • <u>STM</u>: detailed design achieved, ready for fabrication. • <u>QM1</u>: Available at SAp. I/F drawing started • <u>QM2 & FM</u>: I/F available 	
	Progress during the month	
DCU, FCU box QM1 : I/F drawing started DCU STM box delivered Connector panel delivered		
Test Equipments & others		
LTU #1	Status	
	<ul style="list-style-type: none"> ➤ Specifications: available (see documentation). ➤ Hardware & software architecture definition: achieved. ➤ Software procurement: development system delivered ➤ Hardware procurement: Industrial PC, boards delivered ➤ Test on Hermes board achieved ➤ Electronic and mechanic I/F specification achieved. Call for tender achieved ➤ Software development: in finalisation. ➤ Rack I/F: study achievement and fabrication started ➤ LTU study at subcontractor: started ➤ Power bench specification writing on going 	
	Progress during the month	
Soft development + test: Hermes Board debug achievement and development finalisation More Hermes boards ordered I/F rack: study achievement and fabrication started Subcontractor search & call for tender achieved LTU study at subcontractor: started Power bench specification writing		

FPU Simulator #1	Status	
	<ul style="list-style-type: none"> ➤ Specification available ➤ RACK: - Electrical rack available, test on going - Integration: electrical rack+ PC+ PXI rack. Test on going ➤ PXI TRIG IO <ul style="list-style-type: none"> • Hardware test achieved. Second fabrication achieved. VHDL update achieved. Functional test of the 2nd PXI achieved. ➤ PXI BOLO SPIRE <ul style="list-style-type: none"> • Electronic & design Achieved. VHDL soft studies. Test software specification writing achieved. Test board configuration study & realisation achieved. Functional test achieved. Stability checked out, prototype demonstration, fabrication in progress • 5 delivered, test of those 5, technical performances test report writing ➤ PXI heater/Supply <ul style="list-style-type: none"> • Design achieved. Manufacturing file <input type="checkbox"/>ritten. Test software specifications achieved. Test board configuration study & realization achieved. Onboard VHDL software study achieved. • 4 delivered, test of 2 of them, technical performances test report writing ➤ PXI Cernox DC & AC <ul style="list-style-type: none"> • Analogue studies & design achieved. Complementary tests achieved. Manufacturing file writing achieved, Test software specifications achieved. Test board configuration study & realisation achieved. • Onboard VHDL software study over at 50%. PXI part fabrication started week 21 (sub-contractor SPCI & ERTE). • Functional test achieved, Fabrication achieved • 6 delivered, 3 of them tested ➤ Software <ul style="list-style-type: none"> • PXI BOLO SPIRE, PXI HEATER / SUPPLY, PXI CERNOX, PXI TRIGGER IO test software development achieved. • Supervision software development finalisation , test with PXI prototypes ➤ Documentation <ul style="list-style-type: none"> • User manual and log book writing started 	
	Progress during the month	<p>User manual and log book writing started PXI BOLO SPIRE: 5 delivered, test of those 5, technical performances test report writing PXI heater supply : 4 delivered, test of 2 of them, technical performances test report writing PXI CERNOX : 6 delivered, 3 of them tested Supervision Software: development finalisation Rack: study achievement</p>
FPU Simulator #2	Status	
	Progress during the month	
	Orders placed for the 2 nd simulator	

Part procurement	Status	
	<ul style="list-style-type: none"> ➤ Declared components list update: edition 13 ➤ OP400 qualification review 12/02/02. Fabrication started. ➤ Harnesses connector estimation carried out. ➤ ATP update with Tecnologica 	
	Progress during the month	
Routine work Precap on 1 st lot of OP400 (HCM): 1088#		
Harness	Status	
	<ul style="list-style-type: none"> ➤ DCU at JPL test Harness delivered to CEA and sent to JPL ➤ Connectors procurement on going ➤ Work with the AIV to determine SPIRE test harness in progress 	
	Progress during the month	
SACEE connectors partial delivery Work with the AIV to determine SPIRE test harness		
Containers	Status	
	<ul style="list-style-type: none"> ➤ Specification available. 	
	Progress during the month	
None		
AIV	Status	
	<ul style="list-style-type: none"> ➤ DRCU development tree available (last version 30/11/2001) ➤ DCU Board Test plan writing in progress. ➤ DRCU AIV plan available. 	
	Progress during the month	
DRCU AIV plan finalised Work with DCU team about the DCU Test plan		
PA/QA	Status	
	<ul style="list-style-type: none"> ➤ DML and DPL draft available. ➤ Reference documentation list update on going ➤ Requirement Cross verification table achieved ➤ ADP SPIRE on going 	
	Progress during the month	
Updating of the reference document list. Non conformity management ADP SPIRE on going Documentation check		

Problem Areas	Remedial Actions
SCU development is longer than scheduled: delivery to SAp 18/04/2003	➤ None

Milestones		Status
DCU EM QM1 delivery to SAp from JPL	10/02/2003	On schedule
DRCU QM1 harnesses need date	10/02/2003	On shedule
LTU DRCU available	03/04/2003	On schedule
SPIRE FPU simulator #1 delivery to SAp	30/01/2003	On schedule
Detector test cryostat delivery to SAp by JPL	15/02/2003	On schedule
MCU QM1 + simulator need date delivery to SAp	03/03/2003	?????
SCU QM1 delivery by SEDI need date	19/02/2003	Delayed to 18/04
DRCU QM1 delivery to RAL	12/05/2003	Delayed to 23/06/2003
SPIRE FPU simulator #2 need date	29/09/2003	On schedule
SCU QM2 need date	11/2003	On schedule
MCU QM2 delivery to SAp need date	27/08/2003	11/03
DRCU QM2 delivery to RAL	05/01/2004	On schedule (*)
MCU FM delivery to SAp need date	30/04/2004	On schedule
SCU FM need date	30/04/2004	06/04
DRCU FM ready for delivery to RAL	30/07/2004	On schedule (*)

(*): MCU QM2 & PFM as well as PSU FM delivery dates not taken into account.

Documentation progress this month		
Title	Reference	Progress
FPU simulator architecture	SIG-01-266-PDA	Issue 3.0
FPU simulator: supervision software architecture	DAPNIA-SIS-02-221-PDA	Issue 3.0
FPU simulator: I/F specification between PXI Trigger IO, supervision software & LTU	SIG-02-02-PD	Issue 3.0
FPU simulator: File input specification	SIS-02-222-PAD	Issue 2.0
FPU simulator specification for DCU SCU test	SIG-SPIRE-PDA-030-01	Issue 2.0
PSU SPIRE specification	SAp-SPIRE-DS-012-02	Issue 1.0
DRCU AIV Plan	SAp-SPIRE-HT-0082-02	1.3 05/11/2002

Documentation List			
Title	Reference	Version, date	
Reference documentation			
➤ SPIRE Instrument Development Plan IIDR	/	Issue 1.1	12/4/2001 IIDR
➤ SPIRE Major Milestone List issue 1.3 IIDR	SPIRE-RAL-PRJ-000455	Issue 1.3	
➤ SPIRE Instrument Requirements	SPIRE-RAL-34	Issue 1.1	10/01/2002
➤ ICD cooler	HSO-SBT-ICD-012	/	
➤ SCAL ICD	HSO-CDF-ICD-011	2.0	06/02/2002
➤ PCAL ICD	HSO-CDF-ICD-013	2.0	06/02/2002
➤ Detector SSSD	SPIRE-JPL-PRJ-000956	Issue 3.1 – draft	
➤ Shutter SSSD	Not yet	/	
➤ Instrument Interface Document part A	SCI-PT-IIDA-04624	3.0	01/07/2002
➤ Instrument Interface Document part B SPIRE	SCI-PT-IIDB/SPIRE-02124	2.2	01/07/2002
➤ SPIRE configurable document tree	SPIRE-RAL-PRJ-00033	3.1	03/05/2001
➤ SPIRE product tree	SPIRE-RAL-PRJ-00455	1.0	09/11/1999
➤ SPIRE instrument development plan	SPIRE-RAL-PRJ-0035	1.0	20/05/2000
➤ SPIRE management plan	SPIRE-RAL-PRJ-00029		01/01/2001
➤ SPIRE Data ICD	SPIRE-RAL-DOC-001078	1.0 draft1	15/01/2002
➤ SPIRE instrument AIV plan	SPIRE-RAL-PRJ-000410	2.1	29/03/2001
➤ SPIRE harness definition	SPIRE-RAL-PRJ-000608	1.0	08/07/2002
Management			
➤ Management plan for the Herschel project.	SAp-FIRST-JLA-0038-01	3.0	23/11/2001
➤ Actions list	SAp-FIRST-DR-0050-01		
➤ DRCU & WIH Development Plan	SAp-SPIRE-JLA-0047-01	3.0	27/11/2001
➤ SPIRE product tree	SAp-FIRST-DR-0071-02	1.2	
➤ WBS Herschel	SAp-FIRST-DR-0043-01	2.1	
➤ WBS SPIRE	SAp-FIRST-DR-0045-01	2.1	
➤ SPIRE master schedule	SAp-SPIRE-DR-0053-02	3.6	25/11/2002
➤ DCU EM QM1 at JPL detailed schedule	SAp-FIRST-DR-0050-01	5.3	20/11/2002
➤ SPIRE FPU simulator detailed schedule	SIG-FIRST-PdA-0052-01	15.0	29/12/2002
➤ SCU QM1 detailed schedule	SEI-SPIRE-MM-0049-01	12.0	22/11/2002
➤ LTU & power bench detailed schedule	SAp-FIRST-DR-0069-02	3.4	21/11/2002
DRCU			
➤ DRCU Specifications document	SAp-SPIRE-Cca-0025-00	Issue 0.92	26/06/2002
➤ DRCU Development Tree	H0030		30/11/2001
➤ DRCU ICD	SAp-SPIRE-Cca-0075-02	0.7	26/06/2002
➤ DRCU DPU ICD	SAp-SPIRE-Cca-0076-02	0.7	26/06/2002
➤ DCU design document	SAp-SPIRE-FP-0063-02	0.2	05/07/2002
➤ Test plan DAQ IF	SAp-SPIRE-FP-0067-02	0.1 draft	
➤ Test plan BIAS	SAp-SPIRE-FP-0066-02	0.1 draft	
➤ Test plan LIA P	SAp-SPIRE-FP-0064-02	0.1 draft	
➤ Test plan LIA S	SAp-SPIRE-FP-0065-02	0.1 draft	
➤ SPIRE test configuration,	SAp-SPIRE-LD-0015-01	3.0	08/2001
➤ FPU simulator specifications for DCU / SCU test	SIG-SPIRE-PdA-0030-01		19/03/2001
➤ SPIRE LTU specifications	SAp-SPIRE-FD-0071-02	1.0	22/04/2002
➤ DRCU AIV Plan	SAp-SPIRE-HT-0082-02	1.3	05/11/2002
➤ SCU design document	SEDI-SCU-MM-2002-1	0.6	30/06/2002
➤ PSU SPIRE specification	SAp-SPIRE-DS-012-02	1.0	24/10/2002

QA				
➤	Standard product assurance plan	SAp-GERES-Flo-436-00	1.0	09/11/2000
➤	SPIRE liste des documents à produire	SAp-SPIRE-Flo-0028-00	0.2	15/12/2000
➤	Organisation de la gestion documentaire sur Herschel au SAp	SAp-FIRST-DR-0053-01	1.1	06/12/2001
➤	Gestion des documents sur la base Herschel	SAp-FIRST-DR-0072-02	1.3	15/04/2002
➤	Procédures de contrôle projet sur Herschel	SAp-FIRST-DR-0125-02	1.4	05/09/2002
➤	DRCU processor board PA specification	SAp-SPIRE-Flo-0020-00		10/01/2001
➤	Plan d'action de AP du projet Herschel	SAp-FIRST-Abx-0137-02	Issue 1.1	18/06/2002
➤	Evaluation report for test plan of DCU boards	SAp-SPIRE-JF-0079-02	Issue 1.0	
➤	DRCU architecture and reliability analysis report	Sap-SPIRE-Flo-0039-01		21/08/2001