CEA/SAp October 2002 Status and Progress Report

Management & System

Meetings	
02/10/2002	Herschel P.A internal team presentation
04/10/2002	Preparation of the functional and performance tests of DCU EM QM1 at Boulder
22/10/2002	Wires & DRCU electronic co-ordination
23/10/2002	Progress on MCU at LAM
25/10/2002	Internal meeting: DCU electronics development & test schedule
30/10/2002	SCU conception review

Management act.	
Project control	➢ SPIRE master schedule updated. ➢ DCU EM QM1 detailed schedule. ➢ SPIRE FPU simulator detailed schedule update. ➢ Action list update. ➢ SPIRE reporting.
SAp / JPL / Caltech	➢ F. Pinsard stay at Caltech : • 11/04 to 10/06: DAQ IF + board test • 24/06 to 12/07: BIAS board test • 29/07 to 15/08: LIA-P • 02/09 to 30/09: LIA-S test board + functional system test • 01/03 (TBC): functional & performance tests

Problem Areas	Remedial Actions
Sorting out of the Grounding and EMI/EMC issue (outcome of the Grounding Scheme review) has delayed the finalisation of the PSU specification writing and the PSU call for tender accordingly.	➢ FM will likely have to be powered by a powerbench as long as the PSU FM is not available. ➢ The PSU FM availability being on the critical path, the DRCU FM could be delayed. ➢ See DRCU workpackage section.
Funding issue for the cold tests at Boulder due to the schedule shift.	➢ Under discussion.
Definition of the MCU tele-commanding still not frozen.	➢ A dedicated meeting is foreseen asap.
MCU QM2 and PFM delivery by LAM to CEA on the critical path (respectively scheduled 12/03 & 07/04).	➢ The realisation of the MCU QM2 & PFM is fully sub-contracted. There is little hope to have an earlier delivery. No solution yet.
DCU STM at a stand still waiting for Alcatel agreement on foot number and screw diameter.	➢ SPIRE system to urge Alacatel to act.

Actions

Still Opened

Ref.	*Meeting*	*Actionnee*	*Due date*	*Action*
/	/	/	/	/

Closed

Ref.	*Meeting*	*Actionnee*	*Due date*	*Action*
/	/	/	/	/

Project Milestones

Main Delivery Milestones	*Resp.*	*Baseline*	*Current*
DRCU QM1 delivery to RAL	SAp	12/05/2003	20/05/2003
FPU Simulator (version 1) delivery to RAL	SAp	12/05/2003	20/05/2003
DRCU QM2 delivery to RAL	SAp	05/01/2004	On schedule (*)
DRCU FM delivery to RAL	SAp	30/07/2004	On schedule (*)

(*): MCU QM2 & PFM delivery dates not taken into account.

DRCU

DCU/QM1

Status

- **DAQ IF**
  - 2 test boards available at JPL
  - Test completed.
- **BIAS**
  - Board assembly achieved 29/05
  - Board test performed
- **LIA-P**
  - PCB fabrication achieved
  - Board test performed
- **LIA-S**
  - Board assembly achieved
  - Board test performed
- **Back-Planes**
  - Functional test backplane built.
  - Performance test backplane design & PCB layout achieved. Fabrication finalisation
- **Test plan**
  - Test plans: LIA-P, LIA-S, BIAS, DAQ-IF available in draft form. Update in progress.
  - Functional test plan: writing finalisation.
- **Test**
  - Functional test achieved
  - Test on DAQ IF achieved
  - I/F DPU (FPGA) board validation achieved

Progress during the month

Functional test plan writing finalisation
Performance test backplane fabrication finalisation
I/F DPU (FPGA) board validation
Boards test plan upgrade
Test on DAQ IF

SCU/QM1

Status

- Heaters: prototype test achieved.
- Temperature sensors: test successful
- DPU I/F command and data I/F achieved.
- Analog port study achievement, software preliminary study in progress.
- Test board analog port study in progress.

- **SCU Documentation**
  - Draft Specification and preliminary (H/W & VHDL) design available.
  - Draft DPU/SCU ICD issued.
  - Test plan writing in progress

- **Functions**
  - Heater & temperature: implementation achieved
  - Calibrator: implementation achieved.
  - HSK: prototype board in fabrication, 2 people were added for a few month's to study it, the test software and a FPGA to convert different communication protocols.
  - SCU logic (pinout): study achieved
  - SCU logic (logic): study in finalisation

- **Boards**
  - Temperature: design PCB achieved. PCB layout achieved.
  - Cchkif: design PCB achieved. Board scheme finalisation.
  - Back plane: PCB design & layout achieved.

Progress during the month

MCU	**Status** ➢ Design available at LAM & SAp ➢ Sub-contractor selected. **Progress during the month** ➢ CEA/LAM meeting ➢ MCU Deliveries from LAM to CEA: QM1: 03/03/2003 QM2: 12/03 (2 months behind schedule at least) PFM: 07/04
PSU	**Status** ➢ Separate power bench will be used for QM1 and QM2 and FM. ➢ Draft Specification available. ➢ Call for tender process started ➢ Contractual specification writing **Progress during the month** Specification writing Call for tender process started
DRCU Boxes	**Status** ➢ Modeling completed. ➢ DCU STM board front panel design & fabrication achieved. Mounting achieved ➢ DCU STM rack available ➢ FCU box thermal & dynamic studies achieved ➢ **DCU Box.** • STM: detailed design achieved, fabrication in progress. • QM1: available at SAp. • QM2 & FM: I/F available. ➢ **FCU Box.** • STM: detailed design achieved, ready for fabrication. • QM1: Available at SAp. Thermal & dynamic studies in progress • QM2 & FM: I/F available **Progress during the month** DCU STM box fabrication. DCU STM rack delivery DCU STM boards mounting FCU box thermal & dynamic studies achievement.

Test Equipments & others

LTU #1

Status

- Specifications: available (see documentation).
- Hardware & software architecture definition: achieved.
- Software development: in progress.
- test on Hermes board on going
- Software procurement: development system delivered
- Hardware procurement: Industrial PC, boards delivered.
- Electronic and mechanic I/F specification achievement. Call for tender started
- Rack I/F studies started
- Power bench specification writing started

Progress during the month

Software development + test on Hermes board
Electronic and mechanic I/F specification achievement. Call for tender started.
Power bench specification writing started
Rack I/F studies started

FPU Simulator #1

Status

- Specification available
- RACK: - Electrical rack available, test on going
  - Integration: electrical rack+ PC+ PXI rack. Test on going

- **PXI TRIG IO**
  - Hardware test achieved. Second fabrication achieved. VHDL update achieved. Functional test of the 2nd PXI achieved.

- **PXI BOLO SPIRE**
  - Electronic & design Achieved. VHDL soft studies. Test software specification writing achieved. Test board configuration study & realisation achieved. Functional test achieved. Stability checked out, prototype demonstration, fabrication launch

- **PXI heater/Supply**
  - Design achieved. Manufacturing file ritten. Test software specifications achieved. Test board configuration study & realization achieved. Onboard VHDL software study achieved.
  - PXI part fabrication started week 21 (sub-contractor SPCI & ERTE).

- **PXI Cernox DC & AC**
  - Analogue studies & design achieved. Complementary tests achieved. Manufacturing file writing achieved, Test software specifications achieved. Test board configuration study & realisation achieved.
  - Onboard VHDL software study over at 50%. PXI part fabrication started week 21 (sub-contractor SPCI & ERTE).
  - Functional test achieved, Fabrication launch

- **Software**
  - PXI BOLO SPIRE, PXI HEATER / SUPPLY, PXI CERNOX, PXI TRIGGER IO test software development achieved.
  - Supervision software development finalisation , test with PXI prototypes

Progress during the month

PXI BOLO SPIRE: performances report study.
PXI heater/supply: performances report study.
SOFTWARE: supervision software development finalisation
RACK: - Electrical rack fabrication, delivery and test.
- Integration: electrical rack+ PC+ PXI rack. Test

FPU Simulator #2	**Status**
	Progress during the month
	Orders placed for the 2nd simulator
Part procurement	**Status**
	➢ Declared components list update: edition 13 ➢ OP400 qualification review 12/02/02. Fabrication started. ➢ Harnesses connector estimation carried out. ➢ ATP update with Tecnologica
	Progress during the month
	Routine work
Harness	**Status**
	➢ DCU at JPL test Harness delivered to CEA and sent to JPL ➢ Connectors procurement on going ➢ Work with the AIV to determine SPIRE test harness in progress
	Progress during the month
	SACEE connectors partial delivery Work with the AIV to determine SPIRE test harness
Containers	**Status**
	➢ Specification available.
	Progress during the month
	None
AIV	**Status**
	➢ DRCU development tree available (last version 30/11/2001) ➢ DCU Board Test plan writing in progress. ➢ DRCU AIV plan in progress.
	Progress during the month
	DRCU AIV plan
PA/QA	**Status**
	➢ DML and DPL draft available. ➢ Reference documentation list update on going ➢ Requirement Cross verification table achieved
	Progress during the month
	Updating of the reference document list. Building of Requirement Cross verification table achievement. Non conformity management ADP SPIRE preparation Documentation check

Problem Areas	Remedial Actions
	➢

Milestones		Status
DCU EM QM1 delivery to SAp from JPL	10/02/2003	On schedule
DRCU QM1 harnesses need date	12/2002	On schedule
LTU DRCU available	24/03/2003	On schedule
SPIRE FPU simulator #1 need date delivery to SAp	10/02/2003	On schedule
Detector test cryostat delivery to SAp by JPL	15/02/2003	On schedule
MCU QM1 + simulator need date delivery to SAp	03/03/2003	On schedule
SCU QM1 delivery by SEDI need date	19/02/2003	On schedule
DRCU QM1 delivery to RAL	**12/05/2003**	**20/05/2002**
SPIRE FPU simulator #2 need date	29/09/2003	On schedule
SCU QM2 need date	11/2003	On schedule
MCU QM2 delivery to SAp need date	27/08/2003	11/03
DRCU QM2 delivery to RAL	**05/01/2004**	**On schedule (*)**
MCU FM delivery to SAp need date	30/04/2004	On schedule
SCU FM need date	30/04/2004	06/04
DRCU FM ready for delivery to RAL	**30/07/2004**	**On schedule (*)**

(*): MCU QM2 & PFM delivery dates not taken into account.

Documentation progress this month		
Title	**Reference**	**Progress**

Documentation List		
Title	**Reference**	**Version, date**
Reference documentation		
➢ SPIRE Instrument Development Plan IIDR	/	Issue 1.1 12/4/2001 IIDR
➢ SPIRE Major Milestone List issue 1.3 IIDR	SPIRE-RAL-PRJ-000455	Issue 1.3
➢ SPIRE Instrument Requirements	SPIRE-RAL-34	Issue 1.1 10/01/2002
➢ ICD cooler	HSO-SBT-ICD-012	/
➢ SCAL ICD	HSO-CDF-ICD-011	2.0 06/02/2002
➢ PCAL ICD	HSO-CDF-ICD-013	2.0 06/02/2002
➢ Detector SSSD	SPIRE-JPL-PRJ-000956	Issue 3.1 – draft
➢ Shutter SSSD	Not yet	/
➢ Instrument Interface Document part A	SCI-PT-IIDA-04624	3.0 01/07/2002
➢ Instrument Interface Document part B SPIRE	SCI-PT-IIDB/SPIRE-02124	2.2 01/07/2002
➢ SPIRE configurable document tree	SPIRE-RAL-PRJ-00033	3.1 03/05/2001
➢ SPIRE product tree	SPIRE-RAL-PRJ-00455	1.0 09/11/1999
➢ SPIRE instrument development plan	SPIRE-RAL-PRJ-0035	1.0 20/05/2000
➢ SPIRE management plan	SPIRE-RAL-PRJ-00029	01/01/2001
➢ SPIRE Data ICD	SPIRE-RAL-DOC-001078	1.0 draft1 15/01/2002
➢ SPIRE instrument AIV plan	SPIRE-RAL-PRJ-000410	2.1 29/03/2001
➢ SPIRE harness definition	SPIRE-RAL-PRJ-000608	1.0 08/07/2002
Management		
➢ Management plan for the Herschel project.	SAp-FIRST-JLA-0038-01	3.0 23/11/2001
➢ Actions list	SAp-FIRST-DR-0050-01	
➢ DRCU & WIH Development Plan	SAp-SPIRE-JLA-0047-01	3.0 27/11/2001
➢ SPIRE product tree	SAp-FIRST-DR-0071-02	1.2
➢ WBS Herschel	SAP-FIRST-DR-0043-01	2.1
➢ WBS SPIRE	SAP-FIRST-DR-0045-01	2.1
➢ SPIRE master schedule	SAp-SPIRE-DR-0053-02	3.5 30/10/2002
➢ DCU EM QM1 at JPL detailed schedule	SAP-FIRST-DR-0050-01	5.0 30/10/2002
➢ SPIRE FPU simulator detailed schedule	SIG-FIRST-PdA-0052-01	14.0 30/10/2002
➢ SCU QM1 detailed schedule	SEI-SPIRE-MM-0049-01	12 30/10/2002
➢ LTU & power bench detailed schedule	SAp-FIRST-DR-0069-02	3.3 30/10/2002
DRCU		
➢ DRCU Specifications document	SAp-SPIRE-Cca-0025-00	Issue 0.92 26/06/2002
➢ DRCU Development Tree	H0030	30/11/2001
➢ DRCU ICD	SAp-SPIRE-Cca-0075-02	0.7 26/06/2002
➢ DRCU DPU ICD	SAp-SPIRE-Cca-0076-02	0.7 26/06/2002
➢ DCU design document	SAp-SPIRE-FP-0063-02	0.2 05/07/2002
➢ Test plan DAQ IF	SAp-SPIRE-FP-0067-02	0.1 draft
➢ Test plan BIAS	SAp-SPIRE-FP-0066-02	0.1 draft
➢ Test plan LIA P	SAp-SPIRE-FP-0064-02	0.1 draft
➢ Test plan LIA S	SAp-SPIRE-FP-0065-02	0.1 draft
➢ SPIRE test configuration,	SAp-SPIRE-LD-0015-01	3.0 08/2001
➢ FPU simulator specifications for DCU / SCU test	SIG-SPIRE-PdA-0030-01	19/03/2001
➢ SPIRE LTU specifications	SAp-SPIRE-FD-0071-02	1.0 22/04/2002
➢ DRCU AIV Plan	SAp-SPIRE-HT-0082-02	1.2 23/09/2002
➢ SCU design document	SEDI-SCU-MM-2002-1	0.6 30/06/2002
QA		
➢ Standard product assurance plan	SAp-GERES-Flo-436-00	1.0 09/11/2000
➢ SPIRE liste des documents à produire	SAp-SPIRE-Flo-0028-00	0.2 15/12/2000
➢ Organisation de la gestion documentaire sur Herschel au SAp	SAp-FIRST-DR-0053-01	1.1 06/12/2001
➢ Gestion des documents sur la base Herschel	SAp-FIRST-DR-0072-02	1.3 15/04/2002
➢ Procédures de contrôle projet sur Herschel	SAp-FIRST-DR-0125-02	1.2 13/05/2002
➢ DRCU processor board PA specification	SAp-SPIRE-Flo-0020-00	10/01/2001
➢ Plan d'action de AP du projet Herschel	SAp-FIRST-Abx-0137-02	Issue 1.1 18/06/2002
➢ Evaluation report for test plan of DCU boards	SAp-SPIRE-JF-0079-02	Issue 1.0
➢ DRCU architecture and reliability analysis report	Sap-SPIRE-Flo-0039-01	21/08/2001