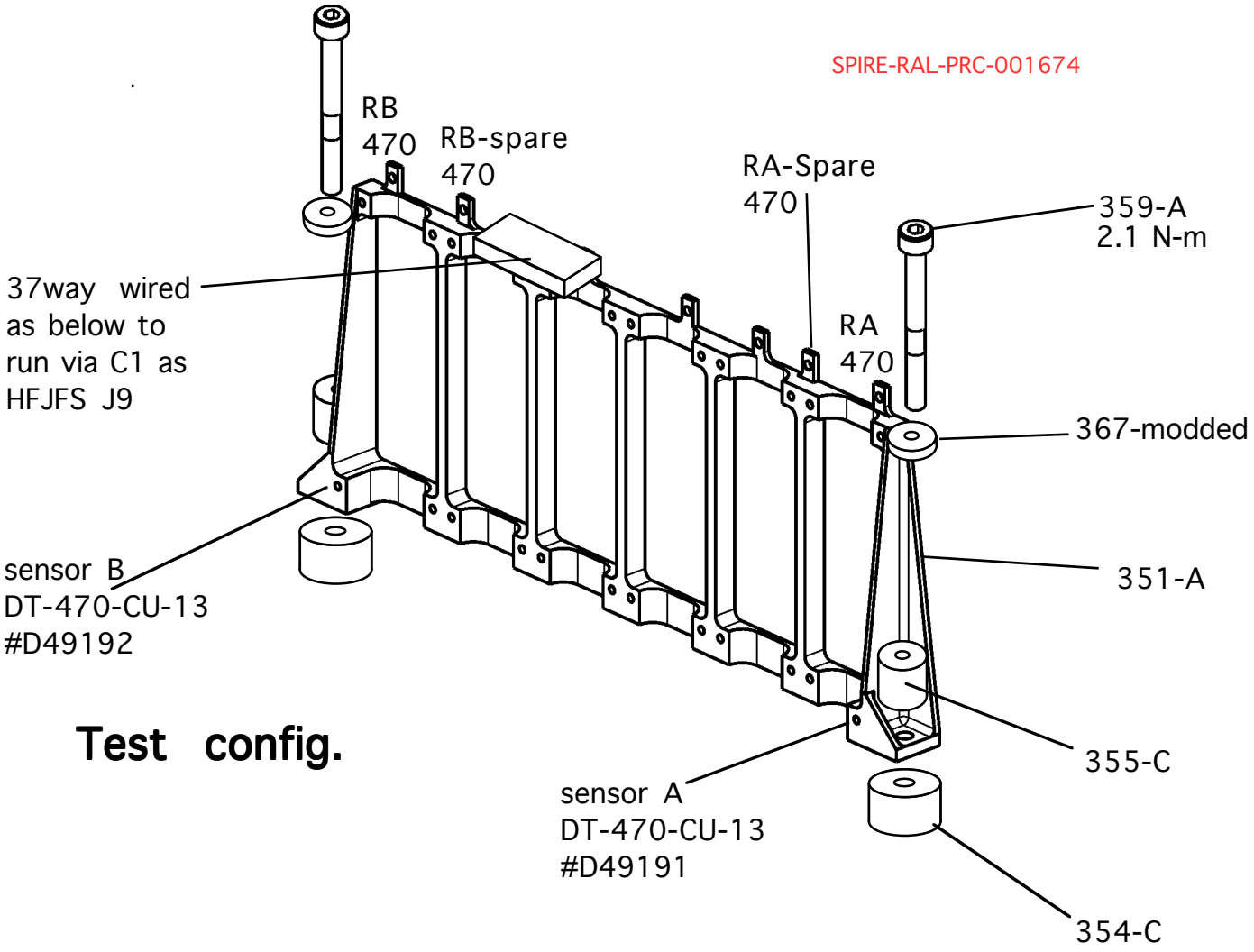

Test config.

Using instrument harness. Resistors A & B connected at warm end to Dave's PC card.

Lakeshore diode sensors to be standardly conditioned, suggesting using an algorithm that differences zero mA and conditioning mA to substract out thermal emfs in the voltage sense lines.

With HOB around 10K, adjust PC card output to dissipate 30mW in heater RA.

Turn off & settle. Record sensors A and B plus nearby baseplate temperature.
Turn on power to RA, don't worry if drifts a bit off 30mW, but after settling measure power plus record sensors A and B plus nearby baseplate temperature.

Turn off & settle. Record sensors A and B plus nearby baseplate temperature.
Turn on power to RB, don't worry if drifts a bit off 30mW, but after settling measure power plus record sensors A and B plus nearby baseplate temperature.

Turn off & settle. Record sensors A and B plus nearby baseplate temperature.

JD
2/6/03

? John Delderfield 2003.06.02 12:09:34 + 01'00'

37-way on C1

Harness Use OF P09	Pin number	Test use
PTC Bias_A +ve	1	Sensor A I+
PTC Bias_A –ve	20	Sensor A I-
PTC Bias_A Shield	2 (A3)	Shield
PTC Ground_A	2 (A3)	JFET Chassis
PTC JFETV Bias_A +ve	21	Sensor A V+
PTC JFETV Bias_A -ve	3	Sensor A V-
PTC JFETV Bias_A Shield	2 (A3)	Shield
SLW_BIAS_A1+ve	22	Sensor B I+
SLW_BIAS_A1-ve	4	Sensor B I-
SLW_BIAS_A1 shld	6(B3)	Shield
SLW_BIAS_A2 +ve	5	Sensor B V+
SLW_BIAS_A2 -ve	24	Sensor B V-
SLW_BIAS_A2 shld	23(B3)	Shield
SLW_JFETV_A1 +ve	25	-
SLW_JFETV_A1 -ve	7	-
SLW_JFETV_A1 shld	6(B3)	-
SLW_JFETV_A2 +ve	8	Resistor A I+
SLW_JFETV_A2 -ve	27	Resistor A I-
SLW_JFETV_A2 shld	6(B3)	Shield
SLW GND WIRE_A	6(B3)	JFET Chassis
SSW_BIAS1_A +ve	28	Resistor A I+
SSW_BIAS1_A –ve	10	Resistor A I-
SSW_BIAS1_A shld	9(C3)	Shield
SSW_JFETV1_A +ve	11	Resistor A V+
SSW_JFETV1_A -ve	30	Resistor A V-
SSW_JFETV1_A shld	29(C3)	Shield
SSW GND WIRE_A	12(C3)	JFET Chassis
SSW_BIAS2_A +ve	13	Resistor B I+
SSW_BIAS2_A –ve	32	Resistor B I-
SSW_BIAS2_A shld	31(C3)	Shield
SSW_JFETV2_A +ve	33	Resistor B I+
SSW_JFETV2_A -ve	15	Resistor B I-
SSW_JFETV2_A shld	14(C3)	Shield
S_HEATER GROUND A	NC	JFET Chassis
SLW_JFET_HEATER_A +ve	17	Resistor B V+
SLW_JFET_HEATER_A -ve	36	Resistor B V-
SLW_JFET_HEATER_A shld	18(D3)	Shield