SUBJECT: Board Report for the DPU **DDR**

PREPARED BY: K.J. King

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Distribution

1. INTRODUCTION

This Detailed Design review was held at IFSI on the 6th-7th December 2001. The review was based on the documentation package provided by IFSI at that time (see below) with presentations provided on selected documents

Members of the Board were:
K.J. King (Chairman)
D. Griffin
A. de Jonge

Also in attendance:
R. Orfei
R, Cerulli
S. Molinari

1.1 Documentation

The following table gives the filenames of the documents that were reviewed.

DPU CPU Board Specification(DPU-SP-CGS-001_Issue1)_OK.PDF
DPU-ICU_Development_Plan_(Issue1_3)OK.PDF
DPU-ICU_ESD_Control_Procedure_Issue11_OK.PDF
DPU_AIV&Test_plan_(Issue1)OK.PDF
DPU_Boot_Software_Architectural_Design_Document_(DPU-AD-CGS-001_Issue1)OK.PDF
DPU_Boot_Software_Software_Requirements_(DPU-SQ-CGS-001_Issue2)OK.PDF
DPU_CL_DPL-ML_Lists_(Issue1_0)OK.PDF
DPU_Communication_Matrix_Issue1.PDF
DPU_Configuration_Status_List_(Issue1)OK.PDF
DPU_DC-DC Board_Specification_(DPU-SP-CGS-004_Issue1)OK.PDF
DPU_ICD_(Issue1_0)OK.PDF
DPU_Interface_Board_Specification_(DPU-SP-CGS-002_Issue1)OK.PDF
DPU_Motherboard_Specification_(DPU-SP-CGS-005_Issue1)OK.PDF
DPU_PAplan_Issue1.PDF
DPU_Subsystem_Specification_Document_(Issue1_2)OK.PDF
OBS_Logical_Model_OK.PDF
OBS_PA_Plan_Issue10_OK.pdf
OBS_Software_Specification_Document_(Draft01)OK.PDF
OBS_URD_(Issue1)OK.PDF

1.2 General Summary

Hardware: The board is generally satisfied that the design will meet the requirements as specified in the SSD, however there are a several areas where we would like to see an analysis/justification of the design choice. These are given as actions in the following report.

Software: The board is accepts that the proposed design is likely to meet the basic requirements of the OBS, however, we cannot confirm the acceptability of the software design as presented because

a) there is not a full set of software requirements,
b) there is not a fully documented design (only a presentation) and
c) there has been no apparent verification that the design meets the available software requirements.

In general the OBS documentation needs to be generated so that the design can be reviewed.

There is an additional concern that OBS production has already started (for HIFI) which will constrain SPIRE to accept an OBS architecture not optimised for the SPIRE instrument.

DDR Status
For documentation, general comments will be collected by the board and issued as a RID on the current version of the document and provided to IFSI. Provided no other items are outstanding, the updated document will be issued.

Once all actions are completed the DRR can be considered completed

2. MEETING MINUTES

2.1 Subsystem Specification Document

Comments on the documentation/presentation

- Remove requirements FUN-04 and FUN-05 as they dare not on the DPU
- Update requirement FUN-06 - to handle the max data rate non-burst mode
- FUN-08 – Note: current estimate of the power consumption is 18W (5W idle)
- DES-04 – IFSI want to change this requirement to remove the maintenance function as this will be provided by the application program held in RAM. However this means we could, in principle, upload a patch, which stopped us updating the program for ever. This could be avoided if the PROM software stopped before executing the application program to allow uplink of new code.
- DES-09 – This requirement is not possible to meet - IFSI wish to rephrase this to 'shall generate less than 1 soft bit error per year'. There is at present no justification for this being adequate replacement for EDAC
- DES-10 - delete
- DES-11 - needs rephrasing - check all memory (data, EEPROM, programme), allow uplink of program even if memory checks are OK (to allow patching a system that does not work)!!
- DES-19 – The DPU will not measure the DPU input current - this is measured by the S/C
- The channels measured by the DPU are not documented - these should be in the DPU ICD
- DES-33 - refer to IID Part A specs
- Figure 1.2 needs updating to show two DC/DC converter boards
- Interrupt levels mean that command interrupt is higher than 1553 subframe interrupt – therefore the clock may be delayed by up to 1ms – it is not clear if this is adequate.
- There is a need for two TC buffers - for immediate and non-immediate commands. The TC interrupt routine has to copy the TC into the correct buffer but it is not clear if this is reflected in the architectural design.
- It is not clear that the DPU automatically switches between 1553 bus A and B as controlled by the CDMS.
- Check Mass budget has been updated - IFSI to send updated interface Control Drawing - movement of bonding stub, change to mass (before Christmas)
- No thermal analysis of DPU has been done - design maximises heat flow to the box feet
- Risk analysis of motherboard failing and killing both DPUs - a single point failure - not in FMECA

Board Recommendations

- Update documentation as outlined above
- Propose a modification to BSW to allow uplink of program even if memory checks are OK before starting execution of the application program (to allow patching a system that does not work).

- Provide a justification for not using EDAC and accepting an error rate of one soft bit error per year per DPU - this is not covered in FMECA
- Clarify whether interrupts are hardwired or not? – it is not clear if assigned priorities are correct and will meet the timing/clock requirements (We believe that the interrupts are hardwired but it is possible to change priority of ISR3 in the interrupt controller and can mask any interrupt)
- The architectural Design should indicate how the two types of TC (immediate and not-immediate) are handled.
- No thermal/mechanical analysis of DPU has been provided, nor any other justification of thermal design – the current design maximises heat flow to the box feet
- A risk analysis should be performed of the possibility of a single point failure on the motherboard causing both Prime and Redundant DPUs to fail.

2.2 FMECA

Comments on the documentation/presentation

- Add loss of commanding to Serial interface failures
- Update S/C I/F failures to cause switch to 1553 bus B
- Add that an error in the EEPROM generates an event packet
- Risk analysis of motherboard failing and killing both DPUs - a single point failure - not in FMECA

Board Recommendations

- Provide a risk analysis of the possibility of a single failure on the motherboard causing both Prime and Redundant DPUs to fail.

2.3 On-Board Software

Comments on the documentation/presentation

- The OBS design uses global memory to pass information between tasks. This needs to be justified or documented according to PA plan
- It is noted that there could be several ms jitter on the time of requesting housekeeping parameters due to interupts by a VM program. This is not expected to be important
- There is a need to clarify how more than one task, in parallel, may use the LS_Task to send and receive responses to/from the DRCU. In particular it is not clear how a VM may interrupt the reception of a housekeeping parameter without the two tasks receiving the wrong data
- It is not clear how DPU frames will be combined into a DPU packet. This apparently needs a new TM buffer fed by ISR_3_Task
- Documentation of architectural design is currently in several presentations, and notes, but no sinfle document
- There is no documentation of the VM characteristics and language - RC offered to provide a compiler plus a simulator of the VM
- Monitoring for autonomy should be in a different task (not the idle task)
- The idle task should handle the watchdog
- The LS_TASK should always check for a response from DRCU, when necessary. Currently it is not defined how a missing response would generate an event packet and autonomous action.
- The OBS should check data from FIFOs is in the expected format before copying into a TM packet
- Clarify how shared data areas are protected
- A consistent naming convention should be used (e.g. for signals)
- The URD needs to be updated

Board Recommendations

- Update documentation as outlined above
- The current note on the DPU Architecture should be updated and issued as an Architectural Design Doc, including Sergio's information on the OBS.
- Make verification matrices of URD-SRD-AD

2.4 Development Plan

Comments on the documentation/presentation

- DRCU Simulator delivery to IFSI is now in January
- Hardware testing is ongoing
- 3rd set of boards will be delivered from CGS on 25th Jan
- 3 sets of test equipment will be available from end of January
- It is not clear if Anna will be available from the end Jan
- There is a need to identify what functionality is required for the April delivery. It is possible to have two or more delivery dates for different versions of the AVM OBS
- Authorisation to Proceed with manufacture is due 16th Jan 2002 (depends on ECP being ready)
- Environment testing will be at Alenia - will be confirmed after ATP. IFSI want to do EMC test along with DRCU. This needs to be arranged
- QMs will take 3.5 months to produce if there are no changes to AVM design
- Schedule does not reflect the real position
- OBS Schedule does not reflect true position
- Delivery of SPIRE MIB is due 12th February

Board Recommendations

- The document needs to be updated to reflect the real process of development, plus intermediate deliveries of OBS for AVM
- IFSI should identify quickly the need for EMC testing with the DRCU

2.5 AIV Plan

Comments on the documentation/presentation

- Plan does not include OBS integration and test
- It is not clear which low-level tests are included in each high-level test.

Board Recommendations

- Update documentation as outlined above

2.6 PA Plans

Three documents were available:
DPU/ICU PA Plan
OBS PA Plan
CGS PA Plan (RO to send to RAL - this is first issue for comments)

Board Recommendations

- Code reviews must be held to check adherence to the PA plan for coding standards to conform to ESA guidelines - as this is not provided any other way

- There is no information about configuration control for VIRTUOSO and other associated tools.
- References should be made to space qualification of the OS and the development environment

2.7 URD

Not presented

- RIDS will be submitted to IFSI to update the document

2.8 DPU ICD

- RIDS will be submitted to IFSI to update the document
- Interface Control Drawings are to be provided/updated

3. ACTIONS

Action ID	Actionee	Description
DPUDDR-01	IFSI	To update the Subsystem Specification Document according to review board observations
DPUDDR-02	IFSI	To propose a modification to the BSW to allow uplink of program even if memory checks are OK before starting execution of the application program (to allow patching a system that does not work).
DPUDDR-03	IFSI	To provide a justification for not using EDAC and accepting an error rate of one soft bit error per year per DPU
DPUDDR-04	IFSI	To clarify whether interrupts are hardwired or not and how the design will meet the timing/clock requirements
DPUDDR-05	IFSI	To provide a justification of the thermal design (thermal analysis)
DPUDDR-06	IFSI	To update the FMECA according to review board observations, including a risk analysis of the possible single point failure on the motherboard causing both Prime and Redundant DPUs to fail.
DPUDDR-07	IFSI	To provide an OBS Design Document based on the current note, the presentations given and the board comments
DPUDDR-08	IFSI	To provide a VM design document and user manual
DPUDDR-09	IFSI	To provide a VM simulator and compiler
DPUDDR-10	IFSI	To update the URD and SSD according to comments provided, including verification matrices of URD-SRD-AD
DPUDDR-11	IFSI	To update the Development Plan to reflect the real process of development, plus intermediate deliveries of OBS for AVM
DPUDDR-12	IFSI	To contact CEA with respect to the need for EMC testing with the DRCU and propose a plan for EMC testing
DPUDDR-13	IFSI	To update the AIV Plans according to review board observations
DPUDDR-14	IFSI	To update the OBS PA Plan according to review board observations
DPUDDR-15	IFSI	To update the OBS URD according to review board observations and RIDS
DPUDDR-16	IFSI	To update the DPU ICD according to review board observations and RIDS