HERSCHEL/SPIRE

DETECTOR CONTROL UNIT
BIAS
TEST PLAN

BIAS BOARD Number:1

	Function	Name	Date	Visa
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DOCUMENT STATUS and CHANGE RECORD

Date	Issue	Affected pages
9/3/2001	0.-	Creation

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PICTURES

1 INTRODUCTION

1.1 PURPOSE

The purpose of this document is to detail the tests that have been performed on the BIAS boards. This document follows a specific order: first the success criteria are given, followed by the testing parameters and finally whether the test was successful or not.

1.2 SCOPE

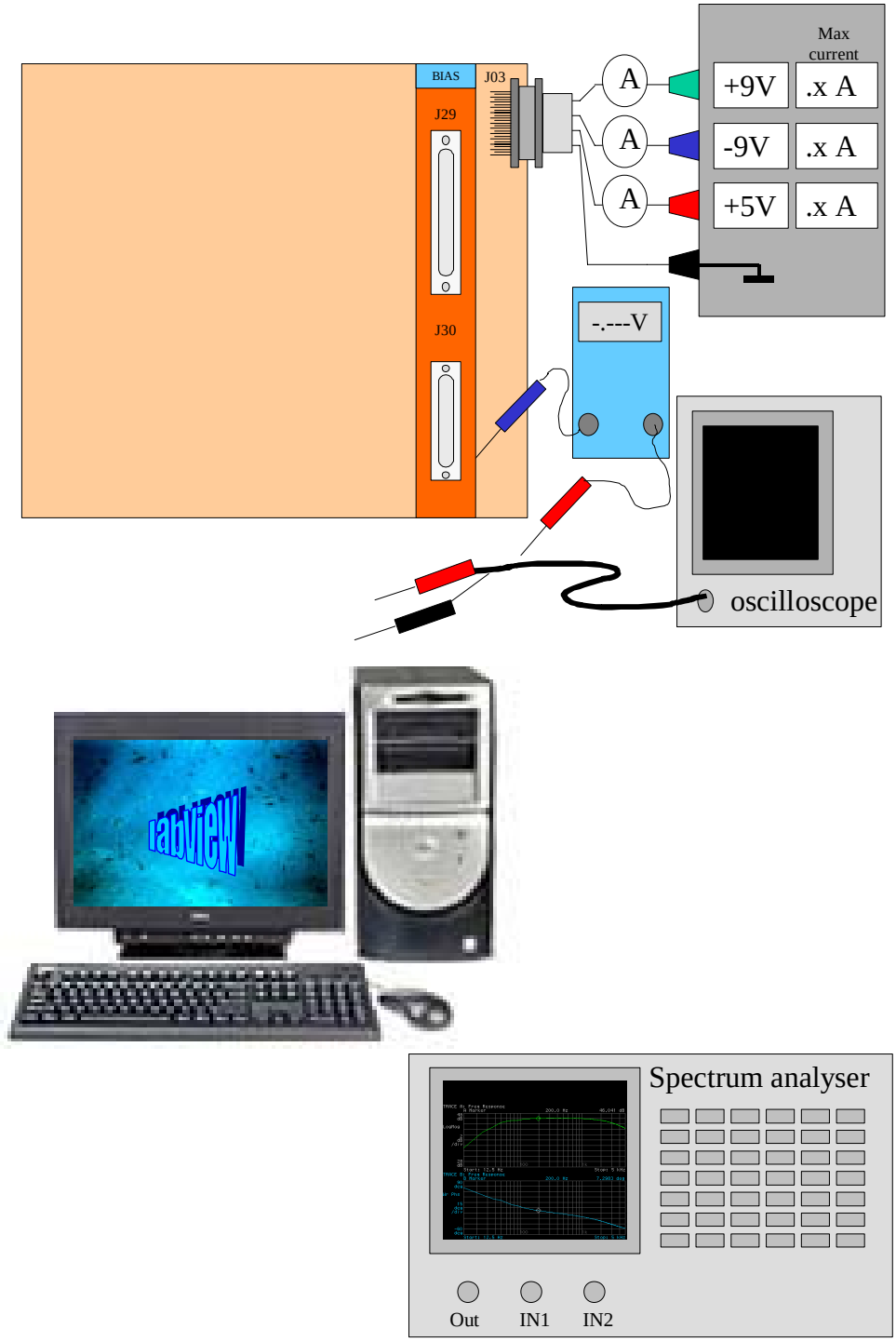
1.3 APPLICABLE DOCUMENTS

1.4 REFERENCE DOCUMENTS

- DETECTOR SUBSYSTEM SPECIFICATION DOCUMENT : FIST-SPI-PRJ-000103
- DRCU SUBSYSTEM SPECIFICATION DOCUMENT : SAp-SPIRE-CCa-25-00

2 GENERAL DESCRIPTION

2.1 OVERVIEW



Picture 2-1: overview

3 TEST EQUIPEMENTS

- DUAL OUTPUT DC POWER SUPPLY	HP E3620A 0-25V 0-1A
- DIGITAL OSCILLOSCOPE	TEKTRONIX 2230
- MULTIMETER	WAVETEK
-2 CHANNEL NETWORK SIGNAL ANALYZER	SRS SR780

4 DCU QM1 ELECTRICAL TESTS

4.1 BIAS test

4.1.1 Visual test

Test number	Test	Test Date	Result	Corrections	Test Status OK/NOK
BIAS_ 1	Check that no components missing and all the component are in the good way.	1/7/02	R172 missing	Add 1ohm resistor For R172	OK
BIAS_ 2	Check that there isn't any visible short circuit	1/7/02	None		OK

BIAS_ 1 BIS	Check that no components missing and all the component are in the good way.	1/7/02	Design error missing the temperature sensor. Error on the footy print of the 37 pins connector S2	**NON CONFORMANCE**	NOK

4.1.2 Test with power supplies

4.1.2.1 Test

Test number	Test	Test check Date	Check Result	Corrections	Test Status OK/NOK
BIAS_ 3	Switch on the lab power Check there is any short circuit.	2/7/02			OK
BIAS_ 4	Measure the static current on +9V (without external loads)	2/7/02	For photometer: 47.8mA For spectrometer:30.6mA		OK
BIAS_ 5	Measure the static current on -9V (without external loads)	2/7/02	For photometer: 36.6mA For spectrometer:20.4mA		OK

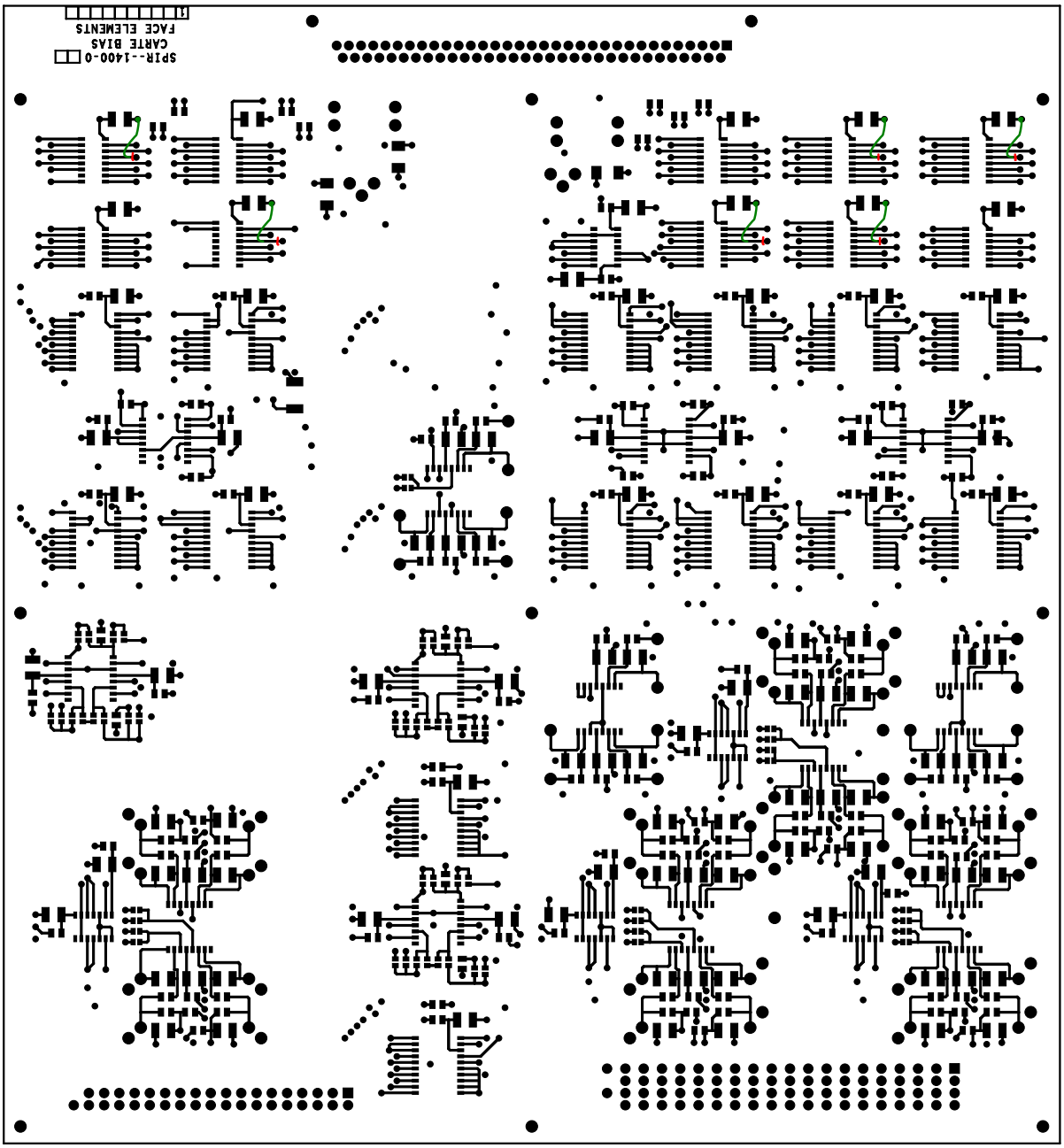
BIAS_ 6.1	Measure the static current on +9V (loaded)	9/7/02	For photometer:114.8 mA For spectrometer:47.7mA		OK
BIAS_ 7.1	Measure the static current on -9V (loaded)	9/7/02	For photometer: 137.6mA For spectrometer:44.4mA		OK

Additional test

Test number	Test	Test check Date	Check Result	Corrections	Test Status OK/NOK
BIAS_3.1	Measure of P9V_P	2/7/02	8.91V		OK
BIAS_3.2	Measure of P9V_P1	2/7/02	8.86V		OK
BIAS_3.3	Measure of N9V_P	2/7/02	-9.23V		OK
BIAS_3.4	Measure of N9V_P1	2/7/02	-9.18V		OK
BIAS_3.5	Measure of P5_P	2/7/02	6.3V NOK **NON CONFORMANCE**	The 15k R262 is replaced by a 1k And the 5k R263 is replaced by three 1k in parallel Then P5_P = 5.03V	OK
BIAS_3.6	Measure of P9V_S	2/7/02	8.91V		OK
BIAS_3.7	Measure of P9V_S1	2/7/02	8.88V		OK
BIAS_3.8	Measure of N9V_S	2/7/02	-9.23V		OK
BIAS_3.9	Measure of N9V_S1	2/7/02	-9.2V		OK
BIAS_3.10	Measure of P5_S	2/7/02	5.6V NOK **NON CONFORMANCE**	The 15k R177 is replaced by a 1k And the 5k R178 is replaced by three 1k in parallel Then P5_P = 5.03V	OK
BIAS_3.11	Power supply for each actif components	2/7/02			OK
BIAS_3.12	Measure of REF5V_P Measure of REF5V_S	2/7/02	5V		OK

NON CONFORMANCE:

Corrections: connect the pin 13 of all 74HC595 to GND instead of P5V.
Red lines = cut (6)
Green lines = new connections (6)



4.1.2.1.1 Jfet Power VDD

Switch ON All JFET power VDD:

Test number	Test	Test check Date	Check Result	Corrections	Test Status OK/NOK
BIAS_ 8	Check with the voltmeter that we have 2.5V on: -All VDD JFET output	3/7/2002 & 9/7/2002	2.45V (with 500ohn resitor between VDD and GND) 2.49V with no load		OK
BIAS_ 9	Load ALL VDD with 500ohm between VDD and GND. And check with an oscilloscope that switching off and on the JFET power doesn't generate any overshoot.	9/7/2002	From 2.45 to 0v in 200µs From 0 to 2.45v in 200µs With no overshoot		OK
BIAS_ 10	Check with the spectrometer that the noise on VDD is <0.3µV/rtHz (2 to 800Hz)	10/7/2002	<200n V/rtHz		OK

Switch OFF All JFET power VDD:

Test number	Test	Test check Date	Check Result	Corrections	Test Status OK/NOK
BIAS_ 11 bis	Check with the voltmeter that we have 0V on: -All VDD JFET output	3/7/2002 & 9/7/2002	0,000V (with 500ohn resitor between VDD and GND) 0.000V with no load		OK

4.1.2.1.2 Jfet Power VSS and Heater

Load all "VSS DAC" and "heater DAC" with "FF"

Test number	Test	Test check Date	Check Result	Corrections	Test Status OK/NOK
BIAS_ 12	Check with the voltmeter that we have -5V on: All VSS and Nhearter output	3/7/2002 & 9/7/2002	-4.96V (with 1K resitor between VSS and GND) (5.01V with no load) NOK for VSS_TC	(VSS_TC) add a connection between pin 20 of U52 and pin16 of U17 connect pin 19 of U52 to REF5V_P instead of SINE_P 3/7/2002	OK
BIAS_ 13	Load ALL VSS and Nhearter outputs with 1000ohm between VSS and GND. And check with an oscilloscope that switching off and on the JFET power doesn't generate any overshoot.	9/7/2002	From -5 to 0V in 300µs From 0 to -5V in 300µs With no overshoot		OK
BIAS_ 14	Check with the spectrometer that the noise on VSS <1µV/rtHz (2 to 800Hz)	10/7/2002	250 nV/rtHz		OK

Load all "VSS DAC" and "heater DAC" with "AA"

BIAS_ 15	Check with the voltmeter that we have –3.33V on: All VSS and Nhearter output	3/7/2002 & 9/7/2002	-1.66V (with 1K resitor between VSS and GND) -1.67V with no load	Bit rotation from lsb to msb (check vhdl)	NOK
		11/7/2002		afterVhdl correction	OK

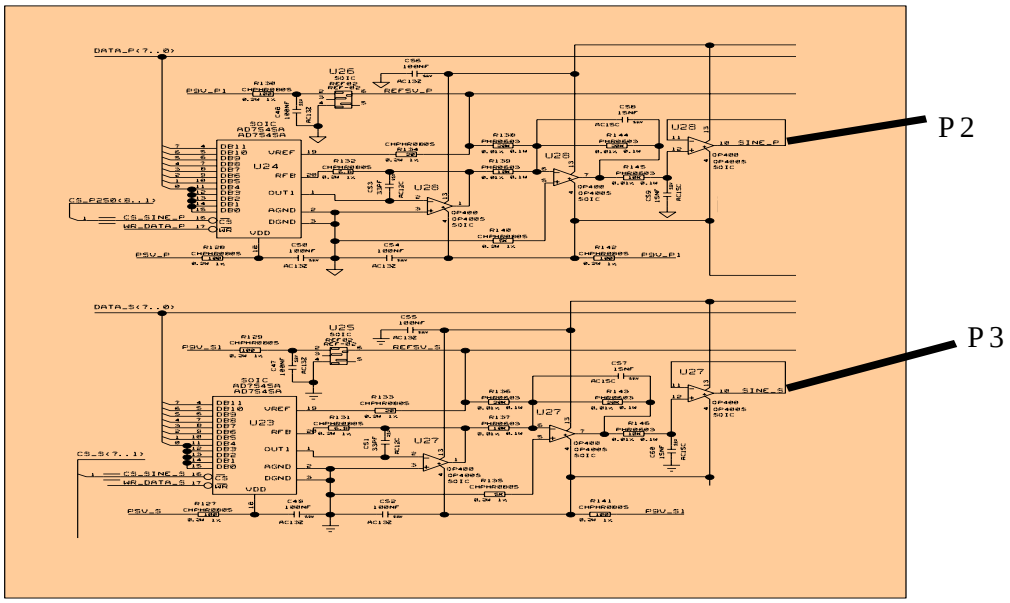
Load all "VSS DAC" and "heater DAC" with "55"

BIAS_ 16	Check with the voltmeter that we have –1.66V on: All VSS and Nhearter output	3/7/2002 & 9/7/2002	-3.29V (with 1K resitor between VSS and GND) 3.33V with no load	Bit rotation from lsb to msb (check vhdl) Vhdl correction 11/7/2002	NOK
		11/7/2002		afterVhdl correction	OK

Load all "VSS DAC" and "heater DAC" with "00"

BIAS_ 17 bis	Check with the voltmeter that we have 0V on: All VSS and Nhearter output		0,000V (with 1K resitor between VSS and GND) 0,000V with no load		OK

4.1.2.1.3 Sine DAC



Load all " sine DAC" with "FE"

Test number	Test	Test check Date	Check Result	Corrections	Test Status OK/NOK
BIAS_ 18	Check with the voltmeter that we have 5V on: - Test point P2 and P3	5/7/2002	0v (7F→ 4.94V)	Bit rotation from lsb to msb (check vhdl)	NOK
		11/7/2002		afterVhdl correction	OK

Load all " sine DAC" with "AA"

Test number	Test	Test check Date	Check Result	Corrections	Test Status OK/NOK
BIAS_ 18	Check with the voltmeter that we have 1.66V on: - Test point P2 and P3	5/7/2002	-1.64v	Bit rotation from lsb to msb (check vhdl)	NOK
		11/7/2002		afterVhdl correction	OK

Load all " sine DAC" with "55"

Test number	Test	Test check Date	Check Result	Corrections	Test Status OK/NOK
BIAS_ 18	Check with the voltmeter that we have –1.66V on: - Test point P2 and P3	5/7/2002	1.64v	Bit rotation from lsb to msb (check vhdl) Vhdl correction 11/7/2002	NOK
		11/7/2002		afterVhdl correction	OK

4.1.2.1.4 ATT DAC

Load all " ATT DAC" with "FF" and all " sine DAC" with "FE"

Test number	Test	Test check Date	Check Result	Corrections	Test Status OK/NOK
BIAS_ 19	Check with the voltmeter that we have 200mV Between each couple PBIAS and NBIAS	5/7/2002	187.4mV (sine DAC with 7F)	Bit rotation from lsb to msb (check vhdl)	OK

Load all " sine DAC" with "AA" and all " sine DAC" with "FE"

BIAS_ 19	Check with the voltmeter that we have 133mV Between each couple PBIAS and NBIAS	5/7/2002	62.9mV	Bit rotation from lsb to msb (check vhdl)	OK

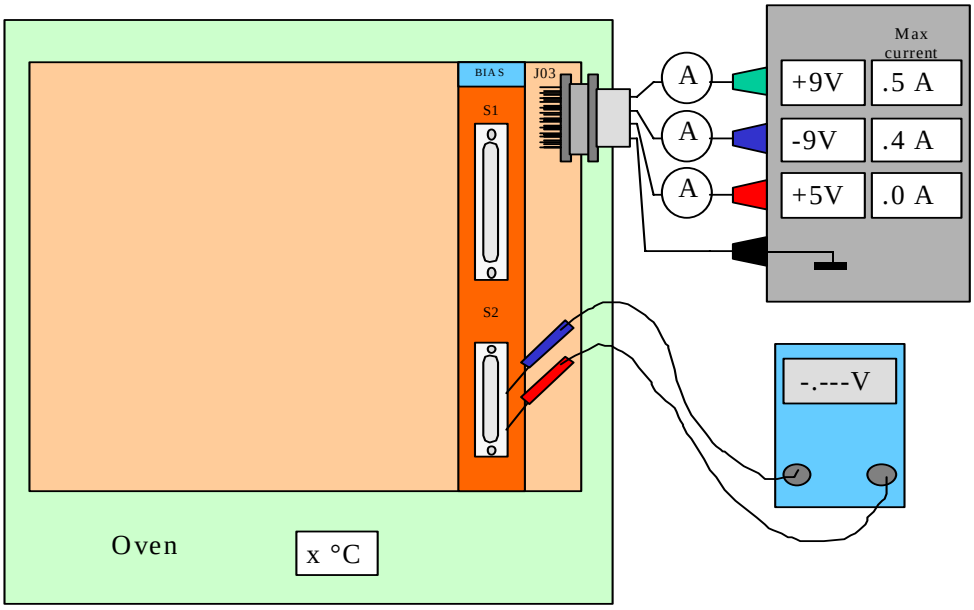
Load all " sine DAC" with "55" and all " sine DAC" with "FE"

BIAS_ 19	Check with the voltmeter that we have 66mV Between each couple PBIAS and NBIAS	5/7/2002	124.5mV	Bit rotation from lsb to msb (check vhdl)	OK

Load all " ATT DAC" with "FF" and run the sine mode

Test number	Test	Test check Date	Check Result	Corrections	Test Status OK/NOK
BIAS_ 20	Measure all the output signal harmonic FOR a frequency of 50Hz (186)	12/7/2002	50Hz: -24dBVrms 150Hz: -85dBVrms 12,8kHz: -90dBVrms		
BIAS_ 20	Measure all the output signal harmonic FOR a frequency of 200Hz (61)		200Hz: -24dBVrms 600Hz: -90dBVrms 51,2kHz: -85dBVrms		
BIAS_ 20	Measure all the output signal harmonic FOR a frequency of 300Hz (41)		300Hz: -25,6dBVrms 900Hz: -95dBVrms 76,8kHz: -85dBVrms		

4.1.2.1.5 BIAS and JFET power TEMPERATURE STABILITIE



Load all DAC with "7F"

Measurement at 0°C

Test number	Test	Test check Date	Check Result	Corrections	Test Status OK/NOK
BIAS_ 21	For VDD Measure with a voltmeter all the output voltage				
BIAS_ 21	For VSS Measure with a voltmeter all the output voltage				
BIAS_ 21	For HEATER Measure with a voltmeter all the output voltage				
BIAS_ 21	For BIAS Measure with a voltmeter all the output voltage				

Measurement at 20°C

Test number	Test	Test check Date	Check Result	Corrections	Test Status OK/NOK
BIAS_ 21	For VDD Measure with a voltmeter all the output voltage				
BIAS_ 21	For VSS Measure with a voltmeter all the output voltage				
BIAS_ 21	For HEATER Measure with a voltmeter all the output voltage				
BIAS_ 21	For BIAS Measure with a voltmeter all the output voltage				

Measurement at 40°C

Test number	Test	Test check Date	Check Result	Corrections	Test Status OK/NOK
BIAS_ 21	For VDD Measure with a voltmeter all the output voltage				
BIAS_ 21	For VSS Measure with a voltmeter all the output voltage				
BIAS_ 21	For HEATER Measure with a voltmeter all the output voltage				
BIAS_ 21	For BIAS Measure with a voltmeter all the output voltage				

5 TRACEABILITY MATRIX

Requirement ID	Description	Test
BDA-DRCU-05	The DRCU is to provide 5 BDA bias signals, adjustable from 0 to 200 mV_{rms}, and 1 bias signal for temperature readout, adjustable from 0 to 500 mV_{rms}. The temperature readout biases are to be divided from a common oscillator. Each bias shall be adjustable with 8-bit precision. The frequency of each bias shall be adjustable between 50 and 300 Hz, with a precision of 5 Hz.	BIAS_ 18 BIAS_ 19 BIAS_ 20
BDA-DRCU-06	The DRCU will provide 15 commandable JFET source voltages with 256 levels. The range of Vss is from 0 V to –5 V.	BIAS_ 12 BIAS_ 15 BIAS_ 16
BDA-DRCU-07	Vdd is to be adjustable from 1.5 to 4 V.	BIAS_ 8
BDA-DRCU-08	Vdd and Vss lines individually must source 1 mA to 5 mA. Noise on Vss < 1 $\mu V/\sqrt{Hz}$, and noise on Vdd < 0.3 $\mu V/\sqrt{Hz}$ within modulated band (50 – 300 Hz), measured at the DRCU DxMA connector.	BIAS_ 10 BIAS_ 14
BDA-DRCU-09	Each of the 15 Vdd and Vss supplies must be commandable ON/OFF for spectrometer and photometer independently, without overshoot. Each Vdd and Vss pair are turned on and off together.	BIAS_ 9 BIAS_ 13
BDA-DRCU-10	The DRCU will provide 2 double-wired JFET heater lines with adjustable amplitude and duration. The supplies must be able to provide 5 V and 25 mA (photometer), 3 V and 10 mA (spectrometer). Each heater line is commandable ON/OFF, with a minimum duration of 10 s.	BIAS_ 12