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Herschel

DPU/ICU Power Budget

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2.1	Added FPGA power drain and changed partial totals and total power
2.2	Modified FPGA power drain and total power
2.4	Updated DPU power drain figures
2.4	Updated FCU power figures

1 INTRODUCTION

1.1 Purpose of the document

The Istituto di Fisica per lo Spazio Interplanetario (IFSI) of the Italian Consiglio Nazionale delle Ricerche (CNR) is responsible for the design and manufacturing of the three Digital Processing/Instrument Control Units for the three instruments to be flown on board of the ESA satellite Herschel Space Observatory: PACS, HIFI and SPIRE.

This documents shows the power budget of the DPU/ICU for the three instruments.

It is to be taken into account that for SPIRE and PACS the power budget is related to the DPU internal supply only, while for the HIFI instrument a dedicated DC/DC converter powers also the HIFI subsystem called Focal plane Control Unit.

1.2 Acronyms and Abbreviations

1.2.1 Acronyms

AD	Architectural Design
ATP	Acceptance Test Plan
ASI	Agenzia Spaziale Italiana (Italian Space Agency)
AVM	Avionic Model
CGS	Carlo Gavazzi Space
CNR	Consiglio Nazionale delle Ricerche
CPP	Coordinated Parts Procurement
CPU	Control Processing Unit
CDMS	Central Data Management System
CMOS	Complementary Metal Oxide Silicon
CGS	Carlo Gavazzi Space SpA
CQM	Cryogenic Qualification Model

DDD	Detailed Design Document
DM	Data Memory
DPU	Digital Processing Unit
EEPROM	Electrically Erasable Programmable Read Only Memory
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
ESA	European Space Agency
FCU	Focal plane Control Unit
HK	HouseKeeping
HSO	Herschel Space Observatory
HW	HardWare
IBDR	Instrument Baseline Design Review
ICD	Interface Control Document
ICDR	Instrument Critical Design Review
ICU	Instrument Control Unit
DPU	Digital Control Unit
IHDR	Instrument Hardware Design Review
IFSI	Istituto di Fisica dello Spazio Interplanetario
ISVR	Instrument Science Verification Review
NA	Not Applicable
OBS	On-Board Software
PA	Product Assurance
PM	Program Memory
PROM	Programmable Read Only Memory
RAM	Random Access Memory
SCC	SpaceCraft Components
SEU	Single Event Upset
SPIRE	Spectral and Photometric Imaging Receiver
S/S	SubSystem
SVM	Service Module
SW	Software
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
TV	Thermal Vacuum

1.3 REFERENCES

1.3.1 Applicable Documents

Document Reference	Name
AD1	FIRST/Planck Instrument Interface Document Part A
AD2	FIRST/Planck Instrument Interface Document Part B Instrument “PACS”
AD3	FIRST/Planck Instrument Interface Document Part B Instrument “HIFI”
AD4	FIRST/Planck Instrument Interface Document Part B Instrument “SPIRE”
AD5	HIFI ICD

1.3.2 Reference Documents

Document Reference	Name

1.3.3 Introduction

The present document is intended to provide the power budget of the DPU/ICU for the three instruments HIFI, PACS and SPIRE. As already said, part of a section will be dedicated to the HIFI FCU subsystem that is powered by a DC/DC converter resident in the ICU.

The power indicated is mostly drained by CMOS digital integrated circuits for which the power consumption is a function of the switching frequency. For most of the components, then, and especially for the most power hungry ones, the exact power consumption will not be known that after the full software is working, especially the software related to the fast serial data acquisition from the subsystems.

It is recalled that the DPU/ICU box will contain two complete units and that the only common board is the motherboard, where in any case all signals of the two units are completely separated. It is also recalled that all the boards will be designed and manufactured by CGS under a contract CGS-ASI.

Each unit will consist (besides the single motherboard) of:

- CPU board
- Interface board
- DC/DC Converter board.

It is also recalled that, in the case of HIFI, one DC/DC converter board will contain two DC/DC converters: one converter for the ICU and one converter for the FCU. In the other cases, i.e. for SPIRE and PACS the nominal (or prime) DC/DC converter board and the redundant DC/DC converter board will host only the converter for the DPU.

2 DPU/ICU Power breakdown

2.1 CPU board power breakdown

In the following table the CPU board power breakdown is shown.

HSO/FIRST-DPU: CPU Board Power Budget [Watt]								
Item	**+5V & 2.5V**		**+15V**		**-15V**		**Duty cycle %**	**Power Supply**
	Nominal	**Peak**	**Nominal**	**Peak**	**Nominal**	**Peak**	**Nominal**	**Nominal**
DSP	1,5	2	0	0	0	0	100	**1,5**
DPR	2	3,2	0	0	0	0	10	**0,2**
TSS901	0,6	1	0	0	0	0	10	**0,06**
SRAM @1MHz	6	6	0	0	0	0	80	**4,8**
EEPROM	0,1	0,5	0	0	0	0	100	**0,1**
Glue logic	1	1	0	0	0	0	80	**0,8**
FPGA	0,125	0,25	0	0	0	0	100	**0,125**
Total	**11,32**	**13,95**	**0**	**0**	**0**	**0**		**7,58**

The power budget is strongly depending on the duty cycle of the various components, but the final power figure can be considered close to the actual one, approaching 7.6 W at the secondary power lines.

2.2 Interface board power breakdown

In the following table the interface board power breakdown is shown.

HSO/FIRST-DPU: PL I/F Board [Watt]								
Item	**+5V**		**+15V**		**-15V**		**Duty cycle %**	**Power Supply**
	Nomin.	**Peak**	**Nomin.**	**Peak**	**Nomin.**	**Peak**	**Nomin.**	**Nomin.**
BU61582	0,7	1,2			3,45	3,825	100	**4,15**
FIFO	0,09	9,9					100	**0,09**
RS422 Receiv.	0,3	0,4					80	**0,24**
RS422 Transm.	0,9	1					80	**0,72**
Analog Section	0,15	0,2	0,111	0,181	0,33	0,535	40	**0,23**
Glue logic DC	1	1					80	**0,8**
Glue logic AC	0,4	0,6					80	**0,32**
FPGA	0,125	0,25					100	**0,125**
	3,66	**18,15**	**0,111**	**0,181**	**3,78**	**4,36**		**6,67**

The power budget is strongly depending on the duty cycle of the various components, and the final power figure can not be considered close to the actual one (with the exception of PACS, as explained later on), as the duty cycle of various components in not well defined yet and it is very much depending on the FIFO use, i.e. the data gathering on the fast serial links from the subsystems to the DPU.

It is to put in evidence that the FIFO are present only in HIFI and SPIRE that have the same monodirectional fast serial links, while in the case of PACS the serial links among the various subsystems are according to the MIL-STD 1355 DS-DE. In the PACS case this standard high speed serial circuit is implemented by a special chip (TSS901) whose peak power drain is 1 W and it is located in the CPU board.

In strict terms, as this chip is not used (and not mounted!) in the case of SPIRE and HIFI, the estimated 0.06 W can be taken out from the CPU power breakdown for these two instruments.

2.3 Power losses breakdown

In the next table the estimated power losses are shown for the various DC/DC converter components. These power losses ca be considered close to the actual ones and hence the 70% efficiency of the DC/DC converters will be likely achieved.

Item	Voltage	Current	Rect losses	Switching losses	Postregulation losses	Control losses	Total losses	Power	Efficiency
Main bus	28			1,47			1,47		70,4%
Out 1	5	3,00	2,40				2,40	15,00	
Out 2	15	0,15	0,12		0,45		0,57	2,25	
Out 3	15	0,15	0,12		0,45		0,57	2,25	
Startup	12	0,02				0,56	0,56		
Self supply	15	0,10				1,50	1,50		
Snubber				0,74			0,74		
Transformer				0,39			0,39		
HIFI option									
Main bus	28			1,47			1,47		70,7%
Out 1 reg	5	0,20	0,16		0,40		0,56	1,00	
Out 2 reg	16	0,50	0,40		1,00		1,40	8,00	
Out 3 reg	16	0,50	0,40		1,00		1,40	8,00	
Out 1	8	0,05	0,04		0,15		0,19	0,40	
Out 2	18	0,08	0,06		0,24		0,30	1,44	
Out 3	18	0,08	0,06		0,24		0,30	1,44	
Self supply	15	0,10				1,50	1,50		
Snubber				0,74			0,74		
Transformer				0,41			0,41		

Main bus switching losses = primary mos

Snubber switching losses = primary snubber

Transformer switching losses = 98% of delivered power

Posregulation losses = 2V (1834); 3V (LM117)

2.4 Total power budget

In the following table all the figures are shown leading to the overall power budget for the three instruments.

	Power1 (W)	Power2 (W)	Total (W)
PACS DPU	14.2	20.3	**25.4**
SPIRE DPU	14.2	20.3	**25.4**
HIFI ICU	14.2	20.3	**25.4**
HIFI FCU	23.8	34	**42.5**

Power1 : the power drained on the secondary power lines.

Power2: the power drained on the primary power lines (+ - 28 V) including a DC/DC converter efficiency of 70%.

Total: The total power including a contingency of 25%.