SPIRE DRCU Programme Review

4 March 2003, SAp, Saclay

Review Board Report

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1. Review objectives and organisation

1.1 Objectives

The objectives of this review were:

- (i) to close out the DRCU Documentation Review, with special attention to interfaces;
- (ii) to review the DRCU development plan and schedule with respect to the instrument delivery schedule, with the aim of maintaining on-time delivery of the instrument PFM;
- (iii) to demonstrate that the risks associated with the warm electronics programme are understood and can be controlled;
- (iv) to examine and set in place the necessary resources and management/communication practices to allow the development plan to be effectively implemented;
- (v) to prepare for and cover most relevant issues for the instrument IHDR (which should then be rather routine for the DRCU).

1.2 Participants and Review Board

The list of participants in the review is given in Annex A. The Review Board comprised

Cardiff University	SPIRE PI
RAL	SPIRE Hardware Project Manager
RAL	SPIRE Instrument Scientist
RAL	SPIRE System Engineer
IFSI	DPU Design Engineer
ESA, ESTEC	SPIRE Instrument System Engineer
ESA, ESTEC	Electronics Engineer
CNES	
CNES	
PPARC	UK Herschel/Planck Programme Director
Leicester University	Independent expert
SRON, Groningen	Independent Expert *
	Cardiff University RAL RAL RAL IFSI ESA, ESTEC ESA, ESTEC CNES CNES PPARC Leicester University SRON, Groningen

* Owing to domestic problem, Kees Wafelbakker was unable to attend the review meeting.

1.3 Review format

The review documentation package was issued on 19 February. The list of documents is attached as Annex B. The documents are available in the SPIRE area on *Livelink*. The review meeting, involving presentations, questions and answers, and meeting of the Review Board, was held on March 4 at SAp, Saclay. The review presentations are given in Annex C.

2. Review Board conclusions

2.1 Summary and recommendations

- 1. The Board was very impressed by the excellent progress made by the DRCU team since the IBDR, and was particularly pleased to note:
 - the thoroughness and high standard of the documentation;
 - the detailed thermal, mechanical and electrical modelling work presented;
 - the progress made in developing and testing the DCU EM.

Whilst the remainder of this report is mainly about problem areas, these achievements and successes are fully acknowledged.

2. A number of detailed technical comments have been made in the course of the documentation review that has been taking place prior to the meeting. The current status of these is summarised in Annex D Additional technical comments were made in the course of the review meeting, and are summarised in Section 3 below. These points should be addressed as part of routine work, and a consolidated summary

prepared for the IHDR. CEA and the SPIRE Project Team are expected to close out the documentation review formally prior to the IHDR.

3. The Review Board is greatly concerned that the current DRCU schedule is not compatible with an ontime delivery of the SPIRE instrument. Several scenarios were presented and considered during the review. These schedule scenarios need to be analysed in further detail, in particular the boundary conditions, the underlying assumptions and the risks involved need to be critically assessed. All efforts should be made to retain the Instrument FM and CQM delivery dates. Decoupling of the QM and FM programmes may be unavoidable for the DRCU (as is already being done in other areas of the Hershcel/Planck project), and the associated risks need to be assessed.

The Board notes that the different scenarios do not diverge until the middle of 2003. It is recommended that the issue is fully reviewed and understood well before the SPIRE IHDR in July, to be able to close it during that review.

- 4. The late availability of the PSU is a matter of serious concern, both from the schedule point of view and because it poses technical risks in that any system-level problems associated with the compatibility of the PSU with the rest of SPIRE would arise very late in the programme. The Board recommends that CEA examine, as a high priority, the possibility of procuring a second PSU Engineering Model that could be delivered to RAL for use in instrument tests.
- 5. SPIRE is a very sensitive instrument with extremely low noise levels and a long cable harness between the FPU and the warm units. The Board did not see evidence that all possible measures are being taken to ensure that the DRCU and the rest of the system it will meet the specification. This incorporates system issues, not just DRCU design aspects. In the context of the DRCU programme, the Board recommends that:

(i) a breadboard test of the DRCU EMC susceptibility be considered;

(ii) the PSU specification be extended (probably in consultation with the selected contractor) to incorporate a more detailed treatment of its noise performance.

- 6. The worst case analysis has not been done for all parts of the system. Eliminating or delaying part of the analysis to a later stage increases risk. The status and CEA policy with respect to the WCA should be clearly stated and justified at the IHDR.
- 7. It is recognised that in obtaining and maintaining the necessary staff resources to implement a programme such as this, the availability of specialised skills and key individuals can be a significant limitation, in addition to financial considerations. The Board recommends that the DRCU team plans actively to ensure the future availability of key staff to the maximum extent possible.
- 8. The Board assesses the success of the review with respect to the stated objectives as follows:

	Objective	Assessment
i	Close out the DRCU Documentation Review, with special attention to interfaces	Achieved, with various minor issues to be addressed as normal work.
ii	Review of the DRCU development plan and schedule with respect to the instrument delivery schedule, with the aim of maintaining on-time delivery of the instrument PFM.	In progress, and remains a high priority for the period between now and the IHDR. Close-out before the IHDR is needed.
iii	Demonstration that the risks associated with the warm electronics programme are understood and can be controlled.	In progress, and remains as a high priority for the IHDR
iv	Examine and setting in place the necessary resources and management/communication practices to allow the development plan to be effectively implemented	Resources are limited at CEA and LAM, and within the SPIRE Project Team. Communications between the teams are now happening in a more effective manner than in the past, and it will be important to maintain this.
v	Preparation for and coverage of the most relevant issues for the instrument IHDR (which should then be rather routine for the DRCU).	Largely achieved - at the IHDR, the schedule/ programmatic issues will be at the forefront.

2.2 List of technical issues

- 1. It appears from the documentation that the effect of the input current noise in the source impedance has not been included in the noise analysis. According to the MAT-02 data sheet, the noise, at 0.25 mA Ic, is about 1.5 pA Hz^{-1/2}. Theoretically it should be 0.4 pA Hz^{-1/2}. From a practical point of view, it could be measured: with a small source resistance, the measured value is voltage noise; for a larger value, it is the Johnson noise of the resistor; and for a very large value it is the current noise.
- 2. From the DCU design document, the noise from the final amplifiers after the multiplexing also looks to be non-compliant. The analysis on p.75 of the DCU Design Document is not clear on this point.
- 3. A PSU configuration that tends to inject noise back to main bus rather than towards the unit is appropriate in this application the adoption of such a configuration should be discussed with the PSU provider.
- 4. The manner in which the JPL detector requirements are apportioned in the design and converted to PSU specifications is not detailed in the documentation. A technical note should be produced for the IHDR giving proof by analysis that the DRCU design plus the PSU spec will result in a system that will meet the requirements.
- 5. Because of the multiplexing, inter-channel interference may occur. To achieve 16-bit resolution, this needs to be tested, by comparing the measurements on one channel when the immediately preceding channel is switched from minimum to maximum. A small amount of interference can be compensated.
- 6. It is recommended that RC filters be incorporated on the inputs of the MAT-02 amplifiers. This will give added ESD protection and also filter out high frequency interference above the frequency where the common mode rejection of the amplifier drops. A possible approach would be to add 100 Ω in series with each input and 100 pF behind each 100 Ω to ground. Filter connectors can also be considered. Filter connectors may be long-lead-items and so if foreseen should be ordered early.
- 7. The electrical system is vulnerable to noise on the bias generators and on the JFET supplies, and these are issues which should be addressed, either by analysis or test. There should be a specification agreed between CEA and JPL for the noise on the JFET bias supplies.
- 8. The sensitivity of the signal chain to noise from the DC-DC converters does not seem to have been quantified. Therefore any specification put on the converters must be a guess. Whatever is specified for the converters, the electronics should be tested against this, or alternatively, tests on the electronics should drive the converter specification
- 9. With the long cable harness between the DRCU and the focal plane, interference is a big issue. This has to be looked at from a system point-of-view, and the DRCU is only a part of this. There are three main sources of noise: low frequency magnetic pickup, radiated RF and conducted structure noise. Shields provide very little attenuation of low frequency magnetic fields. The main defence is to keep everything balanced and use twisted pair wiring everywhere (the pitch and evenness of the twisting is important. RF fields have an effect through direct heating of the bolometers or rectification in active devices, which is why filters at the amplifier inputs are important. Structure currents may be the major source of noise. Some analysis should be done, and room temperature testing carried out to get some handle on how effective the protective measures are.
- 10. Any single-point failures which would affect more that small numbers of pixels (~ 10) should be flagged in the FMECA and the associated risk approved at system level.
- 11. The FCU interfaces must not compromise grounding scheme by returning currents along ground lines. All drives must work differentially across power supplies. This was stated during the presentations, but is not clearly indicated in the FCU documentation. Figure 19 in the SCU description could imply otherwise, and this needs clarification.
- 12. The CEA FPU simulator must be ground isolatable to simulate an isolated FPU. It is grounded by attachment to the DRCU.
- 13. Allowing two weeks only for verification of the EM converters is very much success orientated.
- 14. To aid detailed design, particularly by LAM for the MCU, there must be a budget for the temperature drop across the stacked elements through the PSU into the FCU.

- 15. A characterisation is needed of the time delay versus frequency introduced by the electronics chain (analogue chain + mux/digitisation). This will be important to know whether to it take into account for relative SMEC/pixel datation.
- 16. The DPU-DRCU interface clock can be up to 2.5 MHz. Any relevant documentation should be corrected to reflect this.
- 17. There is a large peak in power delivered to the FPU during the cooler recycle. The corresponding peak power in the FCU should be quantified to check that it poses no problem for the thermal behaviour of the unit.
- 18. Additional damping is under consideration for the mechanisms. It is necessary to check whether there will be any appreciable increase in drive power requirements due to the extra damping. If this is significant in the FPU over and above the present power budgets, it may not be acceptable, and might also generate excessive harness dissipation.
- 19. The deletion of the BSM latch is yet to be confirmed by the Project, so the electronics design should not yet assume that.
- 20. Some DCU connectors show Faraday shield pins, but these pins are either 0 V or N/C. The Faraday shield is terminated to DRCU connectors by tails inside backshells to the connector body. The connector section of the DRCU ICD should be prefixed with a note that the HDD is applicable.

3. List of Annexes

- Annex A: List of participants
- Annex B: List of documents provided for the review
- Annex C: Review presentations
- Annex D: Status of technical comments on review documents