SPIRE DRCU Programme Review

4 March 2003, SAp, Saclay

Review Board Report

SPIRE-UCF-REP-001573

Annexes

Annex A

List of Participants

Jean-Louis	Augueres	CEA
Jean-Paul	Baluteau	LAM
Yvan	Blanc	CNES
Christophe	Cara	CEA
Ray	Carvell	PPARC
Riccardo	Cerrulli	IFSI
John	Delderfield	RAL
Jean	Fontignie	CEA
Matt	Griffin	Cardiff University
Astrid	Heske	ESA
Filippo	Marliani	ESA
Karine	Mercier	CNES
Michel	Mur	CEA
De Antoni	Philippe	CEA
Frederic	Pinsard	CEA
Diminique	Pouliquen	LAM
Eric	Sawyer	RAL
Bruce	Swinyard	RAL
Henri	Triou	CEA
Laurent	Vigroux	CEA
Chris	Whitford	Leicester University

Annex B List of Documents reviewed

title	doc number	actual issue	status
Management plan for the Herschel project.	SAp-FIRST-JLA-0038-01	4.0 23/01/2003	ok
DRCU & WIH Development Plan	SAp-SPIRE-JLA-0047-01	4.0 29/01/2003	ok
SPIRE product tree	SAp-SPIRE-DR-0094-03	1.0 21/01/2003	ok
WBS Herschel	SAP-FIRST-DR-0043-01	2.1 30/11/2001	ok
WBS SPIRE	SAP-FIRST-DR-0045-01	2.1 30/11/2001	ok
SPIRE DRCU QM1master schedule	SAp-FIRST-DR-105-01	1 18/02/2003	ok
DRCU Specifications document	SAp-SPIRE-Cca-0025-00 (SPIRE-SAP-PRJ-000461)	1.0 14/02/2003	ok
DRCU ICD	SAp-SPIRE-Cca-0075-02 (SPIRE-SAP-PRJ-000451)	1.0 14/02/2003	ok
DRCU DPU ICD	SAp-SPIRE-Cca-0076-02 (SPIRE-SAP-PRJ-001364)	1.0 14/02/2003	ok
DCU design document	SAp-SPIRE-FP-0063-02	0.3 18/02/2003	ok
Test plan DAQ IF	SAp-SPIRE-FP-0067-02	0.1 draft	ok
Test plan BIAS	SAp-SPIRE-FP-0066-02	0.1 draft	ok
Test plan LIA P	SAp-SPIRE-FP-0064-02	0.1 draft	ok
Test plan LIA S	SAp-SPIRE-FP-0065-02	0.1 draft	ok
SPIRE test configuration	SAp-SPIRE-LD-0015-01	3.0 08/2001	to be provided at review
FPU simulator specs for DCU / SCU test	SIG-SPIRE-PdA-0030-01	03 14/02/2003	ok
SPIRE LTU specifications	SAp-SPIRE-FD-0071-02	1.0 22/04/2002	ok
DRCU AIV Plan	SAp-SPIRE-HT-0082-02	2.0 03/02/2003	ok
DRCU EM/QM1 preliminary test plan	SAp-SPIRE-HT-0088-02	0.1 14/02/2003	ok
SCU design document	SEDI-SCU-MM-2002-1	0.7 17/02/2003	ok
PSU SPIRE specification	SAp-SPIRE-DS-012-02	1.1 11/12/2002	ok
PA Plan	SAP-GERES-Flo-436-00	1.0 07/11/2000	ok
DPL	SAp-SPIRE-NC-0061-02	1.0 13/02/2003	ok
DML	SAp-SPIRE-NC-0060-02	1.0 13/02/2003	ok
DMPL	SAp-SPIRE-NC-0100-02	1.0 13/02/2003	ok
DCL	SAp-SPIRE-VM-0098-02	14 10/02/2003	ok
Synthesis note about DRCU FMEA and reliability	SAp-SPIRE-JF-0099-03	0.1 10/02/2003	ok
WCA (and derating??)	will be performed later	--	--

Annex C

Review Meeting Presentations

DRCU Programme Review
CEA, Saclay
4 March 2003

Objectives and Key Issues for the Review

Matt Griffin

Objectives

1. Close out of the DRCU documentation review (= DDR), with special attention to interfaces
2. Review the DRCU development plan and schedule with respect to the instrument delivery schedule, with the aim of maintaining on-time delivery of the instrument PFM
3. Demonstrate that the risks associated with the warm electronics programme are understood and can be controlled
4. Consider the necessary resources and management/ communication practices to allow the development plan to be effectively implemented
5. Prepare for and cover most relevant issues for the instrument IHDR (to take place in July), which should then be rather routine for the DRCU)

Review Board

SPIRE Project	Matt Griffin (chair) Bruce Swinyard Eric Sawyer John Delderfield
IFSI	Riccardo Cerulli
ESA	Astrid Heske Filippo Marliani
PPARC	Ray Carvell
CNES	Yvan Blanc
Experts	Kees Wafelbakker Chris Whitford

Agenda

9:00	9:10	10	Introduction and logistics	Jean-Louis Augueres
9:10	9:25	15	Objectives and key issues for the review	Matt Griffin
9:25	9:40	15	Instrument overview	Bruce Swinyard
9:40	10:00	20	DRCU design overview	Christophe Cara
10:00	10:15	15	DCU	Frederic Pinsard
10:15	10:35	20	Coffee	
10:35	10:50	15	SCU	Michel Mur
10:50	11:05	15	MCU	Dominique Pouliquen
11:05	11:20	15	Power Supply Specification	Dominique Schmitt
11:20	11:35	15	DDR close-out	Eric Sawyer
11:35	11:55	20	Instrument Development Plan and Schedule	Eric Sawyer
11:55	12:10	15	Instrument electronics AIV plan	Eric Sawyer
12:10	12:30	20	DRCU AIV plan	Henri Triou
12:30	13:00	30	Questions and clarifications	
13:00	14:30	90	Lunch	
14:30	14:50	20	DRCU Development and Procurement Plan	Jean-Louis Augueres
14:50	15:00	10	Institute staffing and management	Jean-Louis Augueres
15:00	15:30	30	Questions and clarifications	
15:30	15:50	20	Coffee	
15:50	16:50	60	Review Board meeting	
16:50	17:00	10	Review Board feedback	
17:00			Meeting End	

SPIRE Instrument Overview

Bruce Swinyard

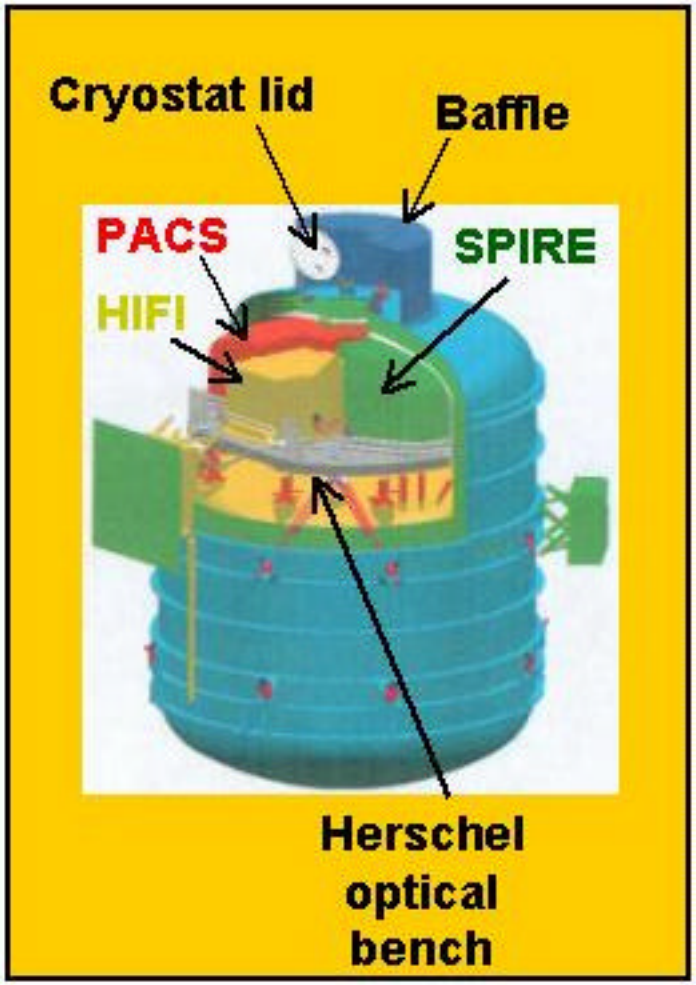
RAL

Instrument Design Drivers

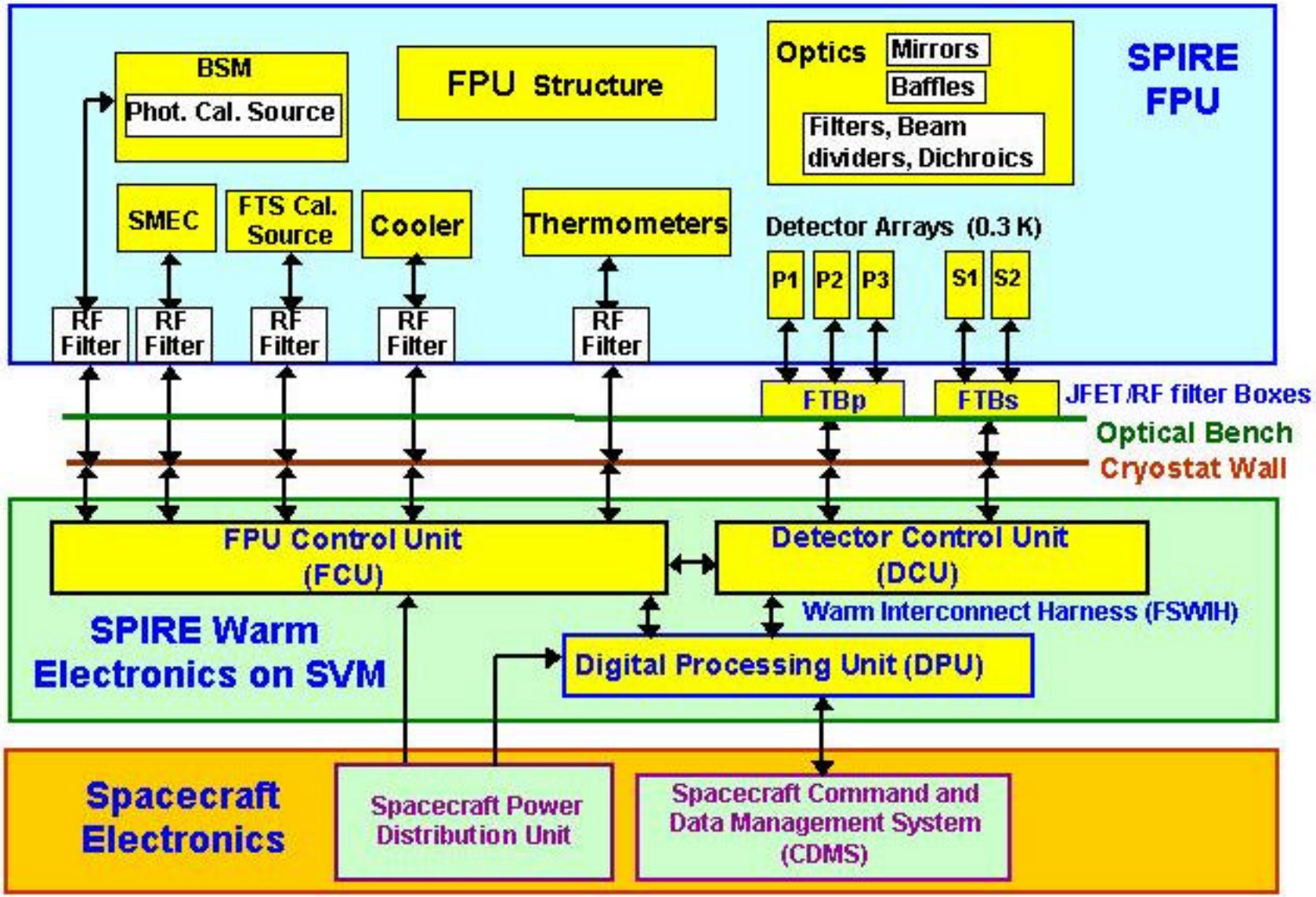
- **Photometer (200-670 microns)**
  - **Deep mapping of extra-galactic sky with highest efficiency and largest possible field of view**
    - Multi-band coverage with simultaneous observation
  - **Point and compact source observation with high efficiency**
- **Spectrometer (200- >610 microns)**
  - **Sensitivity optimised for point/compact source spectroscopy**
  - **Imaging spectroscopy with maximum available field of view**
  - **Wide wavelength coverage**
  - **Variable spectral resolution (few x 10 to few x 100)**
- **Both**
  - **Thermal background dominated by the Herschel telescope**
  - **Simplicity, affordability, reliability, ease of operation**
  - **Complementary to other Herschel instruments and other facilities**

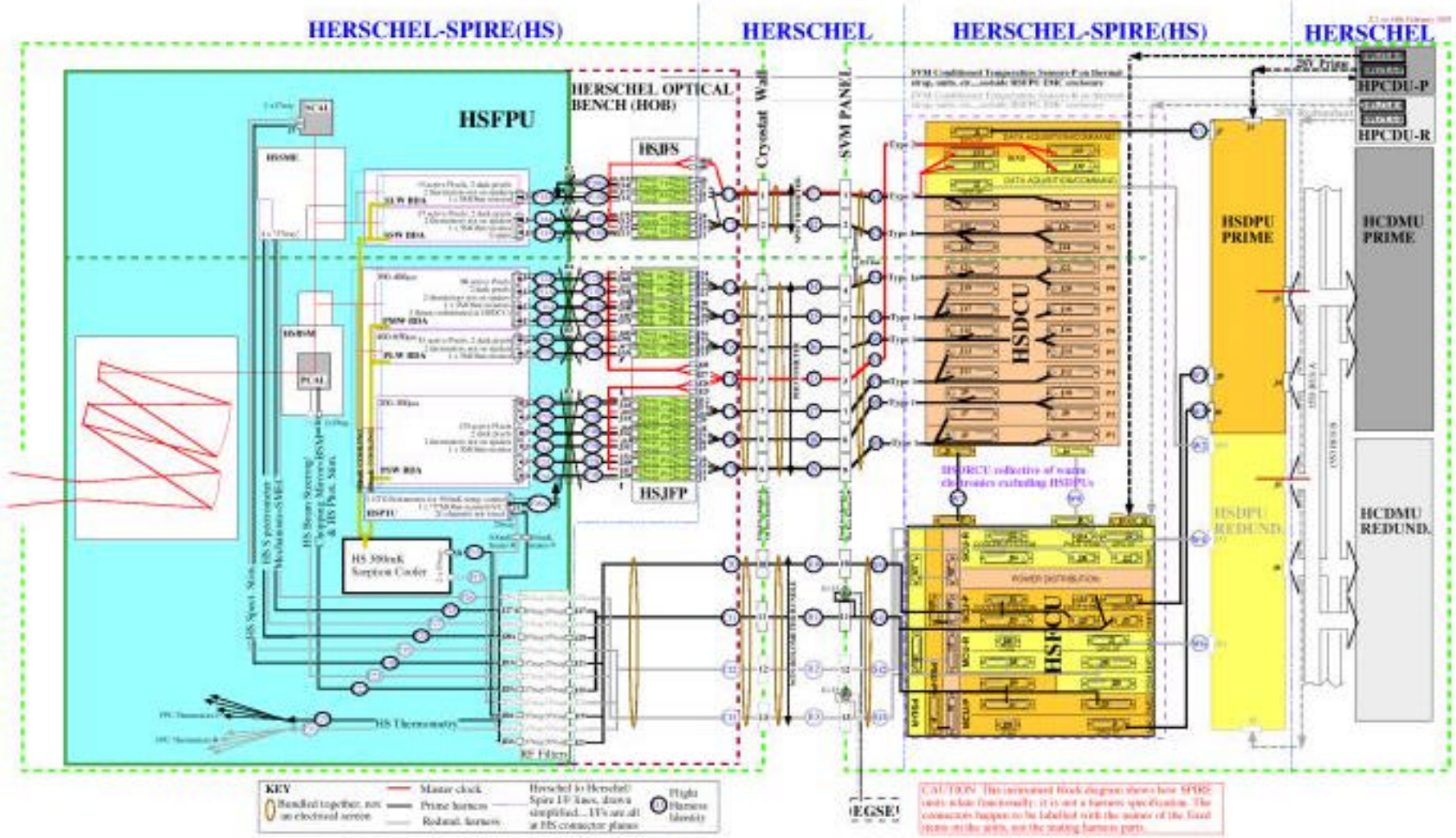
Instrument Summary

- 3-band imaging photometer
  - 250, 360, 520 μm (simultaneous)
  - $\lambda/\Delta\lambda \sim 3$
  - 4 x 8 arcminute field of view
  - Diffraction limited beams (17, 24, 35")
- Imaging FTS
  - 200 - 670 μm
  - > 2 arcminute field of view
  - $\Delta\sigma$ = 0.4 cm^{-1} (goal 0.04 cm^{-1})
    ($\lambda/\Delta\lambda \sim 20 - 100$ (1000) at 250 μm)
- Design features
  - Sensitivity limited by thermal emission from the telescope (80 K; ε = 4%)
  - ^{3}He cooled detector arrays (0.3 K)
  - Feedhorn-coupled spider web NTD bolometers
  - Minimal use of mechanisms
    - Beam steering mirror, FTS mirror drive
  - No on-board data processing

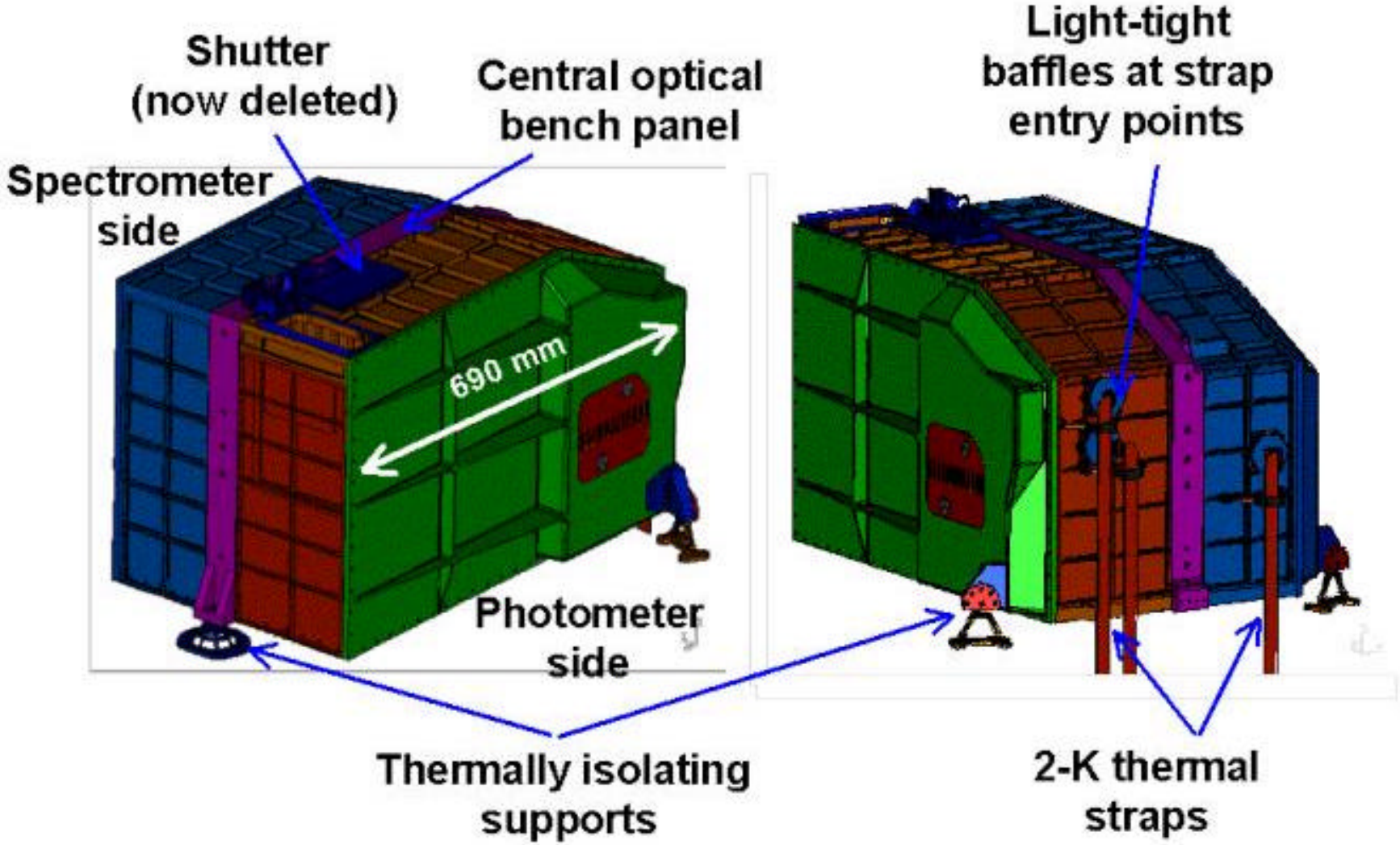


SPIRE Block Diagram

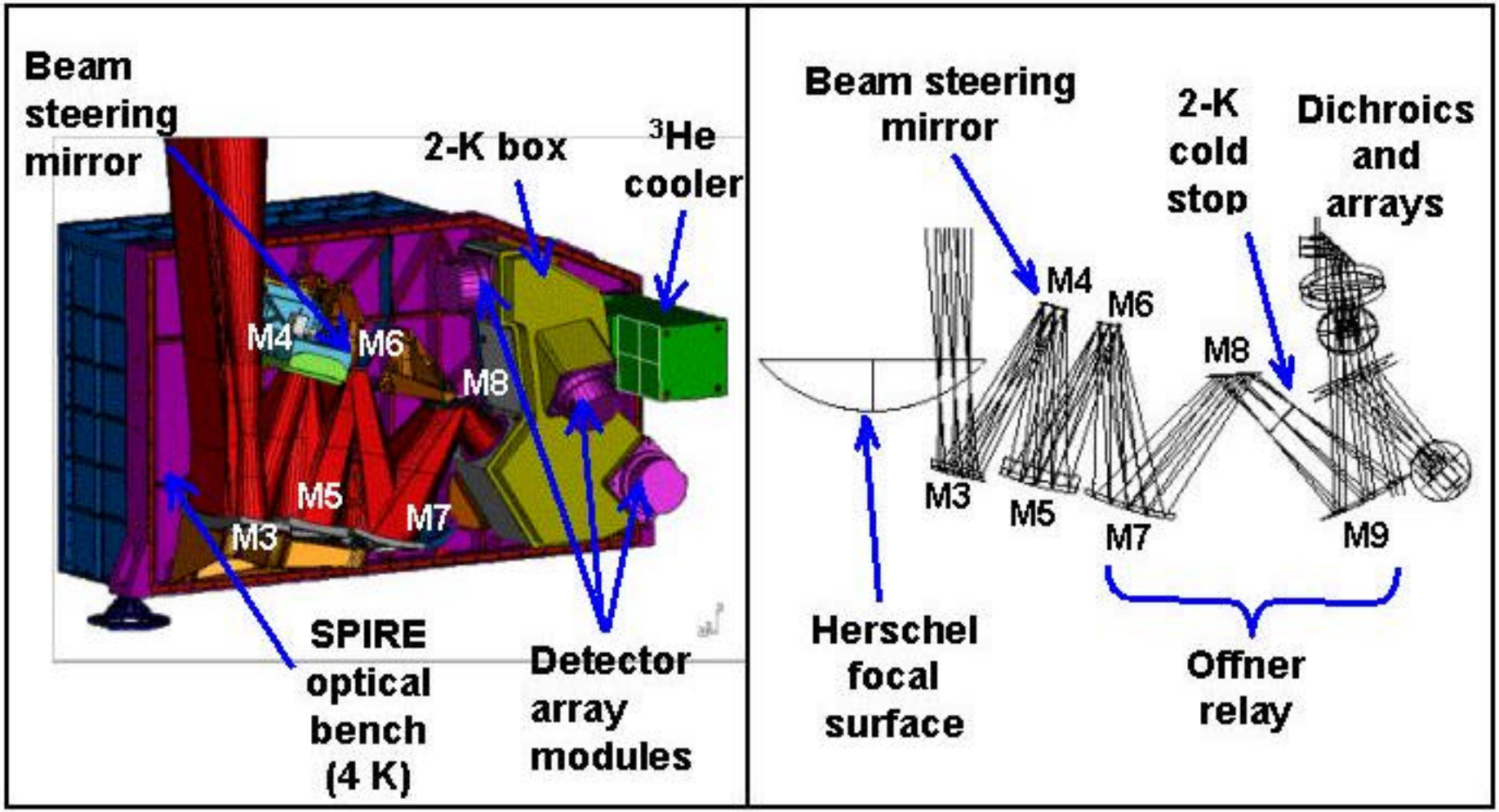



HERSCHEL-SPIRE(HS)
HERSCHEL
HERSCHEL-SPIRE(HS)
HERSCHEL
HSFPU
HERSCHEL OPTICAL BENCH (HOB)
HSBS
HSJFP
Cryostat Wall
SVM PANEL
HSDCU
HSFCU
HSDPU PRIME
HSDPU REDUND.
HPCDU-P
HPCDU-R
HCDMU PRIME
HCDMU REDUND.
HS 300mK Sorption Cooler
HS Thermometry
RF Filters
(EGSE)
KEY
Master clock
Prime harness
Redund. harness
Flight Harness Identity

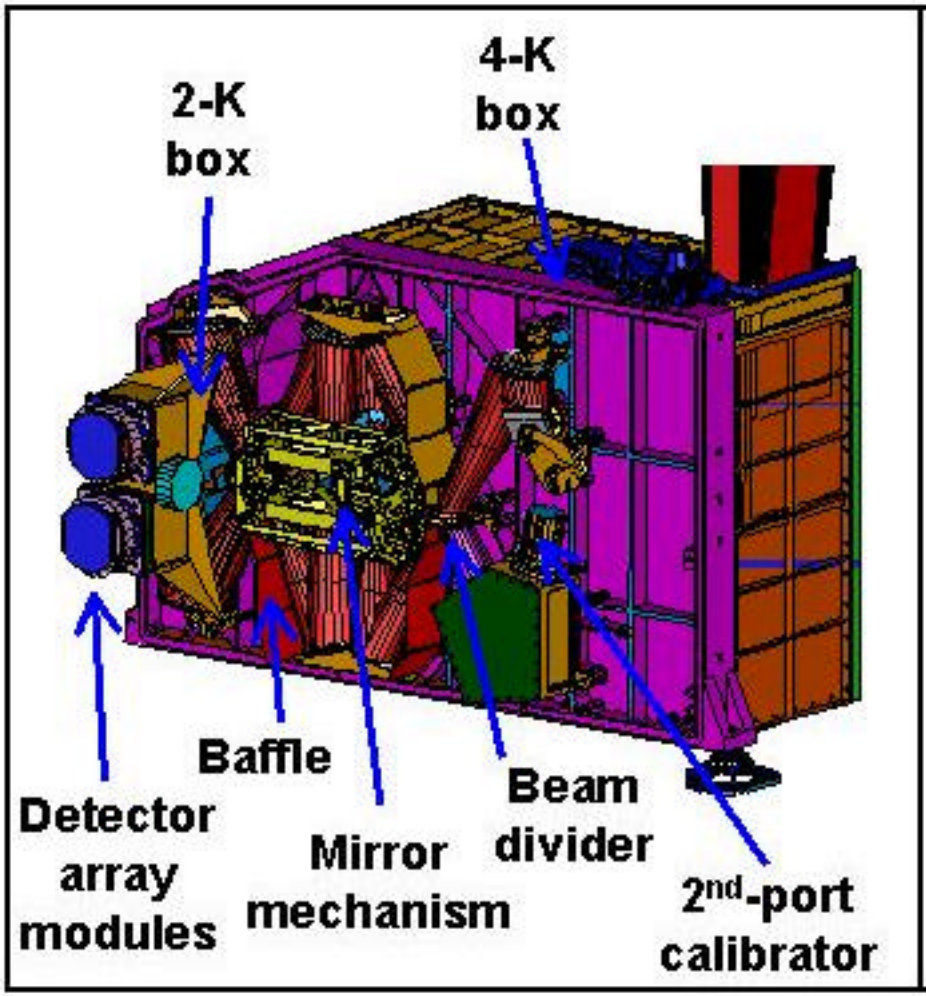
Focal Plane Unit

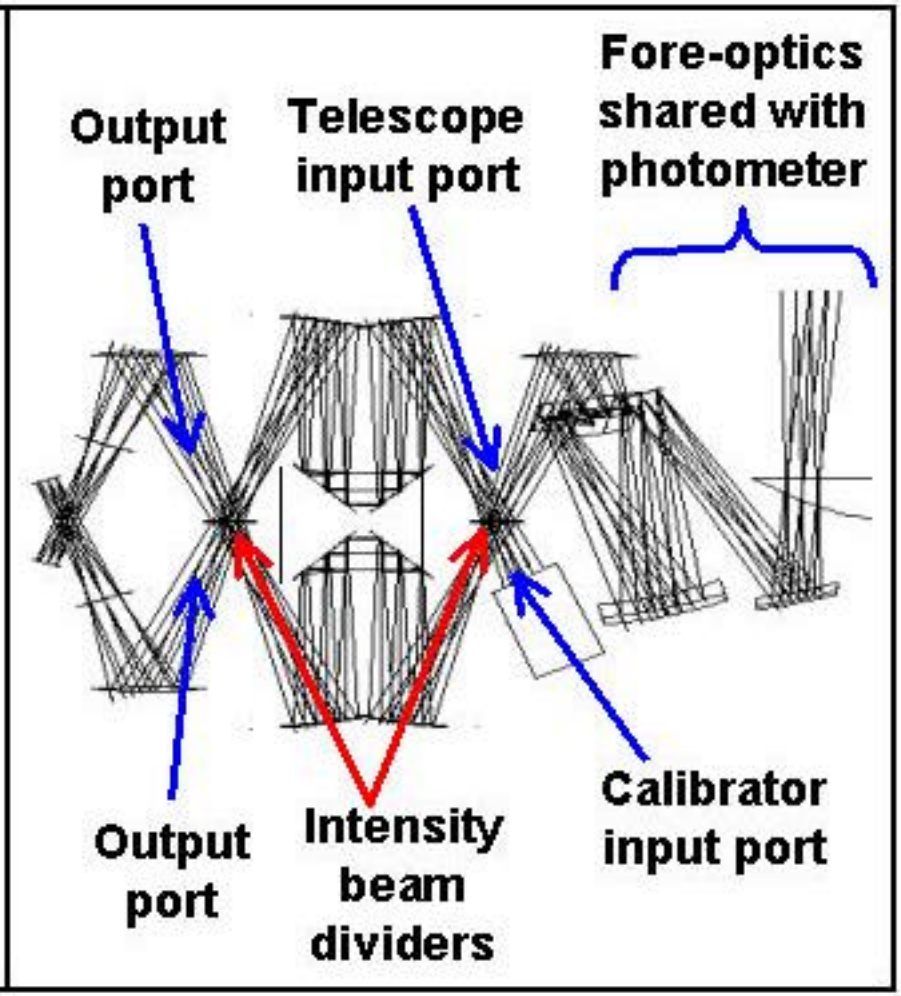


Photometer Layout and Optics



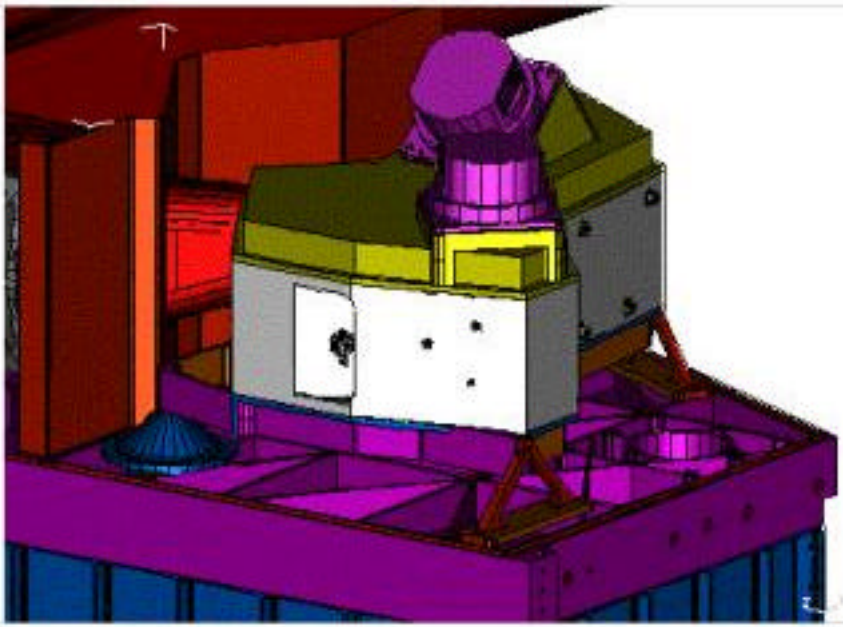
FTS Layout and Optics



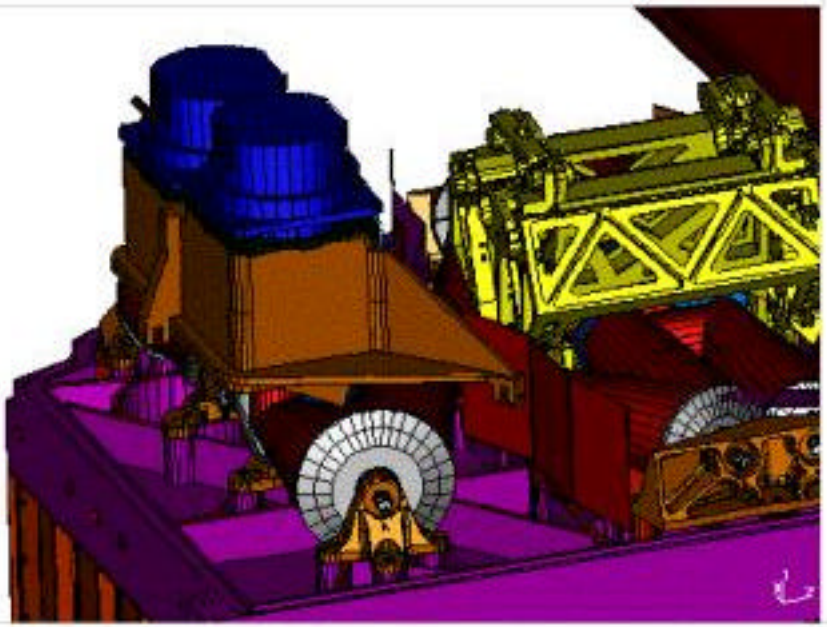


2-K Enclosures for Detector Modules

Photometer

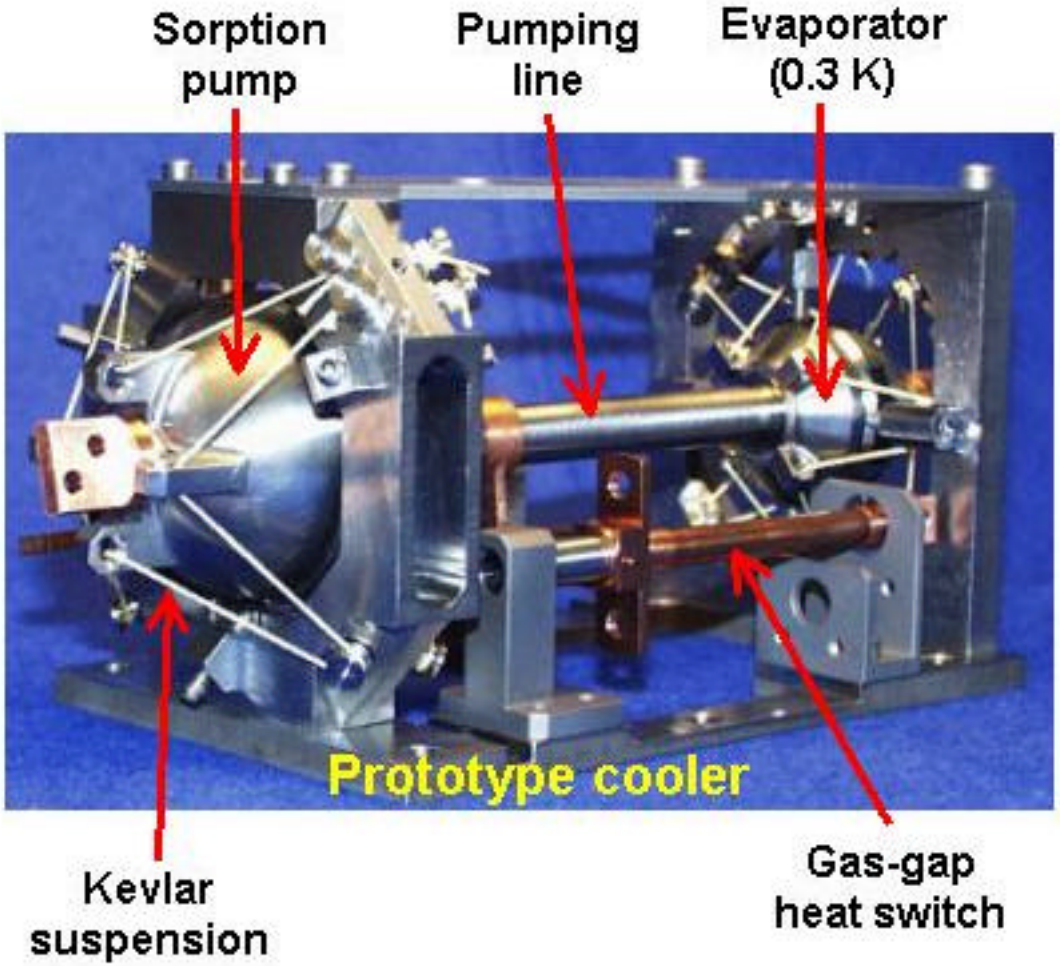


Spectrometer



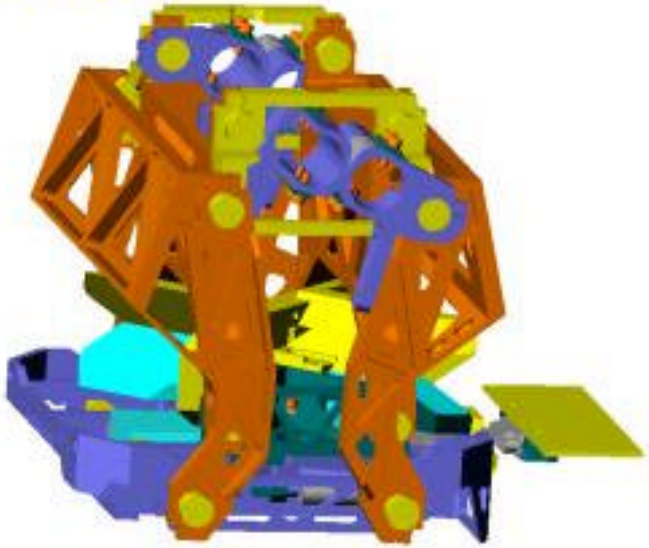
^{3}He Cooler

- Cold stage temp. < 280 mK
- Hold time > 46 hrs
- Cycle time < 2 hrs
- Average load on ^{4}He tank < 3 mW
- Heat lift provided to detector arrays > 10 μW
- Gas-gap heat switches (no moving parts)
- Driven by SCU – DPU controls operations



FTS Mechanism

- Double parallelogram with toothless gear
- Movement range –0.3 to 3.5 cm
- Measurement of position by optical encoder with high resolution 10 nm
- Over part of range have backup LVDT with 100 nm resolution
- Signal conditioning; motor drive and speed control is done by MCU
- Start; stop and movement range controlled by DPU

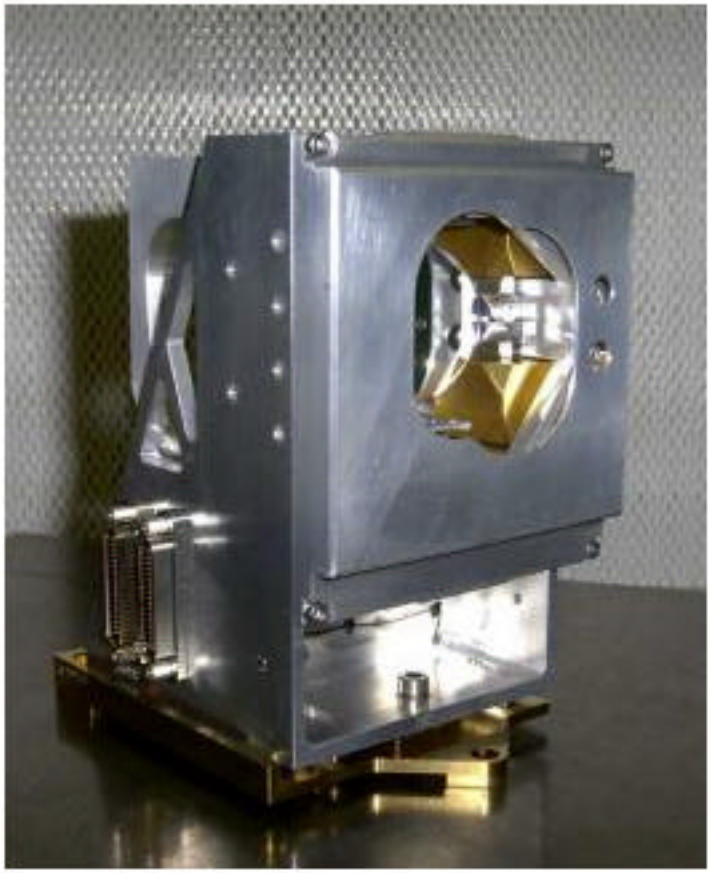


FTS Observing Modes

- **Continuous scan:**
  - Mirror scan rate = 0.5 mm s^{-1}
  - Signal frequency range = 3 - 10 Hz
  - Calibrator in 2nd port nulls telescope background
- **Step-and-integrate:**
  - 2nd port calibrator is off
  - Mirror stepped with integration at each position
  - BSM chops on sky
- **Point source spectroscopy/spectrophotometry**
  - Telescope pointing fixed
  - Background characterised by adjacent pixels
- **Imaging spectroscopy**
  - Beam steering mirror adjusts pointing between scans to acquire fully-sampled spectral image

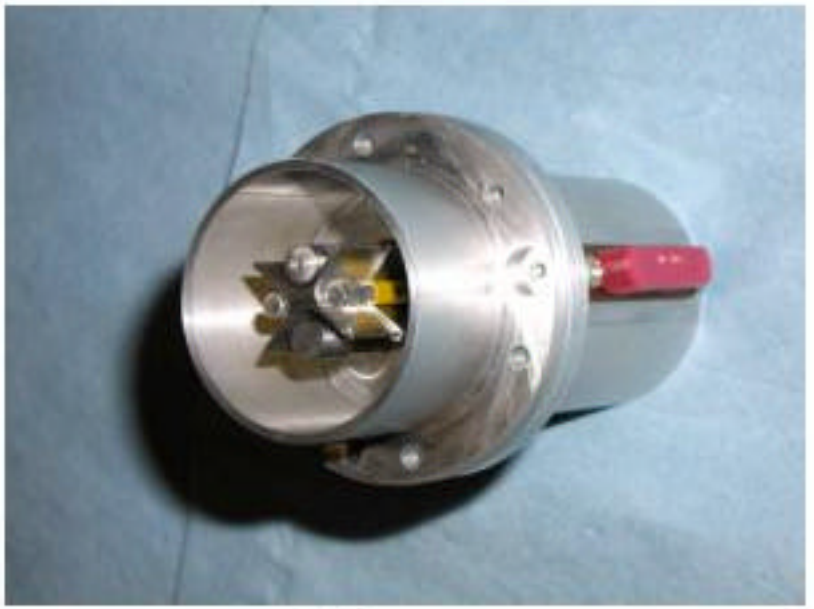
Beam Steering Mirror

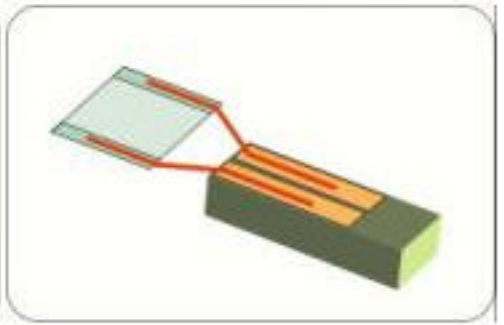
- Two axis mechanism
- Chop axis has +-2.5 degree throw at up to 2 Hz
- Jiggle axis has +-0.5 degree throw at up to 0.5 Hz
- Basic control done in MCU – DPU controls timing



Calibration Sources

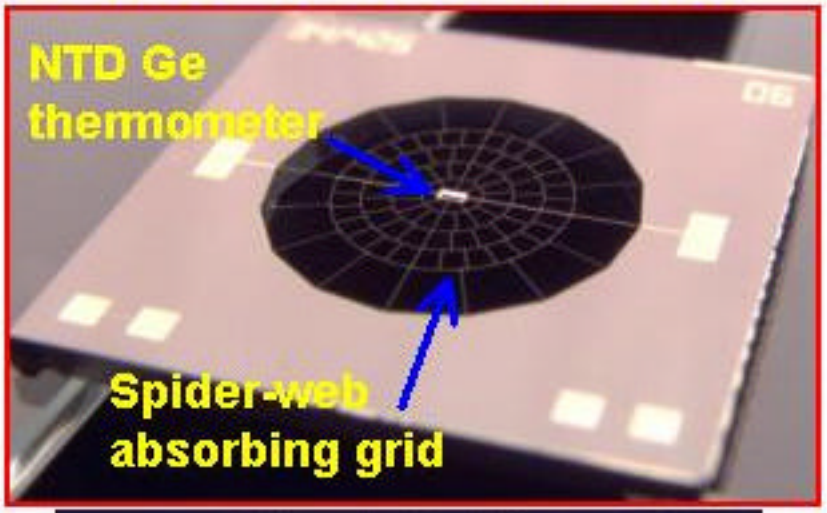
- Two calibration sources are used – SCAL and PCAL
- PCAL mounted on the BSM
- Heaters and thermistors conditioned by SCU
- Timing and temperature control done using DPU

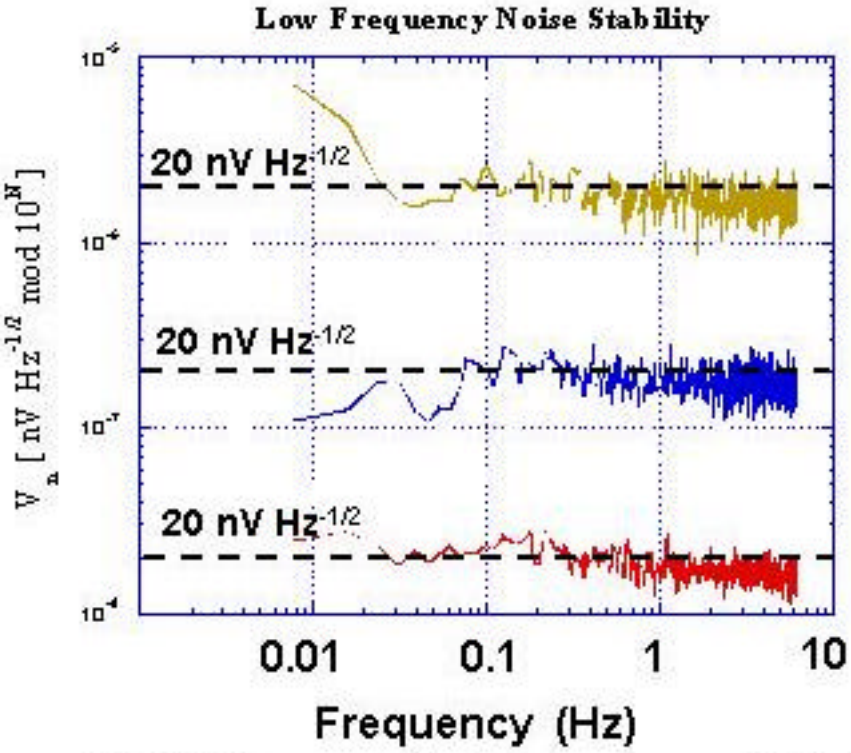


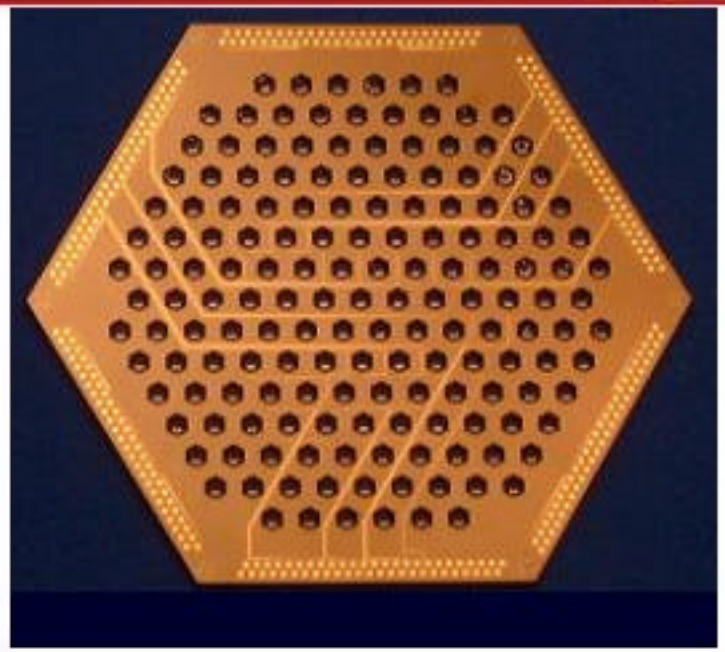


NTD Ge Bolometer Arrays (Caltech/JPL)

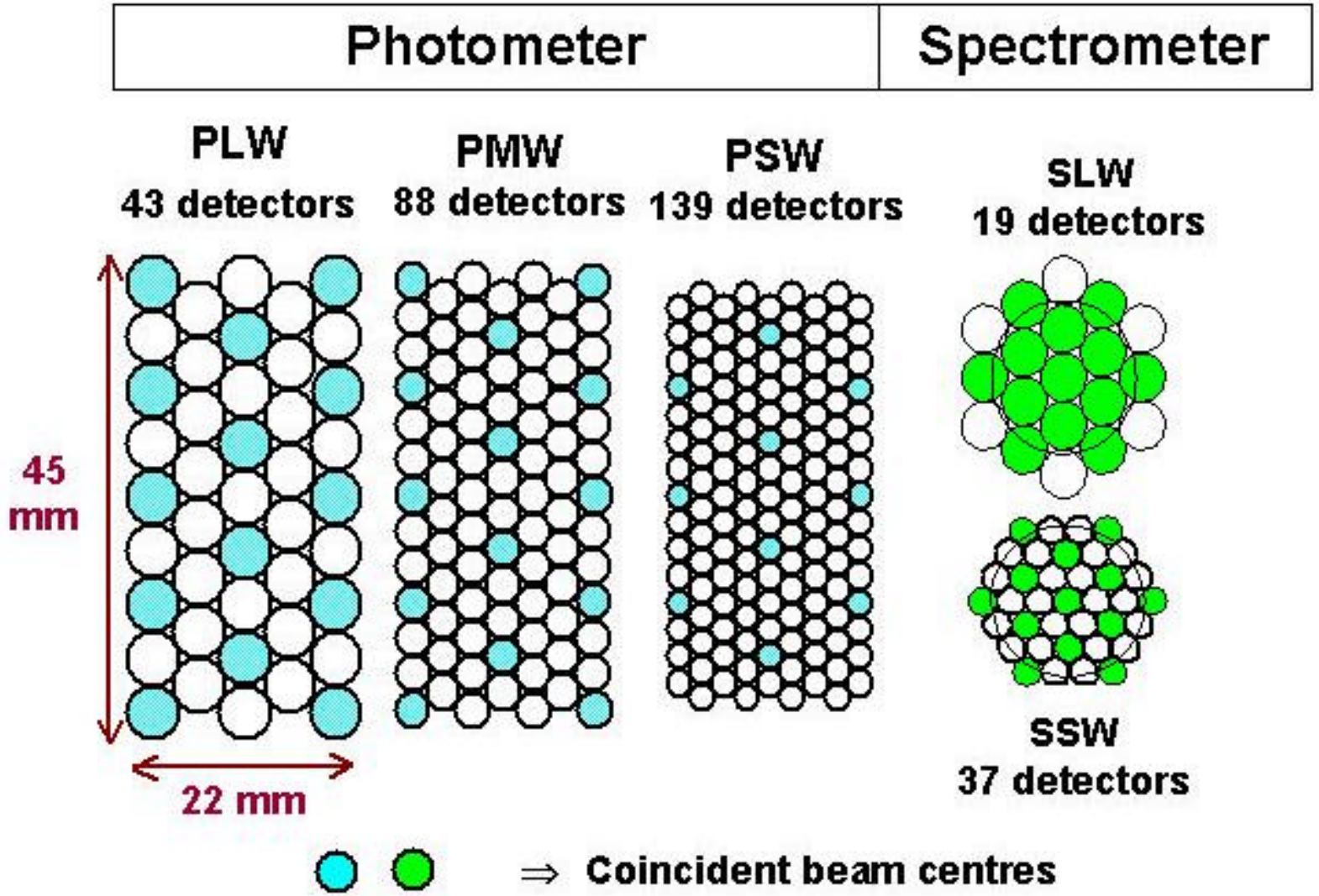
- NEP ~ 3 x 10^{-17} W $Hz^{-1/2}$
- 120-K Si JFET readout
- 1/f noise knee < 100 mHz



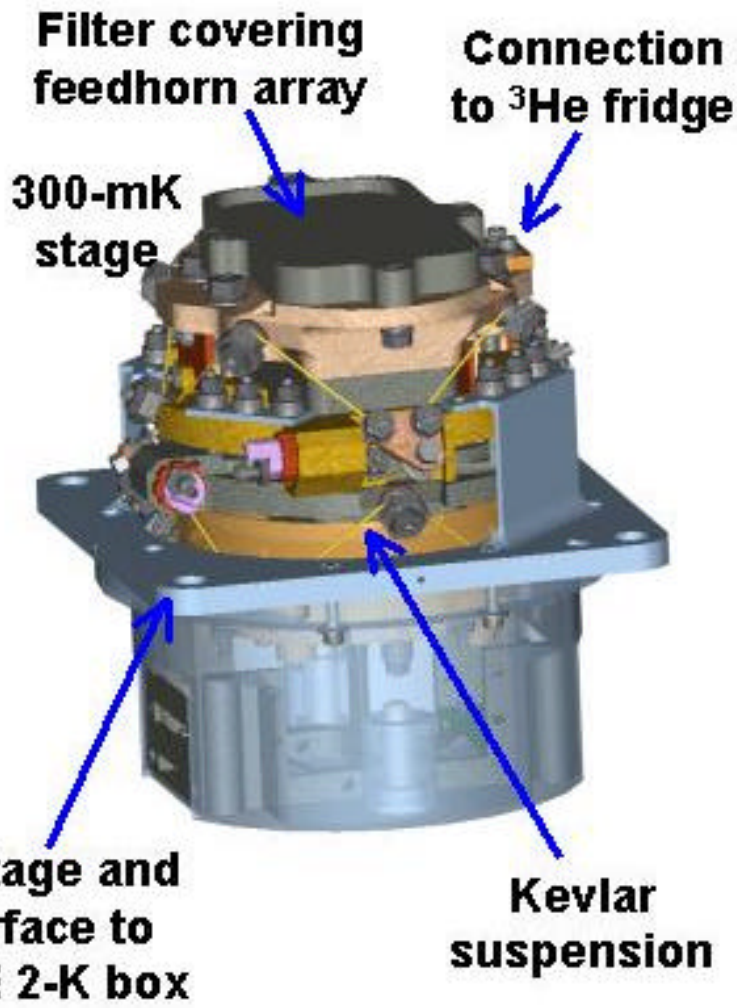


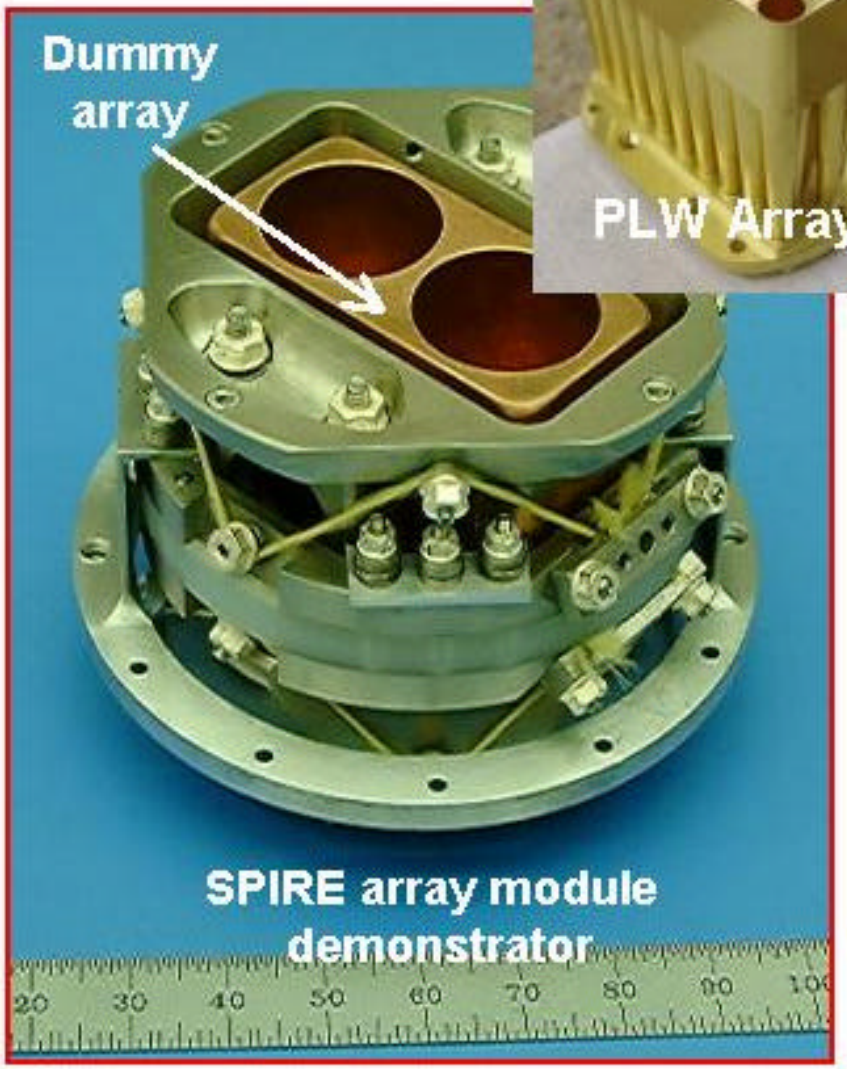


Detector Arrays (2Fλ Feedhorns)

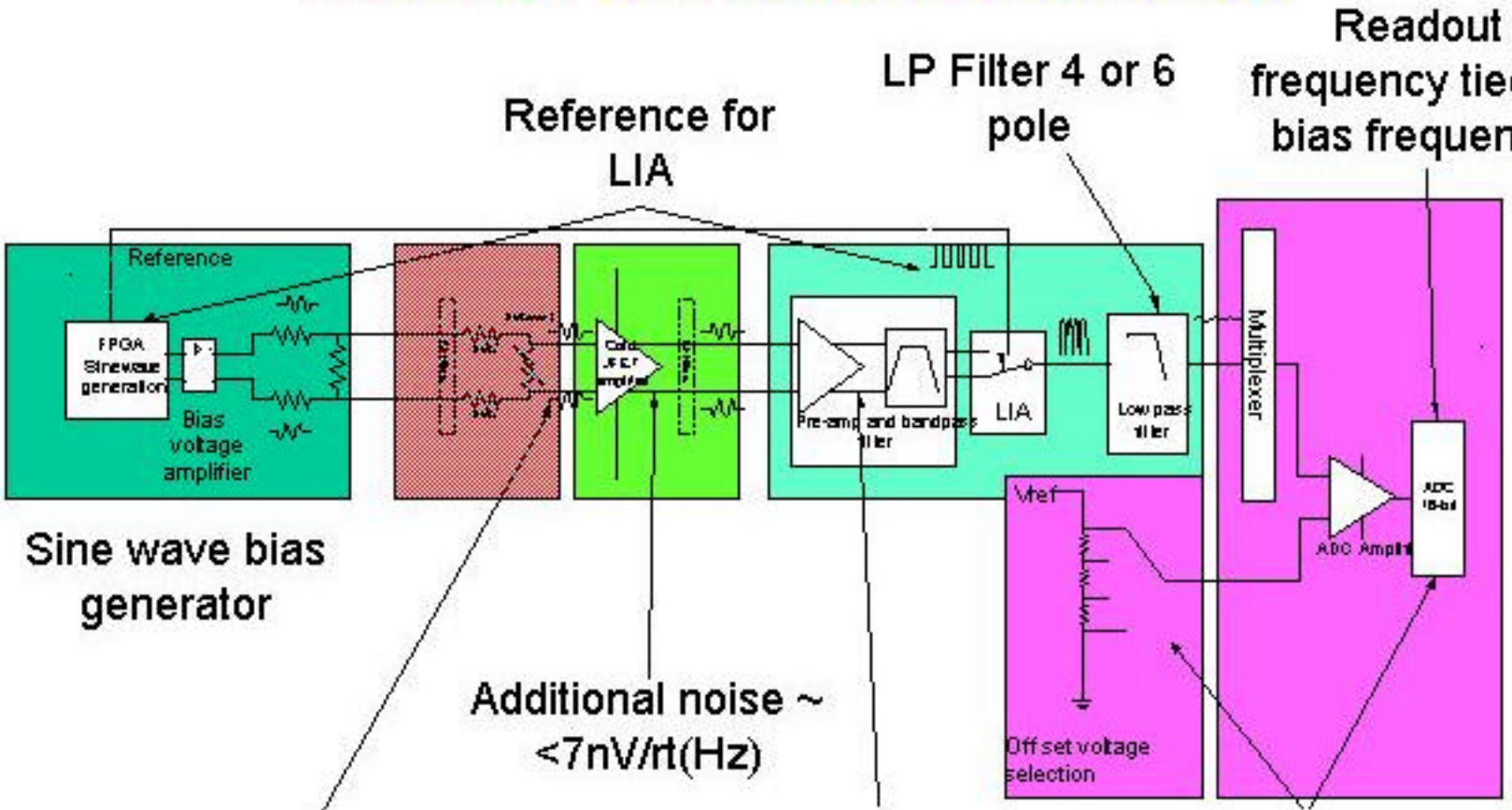


Bolometer Array Module

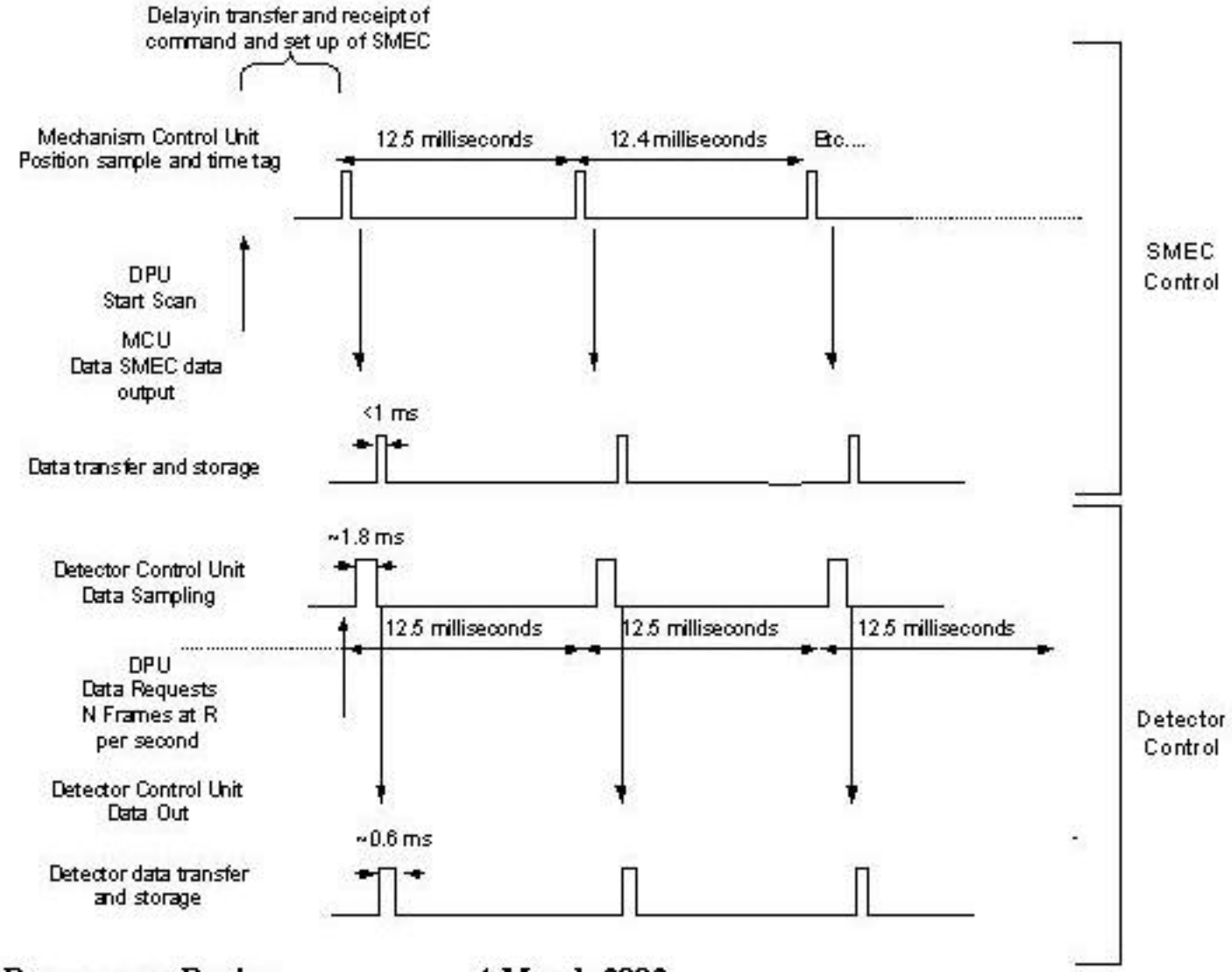




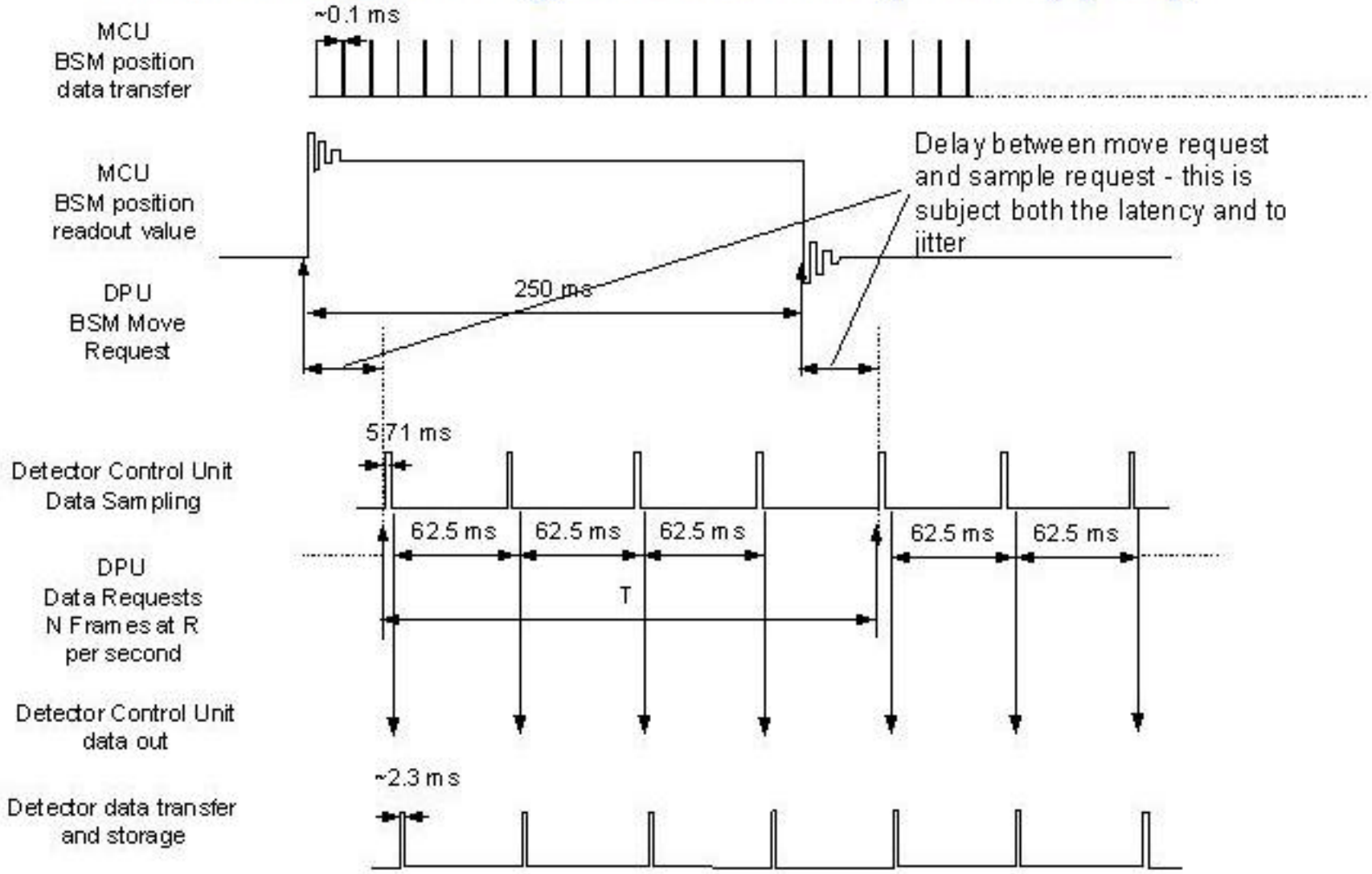
Overview of Detector Electronics



Instrument timing and control (S)



Instrument timing and control (P chopped)



DRCU Design

presented by C. CARA DRCU Engineer

contributors: V. MAUGUEN EEE engineer
T. TOURRETTE Mech. engineer

Overview

- The ***DRCU*** is a two box units:
  - The FPU Control Unit (FCU) comprises
    - The FTS and BSM associated electronics which constitutes the Mechanisms Control Unit (MCU)
    - The Calibrators, cooler and thermometer associated electronics which constitutes the Subsystems Control Unit (SCU)
    - The Power Supply Unit (PSU)
  - The Detector Control Unit (DCU) comprises analog and digital electronics exclusively devoted to bolometers operation
- Additionally power distribution between boxes is achieved by means of harness:
  - FCU to FCU (includes on/off commands for MCU & part of DCU)
  - FCU to DCU (belongs to the ***WIH***)

Origin of Specifications

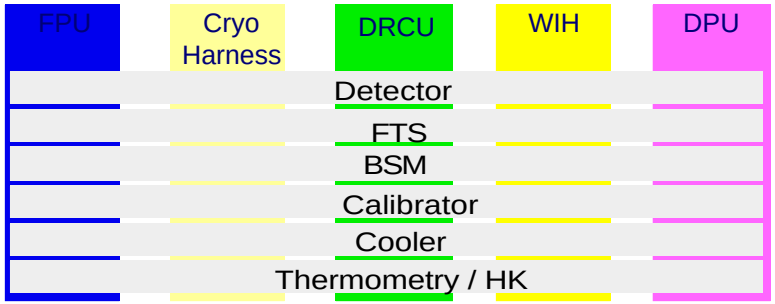
❶ **from S/C:**

- **IID-A**
- **IID-B**

❷ **from System level:**

- **Instrument Requirement Document**
- **Instrument Grounding Diagram**
- **Instrument Harness Definition**

❸ **from sub-systems level:**



Electrical Design (1)

❶ **Overall architecture:**

3+1 electrically independent subunits

DCU: Detector Electronics

MCU: FTS/BSM Electronics

SCU: Calibrator/Cooler/Thermometry Electronics

+ PSU: DCU/MCU/SCU power supplies

❷ **Redundancy/Reliability**

Architecture is driven by 2 main constrains:

☝ **Avoid as much as possible Single Point Failure**

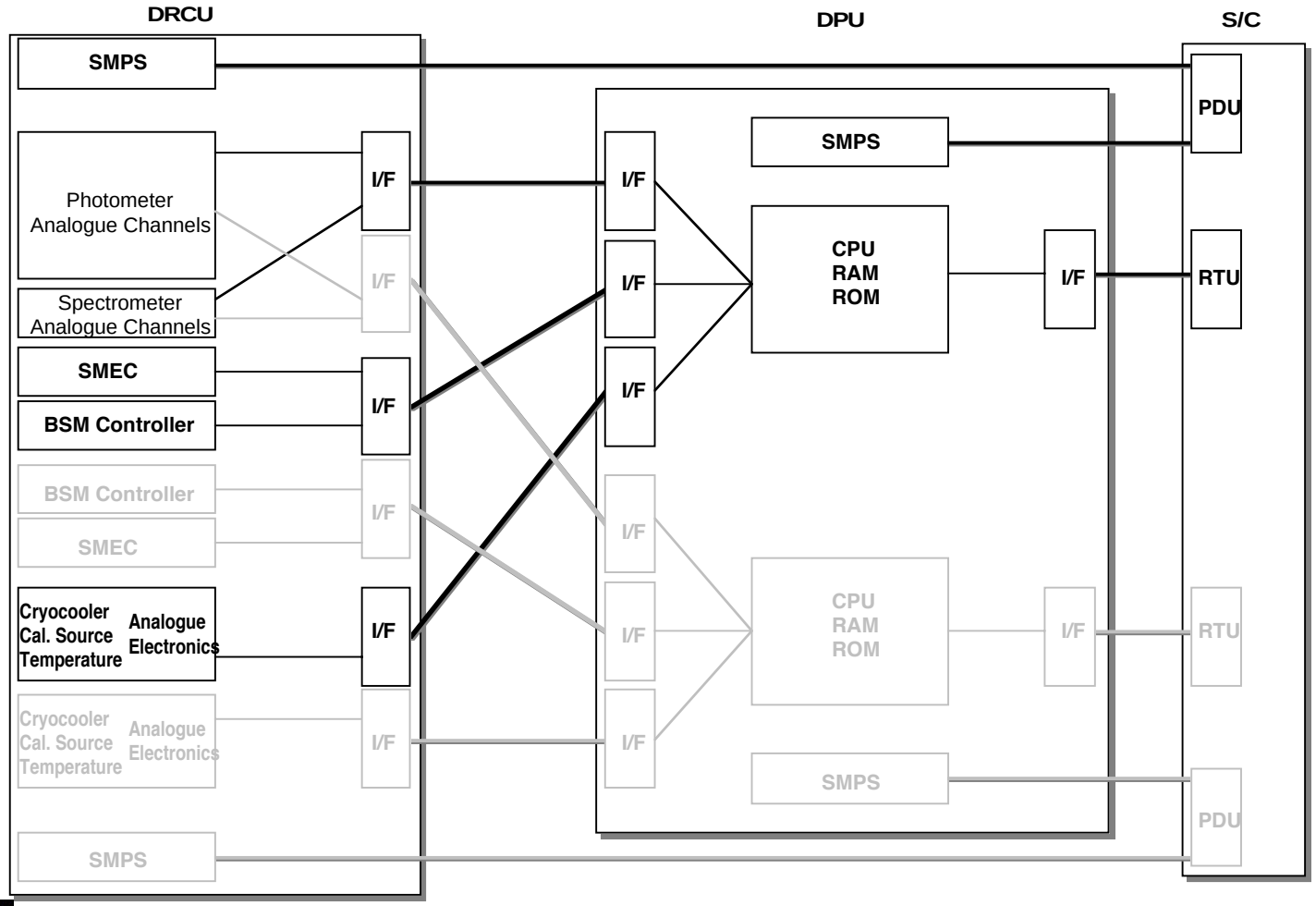
➲ **cold redundancy is applied when possible**

✌ **Limit failure propagation**

➲ **see DCU/LIA over-current protection**

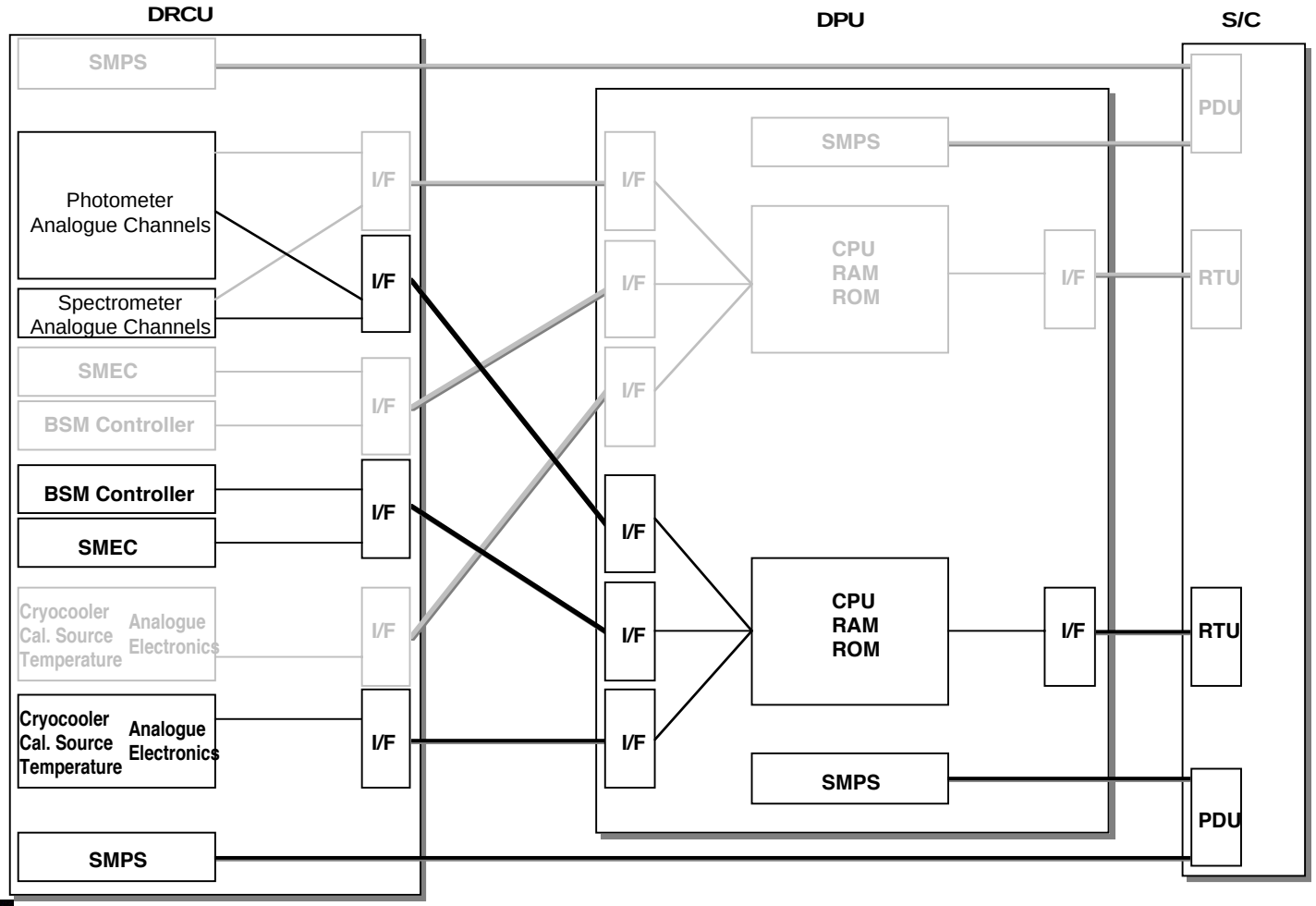
Electrical Design (2)

main configuration



Electrical Design (2)

redundant configuration



Electrical Design (3)

❸ FPU / DRCU interfaces

- Most of interfaces are balanced
- Better rejection of external perturbations
- Common mode rejection optimized by balancing interface impedance where interface is single ended

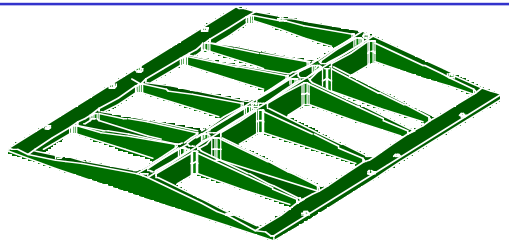
❹ DRCU / DPU interfaces

- Data Interface timing optimization for 1 to 2.5 MHz operation
- DCU data packet pixel re-arranged
- MCU data packet redefined for more flexibility
- Command list updated for the 3 S/S

Electrical Design (4)

- **❺ Grounding scheme**
  - **Finalized Q4/2002**
  - **Goal: to limit propagation toward the FPU of noise sources in SVM (digital electronics, digital interfaces, DC/DC converters, …)**
  - **DRCU electronics is referenced to chassis at DCU and FCU level**
  - **Board ground planes are connected to stiffeners**
  - **Stiffeners/Case contact is low resistance**
  - **Case/SVM panel is low resistance**
  - **➲ Return path impedance for induced perturbation is minimized**

Mechanical/thermal Design (1)

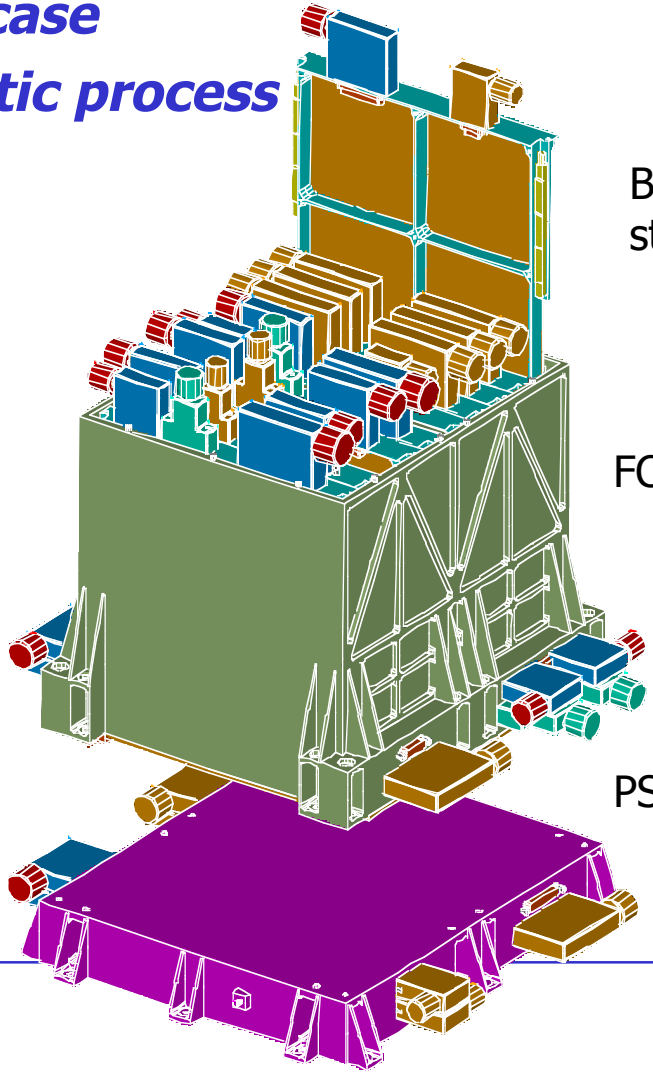


cover

- ***1.5 mm Aluminum (+ stiffeners) case***
- ***Case assembly based on electrolytic process***
- ***Anodic oxidations treated surface***
- ***Boards mounted on stiffeners (screws + glue)***

➲ ***Modeling shows:***

- ***Case eigen frequency: 500 Hz (>140 Hz / IID-A)***
- ***Board frequency: 304 Hz***
- ***Board deformation: ≤ 0.3 mm***



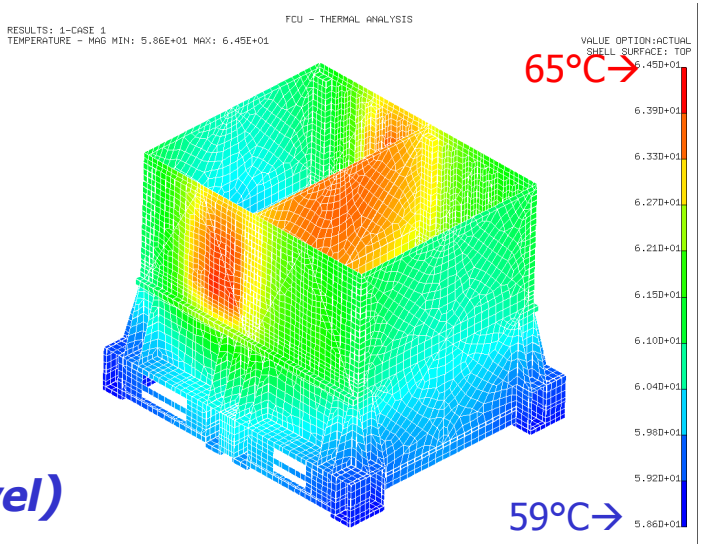
Board on stifferner

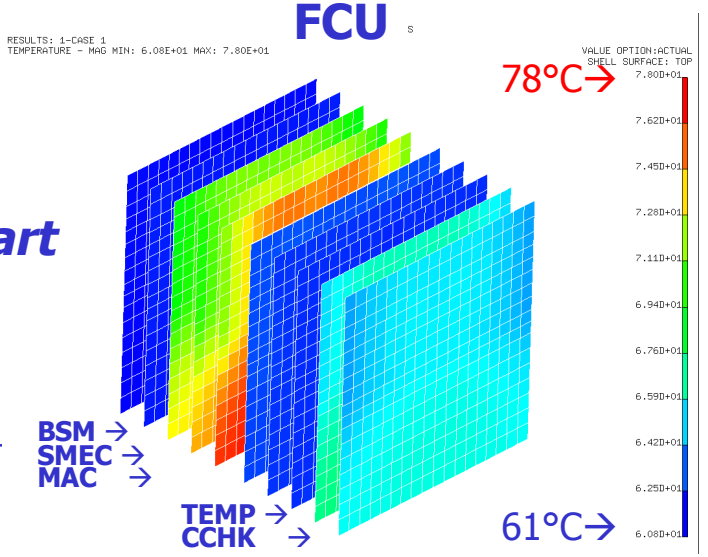
FCU case

PSU case

Mechanical/Thermal Design (2)

- ***Box design optimized for efficient heat transfer to SVM panel:***
  - ***Large contact area with panel:***
    - ***More than 28000 cm2 for DCU***
    - ***More than 100000 cm2 for FCU***
- ***However FCU model shows:***
  - ✔ ***For 55°C panel/ambient temp. (qualif. level)***
  - ✔ ***Δt PSU = 6°C***
  - ➲ ***Maximum box temp. = 65°C***
  - ➲ ***Maximum board (MCU/MAC) temp. = 78°C***
  - ⚠ ***Too close to derating rules (85°C for part case & 110°C for junction)***
  - ➲ ***To conservative estimation to be refined***





Interfaces with S/C

- ***Allocated Budgets are almost meet:***

SIZE	***DCU***	***Design:***	***490x285x305 (mm)***	
		IID-B:	***494x289x305***	
	FCU	***Design:***	***370x325x336 (mm)***	
		IID-B:	***370x325x336***	
MASS	***DCU***	***Design:***	***15.67 kg***	
		IID-B:	***15.50 kg***	
	FCU	***Design:***	***15.28 kg***	
		IID-B:	***15.00 kg***	
DISSIPATION	***DCU***	***Design:***	***33.2 W***	
		IID-B:	***37 W***	
	FCU	***Design:***	***47.6 W***	***80.8 W***
		IID-B:	***42.9 W***	***79.9 W***

Still to be confirmed by PSU contractor technical proposal (end of march)

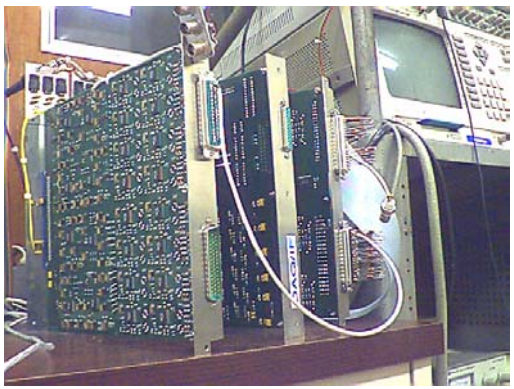
EEE parts

- ***Specification***
  - **A DCL for DCU and SCU (CEA)**
    - **ATP for LLI - 01/03/02**
    - **ATP for QM(2) - 31/01/03**
    - **ATP for FM active parts - 03/02/03**
    - **ATP for FM connectors - 31/01/03**
    - **ATP for passive parts - pending**
  - **A DCL for MCU (LAM)**
- ***Procurement***
  - **All parts are procured through the First/Planck Parts Procurement System**
  - **Except one self-procured: operational amplifier (ref.OP400)**
    - **Specific packaging for cost reduction and size optimization**
    - **Procurement of dices (3000) from Analog Device**
    - **Wafer Lot Acceptance (MIL-STD-883), Packaging, Qualification test (ESA/SCC900 level B), Up-screening (ESA/SCC 9000 level B), LAT 2**

Critical Points

- ***PSU late availability:***
  - ***Grounding scheme limits PSU injected current propagation***
  - ***Need to specify accurately performance at interface level***
  - ***PSU EM model delivered (temporally only) to perform capability tests with QM2 of DRCU***
- ***Late test of the DRCU with CQM FPU:***
  - ***QM2 design starts before test result***
  - ***Risk of late modification of QM2***
  - ***JPL test cryostat with a few bolometers available at CEA***
- ***Board Operating temperature:***
  - ***Operating temperature too close to allowed maximum***
  - ***Model to be refined: PSU Δt, P_{dissip}(board), …***

Warm Electronic DCU Design



FREDERIC PINSARD

Service d'astrophysique CEA/DAPNIA

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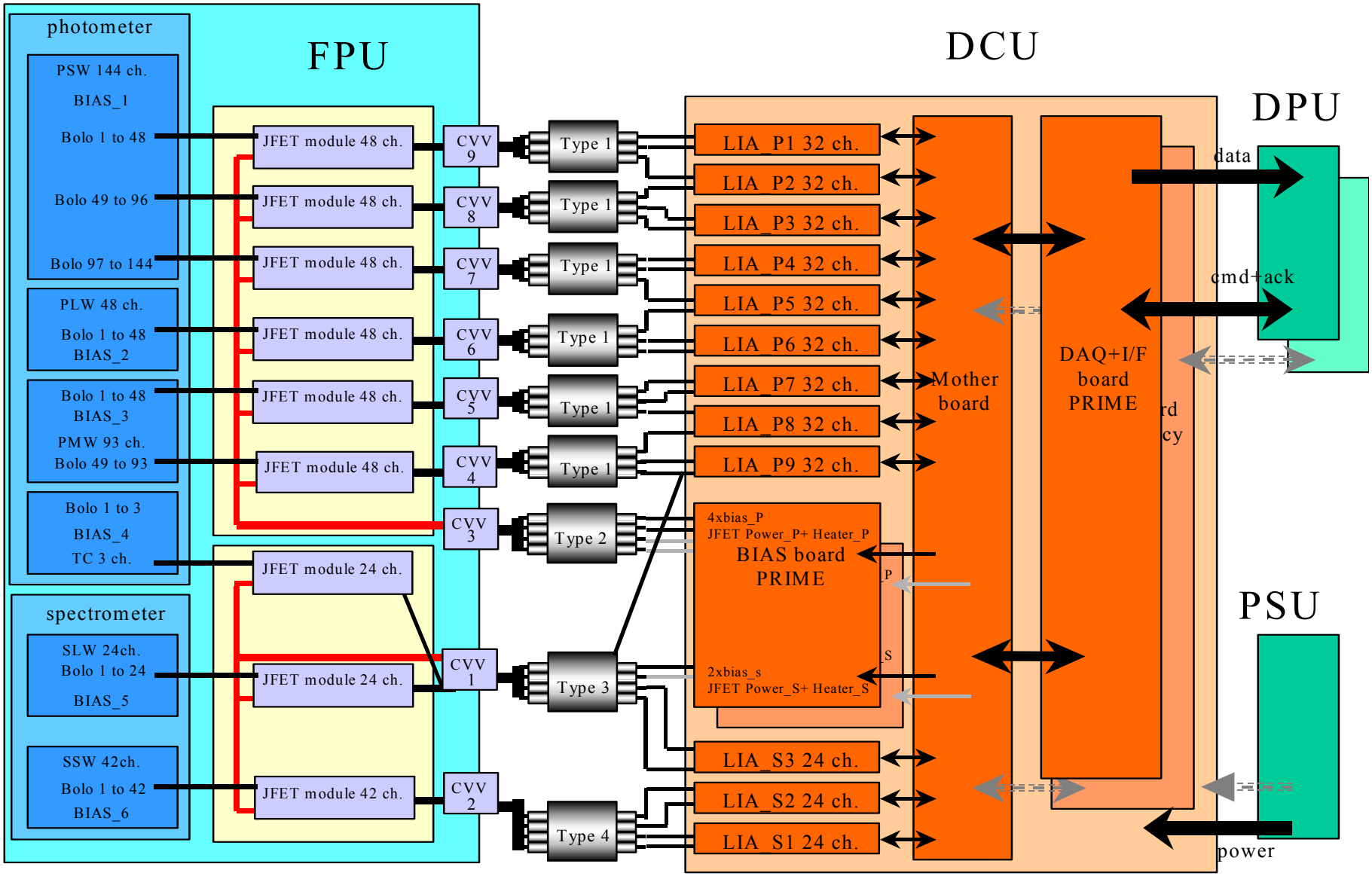
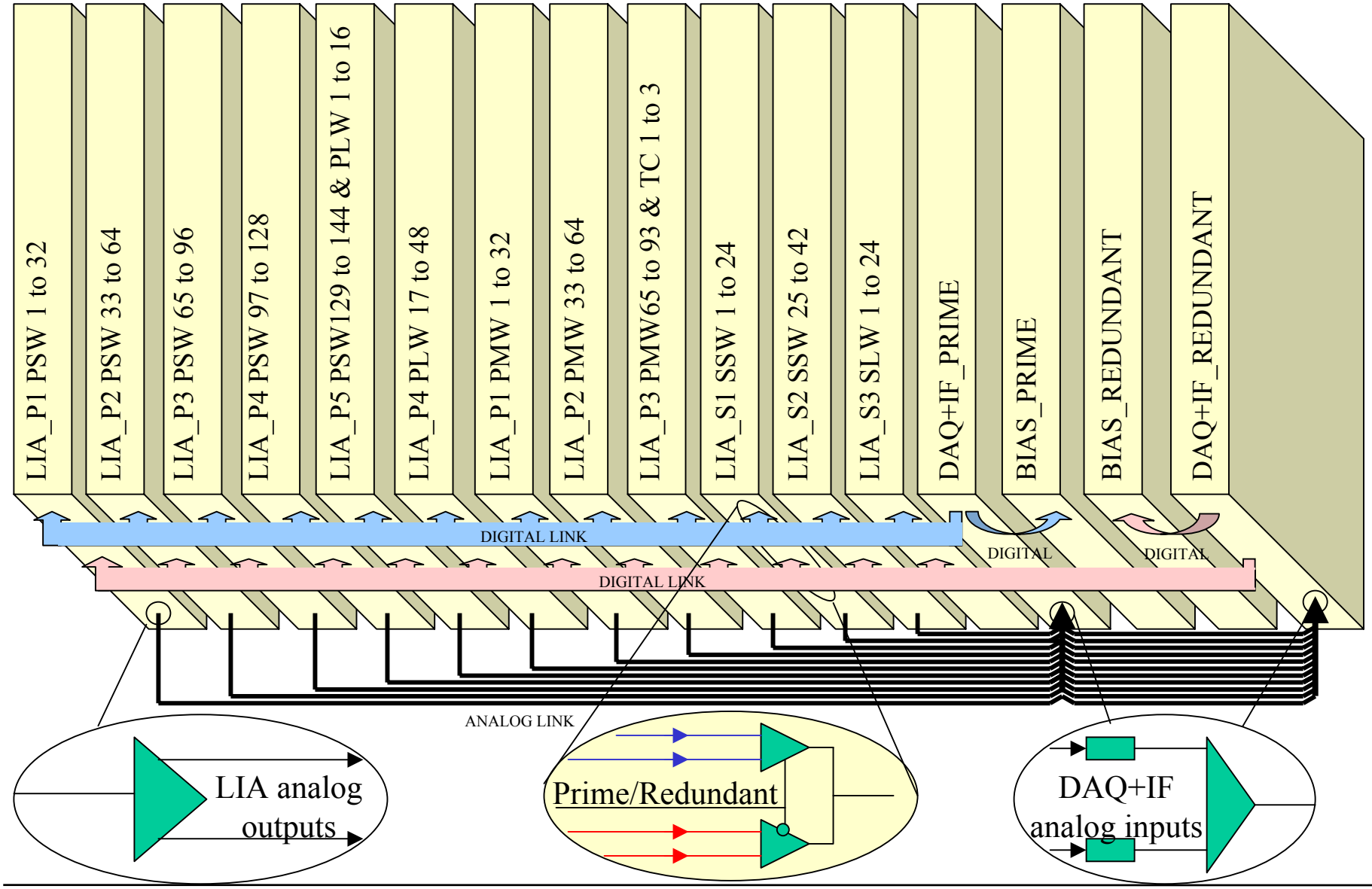
DCU Overview (1)

- The DCU is a one-box unit:
  - The Detector Control Unit comprises analog and digital electronics exclusively devoted to the bolometers' operation.
  - In this box, 16 boards are connected on a back-plane printed circuit board.
    - 9 LIA_P boards process the photometer analog signals.
    - 3 LIA_S boards process the spectrometer analog signals.
    - 2 BIAS boards (1 prime & 1 redundant)
      distribute the bolometers' bias and JFETs' supply.
    - 2 DAQ+IF boards (1 prime & 1 redundant)
      digitize the signals and receive /decode the commands.

DCU Overview (2)

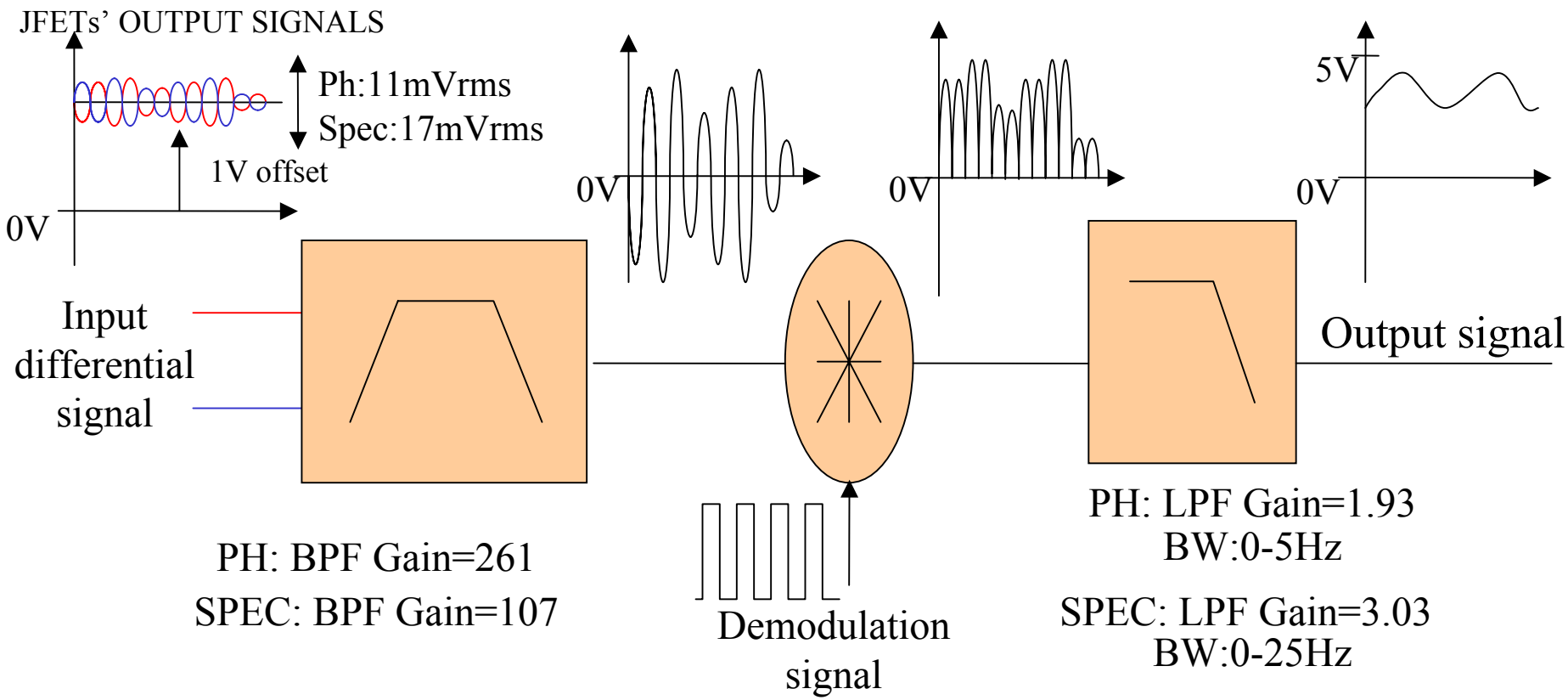


DCU internal connections



LIA (1)

- Analog processing channels:
  - Functions: to receive, amplify, demodulate & filter the bolometers' signals
  - Total number 354 : 288 for the photometer + 66 for the spectrometer



LIA (2)

- QM1 measurement main results:

BPF	Photometer		Spectrometer	
	min	max	min	max
Gain	260	265	113.2	115.5
F_{-3dB} low in Hz	34.4	35.1	35.2	35.9
F_{-3dB} high in Hz	1453	1483	2673	2727

Channel	Photometer		Spectrometer	
	min	max	min	max
Gain	446	449	308	315
F_{-3dB} low in Hz	4.85	4.95	24.9	25.1
CMR	-85dB	--	-80dB	--
Input noise in nVrms/√Hz	--	4.5	--	5.5

NOTE: 3 channels have flaws, but these problems are being investigated

BIAS

- Bias generators:
  - Functions: to generate sine biases for the bolometers and the DC biases for the JFETs and heaters
  - Adjustable sine biases:
    - Photometer : 1sine generator with 4 independent channel amplitudes
    - Spectrometer : 1sine generator with 2 independent channel amplitudes
  - Adjustable DC biases:
    - Photometer : 12 generators for the JFET + 1 for the heater with 7 buffers
    - Spectrometer : 3 generators for the JFET + 1 for the heater with 2 buffers

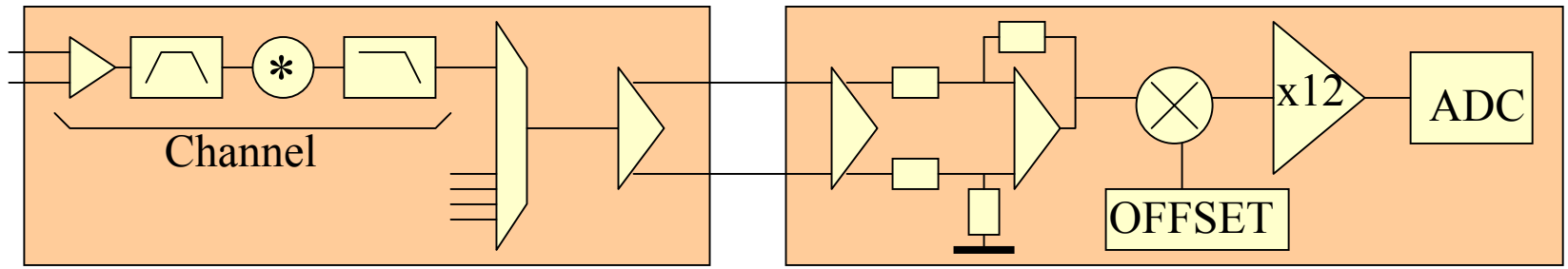
	Sine bias		DC bias		
	Ph/Spec	TC	Vss	Vdd	heater
Voltage range in Vrms	0 to 0.2	0 to 0.5	0 to -5	2.5	0 to –5V
Frequency range in Hz	40 to 305	40 to 305	DC	DC	DC
Output current max in mA	--	--	5mA	5mA	2.5mA/buffer
Noise in nVrms/√Hz	xx	xx	250	200	250

DAQ+IF

- DAQ+IF functions:
  - Digitized data and transfer, timing cycle, command decoding, hk parameter transfer.

	Number	Parameter values	Range
BIAS frequencies	2	40 to1FF	40 to 305Hz
Sample frequencies	2	3 to FF	$F_{BIAS}/3$ to $F_{BIAS}/256$
Demodulation phases shifts	6	0 to FF	0 to 360°
Offsets	354	0 to F	0 to 5V
Data transfer frequency	-	-	2.5Mb/s
HK& command transfer frequency	-	-	3125kb/s
Data ADC	6	-	–2.5 to 2.5V (16 bits)
Photometer picture acquisition	-	-	6ms
Spectrometer picture acquisition	-	-	1.2ms
Frame number	1	0 to FF	1 to 255 or continue

NOISE



Last gain stage on DAQ+IF (FUNC-02-7) Vrms	**2,51E-06**
Offset stage on DAQ+IF (FUNC-02-06) Vrms	**2,68E-06**
Substractor stage on DAQ+IF (Analog receiver) Vrms	**2,43E-06**
Differential receiver stage on DAQ+IF (Analog receiver) Vrms	**2,15E-06**
Differential transmitter stage on LIA Vrms	**2,87E-06**
LIA photometer channel (FUNC-02-05,*-04,*-03,-02,*-01) Vrms	**3,70E-06**
LIA spectrometer channel (FUNC-02-05,*-04,*-03,-02,*-01) Vrms	**6,13E-06**
ADC (DCU-FUNC-03) Vrms	**5,80E-05**
Photometer input noise V/√Hz	**8,20E-09**
Spectrometer input noise V/ √Hz	**6,57E-09**

STATUS

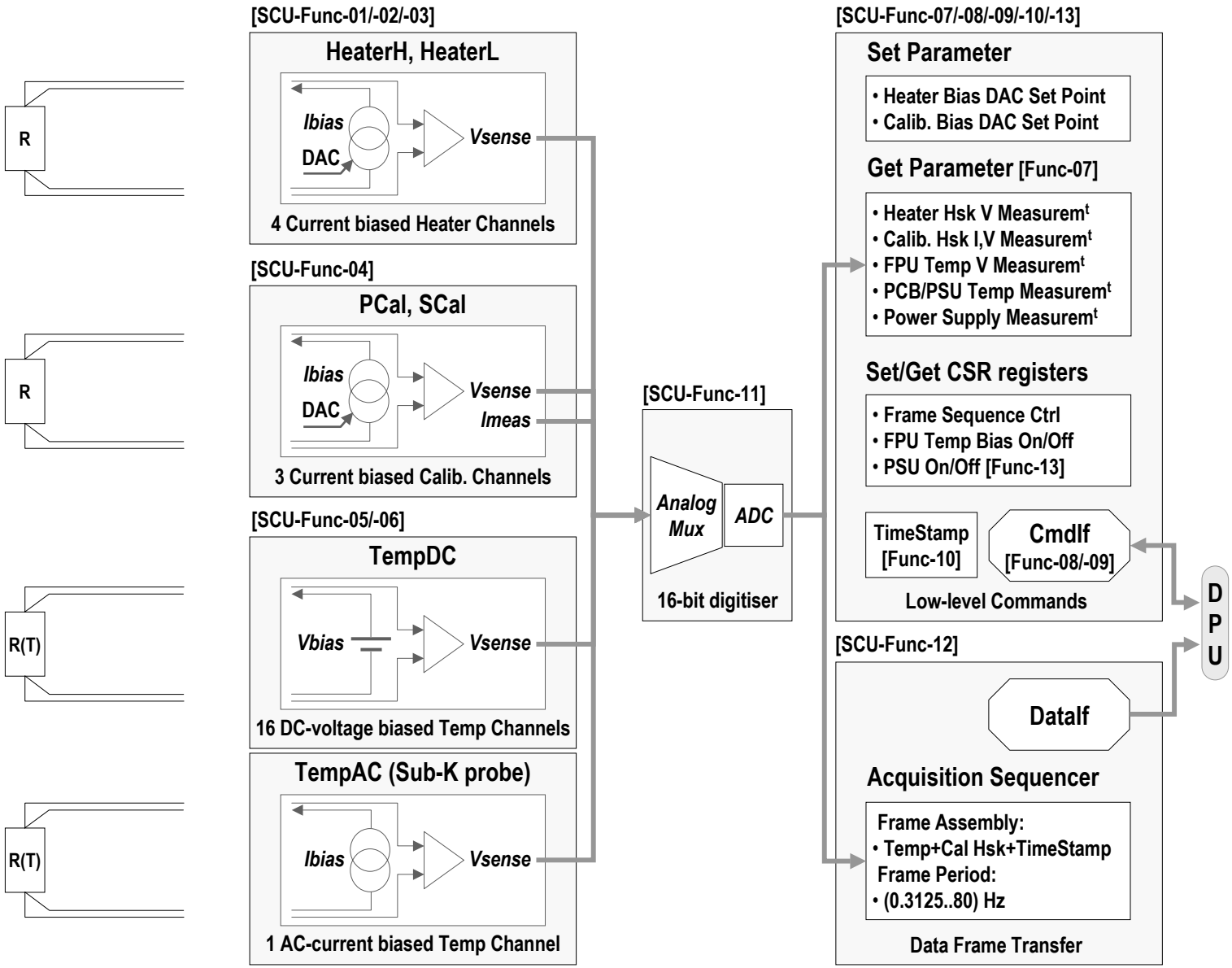
- The DCU QM1 in progress
  - Manufacturing and assembly of the LIA_P2, LIA_S2 and LIA_S3
  - Total noise measurement with the OP484 on DAQ+IF board
- The DCU QM1 future
  - Test of the new LIA boards
  - QM1 assembling
  - QM1 testing alone
  - Testing of the DCU QM1 with the test cryostat from JPL
  - Testing of the DCU QM1 with simulators
  - …

The SCU

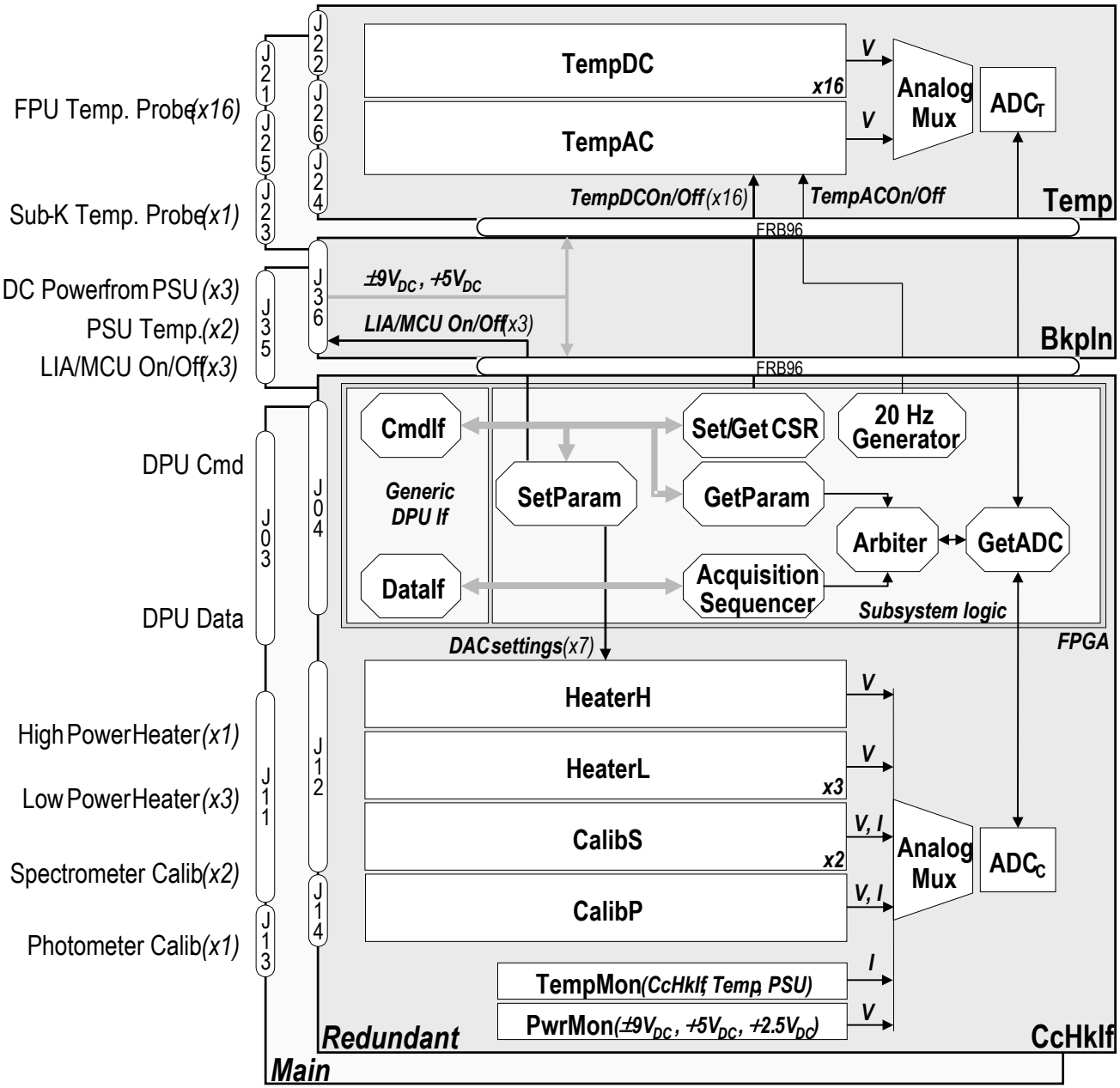
Functions
Architecture
DPU Interface
Subsystem logic
Analogue channels
Boards
Test strategy
Status

Michel MUR (CEA/DSMDAPNIA, 01 69 08 14 67, michel.mur@cea.fr)

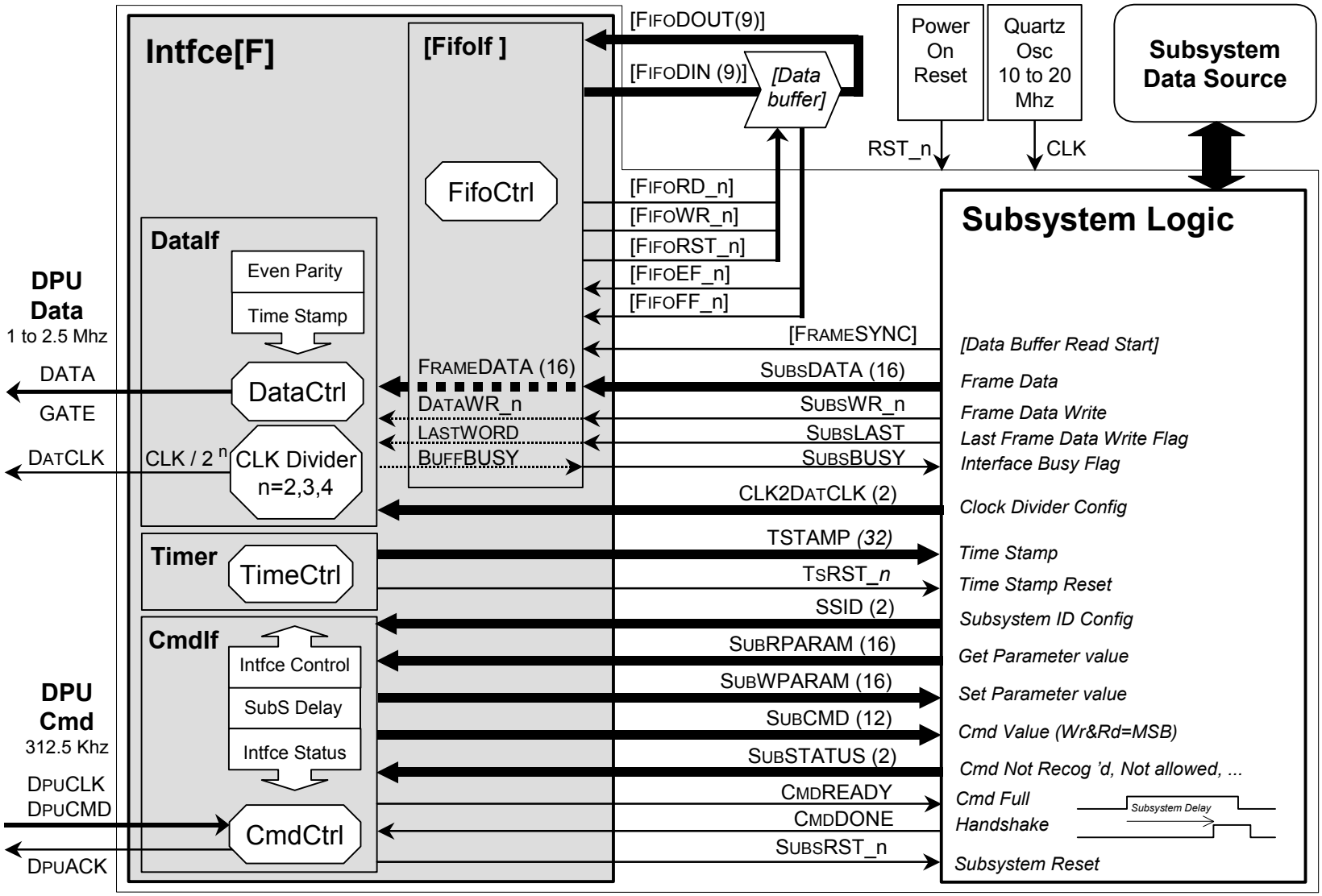
Functional overview



Architecture



Generic subsystem interface: concept



FPGA circuit

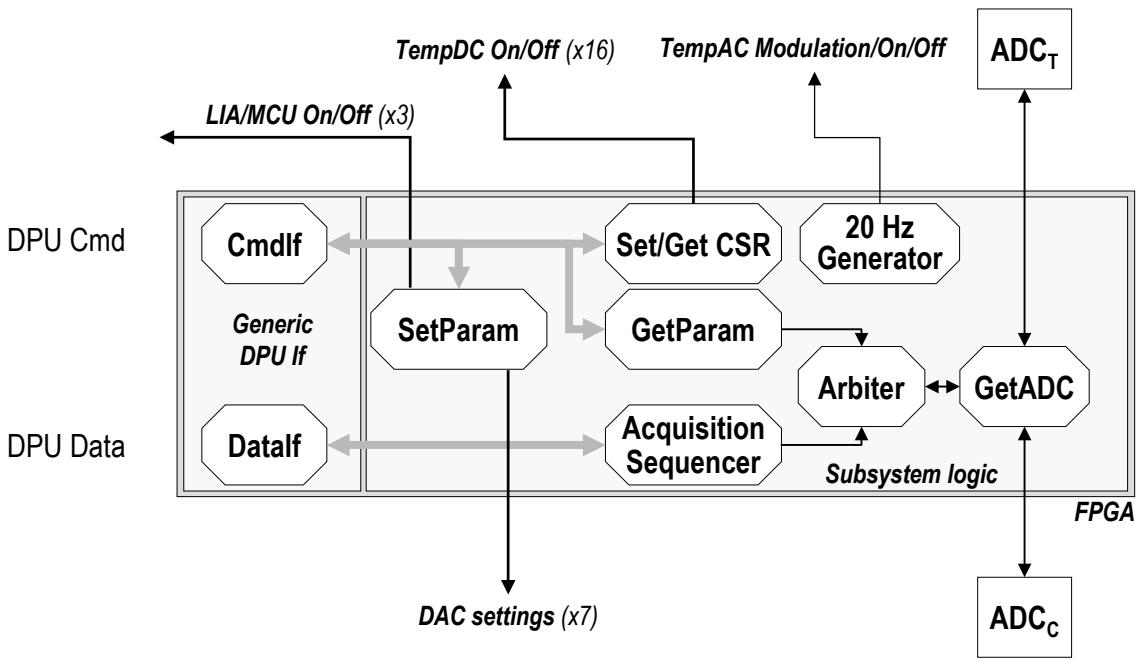
[…] is set for optional FIFO Implementation

Generic subsystem interface: functions

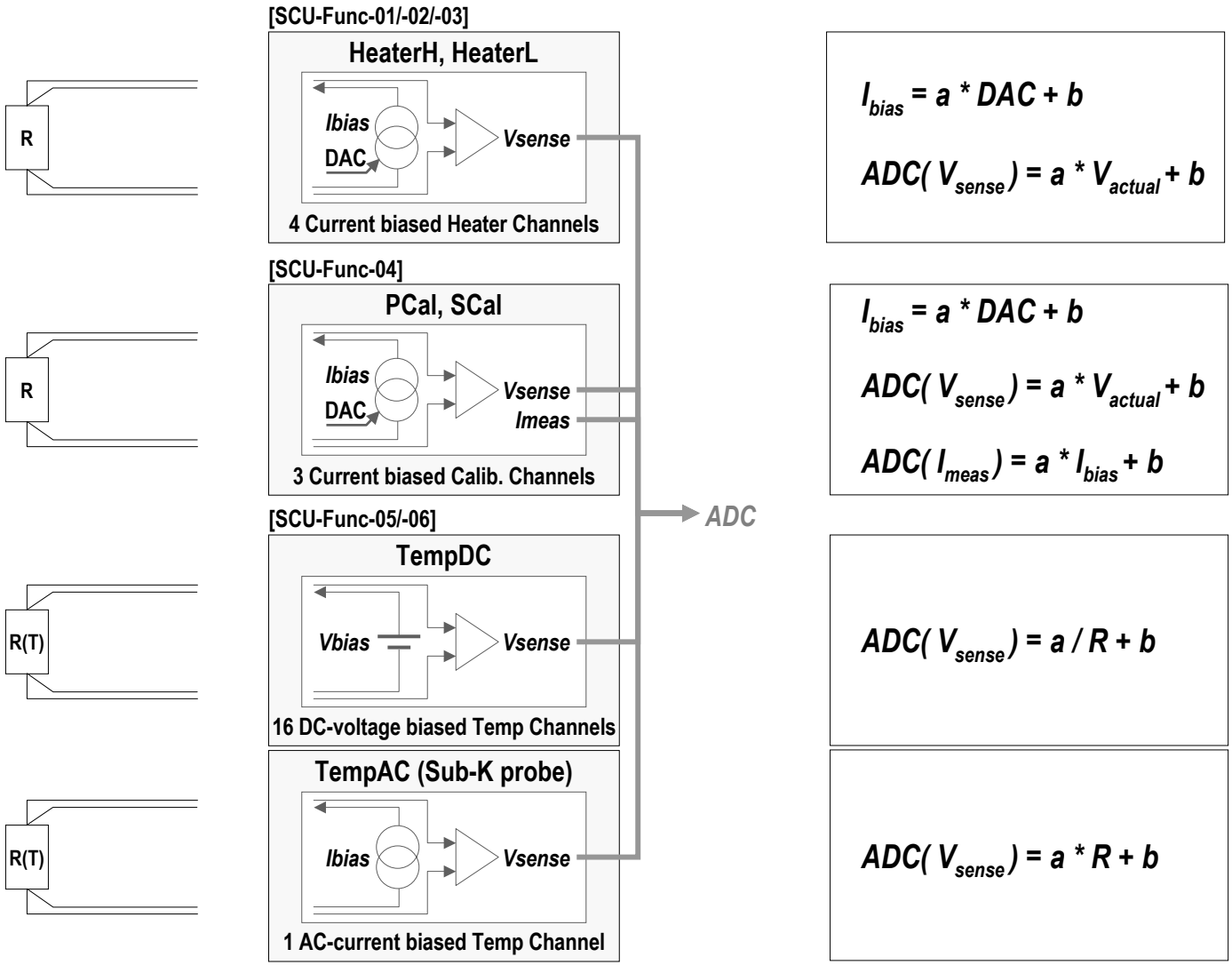
- **Intfce**
  - Virtual component
  - VHDL RTL for synthesis (ACTEL RT54SX32-S FPGA target)
- **CmdIf**
  - Runs with DPU 312.5 kHz Clk alone
  - Deserialises Cmds, serialises Ack
  - Filters local/subsystem commands
  - Supports simple, asynchronous handshake dialogue with subsystem
  - Handles subsystem handshake timeout
- **Timer**
  - Maintains Time Stamp
- **DataIf**
  - Runs from local oscillator
  - Supports [1.. 2.5] MHz data rate
  - Simple, synchronous subsystem word-based data interface
  - Appends Time Stamp and parity to subsystem data
  - Optional First In First Out subsystem buffer
    - *Synchronised by subsystem for frame transmission (Frame Sync)*

SCU subsystem logic

- **Parameter access**
  - Access to all parameters through Cmd interface (GetParameter)
- **Data frame sequence**
  - 0 (infinite),1 .. 31 frames per sequence
  - 0.3125 .. 80 Hz frame frequency
  - Word-per-word transmission (no frame buffer)
  - Maximum analogue parameter collection interval: less than 6 ms
  - Pseudo-random test pattern capability

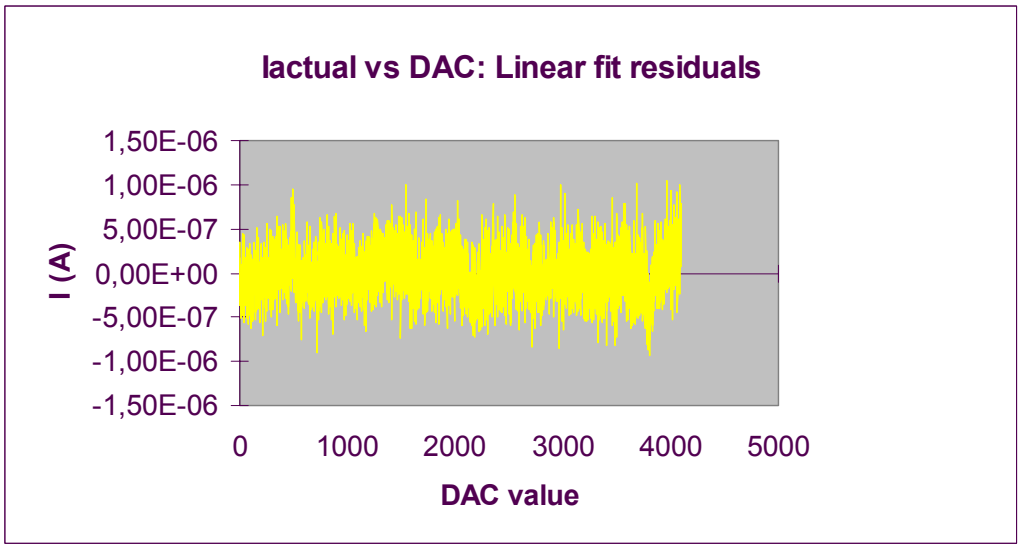


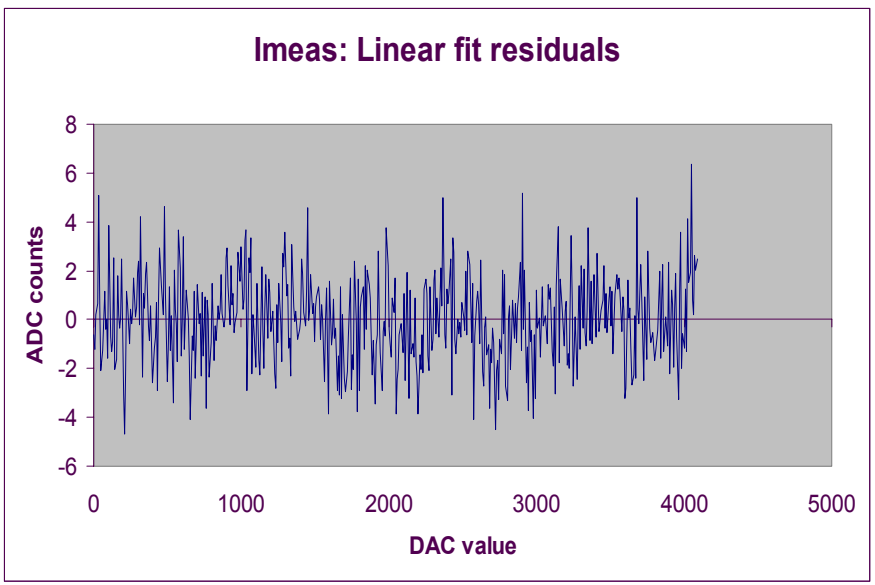
Analogue measurements

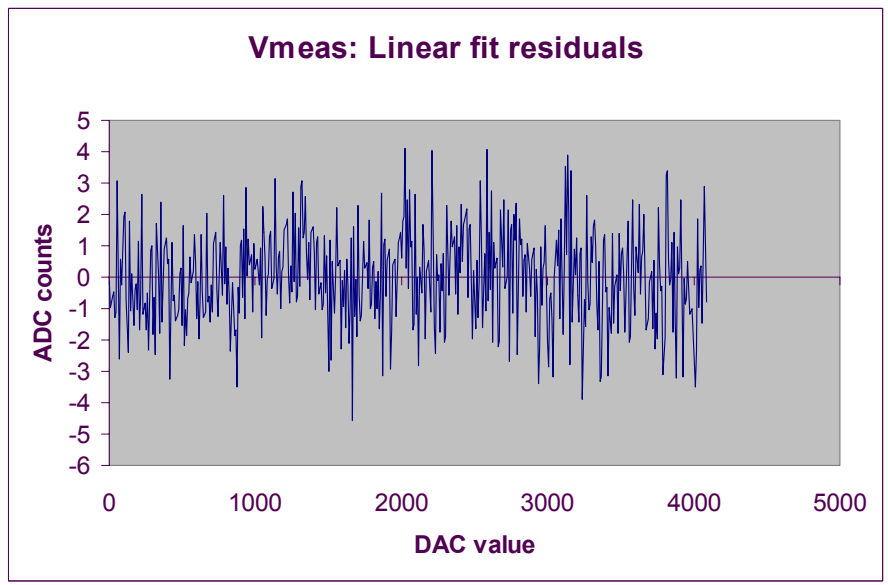


Calibrator prototype: Linearity

- Linearity test at 25°C

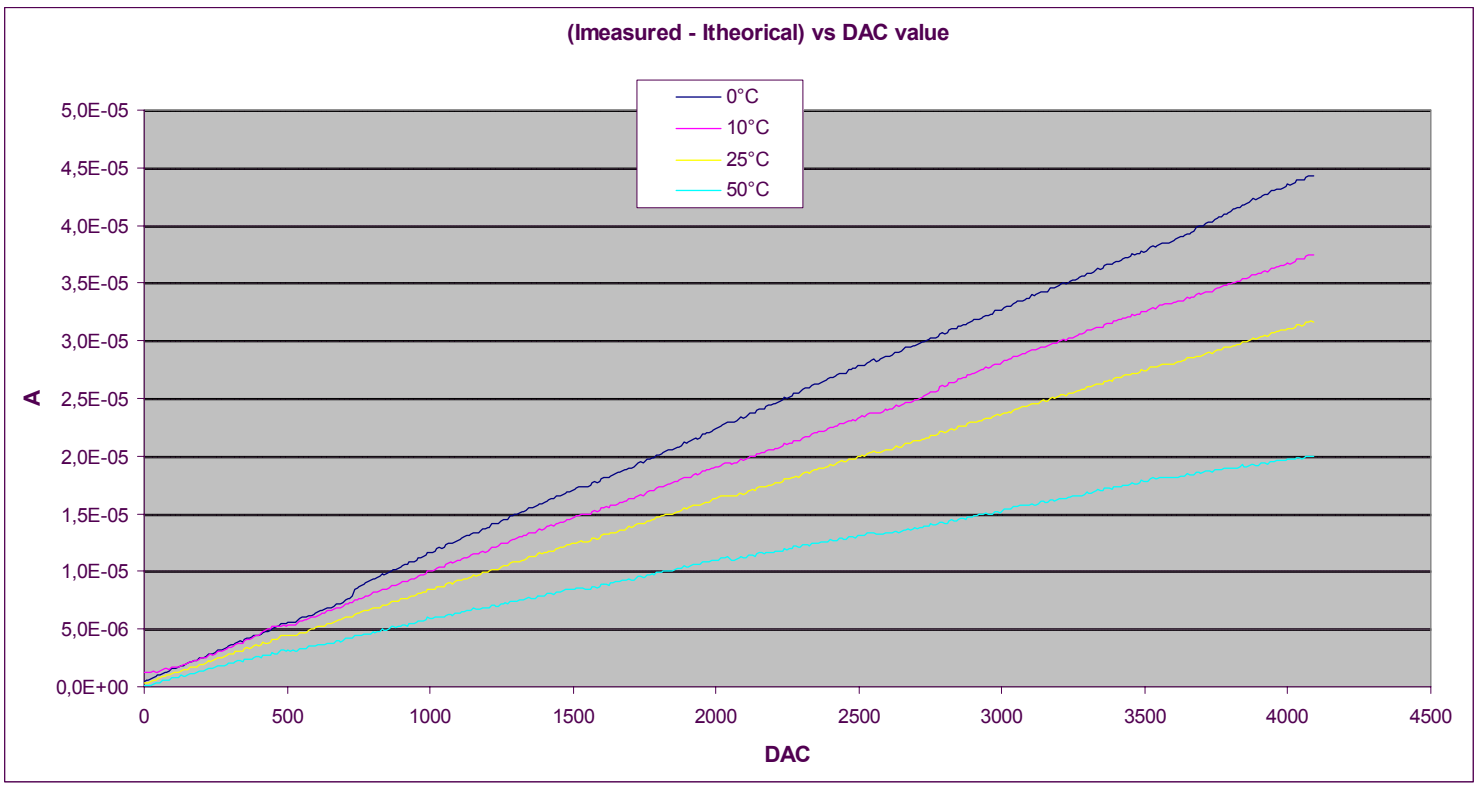




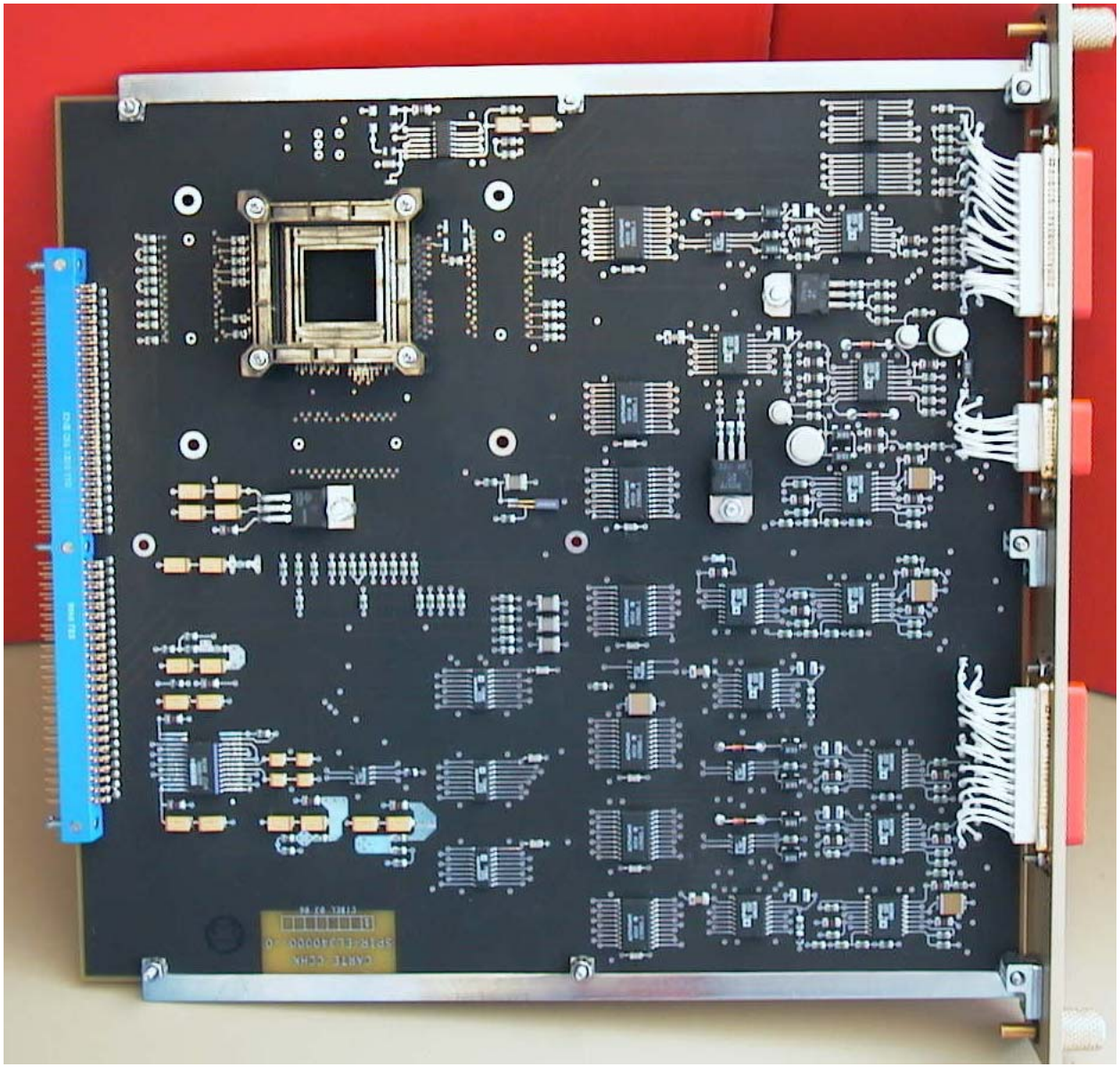


Calibrator prototype: Stability

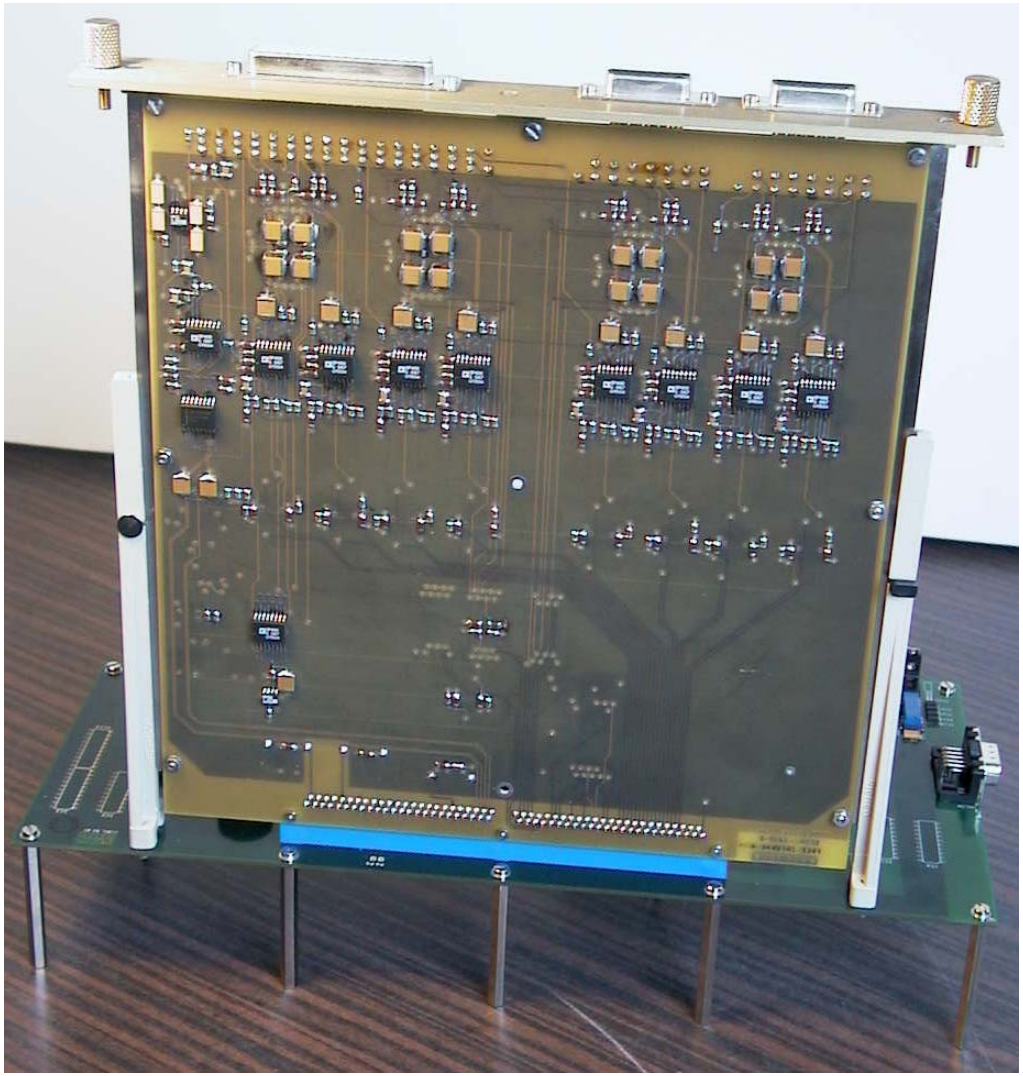
- **Variation with temperature**
  - 4% of the stability budget
  - Prototype current variation: 25uA/50°C@9mA
  - corresponding relative dependence: < 60 ppm/°C.
  - Specification for relative stability: < $5.E^{-3}$/h (maximum temperature drift: 3K/h).
  - Without correction: <4% of the total stability budget
    - *(180 ppm of the requested 5000 ppm/h).*

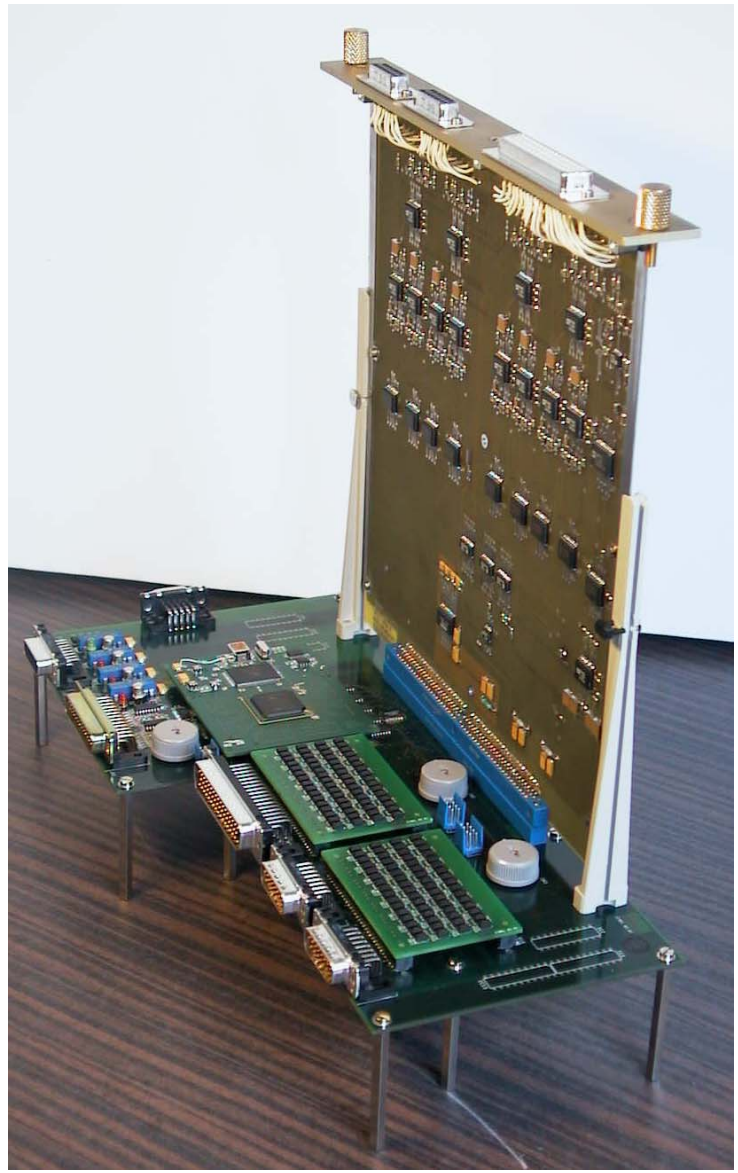


Boards: Cchklf



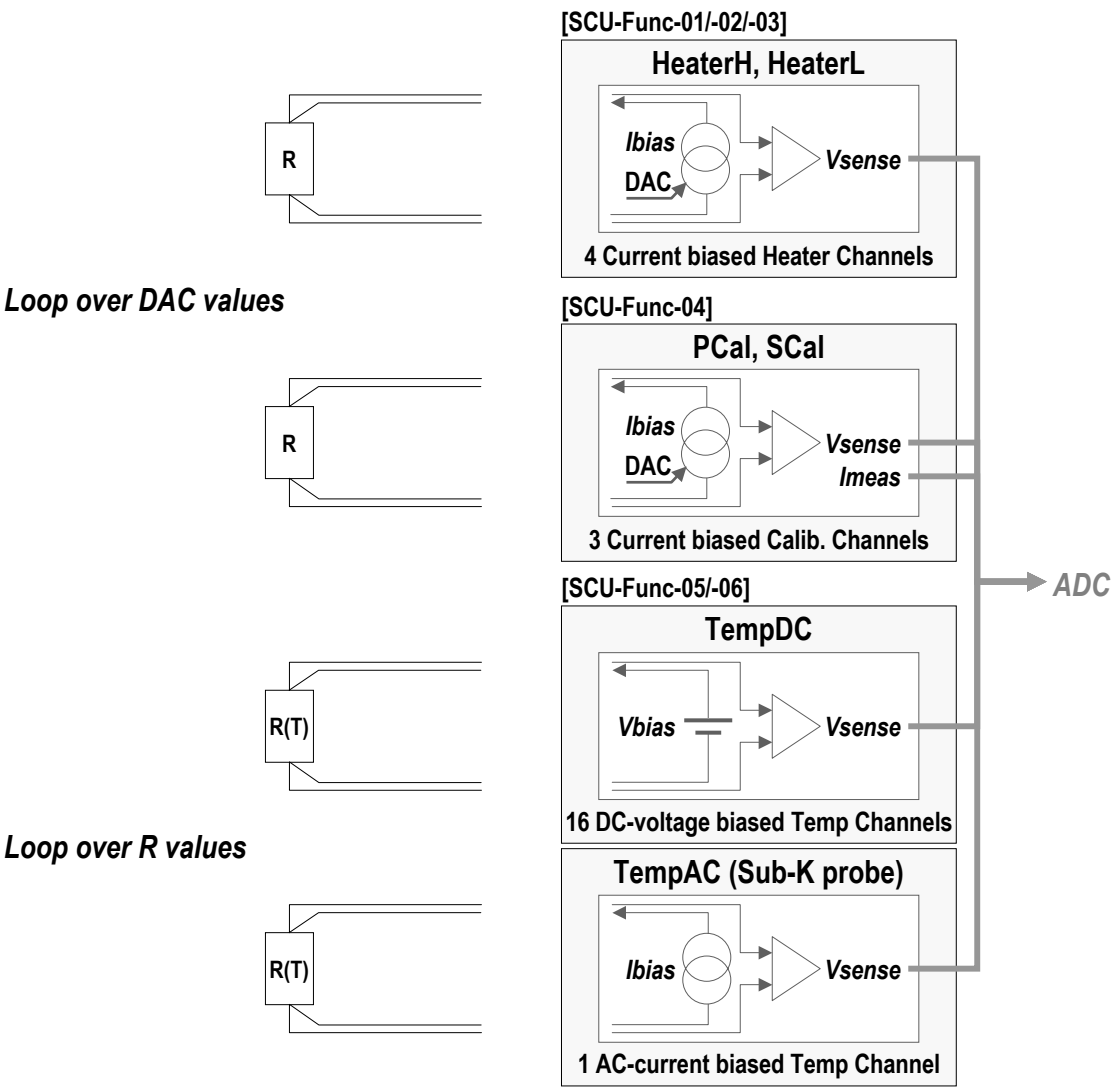
Boards: Temp





Test : measurements

Linear regressions: Measure
- *Slope (a)*
- *Intercept (b)*
- *Residuals*



$I_{bias} = a * DAC + b$

$ADC(V_{sense}) = a * V_{actual} + b$

$I_{bias} = a * DAC + b$

$ADC(V_{sense}) = a * V_{actual} + b$

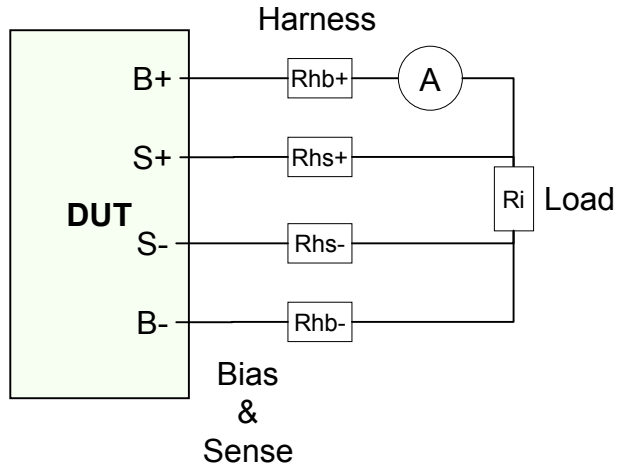
$ADC(I_{meas}) = a * I_{bias} + b$

$ADC(V_{sense}) = a / R + b$

$ADC(V_{sense}) = a * R + b$

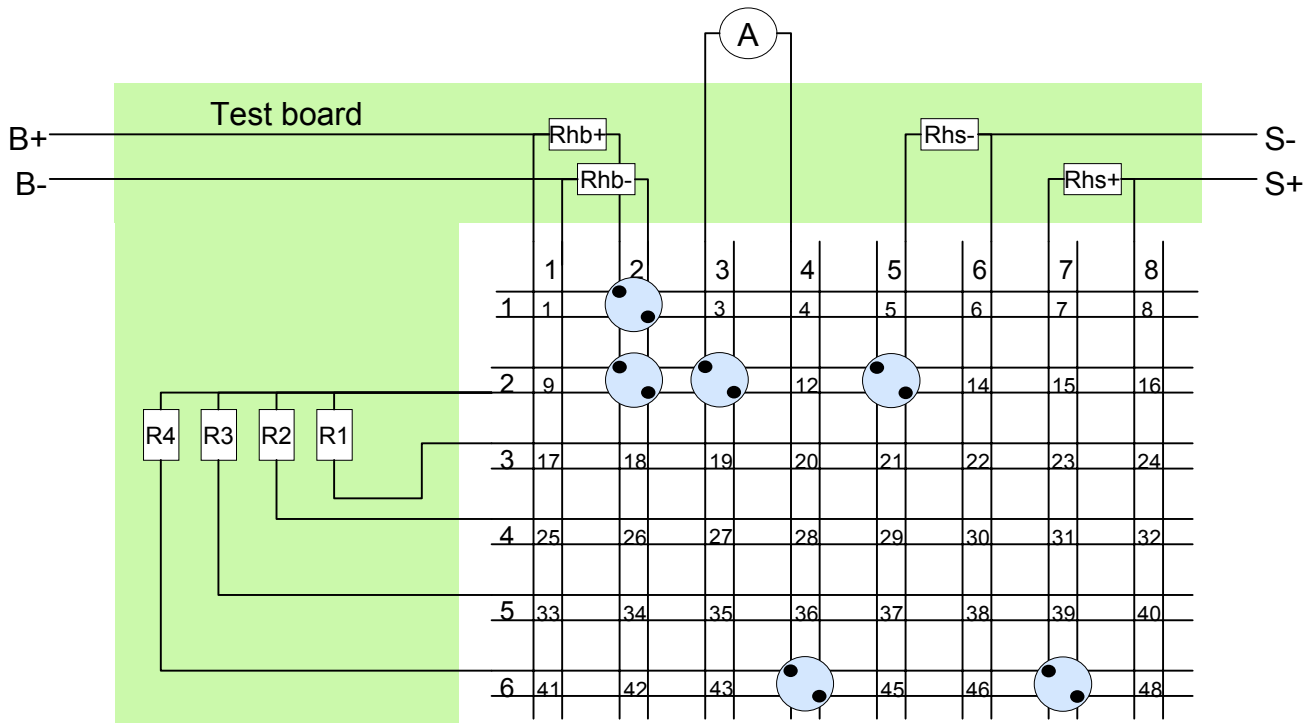
Test : principle

- **Generic circuit (all channels)**
  - Variable load for calibration of a 4-wire measurement circuit
  - Possibility to insert/bypass Rh resistors (to model the harness resistance)
  - Possibility to select one out of several reference loads Ri
  - Path to measure current in a separate ammeter

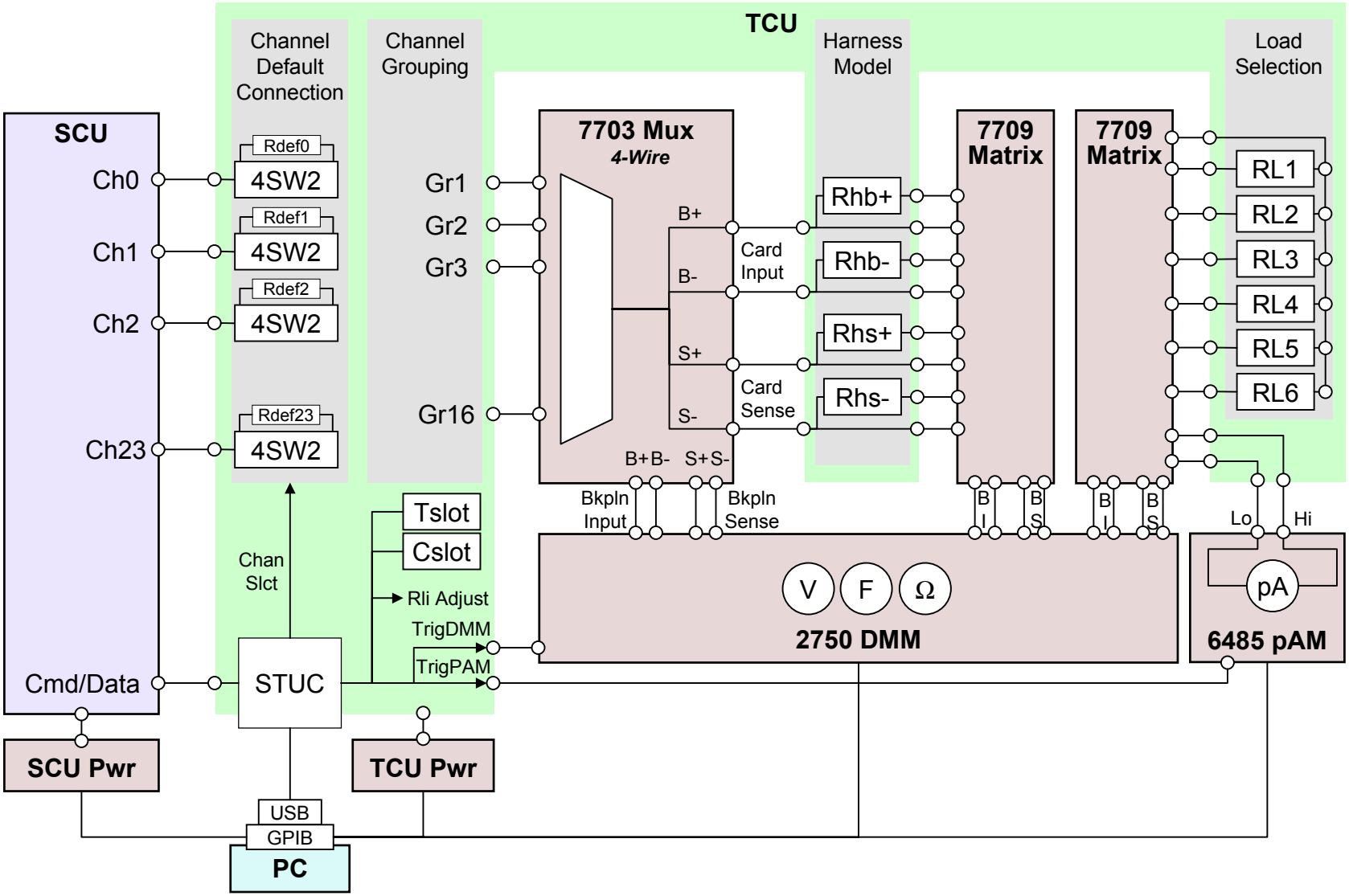


- **Matrix connections**

- **Example**
  - Rhb+, Rhb- inserted
  - Rhs+ inserted
  - Rhs- inserted
  - R4 load selected

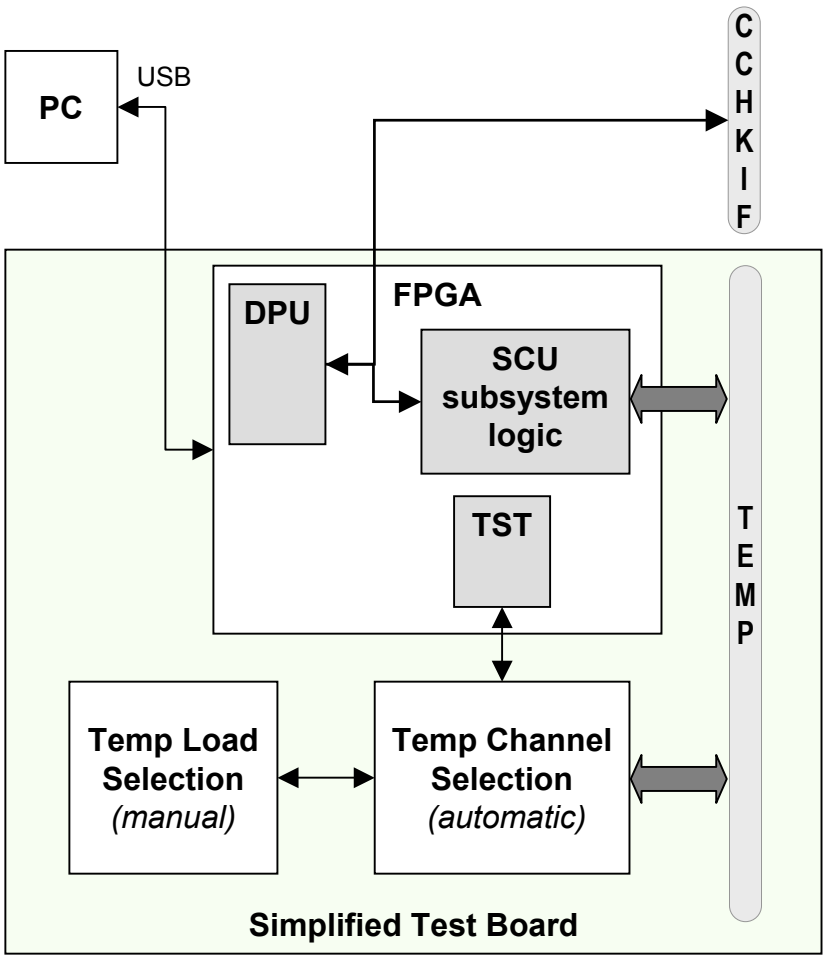


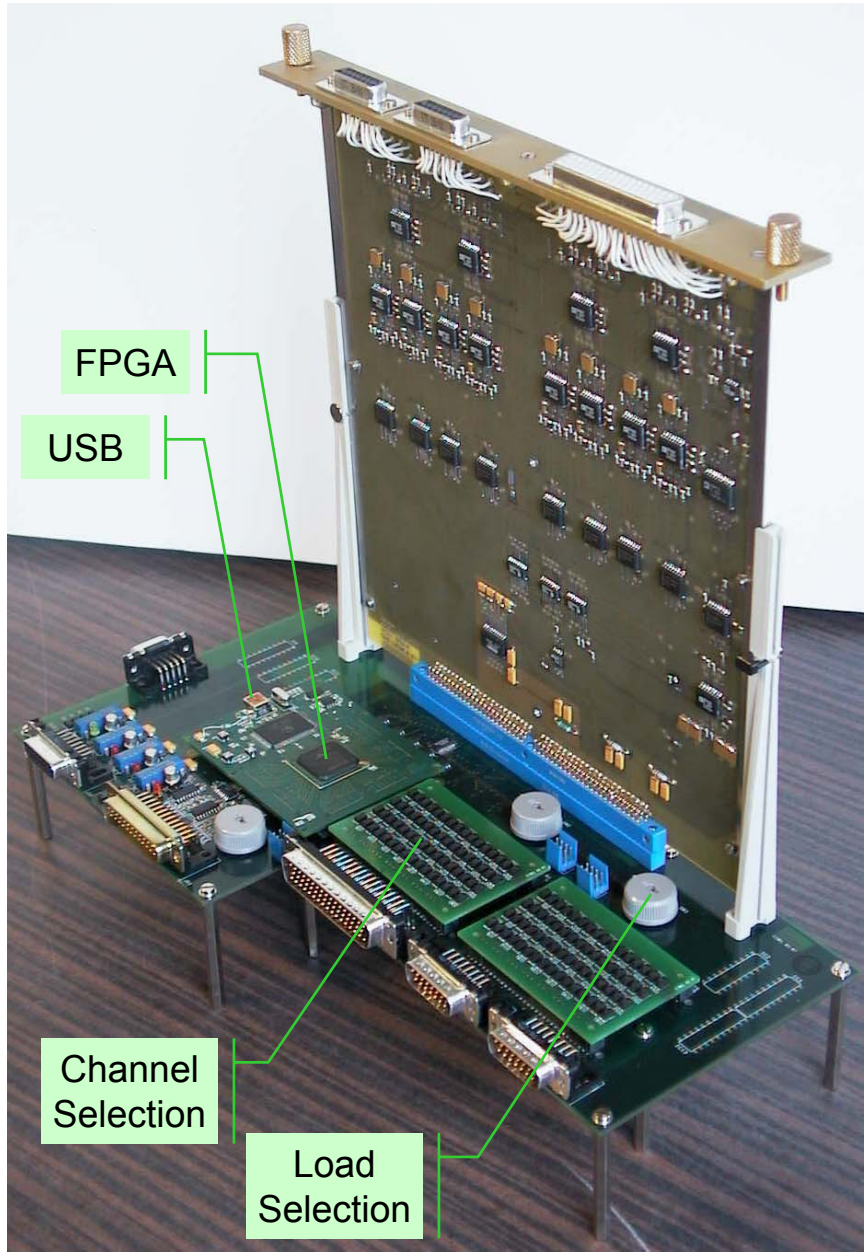
QM2/FM Test : Automated setup



QM1 Test : Simplified setup

- Direct test of Temp board
  - *DPU host interface in FPGA*
  - *Nominal Subsystem logic in FPGA*
- External Test of CchkIF
  - *fixed loads*





Status (QM1)

- **Board design**
  - Completed
- **FPGA design, simulation, Place & Route validation (Actel)**
  - Completed
- **Test preparation**
  - Hardware (Simplified Test Board)
    - *Ready*
  - Software
    - *Primitives (Host commands)*
      - Completed
    - *Application (measurement loops)*
      - In progress
    - *Measurement analysis (simple linear regression analysis)*
      - « Manual » process for QM1
- **Test activity & report**
  - March-April 2003

Mechanisms Control Unit

D. Pouliquen

Laboratoire d'Astrophysique de Marseille

MCU

The MCU controls the SMEC and the BSM mechanisms.

The MCU is designed and developed at LAM with the cooperation of UKATC for the BSM part and of CEA-Sap for the DRCU part.

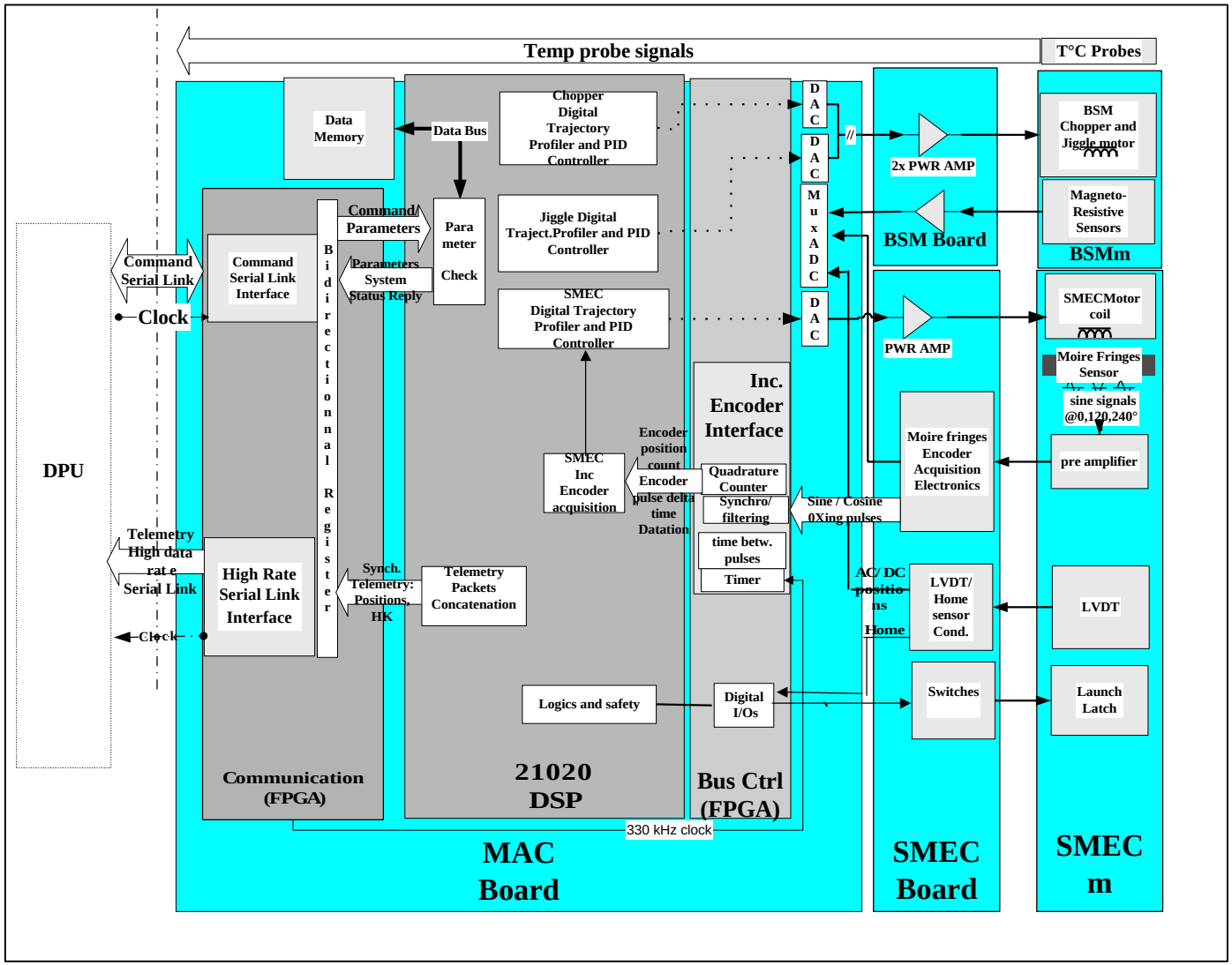
- Based on a DSP 21020, with assembly language software
- Controls 3 axis : 1 for SMECm and 2 for BSM

The MCU comprises 6 boards mounted in the FCU:

- 2 Multi Axis Controller boards (nom+red)
- 2 Spectrometer MEChanism board (nom + red)
- 1 Beam Steering Mirror board (nom+red on the same board)
- 1 backplane board.

MCU : short description (1/3)

- DSP 21020 + mechanism control software
- Interfaces with DPU = one FPGA for both the TM and the TC.
- One analogue board per mechanism to condition the signals to and from the mechanisms (position signals, actuator currents)



MCU : short description (2/3)

SMECm Optical Encoder Position Acquisition

Calculated on the basis of the 3 sine optical encoder signals after pre-amplification, conditioning to be read directly by the DSP via a multiplexed 16 bits ADC for arctangent calculation.

SMECm Optical encoder LED control

Because of the possible decay of flux emitted by the optical encoder LED due to ageing, 8 possible current levels can be set by the MAC board through the digital I/O port (3bits encoding).

SMECm Degraded mode control using the LVDT

For R=100 travel (+/- 3.2 mm)

signals acquisition is done on the SMEC Board and digitised by a 16 bits multiplexed ADC converter

useful range of the LVDT measurement with nominal linearity = +/- 2.54mm extended at twice this length with poorer linearity performance.

SMECm Degraded mode control using the motor back emf

For a complete SMEC mechanism travel

Uses the mechanism stiffness law

permits a velocity control of the mechanism only.

MCU : short description (3/3)

BSM Position = measured by magneto resistive signals

BSM Movement = angular travel in two orthogonal axes. Performed with actuators

BSM Control =

- digital conventional PID (3-term) controller - with corrections for cross-coupling between axes- in the MAC Board.
- Each axis can move independently. Typically, a step command waveform is assumed, and above a certain amplitude (10% of peak), it is profiled to produce a sinusoidal acceleration demand.
- The movement with respect to time is profiled via stored parameters to give a minimum energy, minimum noise position change, particularly for step commands. In general the movements are repetitions of the same position/time profile.
- In addition, in the event of measured behaviour resulting in a fault diagnosis, some system backup procedures are available. Diagnosis of excessive position errors and analysis of recorded transient behaviour during operation can result in modifications to the control system by uploading different parameters.

MCU : Design change since MCU DDR (Oct 2001) [1/3]

- **Addition of boards temperature measurements**

  One temperature sensor added on each nom and red card

  Total = 6 sensors (no sensor on the backplane)

- **Method of SMEC mechanism speed control with the optical encoder revised:**

  the optical encoder zero crossing counting is done exclusively by software. It was previously done by hardware.

  => suppresses offsets adjustments in the hardware

  => simplifies the hardware

  => simplifies the control software

  ECR issued and accepted

  Modification being implemented

MCU : Design change since MCU DDR (Oct 2001) [2/3]

- **Damping of the SMEC mechanism**

  One relay added that short circuits the coils when no power available

  When one coil in use, the other one remains short circuited

  Provides damping to improve the mechanism control

  Prevents the mechanism from banging against the mechanical stop in case of sudden power failure

- **Suppression of the BSM launch latch**

  due to successful vibration tests of the BSM without launch latch

  => simplifies the BSM board

  => erases a problem with the SPIRE harness

MCU : Design change since MCU DDR (Oct 2001) [3/3]

- **Introduction of a BSM damping for launch**

  The need is not clear. Complement of study under progress at UKATC.

- **Introduction of a BSM damping for control**

  Control easier with little dampening => introduction of a resistance in the actuators coils circuit. Done on the QM1, perhaps suppressed on further models.

Decisions concerning the BSM to be taken this week with UKATC and SPIRE system team

MCU : Interfaces documents

- **DRCU ICD Sap-SPIRE-CCa-075-02 Issue 1.0**, 14 Feb 2003

  => MCU / DPU, MCU / PSU and MCU / Mechanisms electrical interfaces

  => MCU command list

- **SPIRE Harness Definition Document,** SPIRE-RAL-PRJ-000608 Issue 1.1, 8 July 2002

  => Mechanisms simulator electrical interfaces (pin out = mechanisms connectors pin out, Sub D connectors)

- **SPIRE FCU MICD,** SPIR-MX-5200-000 Issue E, 26 Sep 2002

  => MCU Connectors position, reference axis, etc…

- **SPIRE Rack type LIA – Plan d'interface,** SPIR-MX-5110-000 Issue A, Oct 2001

  => MCU boards mechanical interfaces

MCU : the models [1/2]

➢ QM0 : for communication tests

- Built at LAM
- New model introduced for planning reasons
- Form & fit, electrical, command interface & flight functions Ok
- ALTERA FPGA including CEA DAPNIA Communication VHDL issue 0.4
- Commercial components, no redundancy
- Not suitable for mechanisms control
- Delivered with mechanisms simulator and cables

➢ QM1 : for CQM tests

- Built at LAM
- Same as QM0 plus mechanism control capability
- To replace the QM0 in the FCU QM1

After QM1 delivery, the QM0 comes back to LAM and can be refurbished at QM1 level.

MCU : the models [2/2]

➢ QM2 : Used to qualify the electronics

- Sub contracted by LAM
- QM2 design = QM1 design
- Form & fit, electrical, command interface & flight functions Ok
- Military components, redundancy
- ACTEL FPGA including CEA FPGA Communication VHDL (black box) issue TBD
- Delivered with mechanisms simulator and cables

QM2 to be used with FPU FM as FCU FM not available on time

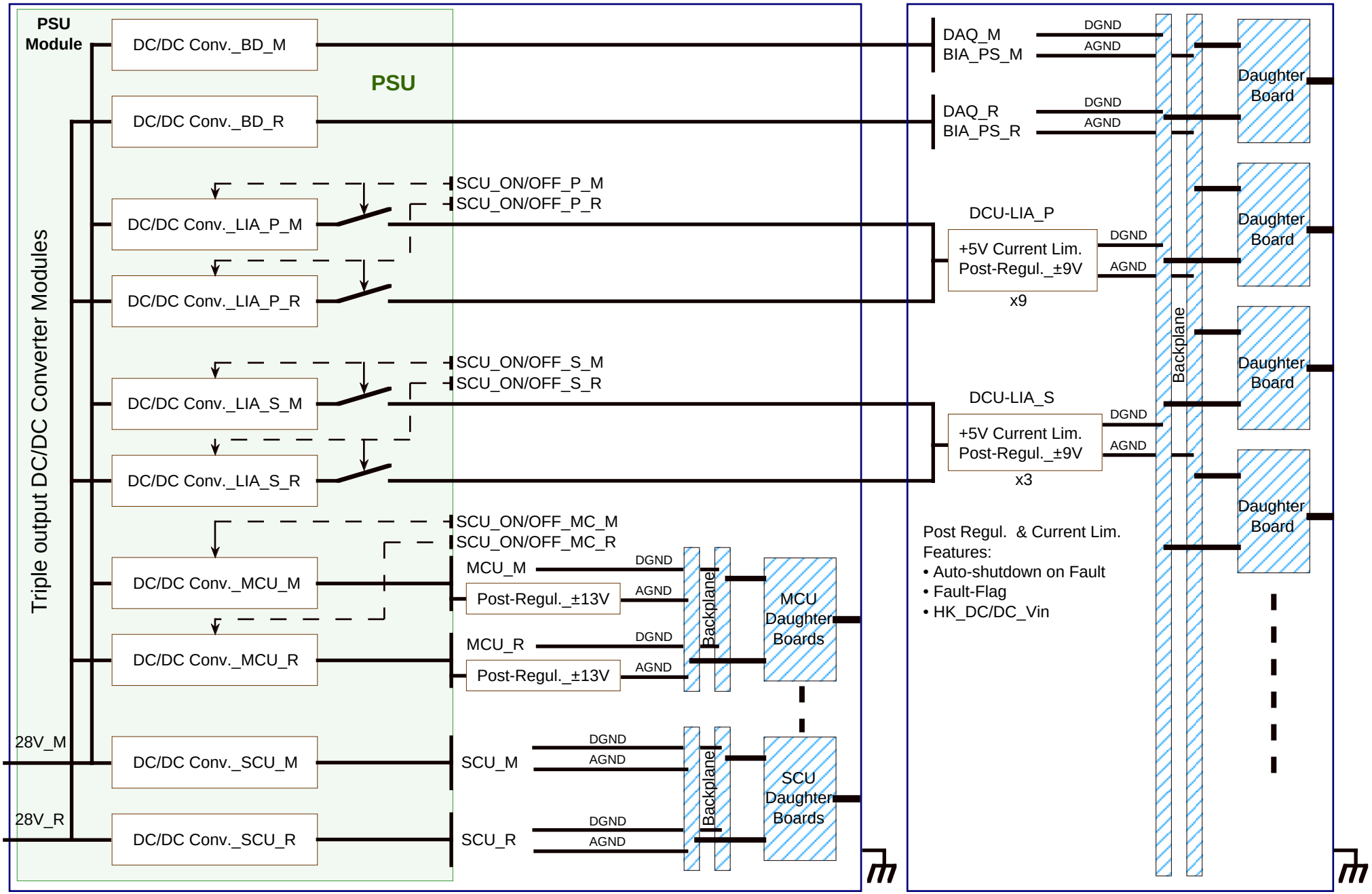
➢ FM and FS

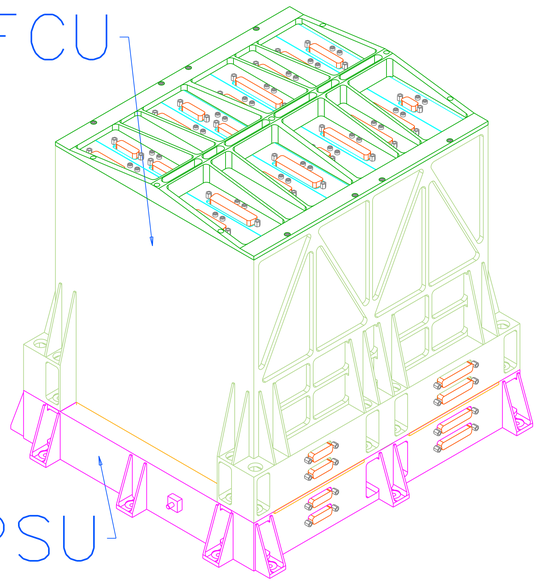
- Complete flight models
- Sub contracted by LAM (same contract and contractor as for the QM2)

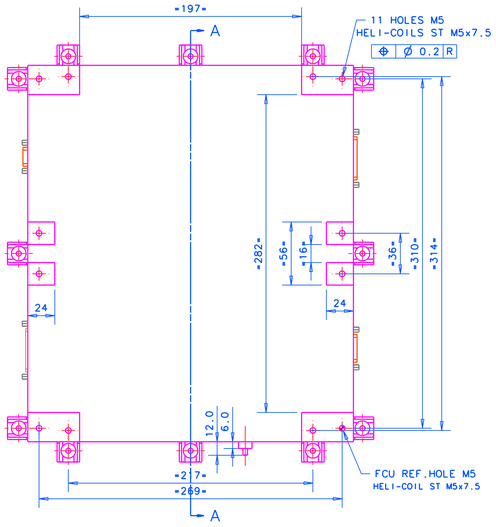
All MCU models to be delivered by LAM to CEA

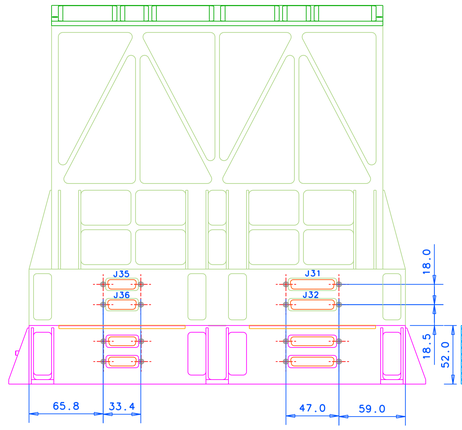
DS-20/06/02

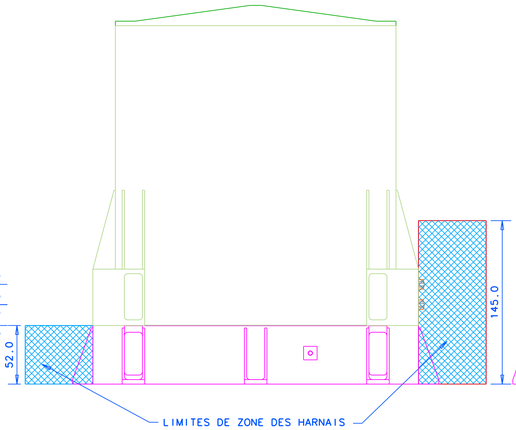
SPIRE PSU_DRCU Power/Grounding Implementation

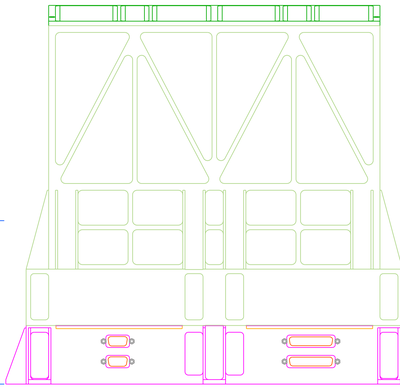


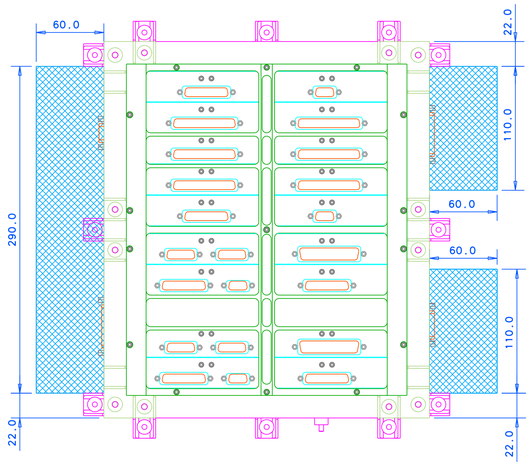


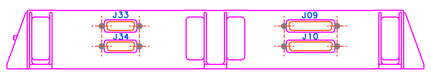


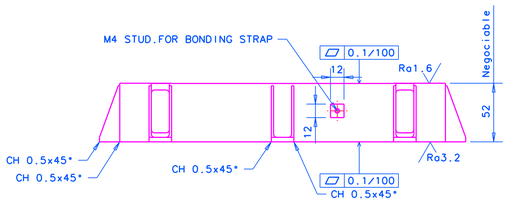


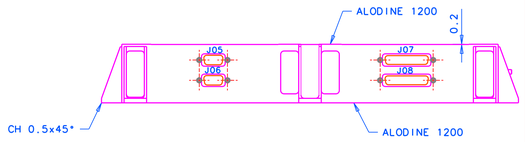


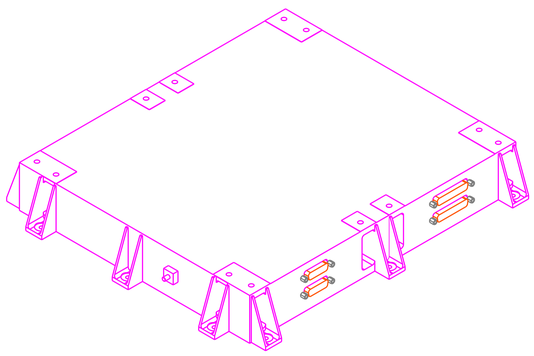


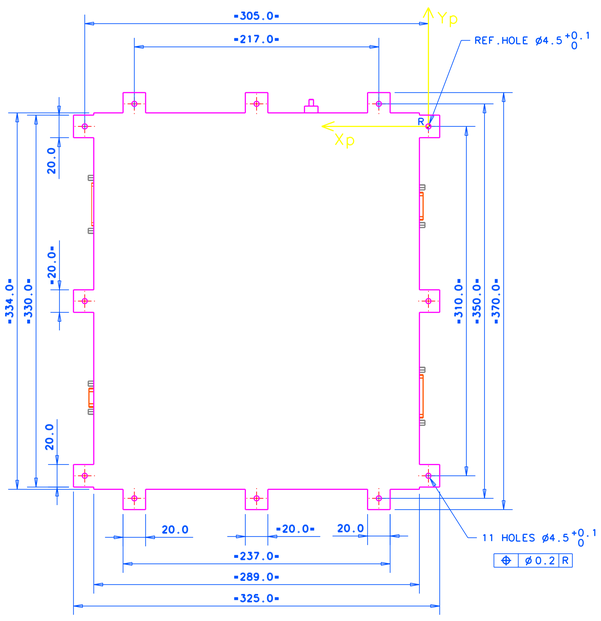


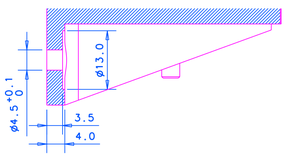








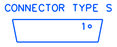




COUPE PARTIELLE A-A ECH:2

CONNECTOR TYPE P

CONNECTOR TYPE S



CONNECTORS		
IDENT	TYPE	FUNCTION
J05	DEMA 9P	PSU-M/PCDU-M
J06	DEMA 9P	PSU-R/PCDU/R
J07	DBMA 25S	PSU-M/DCU
J08	DBMA 25S	PSU-R/DCU
J09	DBMA 25S	PSU-M/MCU-M
J10	DBMA 25S	PSU-R/MCU-R
J33	DAMA 15S	PSU-M/SCU-M
J34	DAMA 15S	PSU-R/SCU-R

indice	Modifications	Date	Dessiné par	Vérifié par	Approu
B	Mise à jour connecteurs	09/02	DHENAIN		
A	Origine	07/02	DHENAIN		

Spécifications particulières

tolérances générales: Indice de rugosité général XXXX — SOUS-TRAIT; Tol.ang.: ±XX°; Casser les angles vifs

Matière: — Protection

Traitement thermique: — Echelle 1/2 — Poids — Niveau qua

SPIRE HSFCU
PSU BOX
MECHANICAL INTERFACE CONTROL DRAWI

SAP/GERES
Tel:01.69.08.78.25
01.69.08.59.76
Fax:01.69.08.79.96

COMMISSARIAT A L'ENERGIE ATOMIQUE — C.E.N SAC

AO — SPIR-MX-5600 000 B

HERSCHEL—SPIRE

FCU-PSU

Model policy:

STM

• Will contribute to the qualification of the FCU box
• Secondary Power supplied by an external power bench

EM

• Not a deliverable item
• Compliant Mechanical and Electrical I/F
• Will be used by the contractor for verification purposes, test of corrective actions…
• Will be borrowed for electrical compatibility test at Saclay

FM

• Flight compliant

Spare

• PCB or part level
• FM repaired and tested at acceptance level within 3 weeks

Expected Schedule:

• ITT in progress, first answers by the end of March

• Market rules completion and kick-off by the end of June (CEA-CCM calendar)

• FM delivery: kick-off + 14 months

AIV DRCU TEST PLAN

- OBJECTIVES (as defined in the development plan)
  - To check Sub systems Performances and Functions at the appropriate level before integration into the instrument,
  - To perform Qualification or Acceptance tests of all individual Sub-systems before integration into the instrument.

- MAIN STEPS

To fulfil the objectives, the AIV plan defines :

- the actions to be performed for each model following the model philosophy (STM, QM1, QM2 and FM),
- the sequencing of the actions performed on units for each model (Flow Charts),
- the detail of each AIV action together with the resources required (SADT diagrams),
- the kind of tests performed on each unit / sub unit to ensure test coherency (Test matrixes),
- the test equipments required for each test (harnesses, LTU, FPU, PB …),
- the documentation (test plans, logbooks, NCR …),

Henri TRIOU SPIRE AIV March 4th. 2003

Classification of AIV actions

The AIV Actions consist in :

Inspections (concerns items delivered by subcontractor) that involves :

Incoming inspections :

- Visual inspection to verify:
- Marking of the box and of the connectors, checking of the connector itself,
- Mechanical integrity of the box,
- Surface treatment status of the box,
- Review of the delivered documentation,

Incoming tests :

- Simplified functional tests.

Assembly that involves :

- Visual inspection,
- Electrical interface verification to check the compatibility (electrical mass, Back Plane isolation …),
- Mechanical assembly,Electrical tests,
- Simplified Functional tests

Integration of units that involves :

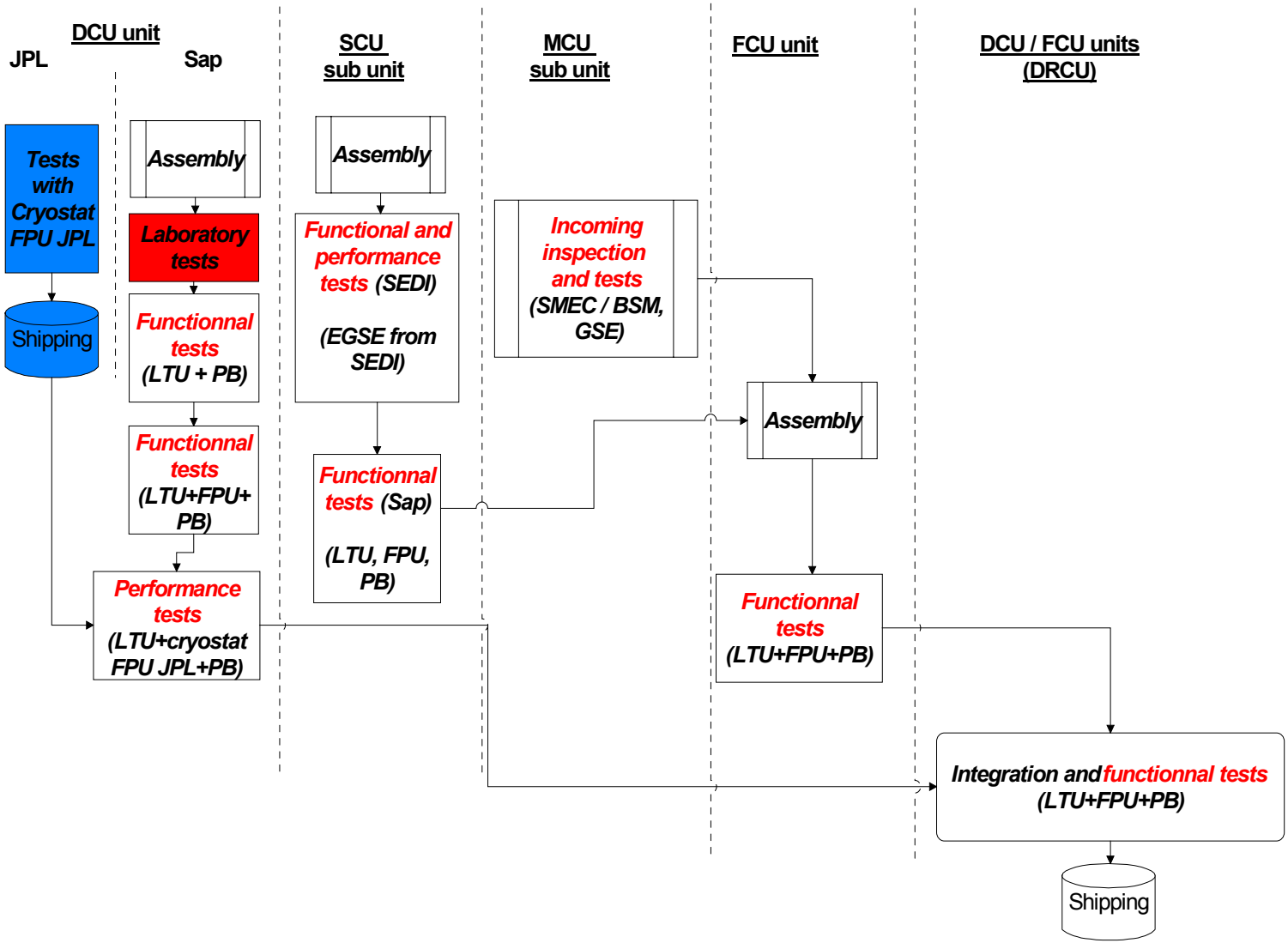
- Visual inspection,
- Electrical interface verification to check the compatibility of units
- Electrical tests

Functional / Performance tests following the system and interface requirements

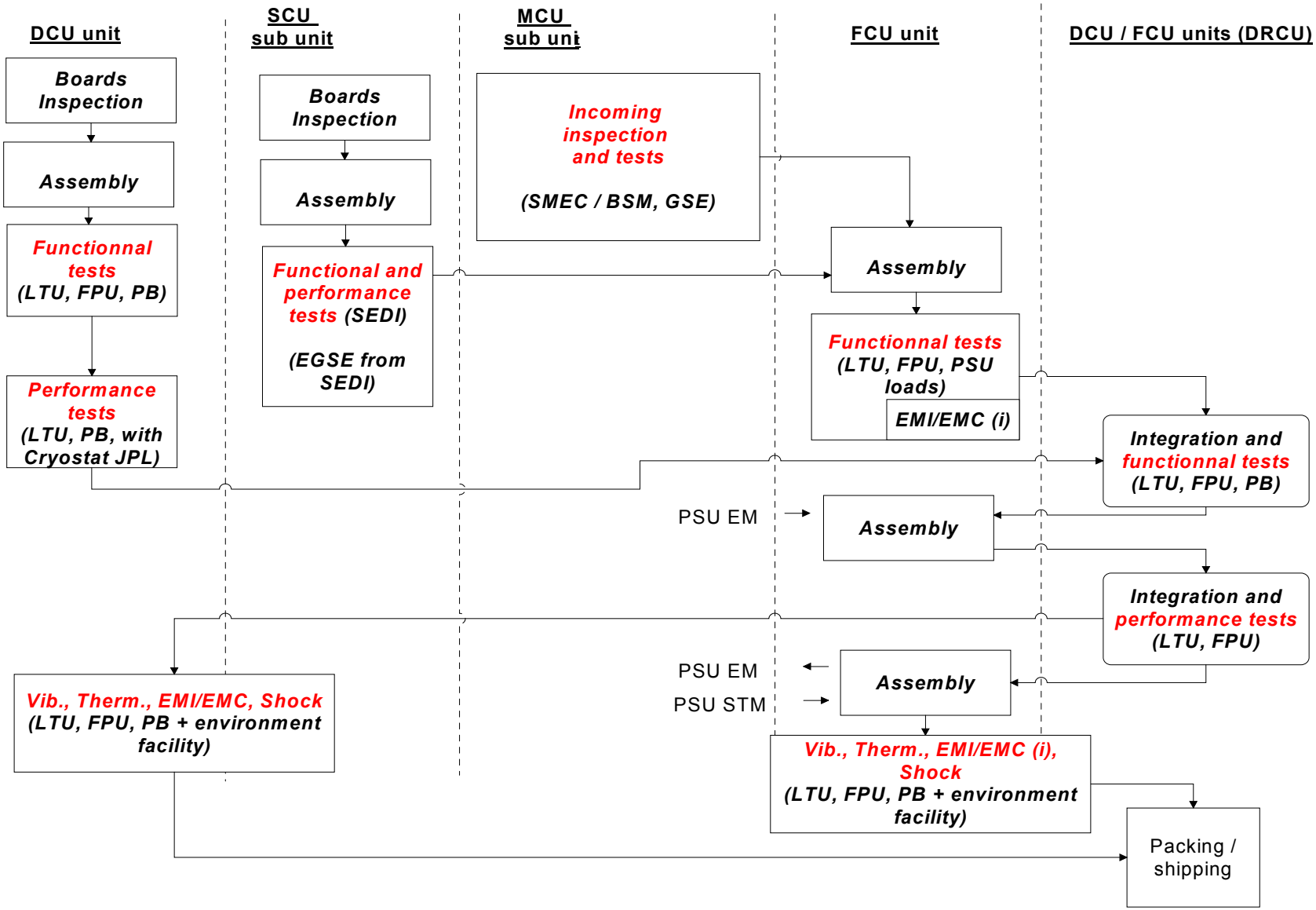
Qualification / Acceptance tests performed under environment conditions following the system and interface requirements

=> We then detail the AIV action flow charts for QM1, QM2 and FM models

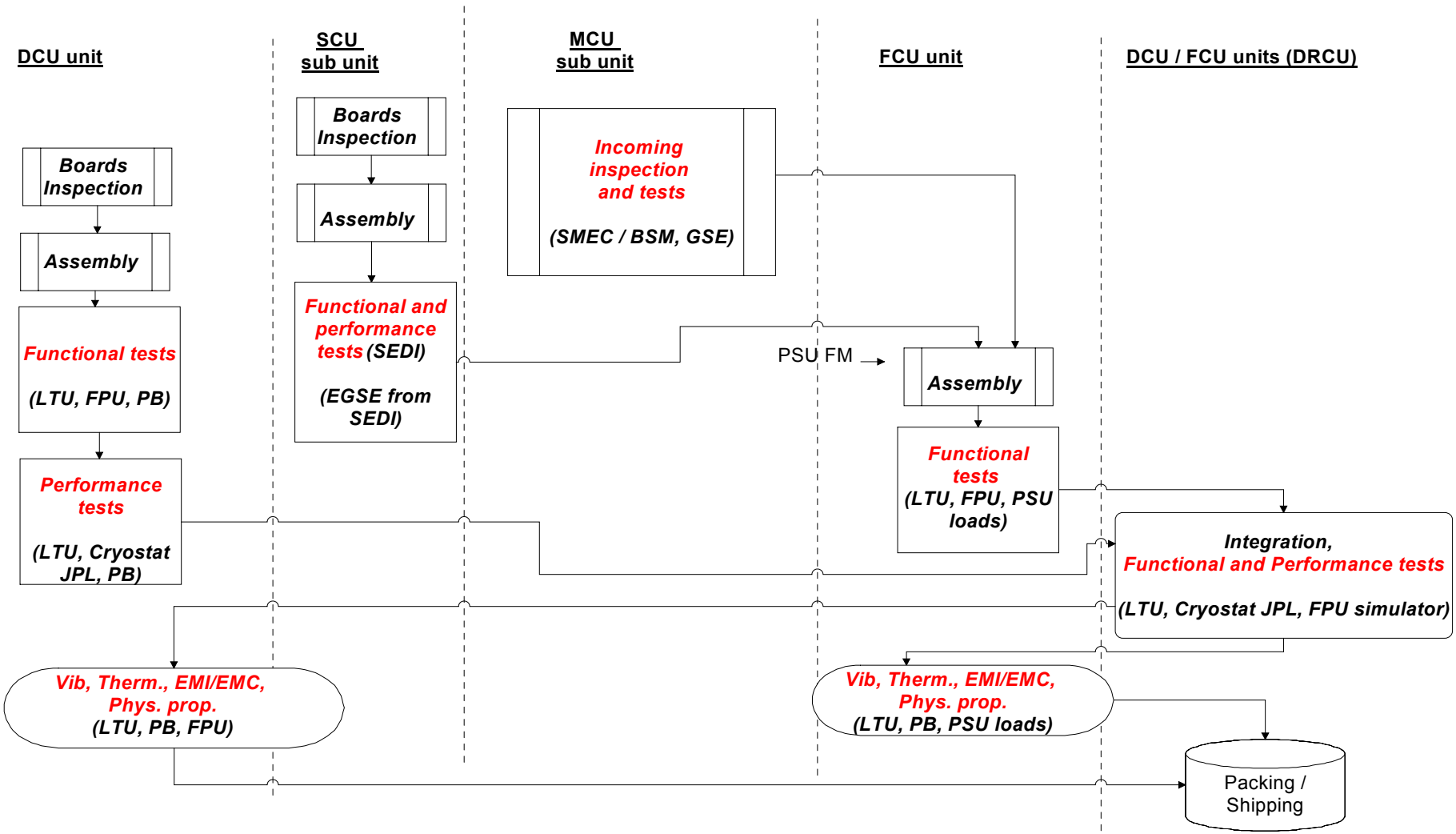
DRCU QM1 model flow chart (QM1 = test mean for CQM)



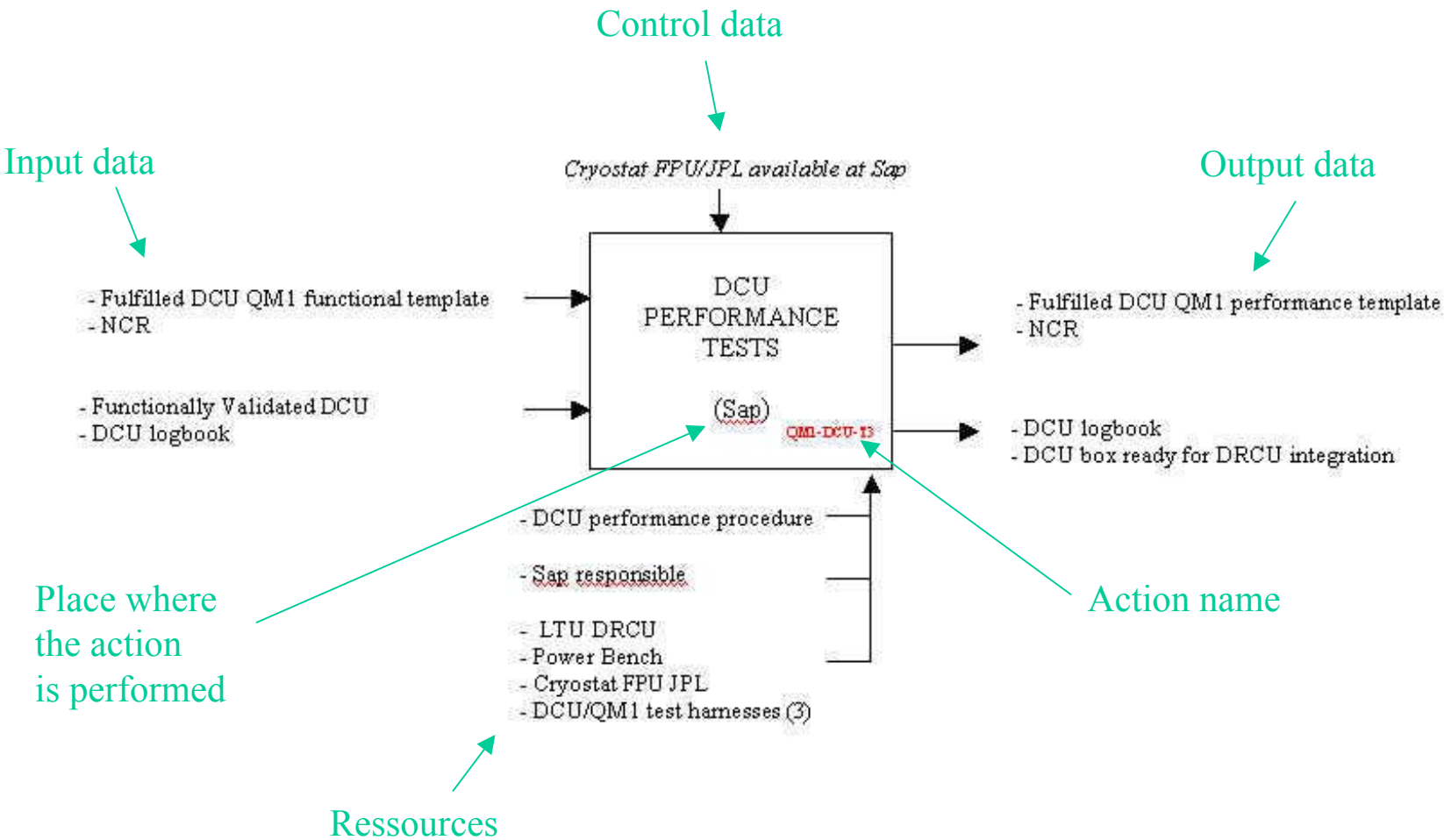
DRCU QM2 model flow chart (QM2 : to prepare integration)



DRCU FM model flow chart (For Acceptance tests)



SADT diagrams



Unit test matrix (DCU or FCU)

Test / Model	QM1	QM2	FM
Inspection	A	A	A(3)
Electrical tests	T	T	T(3)
Functional tests	T	T	T(3)
Performance tests	No Test	No Test	No Test
Vibration tests (*) Qualification level Acceptance level	No Test	T(2)	T(3)
Thermal balance tests	No Test	No Test	No Test
Thermal tests (*) Qualification level Acceptance level	No Test	T_V (2)	T_V (3)
EMI/EMC tests (*) Qualification level Acceptance level	No Test	T(0)	T(3)
Physical properties and conformance to MICD Acceptance level	No Test	No Test	T(3)
Shock	No Test	T(2)	No Test
Packing/Shipping	P	P	P

If FCU :

(0) *with PB*

(1) *PSU EM assembled with the FCU box*

(2) *PSU STM assembled with the FCU box and PB is used*

(3) *PSU FM is assembled with the FCU box*

Sub unit test matrix (SCU or MCU)

Test / Model	STM	QM1	QM2	FM
Inspection	NA	A	A	A
Electrical tests	NA	T	T	T
Functional tests	NA	T	T	T
Performance tests	NA	T	T	T
Vibration tests Qualification level Acceptance level	NA	NA	NA	NA
Thermal balance tests	NA	NA	NA	NA
Thermal tests Qualification level Acceptance level	NA	NA	NA	NA
EMI/EMC tests Qualification level Acceptance level	NA	NA	NA	NA
Physical properties and conformance to MICD	NA	NA	NA	NA
Shock	NA	NA	NA	NA

SCU QM1tests are performed by the SEDI.

For QM2 and FM models, tests are performed using the means and procedures delivered by the SEDI.

MCU performance tests are part of those realized by the LAM. Tests concern the inspection at delivery of the MCU in its FCU like box.

Integrated DCU / FCU test matrix

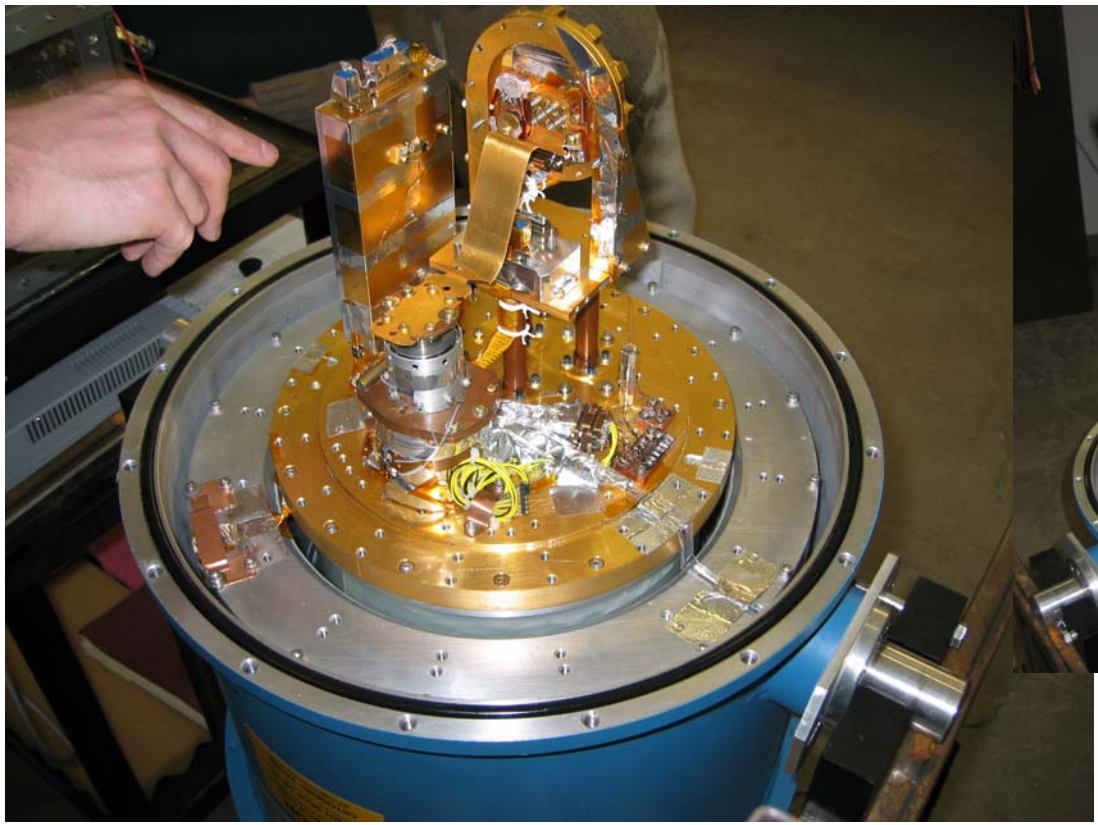
Test / Model	QM1	QM2	FM
Integration / verification	A	A	A(3)
Electrical tests	T	T	T(3)
Functional tests	T	T(0)	T(3)
Performance tests	NA	T(1)	T(3)
Vibration tests Qualification level Acceptance level	NA	No Test	No Test
Shock tests	NA	No Test	No Test
Thermal balance tests	NA	No Test	No Test
Thermal vacuum tests Qualification level Acceptance level	NA	No Test	No Test
EMI/EMC tests Qualification level Acceptance level	NA	No Test	No Test
Physical properties and conformance to MICD	NA	NA	NA

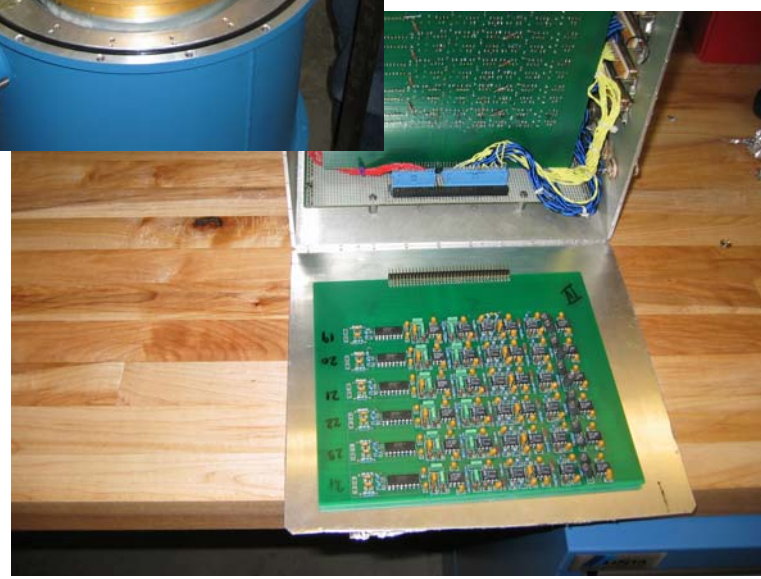
(0) *with the PB*

(1) *the PSU EM is assembled with the FCU box*

(3) *the PSU FM is assembled with the FCU box*

Tests with JPL Cryostat





Test of noise performances,
Housekeeping parameters,
Baccus Cryostat.

DRCU Programme Review
4th Feb 2003

Eric Sawyer

Topics

- DDR documentation
- Instrument development plan
- Instrument schedule
- Instrument status

Documentation

- Review process has been going for some time
- Documents reviewed, comments sent 30 Sept 02
- Response to comments received 2 Dec 02
- Latest documents issued 18 Feb 03
- Review of documents ongoing, but almost complete
- Most comments incorporated, some minor iteration required. Document standard very good

SPIRE development plan.

STM – No electronics, not deliverable to S/C

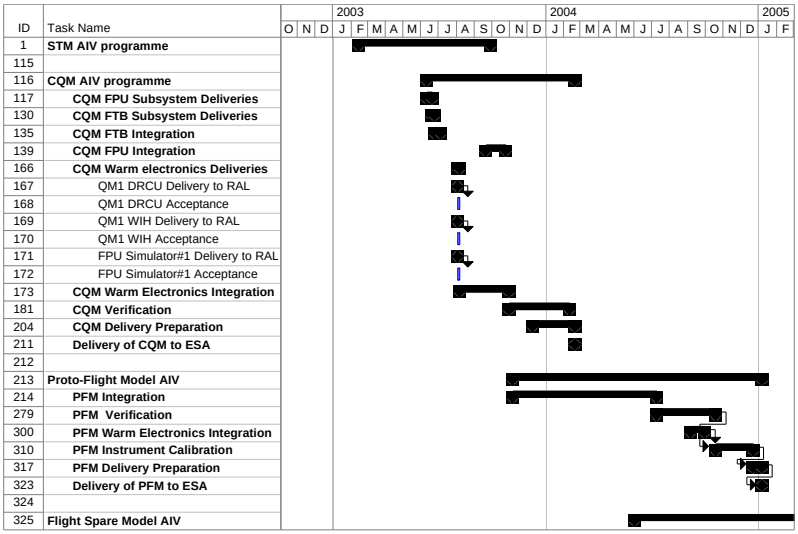
AVM – No DRCU, functions are within the FPU simulator. Deliverable to S/C.

CQM – DRCU required, QM 1. Deliverable.

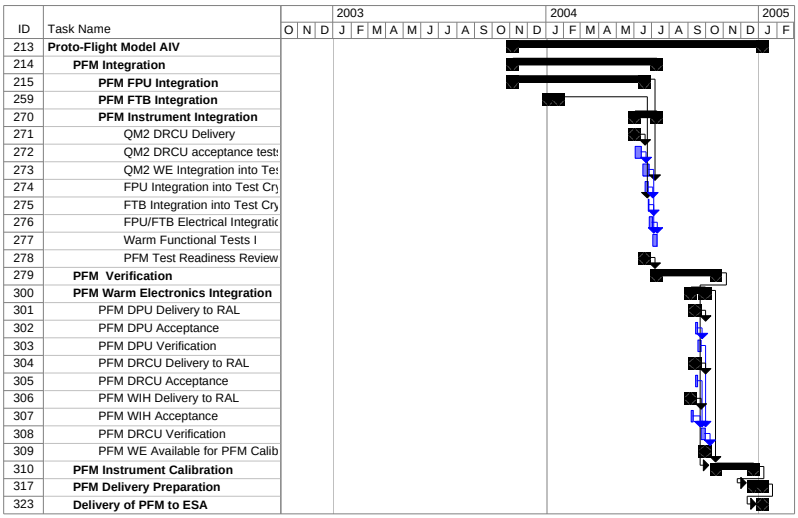
PFM - DRCU required, QM 2 to start then replaced by FM

FS - TBD

Overall instrument schedule CQM



Overall instrument schedule PFM



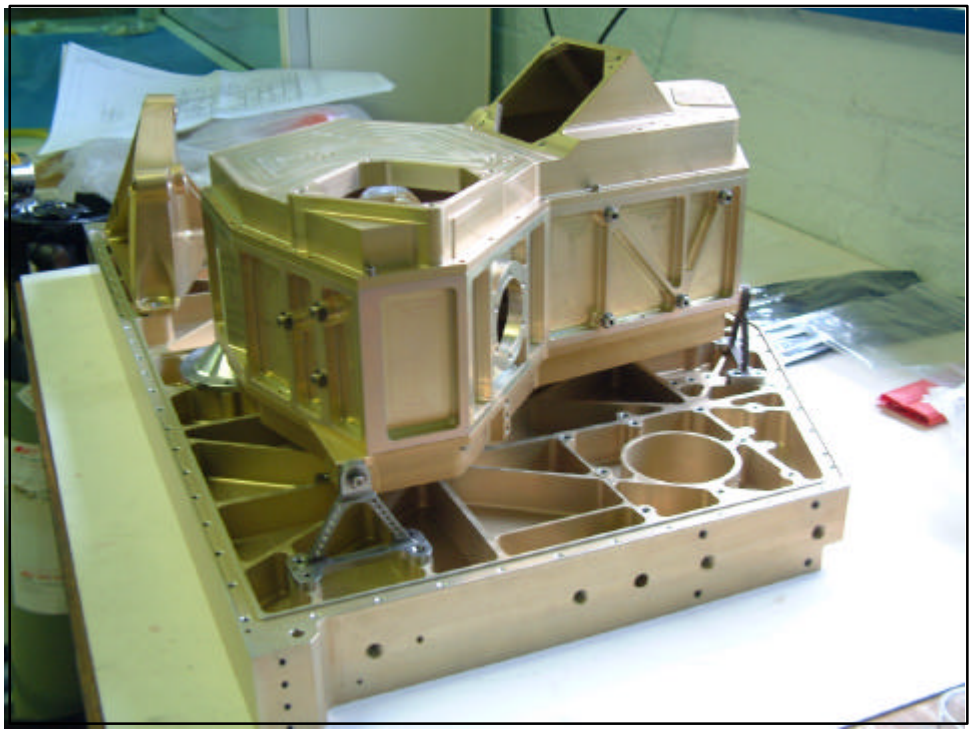
ID	Task Name
213	**Proto-Flight Model AIV**
214	**PFM Integration**
215	**PFM FPU Integration**
259	**PFM FTB Integration**
270	**PFM Instrument Integration**
271	QM2 DRCU Delivery
272	QM2 DRCU acceptance test
273	QM2 WE Integration into Te
274	FPU Integration into Test Cr
275	FTB Integration into Test Cr
276	FPU/FTB Electrical Integratic
277	Warm Functional Tests I
278	PFM Test Readiness Review
279	**PFM Verification**
300	**PFM Warm Electronics Integration**
301	PFM DPU Delivery to RAL
302	PFM DPU Acceptance
303	PFM DPU Verification
304	PFM DRCU Delivery to RAL
305	PFM DRCU Acceptance
306	PFM WIH Delivery to RAL
307	PFM WIH Acceptance
308	PFM DRCU Verification
309	PFM WE Available for PFM Calib
310	**PFM Instrument Calibration**
317	**PFM Delivery Preparation**
323	**Delivery of PFM to ESA**

Schedule summary

- QM1 –July 03 - Consistent with SPIRE schedule provided a delivery to ESA of Feb 04 is acceptable. If an earlier delivery is required then QM1 is not ok.
- QM2 – July 04(TBC) – Required in May 04
- PFM – Feb 05 (TBC) – Required in September 04

Current instrument status

- STM structure manufactured, AIT to start this month
- STM cooler and BSM at RAL, cold vibration test carried out.
- STM/CQM mirrors available
- STM detectors ready to send.
- AVM DPU complete, in test.



SPIRE DRCU Review

CEA-Saclay – March 4, 2003

DRCU Development and Procurement plan

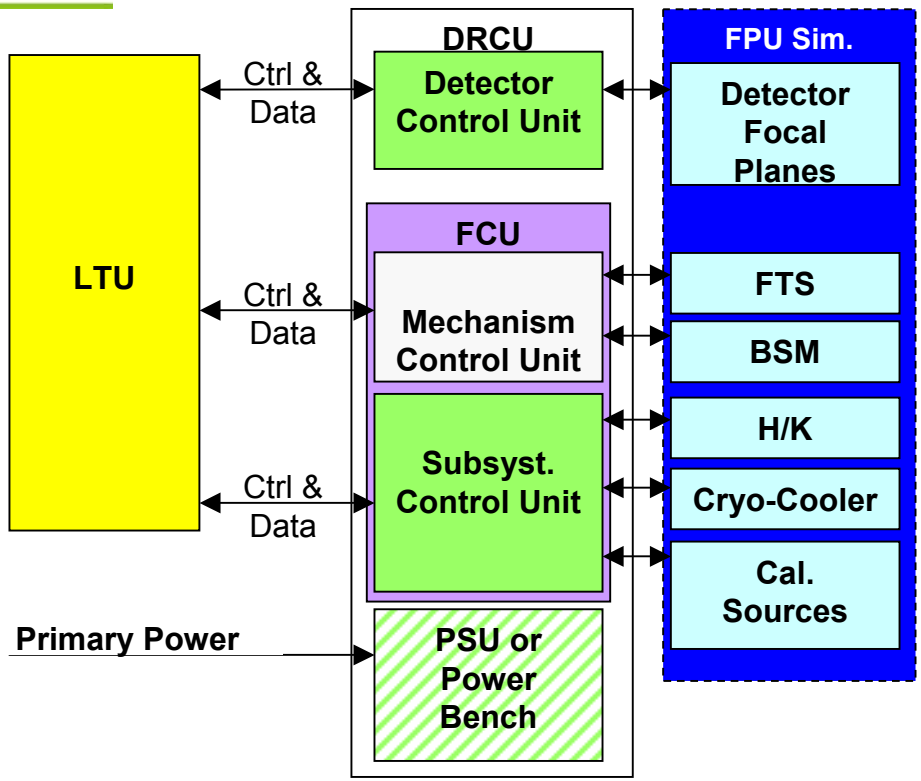
J-L.Auguères

- **CEA Warm Electronics delivery commitments:**

  - **Detector Readout and Control Unit (DRCU)**
    - The DRCU encompasses 3 sub-units and a Power Supply (PSU):
      - Detector Control Unit (DCU) developed by CEA/SAp
      - Subsystem Control Unit (SCU) developed by CEA/SEDI
      - Mechanism Control Unit (MCU) developed by CNRS/LAM
    - The DRCU comprises 3 boxes: mechanical design by CEA/SAp
      - DCU Box.
      - FCU (Focal plane Control Unit) containing the MCU and the SCU;
      - PSU box which is bolted under the FCU box.

  - **Warm Interconnect Harnesses:**
    - Harnesses between the DPU and the 3 DRCU sub-units.
    - Power harness between the PSU and the DCU.

  - **Focal Plane simulator.** developed by CEA/SIS



- **SPIRE Products:**
  - **DRCU**
    - DCU
    - FCU
      - MCU
      - SCU
    - PSU
  - **WIHs**
  - **EGSE**
    - LTU (Local Test Unit)
    - FPU Simulator
    - Power Bench
    - Test harnesses

- **DRCU Model definition:**
  - **STM** (commonalities with PACS WE boxes)
  - **EM**
    - DCU EM realised and test in collaboration with JPL/Caltech
  - **QM1**
    - Form and fit boards in "light" boxes
    - Commercial parts
    - No redundancy
  - **QM2**
    - Comprehensive Flight type model.
    - Intended to undergo environmental tests at Qualification level.
  - **FM**
  - **FS**
    - Spare units
- **CEA deliveries versus ESA models:**
  - **AVM** **None**
  - **CQM** **QM1**
  - **FM/FS** **FM/FS**

- **DRCU model features**

			FCU				
DRCU	**Mechanics**	**DCU**	**MCU**	**SCU**	**PSU**	**Part Grade**	**Perform.**
BB	N/A	Yes	Yes	Yes	-	Standard	NNP
STM	Yes					N/A	N/A
QM1	Simplified -	EEq(*) NCR	EEq NCR	EEq NCR	PB NCR	EEq	NNP
QM2	F -	FEq CR	FEq CR	FEq CR	STM,EM,PB CR	FEq	NNP
FM	F -	F CR	F CR	F CR	F	F	NoP
FS	F ?	F ?	F ?	F ?	F ?	F	NoP

Ext : External (Power Supply only)
EEq : Electrically Equivalent
FEq : Flight Equivalent (any grade but nominal size, consumption and performances)
F : Flight
NCR : Cold Redundancy Not implemented
CR : Cold Redundancy implemented
DeP : Degraded Performance acceptable
NNP : Near Nominal Performance
NoP : Nominal Performance
(*) : The number of readout channels implemented shall at least correspond to the number of detectors of the instrument CQM (photometer and spectrometer).

- **DRCU Models detailed content:**

S-Syst (N1)	S-Syst (N2)	S-Sys (N3)	Part n°	STM	EM	QM1	QM2	FM	FS
DCU									
	DAQ+IF			2 dum	1	1	2	2	1
	BIAS			2 dum	1	1	2	2	1
	LIA-TC			1 dum	0	0	1	1	1
	LIA-S			3 dum	3	3	3	3	1
	LIA-P			8 dum	2	2	8	8	2
	BP-DCU			1 dum	1 (QM1)	1	1	1	1
	DCU Box			1	1 (QM1)	Light	1	1	
FCU									
	SCU								
		CCHK+IF		-	-	1	2	2	1
		Temp+Heat		-	-	1	2	2	1
		BP-SCU		-	-	1?	1	1	1
	MCU			-	-	1	1	1	?
	SCU Box			-	-	Light	-	-	-
	FCU Box			-	-	Light	1	1	-
PSU				1	Lab.	PB	PB/EM	PB/1	Board
Flight Harnesses									
	DRCU-DPU			-	-	1	2	2	-
	PSU-DCU			-	-	1	2	2	-
	PSU-FCU			-	-	1	2	2	-
		PSU-SCU		-	-	1	2	2	-
		PSU-MCU		-	-	1	2	2	-

- **Procurement Plan:**

  - **Boxes and Boards**
    - All models:
      - Design : in house
      - Detailed drawings : industry
      - Realisation : industry
      - Mechanical simulations : industry
      - Thermal simulations : in house
      - Environmental tests : industry

  - **Electronics parts:**
    - Test equipments : Self Procurement
    - QM1 : Self Procurement
    - QM2, FM, FS
      - OP400 (custom packaging) : Self Procurement
      - Others : CPPA

- **Procurement Plan (cont.):**

  - **Harnesses:**

    - Test harnesses
      - Specification : in house
      - Fabrication files : industry
      - Parts (connectors, wires) : Self Procurement
      - Realisation : industry

    - WIH (DPU to DCU, DPU to FCU, DCU to FCU power harness)
      - Specification : in house (+ Alcatel inputs)
      - Fabrication files : in house
      - Parts (connectors, wires) : Self Procurement
      - Realisation : industry
      - Environmental tests : industry

- **Procurement Plan (cont.):**
  - **EGSEs:**
    - FP Simulators (1 deliverable)
      - Specification : in house
      - Design : in house
      - Electronics Board realisation : industry
      - Labview S/W : in house
      - Standard parts (chassis, P.Sup…) : commercial procurement
      - Integration & tests : in house
    - LTUs (Local Test Unit).
      - Specifications (H/W & S/W) : in house
      - Overall Design : in house
      - H/W detailed design & realisation : industry
      - S/W : in house
      - H/W – S/W Integration & tests : in house
    - Power Benches.
      - Specification : in house
      - Overall design : in house
      - Detailed design & realisation : industry
      - Integration and test : industry

- **Procurement Plan (cont.):**
  - **DRCU QM1:**
    - DCU, SCU Boards:
      - Design : in house
      - PCB routing : in house
      - Wiring : industry
      - Electrical tests : in house
      - Functional Tests : in house
      - Performance Validation : in house
    - DCU, SCU Integration & Test : in house
    - FCU Integration & Tests : in house
  - **DRCU QM2:**
    - DCU, SCU Boards:
      - PCB routing : in house
      - Wiring : industry
      - Electrical tests : industry
      - Functional Tests : in house
      - Performance checking : in house
    - DCU, SCU Integration & Test : In house
    - FCU Integration & Tests : in house
    - Environmental tests : industry + CEA

- **Procurement Plan (cont.):**
  - **DRCU FM/FS:**
    - DCU, SCU Boards:
      - PCB routing : in house
      - Wiring : industry
      - Electrical Tests : industry
      - Functional Tests : industry
      - Performance checking : industry
    - DCU, SCU Integration & Test : TBD
    - FCU Integration & Tests : in house
    - Environmental tests : industry + CEA

- **Development Status:**

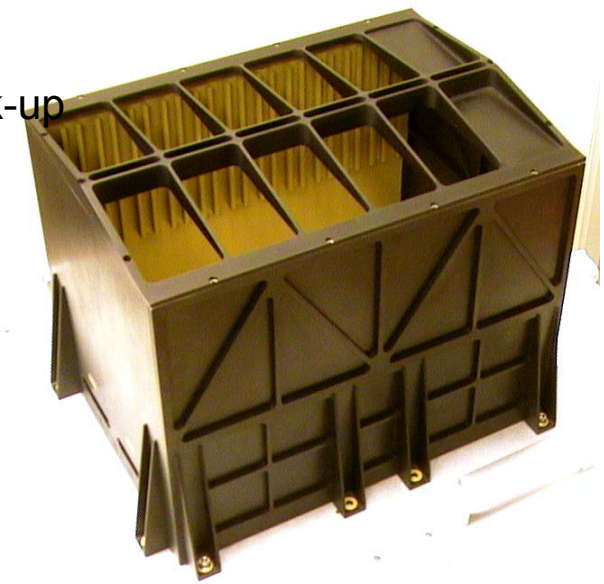
  - **DCU (Detector Control Unit)**
    - QM1:
      - Box and back-plane available.
      - Boards:
        - » 1 DAQ+IF + 1 BIAS, 1 LIA fabricated, functions and performances checked.
        - » 4 LIA under fabrication.
      - Pre-integration started:
        - » Box & Back-plane: OK
        - » Functional test OK
        - » Performance test ongoing

  - **FCU (Focal plane Control Unit)**
    - QM1:
      - Box available
      - SCU (Sub-system Control Unit) cf SCU presentation
      - MCU (Mechanism Control Unit): cf MCU presentation by LAM

- **Development Status (cont.):**

  - **PSU:**
    - Specification available.
    - Call for tender process started.
    - FM fab. Time 14 months (6 months to be added for contract sign off).

  - **Boxes:**
    - I/F (external & internal) and design OK.
    - QM1 "light" boxes (DCU + FCU) available.
    - STM: Box (QM) and Mec. & Thermal mock-up boards available.
    - QM boxes:
      - DCU available (STM box)
      - FCU ready for manufacturing.



- **Development Status (cont.):**

  - **EGSEs**
    - Local Test Unit:
      - Specification & Architecture OK.
      - H/W: procurements OK – fabrication ongoing.
      - S/W: under development.
      - 2 units will be manufactured:
        - » Availability of the 1st unit: March 03
    - FP Simulator:
      - Spec. Architecture & User manual available.
      - First unit: available.
      - Second unit: fabrication started.

    - Power Benches:
      - Specifications available.
      - 3 units will be manufactured
        - » 1st unit available in April 03

- **Development Status (cont.):**

  - **AIV:**
    - AIV plan available.
    - AIV detailed plan and procedures under development.

  - **Harnesses:**
    - Connector procurement OK.
    - Test harness specification ongoing.
    - WIH

  - **PA/QA:**
    - Internal review procedure set up.
    - Doc. List and EIDP definition OK.
    - Non conformity management procedures available.
    - DML and DPL available.

- **Documentation Status:**

  - **Review documentation:**
    - See the CEA document list.
    - These documents have been submitted to internal reviewing process.
    - Next issues submitted to internal Configuration Control.

  - **Documentation management:**
    - Configuration control procedures available.
    - Internal documentation database available.
    - Internal acces via intranet.

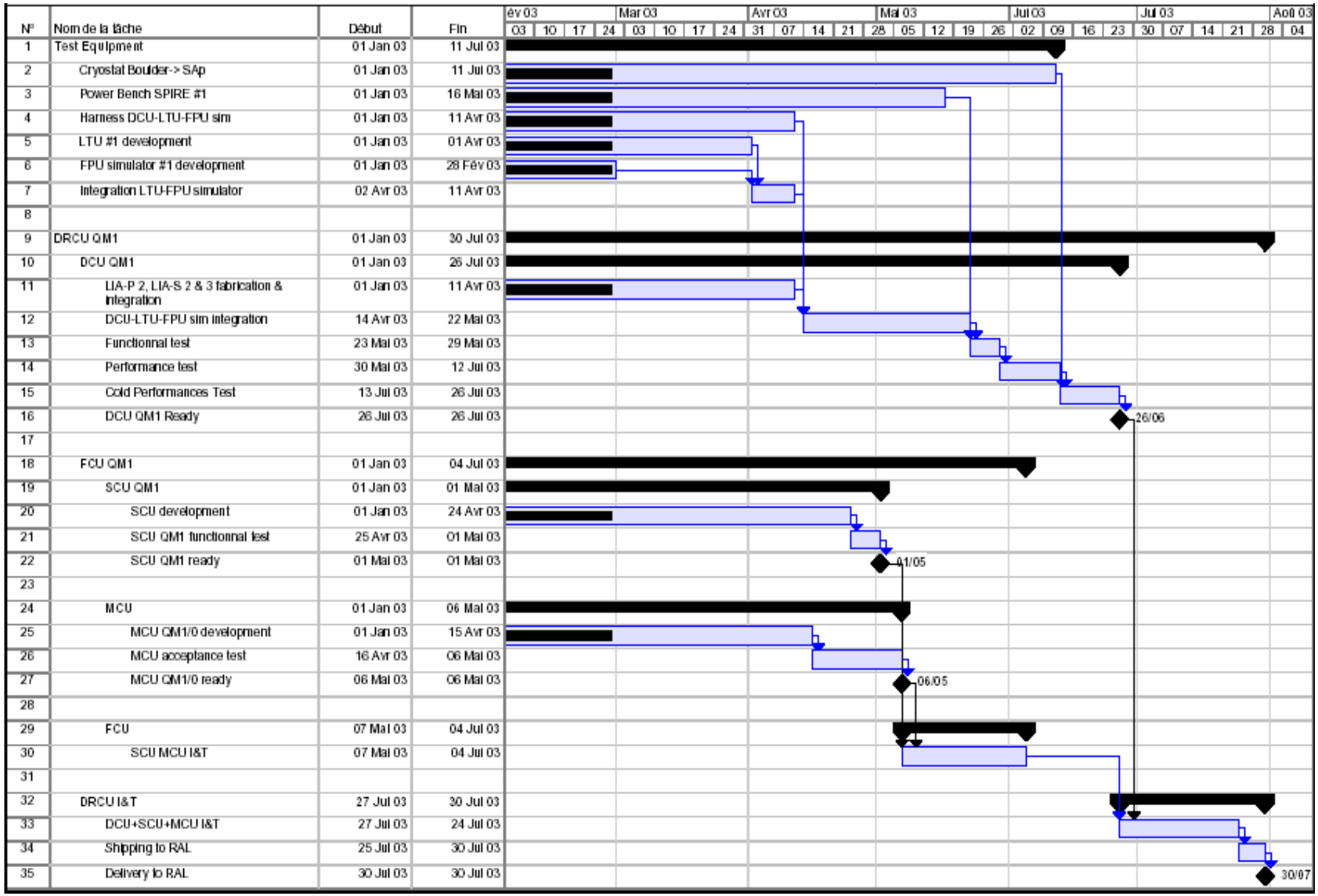
DRCU Documentation Status

Management plan for the Herschel project.	SAp-FIRST-JLA-0038-01	4.0 23/01/2003
DRCU & WIH Development Plan	SAp-SPIRE-JLA-0047-01	4.0 29/01/2003
SPIRE product tree	SAp-SPIRE-DR-0094-03	1.0 21/01/2003
WBS Herschel	SAP-FIRST-DR-0043-01	2.1 30/11/2001
WBS SPIRE	SAP-FIRST-DR-0045-01	2.1 30/11/2001
SPIRE DRCU QM1master schedule	SAp-FIRST-DR-105-01	1 18/02/2003
DRCU Specifications document	SAp-SPIRE-Cca-0025-00 (SPIRE-SAP-PRJ-000461)	1.0 14/02/2003
DRCU ICD	SAp-SPIRE-Cca-0075-02 (SPIRE-SAP-PRJ-000451)	1.0 14/02/2003
DRCU DPU ICD	SAp-SPIRE-Cca-0076-02 (SPIRE-SAP-PRJ-001364)	1.0 14/02/2003
DCU design document	SAp-SPIRE-FP-0063-02	0.3 18/02/2003
Test plan DAQ IF	SAp-SPIRE-FP-0067-02	0.1 draft
Test plan BIAS	SAp-SPIRE-FP-0066-02	0.1 draft
Test plan LIA P	SAp-SPIRE-FP-0064-02	0.1 draft
Test plan LIA S	SAp-SPIRE-FP-0065-02	0.1 draft
SPIRE test configuration	SAp-SPIRE-LD-0015-01	3.0 08/2001
FPU simulator specs for DCU / SCU test	SIG-SPIRE-PdA-0030-01	03 14/02/2003
SPIRE LTU specifications	SAp-SPIRE-FD-0071-02	1.0 22/04/2002
DRCU AIV Plan	SAp-SPIRE-HT-0082-02	2.0 03/02/2003
DRCU EM/QM1 preliminary test plan	SAp-SPIRE-HT-0088-02	0.1 14/02/2003
SCU design document	SEDI-SCU-MM-2002-1	0.7 17/02/2003
PSU SPIRE specification	SAp-SPIRE-DS-012-02	1.1 11/12/2002
PA Plan	SAP-GERES-Flo-436-00	1.0 07/11/2000
DPL	SAp-SPIRE-NC-0061-02	1.0 13/02/2003
DML	SAp-SPIRE-NC-0060-02	1.0 13/02/2003
DMPL	SAp-SPIRE-NC-0100-02	1.0 13/02/2003
DCL	SAp-SPIRE-VM-0098-02	14 10/02/2003
Synthesis note about DRCU FMEA and reliability	SAp-SPIRE-JF-0099-03	0.1 10/02/2003
WCA (and derating??)	will be performed later	--

- **ADP** (as per H/W ADP content (RAL))

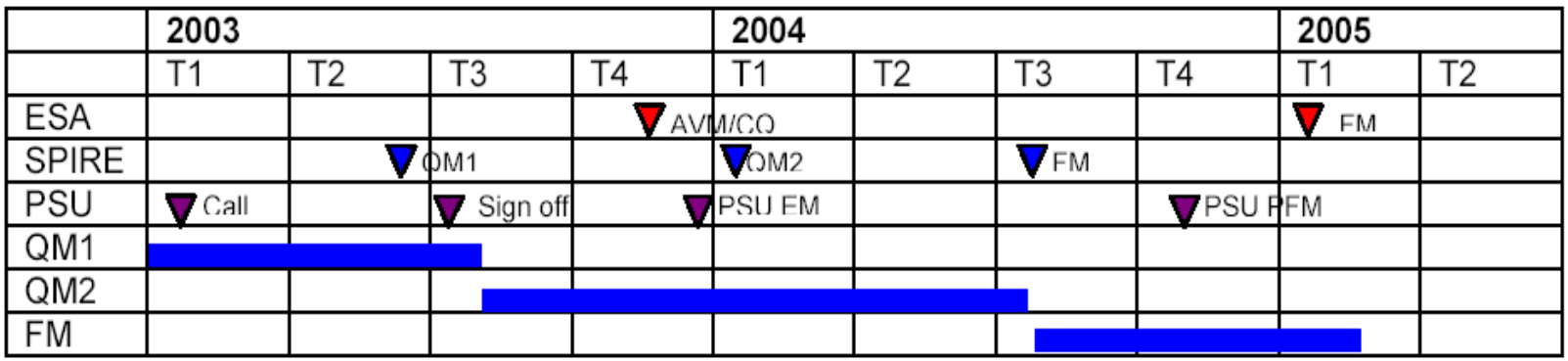
Documents	QM1	FM	Comments	Doc. status QM1
shipping documents	yes	yes	--	
procedure for transport handling and installation	yes	yes		
C of C/Delivery Review Board MOM Al-Lists	yes	yes		
Qualification status list /test matrix	yes	yes	Inluded in DRB minutes/report	
Top level drawings (inc. familly tree)	yes	yes		
Interface drawings	yes	yes		SPIR-MX-5101 000 SPIR-MX-5201 000
Functional diagrams	yes	yes	cut and paste from DRCU subsystem specs	
Electrical circuits diagrams	yes	yes	full diagrams are kept in our premices; i/f electrical diagrams are included in ICD (SAp-SPIR-CCa-075-02 and SAp-SPIR-CCa-076-02)	SAp-SPIR-CCa-075-02 SAp-SPIR-CCa-076-02
As Built Configuration Statis List	yes	yes		
Serialised components list	n/a	yes		
List of waivers	yes	yes	To be included in ABCL	
Copies of waivers	yes	yes	To be included in ABCL	
Operational manual	yes	yes		
Historical record	yes	yes		
Logbook/ Diary of events	yes	yes		
Operating time/Cycle record	N/A	N/A		
Connector mating record	N/A	yes	included in logbook / Diary of events	
Age sensitive Items record	N/A	N/A		
Pressure Vessel History / test record	N/A	N/A		
Calibration data record	N/A	N/A		
Temporary installation record	yes	yes	included in logbook / Diary of events	
Open work / Deffered work / Open tests	if applies	if applies		
List of non-conformance reports	yes	yes	included in ABCL (if any)	
Test reports	yes	yes	list of test reports inclued in EIDP to be determined	
Proof load certificate	N/A	N/A		
Reference list of lower level ADP's	yes	yes	QM1 : MCU only; FM : MCU and PSU	
Cleanliness statement	yes	yes		
Compliance matrix	yes	yes		

DRCU Development and Procurement - QM1 Schedule



N°	Nom de la tâche	Début	Fin
1	Test Equipment	01 Jan 03	11 Jul 03
2	Cryostat Boulder-> SAp	01 Jan 03	11 Jul 03
3	Power Bench SPIRE #1	01 Jan 03	16 Mai 03
4	Harness DCU-LTU-FPU sim	01 Jan 03	11 Avr 03
5	LTU #1 development	01 Jan 03	01 Avr 03
6	FPU simulator #1 development	01 Jan 03	28 Fév 03
7	Integration LTU-FPU simulator	02 Avr 03	11 Avr 03
8			
9	DRCU QM1	01 Jan 03	30 Jul 03
10	DCU QM1	01 Jan 03	26 Jul 03
11	LIA-P 2, LIA-S 2 & 3 fabrication & integration	01 Jan 03	11 Avr 03
12	DCU-LTU-FPU sim integration	14 Avr 03	22 Mai 03
13	Functionnal test	23 Mai 03	29 Mai 03
14	Performance test	30 Mai 03	12 Jul 03
15	Cold Performances Test	13 Jul 03	26 Jul 03
16	DCU QM1 Ready	26 Jul 03	26 Jul 03
17			
18	FCU QM1	01 Jan 03	04 Jul 03
19	SCU QM1	01 Jan 03	01 Mai 03
20	SCU development	01 Jan 03	24 Avr 03
21	SCU QM1 functionnal test	25 Avr 03	01 Mai 03
22	SCU QM1 ready	01 Mai 03	01 Mai 03
23			
24	MCU	01 Jan 03	06 Mai 03
25	MCU QM1/0 development	01 Jan 03	15 Avr 03
26	MCU acceptance test	16 Avr 03	06 Mai 03
27	MCU QM1/0 ready	06 Mai 03	06 Mai 03
28			
29	FCU	07 Mai 03	04 Jul 03
30	SCU MCU I&T	07 Mai 03	04 Jul 03
31			
32	DRCU I&T	27 Jul 03	30 Jul 03
33	DCU+SCU+MCU I&T	27 Jul 03	24 Jul 03
34	Shipping to RAL	25 Jul 03	30 Jul 03
35	Delivery to RAL	30 Jul 03	30 Jul 03

- **Scenario 1:**
  - **The original development plan is kept: QM1, QM2, FM**
    - Schedule risks on QM1 due to:
      1. Cryogenic test with the JPL test Bolometer.
      2. Activities within the holidays period.
    - Limited feedback for QM2: no test with the actual JPL CQM bolometers.



    - The QM2 development takes one year (give or take):
      1. QM2 board layouts have to be revised to take into account: the QM1 feedback and the use of flight component packaging.
      2. The test with the PSU EM.
      3. The environment testing at Qualification level requiring margins.
    - DRCU FM available by end February 2005.

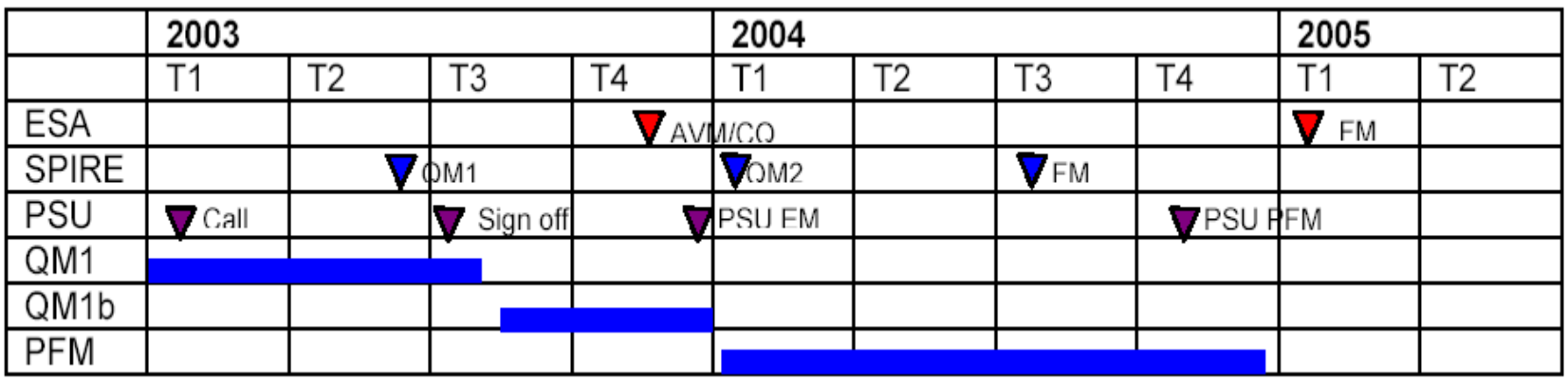
- **Scenario 1 (cont.)**

  - **Pros:**
    1. The full development is carried out minimising the risk.
    2. The PSU EM can be tested with a flight representative model.
    3. The PSU FM power supply can be integrated and tested with the full DRCU FM prior to its delivery.

  - **Cons:**
    1. Late availability of the DRCU FM.

  - **Conclusion:**
    1. This scenario is the nominal one and the optimal one (as it minimises the risk).
    2. The schedule issue could not be an issue as it is likely that other subsystems (WE or focal planes) will have comparable schedule shift (if not worse).

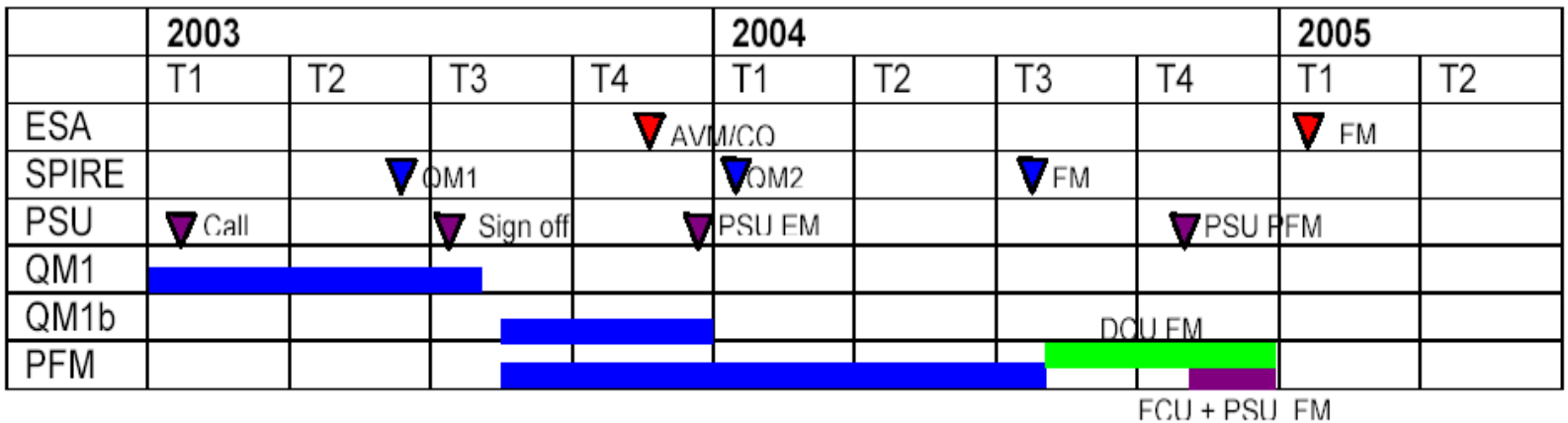
- **Scenario 2:**
  - **The QM2 is cancelled and a QM1b and a PFM are built consecutively:**
    - After the delivery of the QM1, a second QM1 (QM1b) is built.
    - The QM1b is identical to the QM1 (light box, Standard components, no redundancies) but all detector readout and control channels are implemented.
    - The QM1b is intended:
      1. To test as far as possible the PSU (EM) compatibility.
      2. To be used with the Instrument PFM.



- DRCU FM available by the end of 2004.

- **Scenario 2 (cont.)**
  - **Pros:**
    1. Provides a good feedback between the QM1 and the PFM.
    2. Provides electronics to drive the PFM Focal Plane.
    3. The PFM delivery date is "optimised" against the PSU PFM availability date.
  - **Cons:**
    1. PFM development: high risk in case of failure at any level and especially during the environment test.
    2. The Flight Model has to undergo the Qualification level (instead of acceptance).
    3. There is no model to validate the electrical compatibility of the PSU with the PSU EM.
  - **Conclusions:**
    - This scenario has two major drawbacks:
      1. The DRCU development not in line with the PSU development.
      2. High risks are taken due to the PFM policy.
    - Given the schedule shifting risks, the advantage to get the PFM earlier than in the case of the scenario 1 is not obvious.

- **Scenario 3:**
  - **The QM2 is cancelled and a QM1b and a PFM are built in parallel.**
    - The QM1b and its objectives are the same as in the scenario 2.



- In this case, the DRCU FM powered by a power bench could be available by October 2004 but the PSU FM has to be integrated later when available.
- DRCU FM available by the end of 2004.

- **Scenario 3 (cont.):**
  - **Pros:**
    1. Provides electronics to drive the PFM Focal Plane.
    2. The PFM delivery date is "optimised" against the PSU PFM availability date.
    3. The DCU FM can be used with the Focal Plane PFM.
    4. The PSU EM can be tested with a flight representative model.
  - **Cons:**
    1. PFM development: high risk in case of failure at any level and especially during the environment test.
    2. The Flight Model has to undergo the Qualification level (instead of acceptance).
    3. Two models (QM1b and PFM) have to be built in parallel (resource issue).
  - **Conclusion:**
    - This scenario has two major drawbacks:
      1. High risks are taken due to the PFM policy.
      2. High workload peak when the QM1b and the PFM development are in parallel.
    - Given the schedule shifting risks, the advantage to get the PFM earlier than in the case of the scenario 1 is not obvious.

Mechanisms Control Unit

The dates

D. Pouliquen

Laboratoire d'Astrophysique de Marseille

MCU QM0 and QM1

- **QM0 : for communication and LTU tests**
- Design + routing+ tests at LAM + manufacture in industry)
- New model introduced for planning reasons
- Form & fit, electrical, command interface & flight functions nearly Ok
- ALTERA FPGA including CEA DAPNIA Communication VHDL issue 0.4
- Commercial components, no redundancy
- Not suitable for mechanisms control
- Delivered with mechanisms simulator and cables
- Delivery date April 2003
- **QM1 : for CQM tests**
- Design + routing + tests at LAM + manufacture in industry
- Tested with the CQM mechanisms => QM0 modified for mechanism control capability => flight functions Ok at time of delivery
- Delivery date = end of July 2003

MCU QM2

- Design = QM1 (LAM) as delivered to CEA
- Design does not include modifications needed after SPIRE CQM tests
- Subcontracted in the industry (studies, routing, manufacture, electrical and environment tests)
- End of studies = 15 Aug 2003 (t0 + 5 months)

  Studies includes mechanical and thermal studies as the subcontractor is responsible for the MCU thermal and mechanical behaviour.
- QM2 manufacture and tests from 15 Aug 2003 to 31 Jan 2004 (duration : 5.5 months)

  Tests include vibrations, thermal tests and performance tests with simulators all made at LAM
- QM2 delivery to CEA => end Feb 2004 (t0 + 11.5 months)

If need for QM1 design modification arises during CQM programme, the QM2 will not have them. This raises a question (no answer yet) on the ability of QM2 to pilot the FPU mechanisms inside the FPU.

MCU FM & FS

- Design = QM1 + mechanical and thermal studies made and validated at LAM with the QM2
- Design does not include modifications needed after SPIRE CQM nor after FCU QM2 tests (tests made at FCU level, after beginning of FM manufacture i.e. vibr, thermal and EMI)
- If no electrical modification w.r.t. QM1 as delivered to CEA,
  - FM manufacture and tests from 1st Feb 2004 (end of QM2 manufacture + no modifs) to 1st Sep 2004 (duration : 7 months)
  - FM delivery to CEA => 31 Oct 2004 (end of QM2 at LAM + 9 months) : *will not have seen the PFM mechanisms before delivery*
  - FS (=FM) availability at LAM = 1st Nov 2004 (end of FM + 2 months) => available for the project 1st Jan 2005

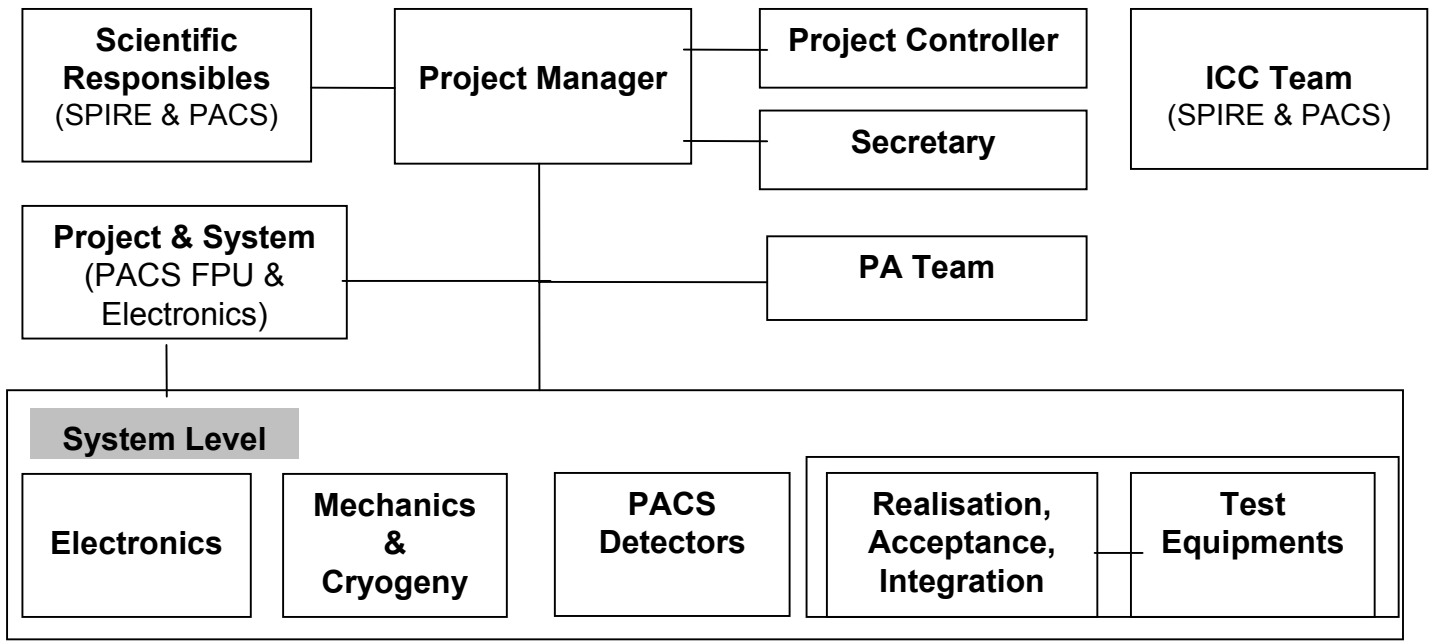
SPIRE DRCU Review

CEA-Saclay – March 4, 2003

Management & Staff

J-L.Auguères

- **Managerial organisation:**
  - **Two projects (SPIRE & PACS), one Herschel team.**
  - **Main reasons:**
    - Resource management flexibility.
    - Common Development.



- **Herschel Teams:**

  - **Project & System Team**
    - Members: Scientific Responsibles, the Project Manager, the PA Responsible and Team key persons.
    - Check system consistency of the design and development against the system requirements.
    - Discuss, sort out technical and programmatic issues, make any decisions at system level.

  - **Electronics Team**
    - Design and development of the Electronics sub-systems.

  - **Mechanic and Cryogeny Team**
    - Design and development of the PACS and SPIRE electronics boxes.
    - Development and setting up and maintenance of the cryogenic test facilities.
    - Design and development of the PACS Photometer Focal Plane mechanics and mounting tools.

- **Herschel Teams (cont.):**
  - **PACS detector team:**
    - In charge of the overall design, the development, the test and the characterisation of the PACS Photometer Focal Plane.
  - **Test Equipment, Realisation and AIV team:**
    - Development and commissioning of the electronics ground test equipment.
    - Realisation and integration of the qualification and Flight models.
    - Qualification, Validation and delivery.
  - **Product assurance team:**
    - Writing and maintenance of the PA documents (PAPs, method and procedures, Parts Lists,…)
    - Reviews and inspections (documentation, working procedures,…)
    - Selection, evaluation and procurement of the electronics parts.
    - Configuration and non conformity management.
    - Evaluation of radiation effects.
    - Incoming inspections.
    - Failure Mode Effects and Causes Analysis.

CEA Management & Staff – Herschel organisation and worksharing

SPIRE Scientific Resp.	L.Vigroux
PACS Scientific Resp.	L.Rodriguez
Project Manager	J-L.Auguères
Project Control	*D.Raval*
Secretary	P.Chavegrand (orders)

System Engineers	
PACS FPU	L.Rodriguez
Electronics	C.Cara
WE SPIRE	D.Schmitt
WE PACS	C.Cara
EMI/EMC	D.Schmitt

Quality	
Xxxxx	
Mechanic	N.Colombel
Electronics	J.Fontignie
Elect. Parts	V.Mauguen
NC/PCB/Flex	L.Dumaye

ICC PACS/SPIRE	
	L.Vigroux
(+ Char. Bolo.)	M.Sauvage
	S.Madden
	Ph.André
(+ Char. Bolo.)	K.Okumura
(+ Char. Bolo.)	R.Gastaud
	D.Elbaz
	J-L.Starck
	P.Querre

Electronics C.Cara		**Mechanic** T.Tourrette		**PACS Photometer** L.Rodriguez		**RAIV** C.Bonnin		**EGSE SPIRE & PACS** F.Daly	
PACS		**PACS**		**Focal Planes**		**Realisation**		**Local Test Units**	
BOLC/BOLA	E.Doumayrou	PhFPU	J.Martignac	Specification &	**J.Martignac**	Elect. Subs. (SCU excl.)			**F.Daly**
	A.Bouère		T.Tourrette	Design	L.Rodriguez	Elect. Engin.	L.Cadélis		E.Poindron
PSU	D.Schmitt		*G.Dhenain*	**FP Test Equipments**		PSU	D.Schmitt		*M.Donati*
Harnesses	*L.Dumaye*	Elect. Boxes	T.Tourrette	BFP T. Fac.		Incom. Inspec.	*F.Le Pelleter*	**FPU Simulators**	
SPIRE			*G.Dhenain*	Specification	**L.Rodriguez**	SPIRE SCU			**P.De Antoni**
DCU	F.Pinsard	**Cryostats**		Design &	Y.Le Pennec		M.Mur		S.Sube
SCU&I/F DPU	**M.Mur**	BOLG	T.Tourrette	Realisation	T.Tourrette		Xxxxx		P.Beauvais
VHDL	O.Gachelin		*G.Dhenain*	PhFPU T. Fac.		PhFPU			D.Anstett
CCHK Board	H.Deschamp	Test BFPs	T.Tourrette	Specification	**L.Rodriguez**		T.Tourrette		O.Dubois
	E.Virique	Test PhFPU	T.Tourrette	Design &	*Y.Le Pennec*		J.Martignac	**Power Benches**	
Temp. Board	E.Zonca	**SPIRE**		Realisation	T.Tourrette	**AIV**			**F.Daly**
Backplane	E.Zonca	Elect. Boxes	T.Tourrette	**Tests & Characterisation**		Electronics			*C.Herviou*
PSU	D.Schmitt		*G.Dhenain*	BFP & PhFPU		SPIRE	H-E.Triou		
Harnesses	*L.Dumaye*	**Mec. Engineering**			**L.Rodriguez**	PACS	C.Bonnin	**Bolometer (LETI)**	
	Xxxxx (A2)		T.Tourrette		Y.Le Pennec	WE boxes	T.Tourrette	Design & realisation	**P.Agnèse**
Electronics CAD			P.Perrin		V.Reveret	EGSE	F.Daly		
	N.Devin				C.Bonnin	EMI/EMC	D.Schmitt	BFP Integration	J-L.Pornin
	M.Seyranian				*T.Orduna*		*C.Herviou*		J-C.Cigna
SAp					*Xxxxx (A2)*		*Xxxxx (A2)*	BFP Test	P.Agnèse
SEDI				**Bolometer Evaluation**		PhFPU PACS		**Cryo-Cooler (SBT)**	
SIS				Eval. Plan	**V.Mauguen**		C.Bonnin	Spec. Design	**L.Duband**
SBT					M.Delcourt		J.Martignac	Realisation	
LETI					L.Rodriguez		*E.Gregoire*	& Test	
Subcont.					Y.Le Pennec		*Xxxxx (A2)*	PA	*B.Veritas*

Annex D

Status of Comments on DRCU Documents

SPIRE Technical Note

Ref: SPIRE-RAL-NOT-1399
Issue: 2.0
Date: 23/03/03

Consolidated Comments on DCRU Documents
Edited: B. Swinyard/E Sawyer; ***reply from CEA 02-12-2002***
Further comments on documents issued for the DDR
New comments in Blue

	Document	**Section**	**Raised by**	**Comment**	**Response**	**Follow-up/current status**
GEN 1	All		EAC (PA)	There is no CIDL Configured Item Document/Drawing List. (ESA and SPIRE requirement).	Configuration Item Data List is under construction.	
2	All		EAC (PA)	There are several TBW's or will insert XYZ here when ready throughout the set of documents.	Will be corrected in next release of document set.	The DDR release?
3	All		EAC (PA)	DCU Design document, purpose and scope of this document be TBW, should not still be undefined at this stage	Document will be corrected : **Action to F.PINSARD**	
4	All		EAC (PA)	PA Plan is missing from this document list.	CEA has already provided its standard PA plan (sent to Kelsh DM, KING KJ , November 2000)	OK please list it

Consolidated Comments on DCRU Documents
Edited: B. Swinyard/E Sawyer; ***reply from CEA 02-12-2002***
Further comments on documents issued for the DDR
New comments in Blue

ID	Document	Section	Raised by	Comment	Response	Follow-up
DRCU0	DRCU Spec. Doc.			Title: Detector Readout and Control Units		
DRCU1	DRCU Spec. Doc. SAP-PRJ-000461 (Sap-SPIRE-CCA-25-00)	2.1	BMS	Figure 2.1a is scrambled Figure 2.1a has "OEP" outside the FPU – it should be inside	Figure is now corrected and is no more scrambled even in pdf format	***v***
2	*ditto*	DRCU-REQ-45	BMS	…and here's the rub! When does the filtering get specified?	The DCU is powered by the FCU's PSU; the DCU's power filtering has no impact at instrument / system level, except for radiated emission matters where IID applies.	***v*** fine, but on the subject of filtering, where is pre-PSD filtering specified?
3	*ditto*	Fig 4.2-b	BMS	This figure does not accord with the power supplies specified elsewhere in the document (DRCU-REQ-43 and DRCU-REQ-99) and is therefore confusing – remove or replace.	YES - This figure does not reflect any more the design and especially for power supplies. Shall be corrected	***v***
4	*Ditto* Also applies to DRCU/DPU I/F Doc	DRCU-REQ-79 (and maybe elsewhere)	BMS	Parameter names used here are not consistent with the interface specification. In the interface doc (…) it uses FPUTEMP# -here the temperatures have more meaningful names – use these please!	ICD shall be modified according to actual SCU design in order to define unambiguously temperature measurement channels. Action on SCU designers List available (see attached file): ICD to be updated	***v*** Is ICD now fixed?
5	*ditto* Also applies to DRCU/DPU I/F Doc	DRCU-REQ-83	BMS	Please define the SCUSTATUS word as soon as possible – it does not appear at all in the I/F parameter list although it can be requested by dedicated command! (cf. ICD section 2.2.14.3 and 2.2.15)	Action on SCU designers Description available (see attached file): ICD to be updated	***v***
6	*ditto*	DRCU-REQ-85 DRCU-REQ-86	BMS	Wrong document called up – should be AD24?	DRCU-REQ-85 and 86 have been modified to: The thermometry sub-system (main part) shall have the following channels	***v***

Consolidated Comments on DCRU Documents
Edited: B. Swinyard/E Sawyer; ***reply from CEA 02-12-2002***
Further comments on documents issued for the DDR
New comments in Blue

ID	Document	Section	Raised by	Comment	Response	Follow-up
					according to AD24 except for cryo-cooler related temperature probes (text in blue) where AD21 is considered	
7	*ditto*	DRCU-REQ-88	BMS	Number of steps for full range operation is over specified – PCAL requirement is for 256 steps – if it is convenient to have a single type of DAC then o.k. else it is unnecessary.	HSO-CDF-ICD-013-2-0 specifies a 12-bit resolution HSO-CDF-ICD-011-2-0 specifies a 12-bit resolution	***v***
8	*ditto*	4.6.1	BMS/JD	Post regulation is shown for LIA supplies but not for DAQ/Bias supplies. Where does this happen?	Post regulators are only required for LIA electronics since input stage of the design has a poor PSRR	Question not answered+ on motherboard
9	*ditto*	4.7.3	BMS	Can we have an extra requirement that the outputs of all FPGA controlled supplies (heaters; mechanism drives etc) are kept low during initialisation and are kept low until commanded otherwise.	YES - This requirement has already been considered for MCU and SCU designs. To be checked for the DCU **Action to F.PINSARD**	Text has been added to spec. in such a place as to make it partially inapplicable
10	*ditto*	DRCU-REQ-120	BMS	What does S/W crash refer to? The DPU or any software local to the DRCU?	This refers to MCU S/W exclusively	***v***
11	*ditto*	4.7.5	BMS	Please check this against the Operating Modes document version 3 issued Jan 2002 as the naming of modes has been changed and we have defined two standby modes one for PHOT and one for SPEC.	Chapter 4.7.5 has been updated: please check	***v Bruce?***
12	*ditto*	DRCU-REQ-122	BMS	Reword and add new requirement: *122: The DRCU shall provide capabilities for the DPU to detect internal failures* *122 bis: The MCU shall provide capabilities to detect and handle failures in the sub-system that might cause immediate danger to the mechanism.*	OK - Has been modified & added	***v***
13	*ditto*	4.9.3	BMS	The diagram is unreadable – please make it bigger	OK size is doubled	***v***

Consolidated Comments on DCRU Documents
Edited: B. Swinyard/E Sawyer; ***reply from CEA 02-12-2002***
Further comments on documents issued for the DDR
New comments in Blue

ID	Document	Section	Raised by	Comment	Response	Follow-up
				it bigger.		
14	*ditto*	5.1.3	BMS	Are these requirements still relavant given that the interface drawing exists?	Will stay in the document even if no more formally useful	***v***
15	*ditto*	8	BMS	The reliability figure for the DCU has been discussed in a technical note. The FMECA has covered the rest of the reliability discussion?		***v***
16	*ditto*	11 and section 1.3	BMS	AD13 through 17 aren't mentioned/used – did they go missing?	AD14 to AD17 have been removed from previous document issue when refreshing AD list.	***v***
17	*ditto*	12	BMS	Table is incorrect? QM1 and QM2 do not have Flight Equivalent power supplies with or without redundancy.	Table is a copy and paste of DRCU Development Plan -> document to be updated (Action : JLA)	***v***
18	*ditto*	4.4.3	PH	REQ-85, the range for the SCAL 4% and 2% source (T-SCAL2, TSCAL4 is listed as 10K to 80K. This should read 4K to 150K	OK range update was missing (demonstrate the interest for generating ECR to keep track of requirement modification	***v***
19		4.2.3	JD	REQ-321-6 must be more precisely defined as "combination of all DRCU noise sources referred to the LIA inputs when each is terminated by 9K to bias ground, including any digital or digitization noise and contributions from the other DRCU units besides the DCU).		***Arose at meeting***

ID	Document	Section	Raised by	Comment	Response	Follow-up
ICD 1	DRCU ICD SPIRE-SAP-PRJ-000451 (Sap-SPIRE-	5.4.3.2.1	DKG	Include jumper connections from pins 1 to 21; 2 to 22, 20 to 30; 4 to 24; 5 to 25; 3 to 6 of J29 and also J30 to allow for robustness in the SMEC Launch Latch	OK - Update missing in the released ICD - Has been done	

ID	Document	Section	Raised by	Comment	Response	Follow-up
	CCA-075-02)			drives.		

ID	Document	Section	Raised by	Comment	Response	Follow-up
DCU 1	DCU Design Description SAp-SPIRE-FP-0063-02	3.2	BMS	What does this table mean? It is not complete.	**ACTION : F. PINSARD**	
2	*ditto*	Whole doc.	BMS	Circuit diagrams are unreadable (e.g. Picture 4-8)	**ACTION : F. PINSARD**	
3	*ditto*	4.1.3.1 4.1.6.1	BMS	I believe the offset in the first part of the picture comes from the JFETs? Please identify the source of the offset is the text or on the picture.	**ACTION : F. PINSARD**	
4	*ditto*	4.1.3.2 4.1.3.3 4.1.6.2 4.1.6.3	BMS	Can we have the transfer functions of the filters in tabular or polynomial form please. Then we can use them in the instrument models.	**ACTION : F. PINSARD**	
5	*ditto*	4.1.8.1	BMS	The description is a bit hard to follow! What is the final relationship between DATA and the amplitude of the bias that is actually output from the circuit? Is the statement about the resistors associated with the absence of the redundant cards from QM1 or does it represent a design option?	**ACTION : F. PINSARD**	
6	*ditto*	4.1.8.1 4.1.11	BMS	There is no description of how the phase of the demodulation signal is altered for each BDA module? I hope this is implemented!	**ACTION : F. PINSARD**	
7	*ditto*	4.1.12.1	BMS	Is FRAME=0 equivalent to continuous	**ACTION : F. PINSARD**	

ID	Document	Section	Raised by	Comment	Response	Follow-up
				output of frames as specified in the ICD? Do both FRAME and START have to be high for data to be output?		
8	*ditto*	4.1.12.3 (Page 61)	BMS	Is an average of two values at all useful? Why isn't it 4 values as in the photometer?	**ACTION : F. PINSARD**	
9	*ditto*	4.1.12.5	BMS	I think I understand how it works but it isn't completely obvious from this section! Just a leetle more explanation?	**ACTION : F. PINSARD**	
10	*ditto*	4.1.12.7	BMS	Do 1 and 2 represent design options to be decided upon?	**ACTION : F. PINSARD**	
-11	*DCU Design Document Sap-SPIRE-FP-0063-02 (version 0.3)*	2.1.1.3	KJK	This section states that there are commands to set the bias generators to either a sine wave bias or an adjustable DC level. These commands are implemented in the DRCU/DPU ICD, but I cannot find in this document where they are implemented in the design.		This is a new comment
12	*Ditto*	3.9.3.8	KJK	Offsets are given in the DRCU/DPU ICD as 4 bit values. This section indicates the design only implements 3 bit values		This is a new comment

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SCU 1	SCU Design Description SEDI/SCU/MM /2002-1	1.1.3	BMS	We don't seem to have a copy of AD5? SEDI-SPIRE-OG-0001-02	The AD5 document is a technical description of the DPU interface, primarily intended to provide common understanding for the 3 DRCU implementations: DCU, MCU and	

ID	Document	Section	Raised by	Comment	Response	Follow-up
					SCU. This document is available.	
2	*ditto*	2.1	BMS	Block diagram shows "AC Modulation(x4)" – why is this when there is only one AC temperature channel?	The block diagram is ambiguous. The AC channel requires 4 signals to support the On/Off and modulation controls, whereas the DC channels require only one signal for On/Off control. Will be clarified in next release.	
3	*ditto*	2.2 3.1 3.2	BMS	We would like some clarification of the operation of the acquisition sequencer and the data frame transfer: i) Which takes priority – the Acquisition Sequencer or the Get Parameter request? We wish to have the data in the frames at even sampling rates – therefore we would wish the Acquisition Sequencer to have priority. A timing diagram would be useful ii) Does the FPGA assemble a complete data then transfer it, or does it transfer the payload piecewise?	i) There is no actual priority between the "Acquisition Sequencer" and "Get Parameter" actions, which are served on a first-come first-served basis. Analysis has shown that the sampling interval specification (all data sampled within 6ms) is guaranteed, even under worst case "Get Parameter" activity. ii) The FPGA transfers the payload piecewise (word per word).	
4	*ditto*	3.2.1.1	BMS	Similar comment – Data Frame and Packet used interchangeably – please use Data Frame as packet means something else to the DPU.	Will be modified on next release.	
5	*ditto*	4.1.1 4.2.1 4.3.1	BMS	Maximum lead resistances are specified in the DRCU Specification document and the Harness Definition Document. These should be used to specify the design?	The harness resistance is a concern for the Sorption Pump Heater, which is marginal at maximum harness resistance [With a 100 Ohm harness resistance, the +-9V circuit saturates at 35.5 mA (500 mW dissipation in the 402 Ohm load occurs at 35.3 mA)]. Requires further investigation, or	

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					relaxation (reduction) of the harness resistance spec.	
6	*ditto*	4.1.4.5 4.2.4.4	BMS	Does this test mean that the effect of the lead resistance can be ignored? The lead resistance does not seem to be included in the simulation – what is the dissipation going to be in the cryoharness?	Knowing the heater currents and harness resistance, the cryoharness dissipation should obviously be considered. This is not specifically a SCU issue.	
7	*ditto*	4.2.4.1	BMS	Check with Lionel Duband whether 4pW is significant in terms of the operation of the heat switch sorption pump.	To my knowledge, still to be checked by the system team.	
8	*ditto*	4.3.1	BMS	The Spec Doc (AD1) specifies 6 kΩ for the heater resistance	Yes. Taken into account in the design. Will be modified on next release.	
9	*ditto*	4.4.1.2 4.4.1.3	BMS	This is an incorrect description of the SCAL sources – the Spec. Doc (AD1 v0.92) has the correct specification (2% and 4% sources) with both types of source having the specification as for "SCALP". The "SCALF" drive is not required, we need 2x the "SCALP" design.	Yes. Taken into account in the design. Will be modified on next release.	
10	*ditto*	4.8	BMS	Is this power supply monitoring associated with the SCU staus word?	No. The power supplies are measured on request and are made available in parameters ScuCHTp05, -n09 and –p09. These values are not checked by the SCU.	
11	*ditto*	5.2.1	BMS	How does this work? Analogue or digital?	As stated, analogue.	

Consolidated Comments on DCRU Documents
Edited: B. Swinyard/E Sawyer; ***reply from CEA 02-12-2002***
Further comments on documents issued for the DDR
New comments in Blue

ID	Document	Section	Raised by	Comment	Response	Follow-up
12	*ditto*	6.1	BMS	The notes on the next page make explicit that all output voltages and currents are held low in the reset state. Maybe make this clear in this section? Also is it really true that the SCU is "stateless" when it leaves reset? I hope that the outputs are definitively held low until commanded otherwise?	At time of writing, the need to have outputs low at start-up was not a requirement, but this feature had been included however. This is now a requirement. Will be described more clearly in next version. The text says " the DPU is stateless once out of reset". This means that after reset, it does not keep track of command history, and always act identically under identical commands.	
13	*ditto*	6.2	BMS	Its not clear how the sampling frequency is set – FRAMECONF? It is reasonably urgent that the SCUSTATUS word is defined as this will be used for error detection in flight and we need to get on with the FDIR.	FrameConf has two fields: The 1-bit "Type" field selects between "normal" and "test pattern" frames, and the "Rate" field R gives the frame rate division factor. The resulting frame repetition rate is 80/(R+1) Hz. Will be updated in next version.	
14	*ditto*	7.1	BMS	Read DRCU-REQ-89 in the latest version of AD1 v0.92 Both SCAL devices are four wire to allow remote sensing of voltage and therefore current stabilisation?	The cross reference table is based on DRCU spec. v0.90. The numbering has changed in spec. v0.92. Will be updated in next release.	
15	*ditto*	4.4	PH	Description of SCAL out of date, flood and point sources no longer used	Yes. Will be updated in next release.	

Consolidated Comments on DCRU Documents
Edited: B. Swinyard/E Sawyer; ***reply from CEA 02-12-2002***
Further comments on documents issued for the DDR
New comments in Blue

ID	Document	Section	Raised by	Comment	Response	Follow-up
DPU-ICD 1	*DRCU to DPU ICD Sap-SPIRE-CCA-076-02*	General comment	RCI at IFSI	One very important comment is that, as far as we know, the DRCU-DPU ICD is the one we wrote (SPIRE-IFS-PRJ-000650 of 2/4/2001). We always said that we will discuss and include in that document the DRCU people comments, but the need of a single document is to avoid ambiguities and unnecessary efforts (i.e. we are the custodian of the ICD).		
2	*ditto*	2.1.1	RCI	DRCU subsystems, if addressed individually reply with a response word with the following ..... Should read: DRCU subsystems, if addressed individually with SYN0=0 reply with a response word with the following ...	OK text modifed	Closed

Consolidated Comments on DCRU Documents
Edited: B. Swinyard/E Sawyer; ***reply from CEA 02-12-2002***
Further comments on documents issued for the DDR
New comments in Blue

ID	Document	Section	Raised by	Comment	Response	Follow-up
3	*Ditto*	2.4.1.2	RCI	when a "Set_parameter" command is received the subsystem responds to the DPU by transferring a command acknowledge word (positive or negative) on the response line. Should read: When a "Set_parameter" command with SYN0=0 is received the subsystem responds to the DPU by transferring a command acknowledge word (positive or negative) on the response line.	§2.1.4.2 ??? Text modified The next sentence has to be modified in the same way. A "Get_paramater" command with a SYN0=1 don't generate any response. This is due to the interpretation of the SYN bit at the interface circuitry level and then independently from the command id itself	Closed
4	*Ditto*	2.1.5.1	RCI	The RES signal shall by modified on the rising edge of the CLK signal and being sampled by the DPU on the next falling edge of the CLK signal. Should read: The RES signal shall be modified on the falling edge of the CLK signal and being sampled by the DPU on the next rising edge of the CLK signal.	Not only text to modify : H/W is designed according to the first sentence as given by this document a long time ago. Why a so late comment, while the H/W is now existing. Must be checked with designers…	'next' is omitted dfrom the text – is it important?

Consolidated Comments on DCRU Documents
Edited: B. Swinyard/E Sawyer; ***reply from CEA 02-12-2002***
Further comments on documents issued for the DDR
New comments in Blue

ID	Document	Section	Raised by	Comment	Response	Follow-up
5	*Ditto*	2.1.5.3	RCI	Delta T1 is missing in the max command rate formula. In any case the formula is very optimistic as the actual max rate (if SYN0=0) is around 500 commands per second.	This value is given for information only. I agree as not very realistic	Not changed OK?
6	*Ditto*	2.2.5.2	KJK	Add / to SetGetPhotoJfetPwr and SetGetPhotoOffset In SetGetPhotoOffset the channel number can only be 0 to 31 (not 0 to 32), which presumably correspond to channel numbers 1 to 32 in table 2.2.6.4. Similarly for SetGetSpectroOffset.	Text & value corrected for both Photometer and Spectrometer. 0 to 31 (physical address) effectively corresponds to 1 to 32 (LIA_P channel number) 0 to 23 (physical address) effectively corresponds to 1 to 24 (LIA_P channel number)	Closed
7	*Ditto*	2.2.5.3	KJK	SetGetSpectroHeaterPwr should be SetGetSpectroHeaterBias (to be consistant with Photo table)	Oops - Corrected	Closed
8	*Ditto*	2.2.6.1.4	KJK	Description for SetDemodPh should be 'Set the bolometer group demodulation phase shift'	Corrected. Command acronyms also corrected to respectively SetPhotoDemaPh and GetPhotoDemoPh (Photo was missing)	Closed
9	*Ditto*	2.2.6.1.6	KJK	Heading should be PhotoHeaterBias to be consistant with table 2.2.5.2.	Oops - Corrected	Closed

Consolidated Comments on DCRU Documents
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Further comments on documents issued for the DDR
New comments in Blue

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10	*Ditto*	2.2.6.5.8	KJK	Description for GetSpLWJfetVSS should be 'Get S-LW JFET source voltage' Description for SetSpLWJfetVSS should be 'Set S-LW JFET source voltage'	Letters inverted - Corrected	Closed
11	*Ditto*	2.2.6.7.1	KJK	I imply from the desciption of the science frames in section 2.3.5 that if bit 3 is set to 1 (test) then bits 2 to 0 may only be set to 0 or 4. What happens for other combinations?	I already address this point with F.PINSARD but with not conclusion. I have the feeling the definition of this command has to be modified or even splitted into 2 or 3 commands; the present definition is to confusing even for us! Action open to enhance this point	Still open, current text is still not clear
12	*Ditto*	2.2.7.1	KJK	If PhotoDivBias (why not BiasDiv - see 2.2.6.1.1?) is set to 0 the sampling frequency will be infinite! What actually happens? Presumably setting Channel_P1 to 0 selects Channel 1 of LIA_P1 etc?	**Action to F.PINSARD to clarify this point**	**Closed**

Consolidated Comments on DCRU Documents
Edited: B. Swinyard/E Sawyer; ***reply from CEA 02-12-2002***
Further comments on documents issued for the DDR
New comments in Blue

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13	*Ditto*	2.2.7.2	KJK	If SpectroBiasDiv (why is it BiasDiv rather than DivBias?) is set to 0 the sampling frequency will be infinite! What actually happens? Presumably setting Channel_S1 to 0 selects Channel 0 of LIA_S1 etc?	**Action to F.PINSARD to clarify this point**	Still open text not changed
14	*Ditto*	2.2.7.3	KJK	Data modes 05 and 06 are reversed with respect to section 2.2.6.7.1	**Action to F.PINSARD to clarify this point**	closed
15	*ditto*	2.2.8.1	KJK	Step 1: to set the Photo Bias Frequency the parameter is PhotoMClkDiv Step 2: to set the Photo Sampling Frequency the parameter id PhotoBiasDiv (or PhotoDivBias) Step 3: There are 448 cases for each BDA Step 25: Why has value EF been chosen? Step 30: There are 448 cases for each BDA Step 38: Why has value EF been chosen?	**Action to F.PINSARD to clarify this point**	Closed, but questions about steps 25 and 38 unanswered – see new question later
16	*Ditto*	2.2.8.4.1	KJK	Step 1: Ther is no such command Step 1: Ther is no such command	**Action to F.PINSARD to clarify this point**	Closed

Consolidated Comments on DCRU Documents
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Further comments on documents issued for the DDR
New comments in Blue

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17	*Ditto*	2.2.15	KJK	There are parameters that are missing compared to previous version of the ICD, such as DAQ and LIA voltage supplies. Is this deliberate or are they to be found somewhere else?	DAQ and LIA supply voltages are no more routed through the SCU (using the now removed DISTRIB module). Those parameters are transmitted as binary flag by the DCU (see §2.2.5.6: PWR_STATUS)	Closed
18	*Ditto*	2.3.5.3.1.	KJK	The table shows a Data Structure length of 294 for frames of Photometer Full Array. There are 288 detector channels to be sampled (see table 2.3.5.3.2). There is one word at the end of the Data Structure containing the ADC Status. What are the other 5 words? Similarly the other Frame lengths are 5 words longer than necessary - or does the table give the total length of the frame rather than the length of the Data Structure?	The last column corresponds to the total length of the frame. Table column heading has been corrected	Closed

Consolidated Comments on DCRU Documents
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Further comments on documents issued for the DDR
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19	*Ditto*	2.3.5.3.2	KJK	It is not clear in which order the pixels are stored in the data frame. Can I assume that the pixels are stored in the order reading across each row (CH1/LIA_P1, CH16/LIA_P2 .....) for each row in turn, starting at the top? Is it true that the first 144 data in this table correspond to the Photometer SW array, the next 96 data correspond to the MW Array and the final 48 data correspond to the LW array? And this is the order in which they will appear in Frame IDs 2, 3, and 4? Is the arrangement similar for the spectrometer table?	The tables (for photometer and spectrometer modes) give the order the analog channels are temporally multiplexed for each ADC. The order the pixels are stored in the data frame is obtained be assuming ADC 1 to ADC 6 interleaved by the FPGA. Then the table is to be read line by line. According to the SPIRE block diagram (from John) the BDA channel to DRCU board cross reference is: - PSW 1 to 144 : J5/J6 = LIA_P1 J7/J8 = LIA_P2 J9/J10 = LIA_P3 J11/J12 = LIA_P4 J13 = LIA_P5 - PLW 1 to 48 : J14 = LIA_P5 J15/J16 = LIA_P6 - PMW 1 to 96 : J17/J18 = LIA_P7 J19/J20 = LIA_P8 J21/J22 = LIA_P9 - SSW 1 to 48 : J23/J24 = LIA_S1 J25/J26 = LIA_S2 - SLW 1 to 24 J27/J28 = LIA_S3 - T/C : J22 = LIA_P9 To get an answer to the second part of your question please refer to the extract of the ICD. Tables are now in colours each one corresponding to a wavelength.	Closed

Consolidated Comments on DCRU Documents
Edited: B. Swinyard/E Sawyer; ***reply from CEA 02-12-2002***
Further comments on documents issued for the DDR
New comments in Blue

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20	*Ditto*	2.3.5.3.4	KJK	I believe frame type T4 contains the 32 bit time reference of the crossing, rather than the delta time. Can you confirm this? I would have expected Frame Type T7 to contain similar data to type T6 (i.e. jiggle position and error signal) Again the table seesm to give the Total Frame Length rather than the Data Structure length. Please clarify.	See proposal for chapter update according to D.FERRAND document MCU/DCU Command Telemetry (20/09/2002) Yes. Column heading modified to Frame length	Closed
21	*Ditto*	2.3.5.3.5	KJK	Why is the Frame T10 of length 30. This implies only 25 hsk parameters, but my reading of section 2.2.14 indicates more parameters are available. Please put a table of which parameters go where in the Frame.	DRCU spec. (DRCU req 79) specifies a list of 24 parameters. Then the legth of the frame is given by: 1 wd for length + 1 wd for frame ID + 24wds for data + wd 1 for Data Status + 2wds for frame time + 1 wd for check word = 30 wds **Action to SCU designers to give such list**	Closed

Consolidated Comments on DCRU Documents
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Further comments on documents issued for the DDR
New comments in Blue

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22	*Ditto*	2.3.6	KJK	I have tried to understand the reference document but I think there is more information needed to allow someone to calculate the pseudo random sequence expected. We need to know which bits are being fed back into the register and whether they are being modified before being fed back. A table of the first few values for each LFSR would be useful to allow us to check our code. Please clarify whether all the data in a single frame has the same value or is a new value calculated for each data in the frame?	Yes such a table has to be given in the ICD. **Action on myself to prepare tables for DCU/MCU and SCU** No - a new value is calculated	Still open

Consolidated Comments on DCRU Documents
Edited: B. Swinyard/E Sawyer; ***reply from CEA 02-12-2002***
Further comments on documents issued for the DDR
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DPU - ICD-23	*DRCU to DPU ICD Sap-SPIRE-CCA-076-02 (version 1.0)*	2.2.5.2	KJK	Command Set/GetPhMLWJfetVss should be Set/GetPhMWJfetVss Command Set/GetPhLWJfetVss is missing Command Set/GetPhotoJfetPwr should be replaced by Set/GetPhSWJfetPwr and Set/GetPhMLWJfetPwr		
DPU - ICD-24	*Ditto*	2.2.7.2	KJK	The values of Vbmax, Vhmax and Vssmax need to be defined in the table as is done in the photometer table		
DPU - ICD-25	*Ditto*	2.2.8.1.1	KJK	VSS1 etc are no longer required parameters to the SetPhSWJfetVss commands in steps 11 to 22		
DPU - ICD-26	*Ditto*	2.2.8.1.1	KJK	Step 25 specifies setting the detector Bias to a DC value (SetPhotoBiasMode= EF). What is the purpose of this? Is the DC bias mode still available (see comment on the DCU Design document)? Similar comment for step 38 in section 2.2.8.1.2		

DPU - ICD-27	*Ditto*	General	KJK	There are many parameters that are not set in the normal power on sequences provided. Therefore I assume there is some default value included in the FPGA code. These default values should be provided.		
DPU - ICD-28	*Ditto*	2.2.2	KJK	I believe the CmdIfStat, CmdIfCtrl and SubSDelay commands can be sent to each of the three DRCU subsystems (DCU, MCU, SCU). This is not clear here as although the section is headed 'DRCU command description' the Unit field for these commends is set to DCU		
DPU - ICD-29	*Ditto*	2.2.2.2	KJK	This command allows the relevant part of the command interface to a DRCU unit (or the unit itself) to be reset by setting the appropriate bit in the I/F control word to zero. If I read this I/F control word should I expect the value obtained to reflect the last value set with this command, or the current status of the interface? Do I have to send a command with value 7 to stop the reset being continually applied?		

DPU - ICD-30	*Ditto*	2.2.2.3	KJK	The SubSDelay parameter is defined as the 'maximum predefined response time' of the interface. As it cannot be set by command I assume this is a constant and could therefore be defined in the interface document. There is no need for this command. However, in section 2.2.3 this parameter is defined as the 'delay between command reception and response'. This value presumably changes with each command and should be a value between zero and the maximum response time. The command is, in this case, useful. Please clarify which interpretation is correct.		
DPU - ICD-31	*Ditto*	2.2.3	KJK	The definition of the conversion between received value and time for parameter SubSDelay is not clear - is the delay provided in microsecs? Is the divisor 319488?		

DPU - ICD-32	*Ditto*	2.2.6.2 and 2.2.6.4	KJK	These tables are not required as the relationship between LIA/Channel and pixel depends on external subsystems (harness and BDAs). The system team should be able to provide the mapping.		
DPU - ICD-33	*Ditto*	2.2.9.3	KJK	The command SetBootRam is specified to have a parameter in AD2 section 4.1.1 step 5 but not here. Which document is correct?		
DPU - ICD-34	*Ditto*	2.2.9.5.1	KJK	Command SetChopLoopMode is writeonly and so should be in a separate section as for SMEC writeonly commands		
DPU - ICD-35	*Ditto*	2.2.9.5.2	KJK	Command GetChopStatus is missing		
DPU - ICD-36	*Ditto*	2.2.9.6.1	KJK	Command SetJigLoopMode is writeonly and so should be in a separate section as for SMEC writeonly commands (section 2.2.9.4.3)		
DPU - ICD-37	*Ditto*	2.2.9.6.2	KJK	This section should be provided and contain the table of Jiggle Readonly commands		

DPU - ICD-38	*Ditto*	2.2.9.7	KJK	There are only 4 Set/GetPack10Param* commands (and their arguments) The Set/GetPack12Param* commands are missing from the table		
DPU - ICD-39	*Ditto*	2.2.13.2	KJK	The frame Number in the Set/GetSeqLength command should range from 0 to 31		
DPU - ICD-40	*Ditto*	2.2.14.1.13	KJK	The description for command SetScuContrl is incorrect		
DPU - ICD-41	*Ditto*	2.2.15	KJK	This section needs to be completed before issue especially for FrameType, and ScuStatus (which is missing from the table)		
DPU - ICD-42	*Ditto*	2.3.5.3.1	KJK	A table showing the time of sampling of each channel/LIA with respect to the start of sampling should be given so that we know the delay between one pixel data and another (This information is in the DCU Design Description, but that is not referenced by this document)		
DPU - ICD-43	*Ditto*	2.3.5.3.2	KJK	The contents of other frame types (e.g. P-SW, PMW, P-LW etc) needs to be indicated.		

DPU - ICD-44	*Ditto*	2.3.5.3.5	KJK	The first frame format should be labelled T4 not T5		
DPU - ICD-45	*Ditto*	2.3.5.3.5	KJK	The Frame Length given in the table for each frame are not correct		
DPU - ICD-46	*Ditto*	2.3.5.4	KJK	As I understand it the frame time is added to the data by the communication interface FPGA. In the case of the MCU there can be a delay between the data for a frame being available and the time at which the frame is created. What is the requirement on the maximum for this delay? Is the relevant SAp document available?		

Consolidated Comments on DCRU Documents
Edited: B. Swinyard/E Sawyer; ***reply from CEA 02-12-2002***
Further comments on documents issued for the DDR
New comments in Blue

ID	Document	Section	Raised by	Comment	Response	Status
MCU-CMD-01	*MCU/DCU Command List ICD and User Manual LAM/ELE/SPI.011011 (version 3.0)*	General	KJK	This document specifies the DRCU/DPU ICD as applicable to it. However the DRCU/DPU ICD document specifies this one as applicable! I suggest that the DRCU/DPU ICD is the controlling document and references this one for parts of the interface not defined there		
MCU-CMD-02	*Ditto*	3.1	KJK	The cold reset command example gives the hex code to send as 90010005. This does not agree with the DRCU/DPU ICD, which says that the command should be 90010002.		
MCU-CMD-03	*Ditto*	3.3	KJK	The description of the initialisation TrajModes does not indicate the location where the SMEC finishes. Also during intialisation several values are found (the position of the endstops, the home position etc). It would be useful to be able to read these in order to monitor changes to these 'fixed' positions		
MCU-CMD-04	*Ditto*	3.3	KJK	The GetSmecStatus parameter specification does not indicate the meaning of each bit in the returned word		
MCU-CMD-05	*Ditto*	3.4	KJK	The GetChopStatus parameter specification does not indicate the meaning of each bit in the returned word		

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MCU-CMD-06	*Ditto*	3.6.1	KJK	It is not clear at what time the telemetry frames will start to be generated after the command is received. Can it be assumed that the first frame will be generated during the next full 360us cycle of the MCU control loop?		
MCU-CMD-07	*Ditto*	3.6.1	KJK	The frame formats are not described		
MCU-CMD-08	*Ditto*	3.6.1	KJK	It is not clear whether the 4 telemetry packets can be requested at the same time. It is implied by the comment in the table that both the BSM and the SMEC packets are generated during FTS scan mode, even though the command scenario in section 4.2.2.1 does not show this.		
MCU-CMD-09	*Ditto*	3.7	KJK	How is the SetDpuPollingTime parameter specified (in micros?). What is the default value?		

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MCU-CMD-10	*Ditto*	4.1.1	KJK	The SetDownloadConf command is specified with a parameter field of 0xC000, but the command definition in section 3.2 does not specify a parameter. Is this parameter for ground testing only? In this case, it should be included in the document with a note indicating the different versions of the command. The SetBootRam command is specified with a parameter of 0x0001, but the command definition in section 3.2 does not specify a parameter. Is this parameter for ground testing only? In this case, it should be included in the document with a not indicating the different versions of the command.		
MCU-CMD-11	*Ditto*	4.2.1	KJK	We should assume in the normal case that the launch latch is unlocked once after launch and is never relocked. Is this the case?		
MCU-CMD-12	*Ditto*	4.2.1	KJK	Is the polling command required from the DPU GetSmecStatus (GETERRORCODE is not defined in the document)?		
MCU-CMD-13	*Ditto*	4.2.2.1	KJK	This sequence assumes the SMEC is at the home position after initialisation or a scan has been performed. However a scan leaves the SMEC at the last TrajStartPosition (according to this procedure). Please clarify where the SMEC is at the end of each type of command.		

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MCU-CMD-14	*Ditto*	4.3.1	KJK	We should assume in the normal case that the launch latch is unlocked once after launch and is never relocked. Is this the case?		
MCU-CMD-15	*Ditto*	4.3.1	KJK	The SetBSMLaunchLatch command is specified with a parameter 0x0002, but in section 3.4 the command is specified to take a parameter value of 0 or 1		
MCU-CMD-16	*Ditto*	4.4	KJK	Is the polling command required from the DPU GetSmecStatus (GETERRORCODE is not defined in the document)? Do we need to execute GetChopStatus and GetJigStatus also?		

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DEV-PLN-01	*DRCU and WIH Development Plan Sap-SPIRE-JLA-0047-01 (version 4.0)*	General	KJK	The plan identifies milestones but with no dates attached. This makes it difficult to monitor progress. Dates should be added, or a separate list maintained.		
DEV-PLN-02	*Ditto*	General	KJK	This plan states that an overall schedule and a master schedule are maintained, but only the QM1 schedule has been provided. Where is the overall schedule?		