Herschel /SPIRE

DRCU AIV plan

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18/09/2002	1.1	- AIV steps for STM added / pages 23-25, - PB delivery to RAL mentioned for QM1 and QM2 / pages 36 and 48, - Detail of assembly actions page 20.
23/09/2002	1.2	- AIV sequence diagrams added (new chapter 10), - Power supply test equipment configurations modified (chapter 12).
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03/02/2003	2.0	Update of the test procedures for : - SCU QM1, QM2 and FM following the decisions taken during the meeting held on 10/12/2002, - DCU EM/QM1 following the decisions taken during the meeting held on 20/12/2002. This induces changes in the test matrixes (refer to pages 14 to 18) and in the sequence diagrams (refer to pages 22 to 24). - PSU (STM, EM, FM) tests and sequence diagrams added.

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TABLE OF CONTENTS

LIST of USED ACRONYMS

AIV	Acceptance, Integration and Validation
AVM	AVionic Model
BB	BreadBoard
BSM	Beam Steering Mirror
CDMS	Command and Data Management Subsystem
CDR	Critical Design Review
CEA	Commissariat à l'Energie Atomique
CQM	Cryogenic Qualification Model
DCU	Detector Control Unit
DDR	Detailed Design Review
DPU	Digital Processing Unit
DRCU	Detector Readout and Control Unit
DTU	DRCU Test Unit
EM	Engineering Model
FCU	Focal Plane Control Unit
FM	Flight Model
FPU	Focal Plane Unit
FS	Flight Spare model
FSE	Factory Support Equipment
FTS	Fourier Transform Spectrometre
GSE	Ground Support Equipment
GSFC	Goddard Space Flight Centre I&TIntegration and Test
H/K	HouseKeeping
I&T	Integration and Test
I/F	Interface
ICC	Instrument Control Centre
ICD	Interface Control Document
IID	Instrument Interface Document
IRD	Instrument Requirements Document
JPL	Jet Propulsion Laboratory
LAM	Laboratoire d'Astrophysique de Marseille
LETI	Laboratoire d'Electronique, de Technologie et d'Instrumentation
LTU	Local Test Unit
MCU	Mechanism Control Unit
OBS	Organisation Breakdown Structure
PACS	Photoconductor Array Camera and Spectrometer
PB	Power Bench
PDR	Preliminary Design Review
PFM	Proto Flight Model
PhFPU	Photometer Focal Plane Unit
PSU	Power Supply Unit
QM	Qualification Model
QMW	Queen Mary and Westfield College
RAL	Rutherford Appleton Laboratory
SAp	Service d'Astrophysique (CEA/DAPNIA)
S/C	SpaceCraft
SCU	Subsystem Control Unit

SEI	Service d'Electronique et d'Informatique (CEA/DAPNIA)
SIG	Service d'Instrumentation Générale (CEA/DAPNIA)
SMEC	Spectrometer MEChanism
SPIRE	Spectral and Photometric Imaging REceiver
STM	Structural and Thermal Model
SVM	SerVice Module
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
TC	Telecommand
TRB	Test Revue Board
TRR	Test Readiness Review
WE	Warm Electronics
WIH	Warm Interconnect Harness

1 Introduction

The SPIRE warm electronics consists of two boxes with direct connection to the FPU, the Detector Control Unit (DCU) and the Focal Plane Control Unit (FCU) (together these boxes are termed the Detector Readout and Control Unit (DRCU)) plus a Digital Processing Unit (DPU) with interfaces to the other two boxes and the spacecraft data handling system. The DCU provides bias and signal conditioning for the detector arrays and cold readout electronics and reads the detector signal. The FCU controls the FPU mechanisms and the 3He cooler and handles housekeeping measurements. The DPU acts as the interface to the spacecraft, including instrument commanding and formats science and housekeeping data for telemetry to the ground.

In the frame of HERSCHEL program, the CEA/Sap will develop and deliver to the SPIRE consortium the following subsystems :

- The Detector Readout and Control Unit (DRCU) models,
- The Warm Interconnect Harness (WIH) models,
- The Focal Plane Unit simulator.

This document deals with the Qualification, Integration and Test of the DRCU of the SPIRE instrument. In particular, it indicates the steps to be followed in the test process of the instrument from Structural and Thermal Model (STM), the first qualification model (QM1) to the final Flight Model (FM) (the tests performed on the Flight Spare model (FS) will not be detailed in that document). It consists in global, high level descriptions of the tests to be performed and gives an overview of the AIV activities required.

It aims at identifying the main AIV steps, the resources required and the documents to be written to fulfill the tests. Detailed tests will then be given in a further document.

2 Applicable documents

[AD1] HERSCHEL/SPIRE DRCU Interface Control Document	SAP-SPIRE-CCa-075-02
[AD2] HERSCHEL/SPIRE DRCU/DPU Interface Control Document	SAP-SPIRE-CCa-076-02
[AD3] Herschel/Planck Instrument Interface Document Part B Instrument “SPIRE”	SCI-PT-IIDB/SPIRE-02124
[AD4] HERSCHEL/SPIRE DRCU Subsystem specification	Sap-SPIRE-CCa-0025-00

3 Reference documents

[RD1] HERSCHEL/SPIRE DCU Design document	Sap-SPIRE-FP-0063-02 Issue 0.2
[RD2] DS-SPIRE development tree	Sap-SPIRE-DS - Version 07/03/2002
[RD3] FIRST/SPIRE DRCU and WIH Development Plan	SAP-SPIRE-JLA-0047-01
Table de configuration de tests	Issue 07/03/02
Spécifications modèle STM équipements électroniques	SAp-FIRST-TT-0011-00

4 Overview of the tests organization

This chapter aims at giving the general rules to be followed for the performance of the AIV actions.

The general AIV Test philosophy is the following :

The AIV will be made through the achievement of :
- Meetings/Reviews
  - TRR : Test Readiness Review,
  - TRB : Test Revue Board.
- Inspections, Assembly
  - Inspection of elements received from subcontractor,
  - Assembly of boards or sub units to constitute units.
- Tests
  - Functional/Performance tests in dedicated laboratories,
  - Qualification/Acceptance tests in environment test facilities.
- Documentation
  - Logbooks that follow the “life” of a tested element,
  - Templates the report the test,
  - Test procedures that specify the test,
  - Non Conformity records that report the non conformities.

The AIV actions will be organized in accordance with the following generic process :
- Inspection/Assembly,
- TRR which is a kind of technical statement before to proceed to a test,
- Functional / Performance test,
- TRB associated with Functional / Performance tests,
- TRR review before Qualification/Acceptance tests,
- Qualification/Acceptance tests,
- TRB,
- Delivery.

For each AIV action, one must identify :
- Who realizes the test and where,
- The content of the test,
- The responsibility, the laboratories (LAM, SEDI, JPL, Sap) involved, the subcontracted elements.

For each model, the AIV actions will be detailed in that document, the test equipment listed in chapter 14 and the documentation specified in chapter 15.

5 Unit descriptions and model philosophy

5.1 Detector Readout Control Unit description

The DRCU mounted on HERSCHEL SerVice Module (SVM) is composed of two subsystems :

- The Detector Control Unit (**DCU**)
  The DCU consists in a warm analogue electronics box for detector read-out analogue signal processing, multiplexing, Analogic/Digital (A/D) conversion, array sequencing.
  The electronic box DCU is composed by electronics modules connected to a back plane. There are 4 types of modules :
  - LIA_P boards (Photometer Analog Board)
  - LIA_S boards (Spectrometer Analog Boards)
  - LIA_TC board (Same as LIA_P board but with different gains)
  - BIAS boards (prime and redundant)
  - DAQ_IF (Data acquisition and interface) boards (prime and redundant)

  The number of each module depends on the configuration (QM1, QM2 or FM) and is given in [RD3].
  The layout of these boards is given in [RD1], § 3.1.1.1.
- The Focal plane Control Unit (**FCU**)
  The FCU consists in a warm analog electronics box for mechanism control, temperature sensing and general housekeeping and 3He refrigerator operation. It encompasses :
  - The Mechanism Control Unit (**MCU**) which is built by the LAM,
  - The Subsystem Control Unit (**SCU**)
  - Power Supply Unit (**PSU**)

The two main DRCU subsystems (DCU and FCU) are called units while the parts of the FCU (SCU, MCU and PSU) are called sub units.

In addition to the mentioned DRCU units and sub units, internal harnesses will be used to electrically connect DRCU units.

5.2 Model philosophy

The model philosophy for DRCU is as follows:

- The DCU breadboards validate the electronics design concepts. This breadboard model will be conceived by Sap and realized at JPL,
- The Structural and Thermal Models (STM) are used to verify the mechanical and thermal behaviours of the structures,
- The EM is used to perform electronic tests on boards; the boards are then part of the QM1,
- The QM1 are used to validate the electronics design concepts and functionality and the electrical I/Fs and budgets. The QM1 model philosophy is given in [RD3], § 3.1.
- The QM2 will be fully qualified (with environmental tests). The QM2 model philosophy is given in [RD3], § 3.1.
- The FM will be in compliance with the flight specifications. The FM model philosophy is given in [RD3], § 3.1.
- The FS will be in compliance with the flight specifications**.** The FS model philosophy is given in [RD3], § 3.1.

5.2.1 Model characteristics

The DRCU model characteristics presenting the complexity level to be reached by each model are given in [RD3], § 3.2.

5.2.2 Model configurations

The DCU, FCU (SCU, MCU) and PSU configurations (in particular, number of boards) for all models are given in [RD3], ANNEX I "**Product vs. Model Summary**".

6 Spare Kits (FS Model) philosophy

The AIV activities described in the frame of this document do not include the FS model. This chapter gives short information about the spare kits that constitute the Flight Spare model.

The boards constituting the FS model come from the same manufacturing procedure as for the Flight Model (same controls after manufacturing). At this stage, no further detailed specifications concerning the tests on spare kits that constitute the Flight Model are given.

7 Test definitions at unit level

Tests at unit level consist in tests performed with appropriate test facilities on DRCU assembled subsystems (DCU, SCU, MCU).

All the instruments delivered to the RAL will be
- tested
- ready for integration in the Warm electronic model of the instrument

This involves :
- ⇨ Unitary test and validation of the units/sub units boards (tests after boards manufacturing)
- ⇨ Successive assembly of the units (DCU, FCU) in their boxes
- ⇨ Integration of the units to constitute the DRCU
- ⇨ Full validation
  - o Verifications after assembly/integration
  - o Functionality
  - o Performance
- ⇨ Carrying out the Qualification tests (for QM2 only)
- ⇨ Carrying out the Acceptance tests (for FM only)

Before the integration phases, several tests are carried out to achieve the verification of each unit. The different unit level test steps for DCU, SCU and MCU are presented below. All of these tests are performed or not depending on the model.

Test name	Test description
Inspection	Visual inspection to verify: - Marking of the box and of the connectors, checking of the connector itself - Mechanical integrity of the box - Surface treatment status of the box Review of the delivered documentation
Verification of the physical properties and the conformance to MICD (**M**echanical **I**nterface **C**ontrol **D**rawing)	- Dimensions - Weight - Centre of gravity - Moments of inertia
Electrical tests	- Grounding and insulation check - Power consumption measurement - Pin check and signal levels verification
Functional tests	- Listed in appendix A
Performance tests	- Listed in appendix B
Vibration tests	- Sinus and random vibration
Thermal balance tests	-Thermal design verification
Thermal vacuum tests	- Functional tests at thermal vacuum environment and thermal cycling (before, during and after)
EMI / EMC tests	- Radiated susceptibility - Radiated emission - Conducted emission - Conducted susceptibility - ESD
Shock	All boxes mounted on the HS SVM (HS FCU and HS DCU)

Table 7-1 Test Definition

8 Test matrixes at sub unit, unit or integrated unit levels

The tests will be performed at units (DCU, FCU), sub unit levels (SCU, MCU, PSU) or integrated unit level (DRCU). The tables given in this chapter summarizes the tests performed at these levels.

8.1 Notations for the test matrixes

This paragraph details the notations used in the tests matrixes.

The AIV actions (or checks) will be carried out either by analysis (**A**) or by test (**T**).

- ⇨ For analysis, we shall note **A,**
- ⇨ For test, we shall note **T**.

The particular activities relative to Packing/Shipping activities will be noted **P**.

The FCU unit and DRCU (DCU/FCU integrated units) will be tested with different PSU configurations; the following notations will therefore be added to the test symbol :

T $^{(0)}$	*These tests will be performed with the PB. This is the configuration which is used by default when nothing is added (***T***),*
T $^{(1)}$	*These tests will be performed while the PSU EM is assembled with the FCU box*
T $^{(2)}$	*These tests will be performed while the PSU STM is assembled with the FCU box and PB is used*
T $^{(3)}$	*These tests will be performed while the PSU FM is assembled with the FCU box*

When the configuration (model/element) does not justify or allow any test (due to test definition), the symbol "NA" is used;

When, in a given model/element configuration, we decide not to perform any test "No Test" is indicated.

The thermal tests may be performed at Ambient Pressure level ($\mathbf{T}_{AP}$ is then written) or at Vacuum conditions ($\mathbf{T}_{V}$ is then written).

Each action (Analysis or Test) referenced in the test matrixes is named with reference to an identified AIV step. The logic is the following :

An AIV action is named "MODEL-ELEMENT-ACTION" where :

- "MODEL" may be "QM1, QM2 or FM ",
- "ELEMENT" may be "DRCU, DCU, FCU, SCU or MCU ",
- "ACTION" may be :
  - "A" if the action is an inspection or assembly procedure or if it consists in the consecutive tests such as verification or simplified electrical tests for example,
  - "T" if the action is a functional, performance, qualification or acceptance test,
  - "I/T" if the action is an integration procedure followed by functional/performance tests such as those made on the DRCU,
  - "P" if the action is a packing/shipping action.
    - The number of the corresponding action is indicated after its name : "i".

As an example, the functional tests performed at Sap on DCU QM1 will be referenced as "QM1-DCU-T2".

In addition, in order to easily report to the AIV flow charts, the identified actions are referenced with respect to the corresponding paragraph of the AIV flow chart chapter (chapter 11).

8.2 Test matrix at integrated unit level

Integrated DCU / FCU (DRCU) test matrix :

Test / Model	QM1 § 11.2.5	QM2 § 11.3.5 and § 11.3.6	FM § 11.4.5
Integration / verification	**A** QM1-DRCU-I/T1	**A** QM2-DRCU-I/T1 QM2-DRCU-I/T2	**A**$^{(3)}$ FM-DRCU-I/T1
Electrical tests	**T** QM1-DRCU-I/T1	**T** QM2-DRCU-I/T1 QM2-DRCU-I/T2	**T**$^{(3)}$ FM-DRCU-I/T1
Functional tests	**T** QM1-DRCU-I/T1	**T**$^{(0)}$ QM2-DRCU-I/T1	**T**$^{(3)}$ FM-DRCU-I/T1
Performance tests	NA	**T**$^{(1)}$ QM2-DRCU-I/T2	**T**$^{(3)}$ FM-DRCU-I/T1
Vibration tests Qualification level Acceptance level	NA	No Test	No Test
Shock tests	NA	No Test	No Test
Thermal balance tests	NA	No Test	No Test
Thermal vacuum tests Qualification level Acceptance level	NA	No Test	No Test
EMI/EMC tests Qualification level Acceptance level	NA	No Test	No Test
Physical properties and conformance to MICD	NA	NA	NA

Test Matrix 8-1 DRCU test matrix

We here recall the notations :

(0) *These tests will be performed with the PB*
(1) *These tests will be performed while the PSU EM is assembled with the FCU box*
(2) *These tests will be performed while the PSU STM is assembled with the FCU box and PB is used*
(3) *These tests will be performed while the PSU FM is assembled with the FCU box*

8.3 Test matrixes at unit level

DCU test matrix :

Test / Model	STM § 11.1	QM1 § 11.2.1	QM2 § 11.3.1	FM § 11.4.1
Inspection	**A** STM-DCU-A1	**A** QM1-DCU-A1	**A** QM2-DCU-A1	**A** FM-DCU-A1
Electrical tests	**T**(**) STM-DCU-A1	**T** QM1-DCU-A1	**T** QM2-DCU-A2	**T** FM-DCU-A2
Functional tests	NA	**T** QM1-DCU-T1 QM1-DCU-T2	**T** QM2-DCU-T1	**T** FM-DCU-T1
Performance tests	NA	**T** QM1-DCU-T3	**T** QM2-DCU-T2	**T** FM-DCU-T2
Vibration tests (*) Qualification level Acceptance level	 **T** STM-DCU-T1	No Test	 **T** QM2-DCU-T3	 **T** FM-DCU-T3
Thermal balance tests	**T** STM-DCU-T2	No Test	No Test	No Test
Thermal tests (*) Qualification level Acceptance level	$\mathbf{T}_{AP}$(***) STM-DCU-T1	No Test	 $\mathbf{T}_V$ QM2-DCU-T3	 $\mathbf{T}_V$ FM-DCU-T3
EMI/EMC tests (*) Qualification level Acceptance level	NA	No Test	 **T** QM2-DCU-T3	 **T** FM-DCU-T3
Physical properties and conformance to MICD Acceptance level	No Test	No Test	No Test	 **T** FM-DCU-T3
Shock	No Test	No Test	**T** QM2-DCU-T3	No Test
Packing/Shipping	NA	**P** QM1-DCU/FCU-P1	**P** QM2-DCU/FCU-P1	**P** FM-DCU/FCU-P1

Test Matrix 8.3-1 DCU test matrix

(*) *Except for the STM, these tests are performed for qualification or acceptance of the units. These tests are performed under environment conditions, when the units are ready for DRCU integration. However, these environment tests will be performed at DCU unit level. The verification tests will be performed at DRCU unit level after these tests*

(**) *The STM electrical tests are simple electric verifications of resistor values*

(***) *For the STM, these thermal tests will be simplified; in particular, they will be performed at ambient pressure.*

$\mathbf{T}_{AP}$: Ambient Pressure level
$\mathbf{T}_V$: Vacuum conditions

We notice that compliance to MICD constraints are only applicable to DCU and FCU for only these two units have associated requirements. In the frame of the AIV plan, the MICD tests will be performed for FM only.

FCU test matrix :

Test / Model	QM1 § 11.2.4	QM2 § 11.3.4	FM § 11.4.4
Inspection	**A** QM1-FCU-A1	**A** QM2-FCU-A1 QM2-FCU-A2 QM2-FCU-A3	**A**(3) FM-FCU-A1
Electrical tests	**T** QM1-FCU-A1	**T** QM2-FCU-A1 QM2-FCU-A2 QM2-FCU-A3	**T**(3) FM-FCU-A1
Functional tests	**T** QM1-FCU-T1	**T** QM2-FCU-T1	**T**(3) FM-FCU-T1
Performance tests	No Test	No Test	No Test
Vibration tests (*) Qualification level Acceptance level	No Test	**T**(2) QM2-FCU-T2	**T**(3) FM-FCU-T2
Thermal balance tests	No Test	No Test	No Test
Thermal tests (*) Qualification level Acceptance level	No Test	$\mathbf{T}_V$(2) QM2-FCU-T2	$\mathbf{T}_V$(3) FM-FCU-T2
EMI/EMC tests (*) Qualification level Acceptance level	No Test	**T**(0) QM2-FCU-T1	**T**(3) FM-FCU-T2
Physical properties and conformance to MICD Acceptance level	No Test	No Test	**T**(3) FM-FCU-T2
Shock	No Test	**T**(2) QM2-FCU-T2	No Test
Packing/Shipping	**P** QM1-DCU/FCU-P1	**P** QM2-DCU/FCU-P1	**P** FM-DCU/FCU-P1

Test Matrix 8.3-2 FCU test matrix

We hereafter recall the notations :

(*) *These tests are performed for qualification or acceptance of the units. These tests are performed under environment conditions, when the units are ready for DRCU integration. However, these environment tests will be performed at FCU (with different PSU configurations) unit level. The verification tests will be performed at DRCU unit level after these tests*

(0) *These tests will be performed with the PB*
(1) *These tests will be performed while the PSU EM is assembled with the FCU box*
(2) *These tests will be performed while the PSU STM is assembled with the FCU box and PB is used*
(3) *These tests will be performed while the PSU FM is assembled with the FCU box*

8.4 Test matrixes at sub unit level

SCU test matrix :

Test / Model	STM	QM1 § 11.2.2	QM2 § 11.3.2	FM § 11.4.2
Inspection	NA	**A** QM1-SCU-A1	**A** QM2-SCU-A1	**A** FM-SCU-A1
Electrical tests	NA	**T** QM1-SCU-A1	**T** QM2-SCU-A2	**T** FM-SCU-A2
Functional tests	NA	**T** QM1-SCU-T1 QM1-SCU-T2	**T** QM2-SCU-T1 QM2-SCU-T2	**T** FM-SCU-T1 FM-SCU-T2
Performance tests	NA	**T** QM1-SCU-T1	**T** QM2-SCU-T1	**T** FM-SCU-T1
Vibration tests Qualification level Acceptance level	NA	NA	NA	NA
Thermal balance tests	NA	NA	NA	NA
Thermal tests Qualification level Acceptance level	NA	NA	NA	NA
EMI/EMC tests Qualification level Acceptance level	NA	NA	NA	NA
Physical properties and conformance to MICD	NA	NA	NA	NA
Shock	NA	NA	NA	NA

Test Matrix 8.4-1 SCU test matrix

Notes :
- *For QM1, the mentioned tests are performed by the SEDI,*
- *For QM2 and FM models, the mentioned functional performance tests are part of those realized by the subcontractor (based on those specified by the SEDI when developing the QM1 model). These tests will be performed using the means and procedures delivered by the SEDI.*

MCU test matrix :

Test / Model	STM	QM1 § 11.2.3	QM2 § 11.3.3	FM § 11.4.3
Inspection	NA	**A** QM1-MCU-A1	**A** QM2-MCU-A1	**A** FM-MCU-A1
Electrical tests	NA	**T** QM1-MCU-A1	**T** QM2-MCU-A1	**T** FM-MCU-A1
Functional tests	NA	**T** QM1-MCU-A1	**T** QM2-MCU-A1	**T** FM-MCU-A1
Performance tests	NA	**T**	**T**	**T**
Vibration tests Qualification level Acceptance level	NA	NA	NA	NA
Thermal balance tests	NA	NA	NA	NA
Thermal tests Qualification level Acceptance level	NA	No Test	No Test	No Test
EMI/EMC tests Qualification level Acceptance level	NA	No Test	No Test	No Test
Physical properties and conformance to MICD	NA	NA	NA	NA
Shock	NA	NA	NA	NA

Test Matrix 8.4-2 MCU test matrix

Note : The mentioned performance tests are part of those realized by the LAM. We shall perform these tests using the means and procedures delivered by the LAM.

The only AIV actions performed at Sap concern the inspection at delivery of the MCU in its FCU like box. This action will be referenced as named QM1-MCU-A1, QM2-MCU-A1 and FM-MCU-A1 depending on the model which is concerned.

The MCU removal from its FCU like box and its integration within the SCU FCU box involves all necessary electrical and mechanical verifications as well as the necessary (TBD) functional/performance tests. These actions are referenced in the FCU assembly actions named QM1-FCU-A1, QM2-FCU-A1 and FM-FCU-A1 following the model which is concerned.

8.5 PSU test matrix

The table hereafter summarizes the tests performed on the PSU after the delivery at SAp.

Test name	STM	EM	FM
Incoming inspection	A STM-PSU-A1	A EM-PSU-A1	A FM-PSU-A1
Incoming tests	T* STM-PSU-T1	T EM-PSU-T1	T FM-PSU-T1

Test Matrix 8.5-1 MCU test matrix

T The STM functional tests are simple electrical verifications of resistor values.*

9 Assembly, Integration, Verification and Packing/Shipping phases

In this document, we call Assembly, Integration, Verification, the phases that allow to assemble or integrate units together along with the associated tests and verifications.

The packing/shipping activities consists in the actions and verifications needed when packing/shipping elements to be delivered.

The corresponding actions are detailed in this chapter. Basically, they consist in the assembly/integration/packing/shipping itself together with the associated verification tests (depending on the action, these may be electrical tests, simplified tests of functionalities, visual inspections).

The Assembly phases consist in gathering elements in a box so as to create a new unit (examples : the assembly of the boards to create the DCU, the SCU/MCU/PSU assembly to create the FCU).

The Integration phases consist in connecting several units together to perform a test (as an example, the DRCU consists in the DCU – FCU integration).

Both of these phases are quite simple for they only involve connection verifications (mechanic, electric), electrical compatibilities and some simplified performance verifications (TBD).

9.1 List of Inspection, Assembly or Integration actions

At Sap, there are several actions consisting in Inspection, Assembly or Integration. These are listed below :

STM model				
1. DCU		Assembly		STM-DCU-A1
QM1 model				
2. DCU		Assembly		QM1-DCU-A1
3. SCU		Assembly		QM1-SCU-A1
4. MCU	Inspection			QM1-MCU-A1
5. FCU : SCU/MCU		Assembly		QM1-FCU-A1
6. DRCU : DCU/FCU			Integration	QM1-DRCU-I/T1
QM2 model				
7. DCU	Inspection			QM2-DCU-A1
8. DCU		Assembly		QM2-DCU-A2
9. SCU	Inspection			QM2-SCU-A1
10. SCU		Assembly		QM2-SCU-A2
11. MCU	Inspection			QM2-MCU-A1
12. FCU : SCU/MCU		Assembly		QM2-FCU-A1
13. DRCU : DCU/FCU(SCU/MCU)			Integration	QM1-DRCU-I/T1
14. FCU : SCU/MCU/PSU_EM		Assembly		QM2-FCU-A2
15. DRCU : DCU/FCU(SCU/MCU/PSU_EM)			Integration	QM1-DRCU-I/T2
16. FCU : SCU/MCU/PSU_STM		Assembly		QM2-FCU-A3
FM model				
17. DCU	Inspection			FM-DCU-A1
18. DCU		Assembly		FM-DCU-A2
19. SCU	Inspection			FM-SCU-A1
20. SCU		Assembly		FM-SCU-A2
21. MCU	Inspection			FM-MCU-A1
22. FCU : SCU/MCU/PSU_FM		Assembly		FM-FCU-A2
23. DRCU : DCU/FCU(SCU/MCU/PSU_FM)			Integration	QM1-DRCU-I/T1

9.2 Detail of Inspection actions

The following inspection tests will be performed each time an unit is received from subcontractor. Inspection action involves an incoming inspection as well as Incoming tests. These are detailed hereafter :

- **Incoming inspections** : Visual inspection to verify:
  - Marking of the box and of the connectors, checking of the connector itself,
  - Mechanical integrity of the box,
  - Surface treatment status of the box,
  - Review of the delivered documentation,
- **Incoming tests** : Simplified functional tests [(i)].

[(i)] Simplified functional tests may be performed using subcontractor's test procedures and test equipments.

These inspection actions concern the actions 4, 7, 9, 11, 17, 19 and 21 as listed in § 9.1.

9.3 Detail of Assembly actions

The following tests will be performed during Assembly :

- Visual inspection,
- Electrical interface verification to check the compatibility (electrical mass, Back Plane isolation …),
- Mechanical assembly,
- Electrical tests,
- Simplified Functional tests [(ii)].

These assembly actions concern the actions 1, 2, 3, 5, 8, 10, 12, 14, 16, 10, 20 and 22 as listed in § 9.1.

[(ii)]The simplified functional tests will be performed progressively during the assembly. Theoretically, the assembly phase ends when the unit is closed and no more action performed inside it.
Note that functional and performances tests may be performed before the unit is closed in order to allow modifications. Therefore, we will allow this phase to last until the delivery of the unit (all models) or the shipping to environment test facilities (for QM2 and FM).

9.4 Detail of Integration actions

The following tests will be performed after DCU/FCU integration :

- Visual inspection,
- Electrical interface verification to check the compatibility of DCU with FCU (and PSU if required),
- Electrical tests.

These integration actions concern the actions 6, 13, 15 and 23 as listed in § 9.1.

Note : an integration action is always associated the functional or performance test for which the integration is required

9.5 Packing/Shipping actions

The packing/shipping actions consist in the AIV actions required to transfer an unit. This is required when shipping an unit to a test facility (for environment tests at Intespace or other test facility for example), when shipping the DRCU to the RAL or transferring the DCU from JPL to Sap.

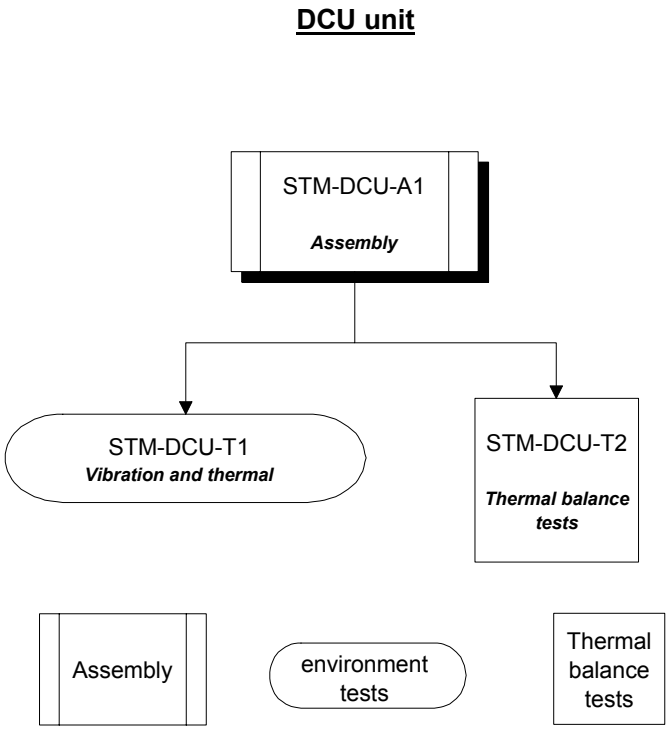
10 AIV sequence diagrams

The AIV actions (Assembly, functional, performance, qualification or acceptance tests, shipping, Integration …) that will be performed for the STM, QM1, QM2 and FM are sequenced as detailed in the following diagrams.

Each identified action is detailed in its goals and means in the AIV flow charts given in chapter 11.

10.1 STM sequence diagram

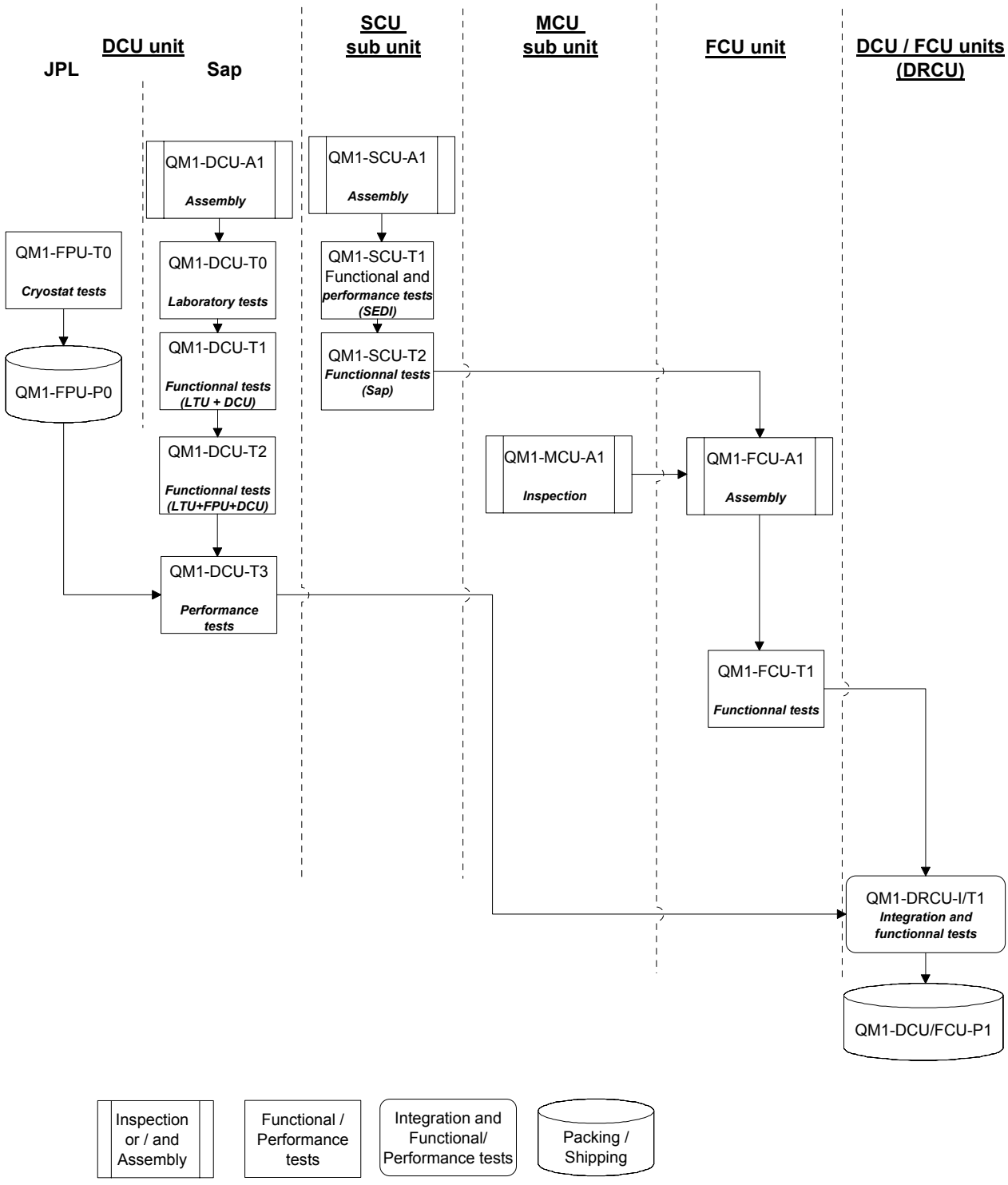
The hereafter diagram gives the sequence of the AIV actions to be performed on the STM.



Sequence diagram 10.1-1 STM sequence diagram

10.2 QM1 sequence diagram

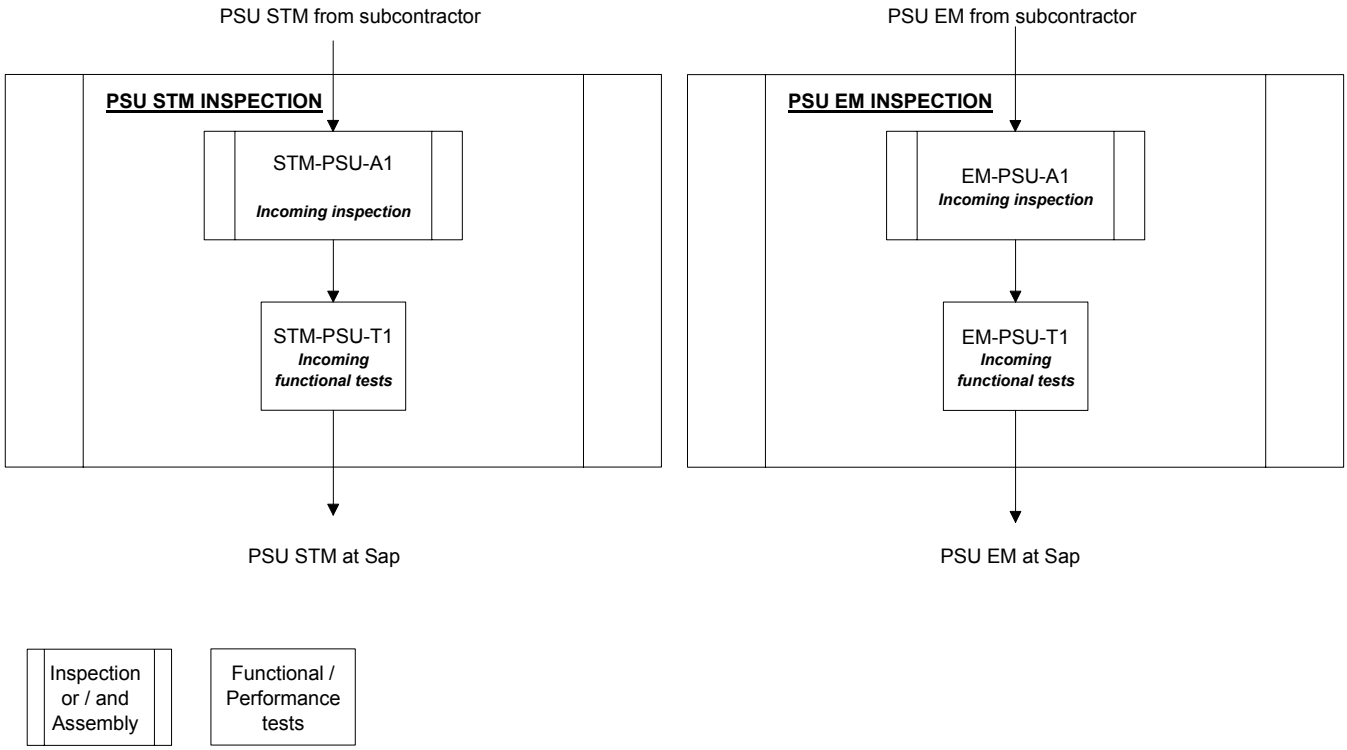
The hereafter diagram gives the sequence of the AIV actions to be performed on the QM1.



Sequence diagram 10.2-1 QM1 sequence diagram

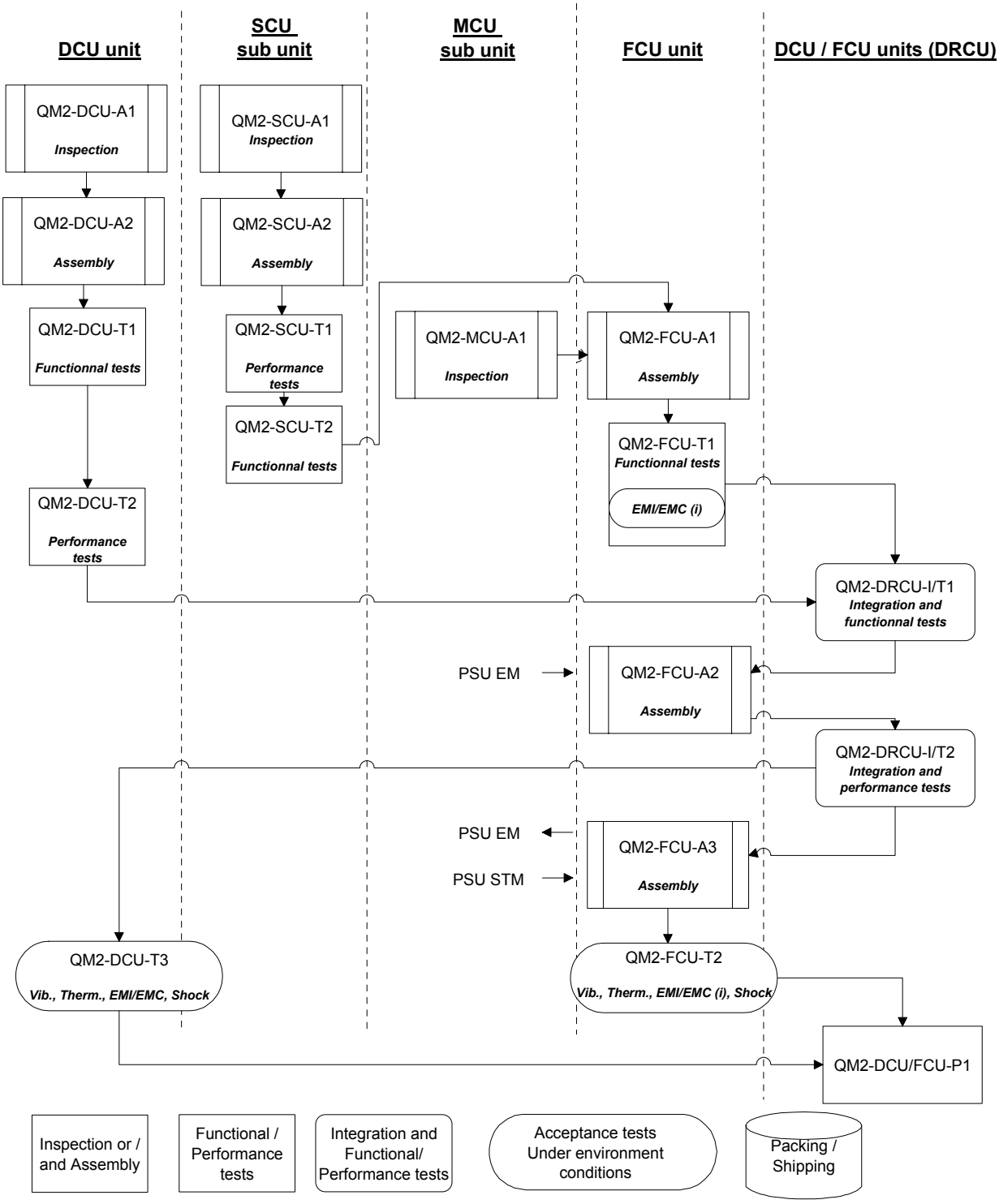
10.3 QM2 sequence diagram

Before to detail the QM2 sequence diagram, we thereafter detail the sequence diagrams concerning the PSU EM and PSU STM :



Sequence diagram 10.3-1 PSU STM and PSU EM sequence diagrams

The hereafter diagram gives the sequence of the AIV actions to be performed on the QM2.

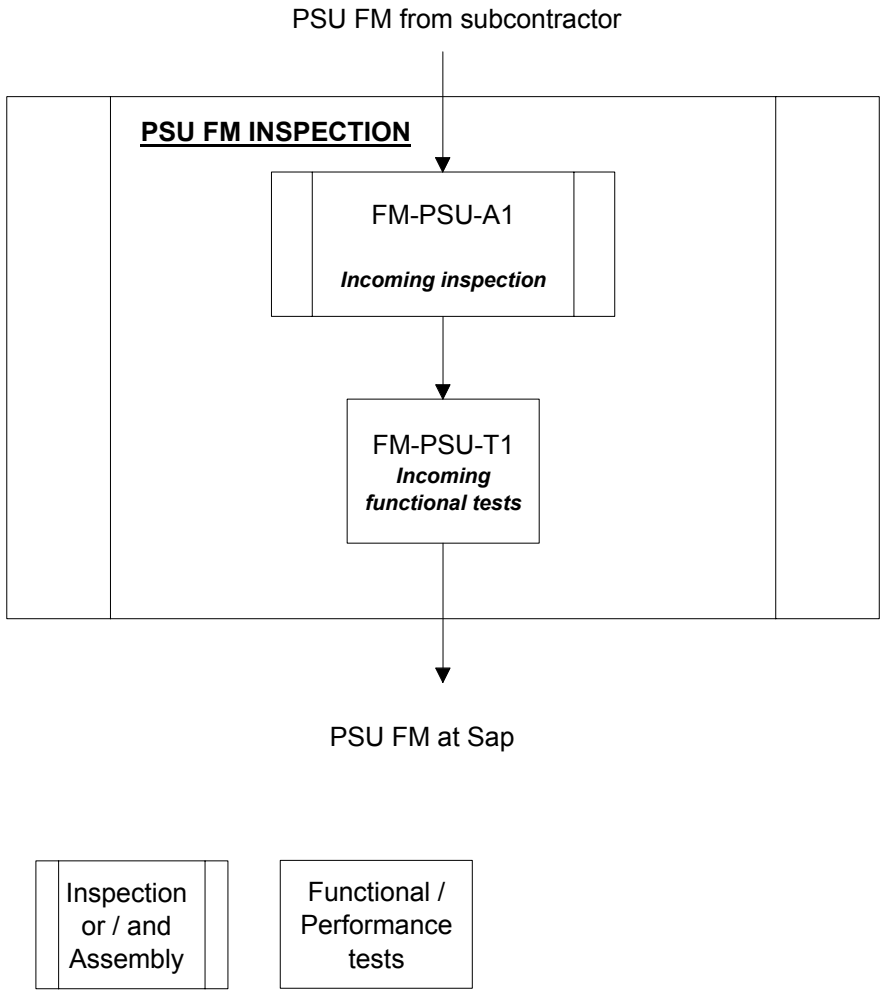


Sequence diagram 10.3-2 QM2 sequence diagram

(i) if not being performed during QM2-FCU-T1, EMI/EMC tests will be performed during QM2-FCU-T2

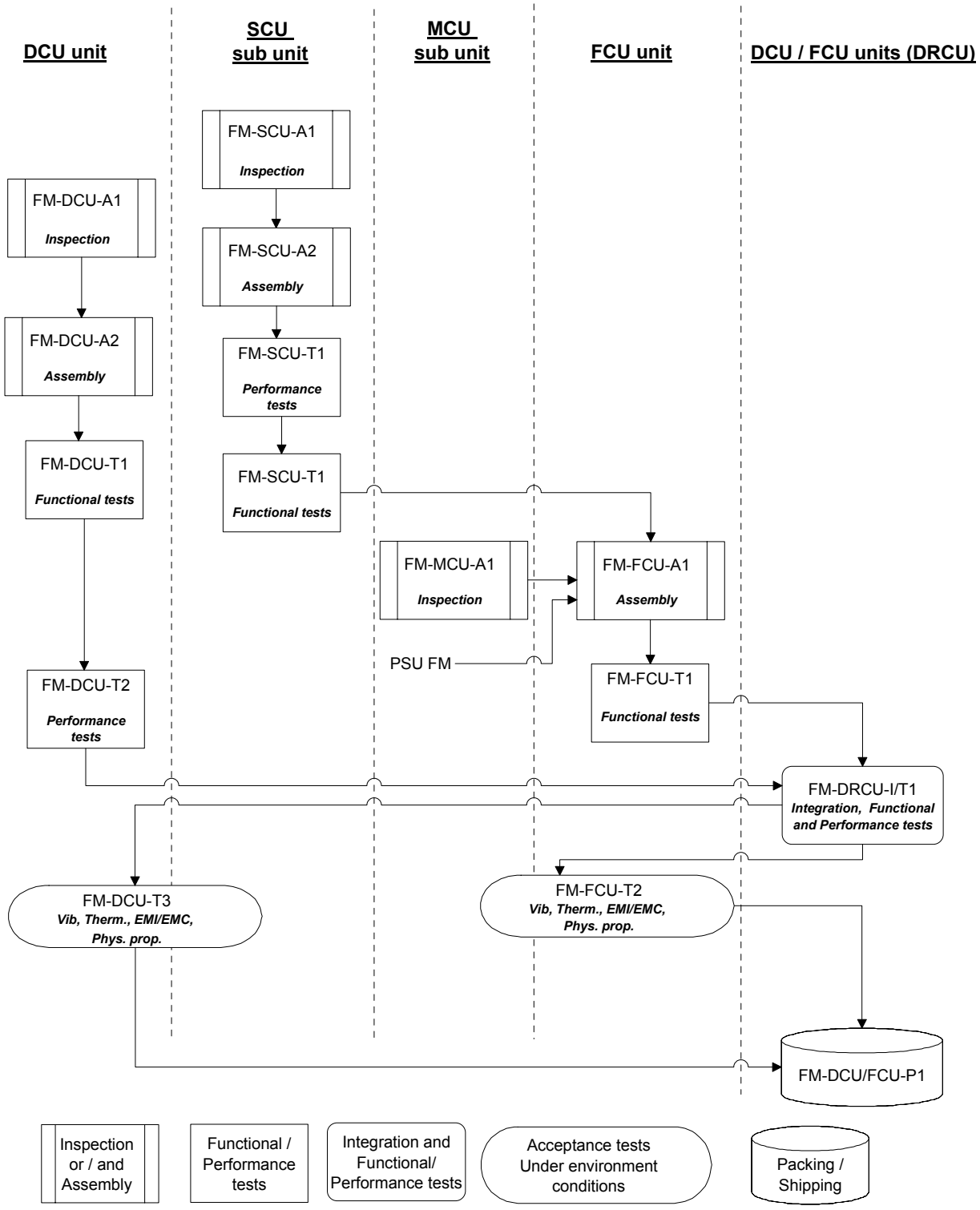
10.4 FM sequence diagram

Before to detail the FM sequence diagram, we thereafter detail the sequence diagrams concerning the PSU FM :



Sequence diagram 10.4-1 PSU FM sequence diagram

The hereafter diagram gives the sequence of the AIV actions to be performed on the FM.



Sequence diagram 10.4-2 FM sequence diagram

11 AIV actions diagrams (flow charts)

The AIV action diagrams, called flows charts, are here given using the following standard representation : Each box represents an ACTION (Test, Integration …) which requires :

- INPUT DATA that will be modified by the action (test document to be fulfilled for example),
- MEANS that are necessary to perform the action (test facilities, human resources, documentation …)
- CONTROL DATA that consist in conditions that allow or not the ACTION to be performed

The OUTPUT DATA then represent the result of the ACTION (fulfilled test plan, list of points not in concordance with requirements).

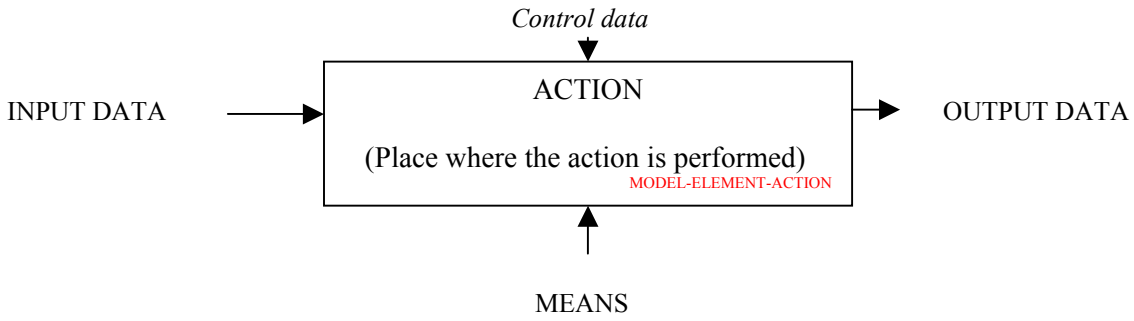
Each action shall be summarized in its goals (the purpose of the action). In accordance with the test matrixes given in chapter 8, the actions will be referenced by a name indicating the model, the element and the action performed as described below :

An AIV action is named "MODEL-ELEMENT-ACTION" where :

- "MODEL" may be "QM1, QM2 or FM ",
- "ELEMENT" may be "DRCU, DCU, FCU, SCU or MCU ",
- "ACTION" may be :
  - "A" if the action is an inspection or assembly procedure or if it consists in the consecutive tests such as verification or simplified electrical tests for example,
  - "T" if the action is a functional, performance, qualification or acceptance test,
  - "I/T" if the action is an integration procedure followed by functional/performance tests such as those made on the DRCU,
  - "P" if the action is a packing/shipping action.
    - The number of the corresponding action is indicated after its name : "i".

As an example, the functional tests performed at Sap on DCU QM1 will be referenced as "QM1-DCU-T2".

This leads to the following kind of diagram :



AIV flow chart

We will use logbooks to follow the life of each unit. When an assembly is performed, the logbook of the new created unit is opened.

For the manufactured elements such as boards, we shall use documents called event records. These records are opened once the manufactured elements are received.

The documents used to note the irregularities or points not in accordance with the requirements observed during a test are called Non Conformity Records (NCR).

The following pages detail the flow charts for the actions performed for each model (STM, QM1, QM2 and FM).

11.1 Representation of the AIV activities for the STM

The AIV activities for the STM concern only the DCU.

11.1.1 DCU STM assembly

At Sap, we receive DCU STM from subcontractor. Assembly activity will be performed in Sap after visual inspection of the received DCU STM.

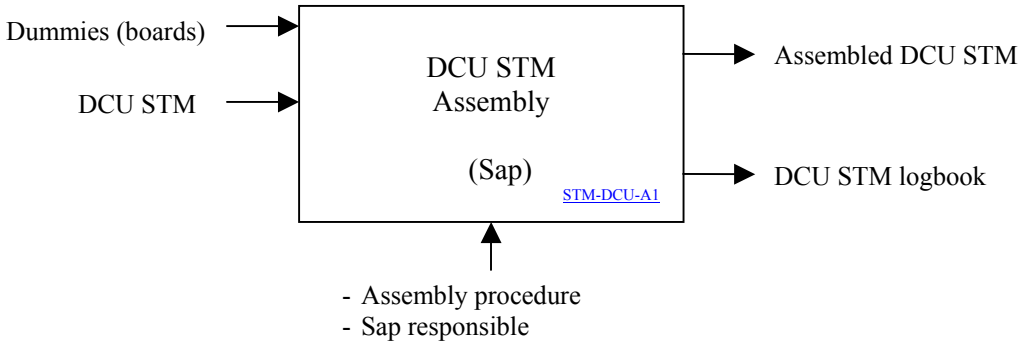


Diagram 11.1.1-1 DCU/STM assembly activities

11.1.1.1 DCU STM environment tests

The DCU STM will undergo vibration and thermal tests in environment conditions. The AIV flow chart is the following :

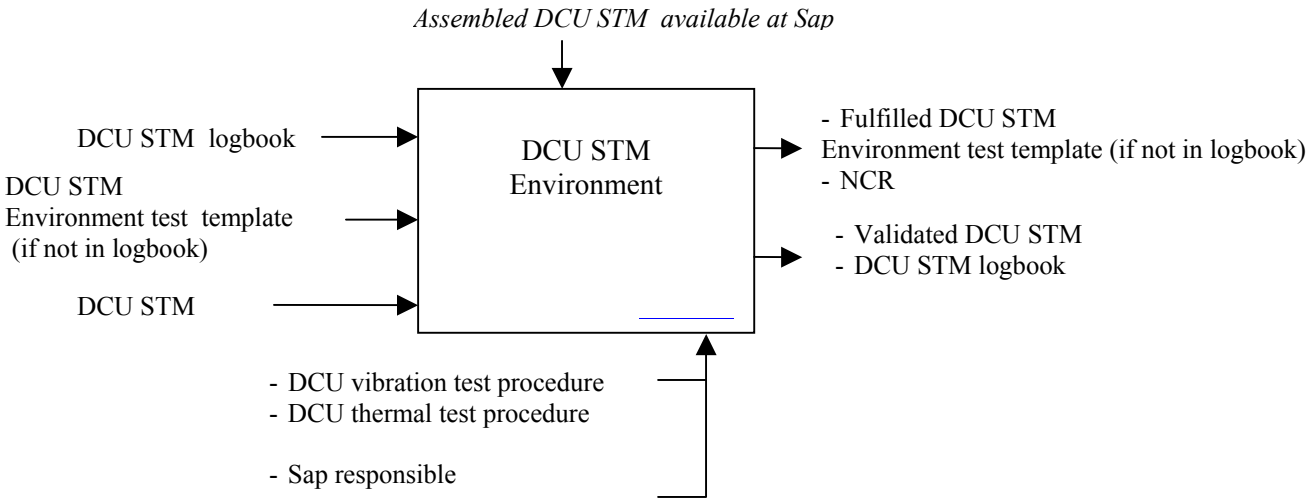


Diagram 11.1.1-2 DCU STM environment tests

The vibrations will be performed at qualification level,
The thermal tests will be performed at ambient pressure.

These environment tests as well as the resources required for each test will be detailed in further AIV documents.

11.1.2 DCU STM thermal balance tests

The DCU STM will undergo thermal balance tests. The AIV flow chart is the following :

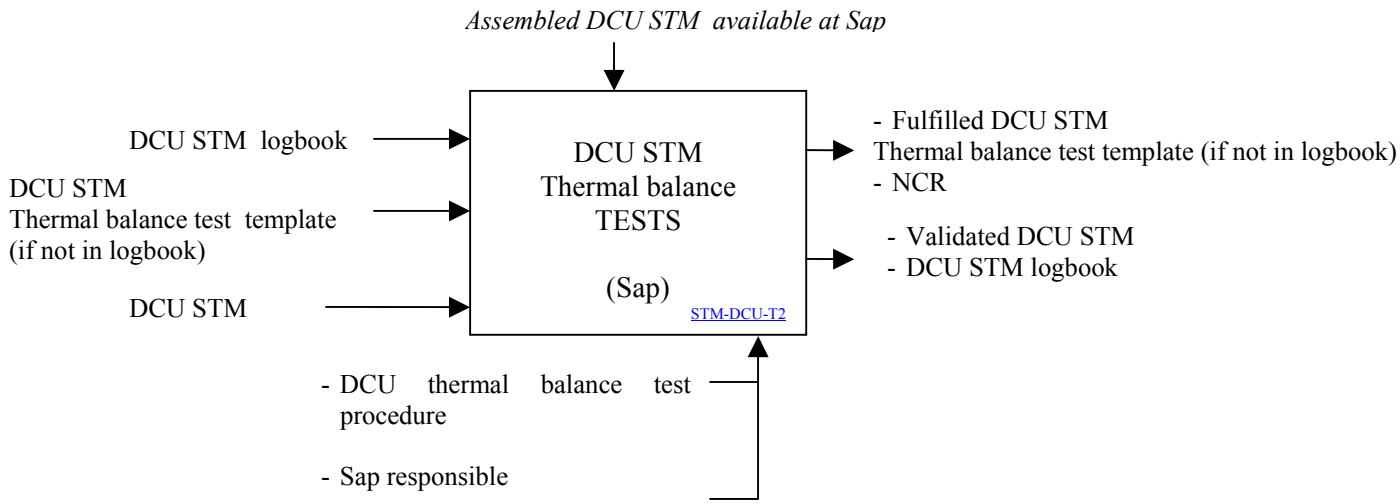


Diagram 11.1.2-1 DCU STM thermal balance tests

These thermal balance tests as well as the resources required for each test will be detailed in further AIV documents.

11.2 Representation of the AIV activities for the EM/QM1

We will thereafter describe the AIV steps for DCU, FCU (MCU, SCU) units.

11.2.1 DCU EM/QM1

Before the DCU QM1 delivery to RAL, the following AIV activities are performed :

The DCU EM/QM1 AIV activities consist in :
- the functionnal/performance tests on boards,
- the DCU EM/QM1 assembly
- the DCU EM/QM1 functionnal/performance tests using dedicated test equipments
- then, following these preliminary AIV activities, the complete DCU functionnal tests consisting in :
  - the DCU/LTU integration
  - the functionnal tests with LTU/DCU configurartion
  - the LTU, DCU, FPU simulator integration,
  - the functionnal tests with LTU/DCU/FPU simulator configurartion.

Simultaneously, in order to perform the DCU performance tests, the AIV will handle the following actions with the JPL cryostat :
- test of the JPL cryostat with JPL electronics,
- reception the cryostat at Sap
- connection of the DCU to the cryostat
- achievement of the DCU performance tests in that configuration

These steps are detailed in the following flow charts :

Preliminary AIV activities on the DCU EM/QM1 :

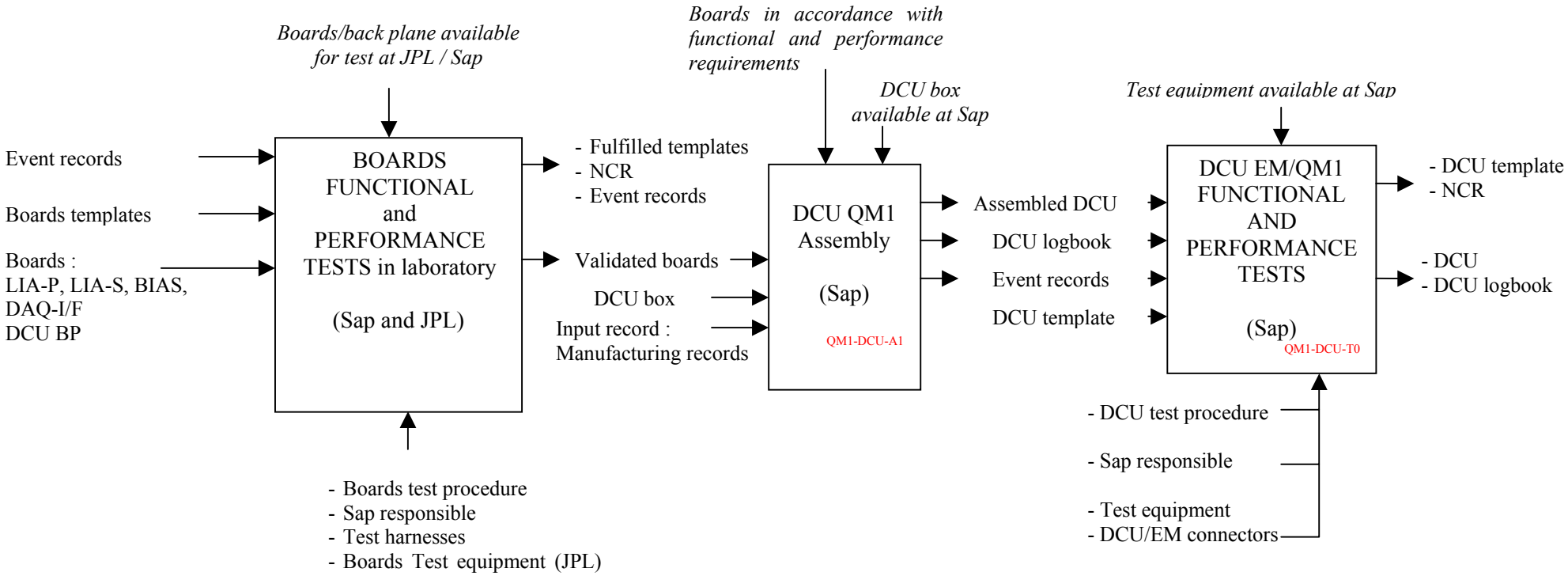


Diagram 11.2.1-1 DCU EM/QM1 boards tests and assembly

AIV activities related to JPL FPU cryostat :

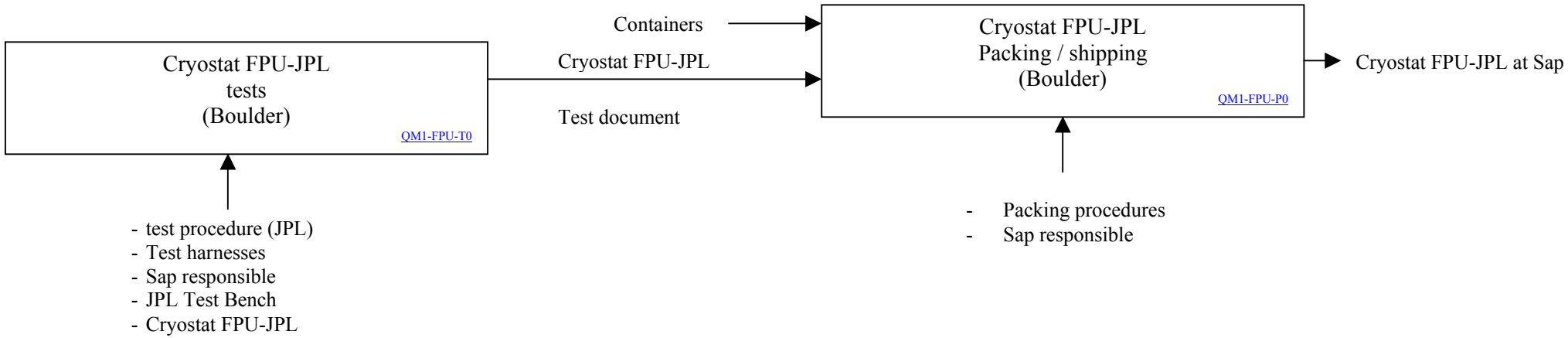


Diagram 11.2.1-2 DCU QM1 cryostat related activities at JPL

Note : Inspection tests of the received cryostat FPU JPL will also be planned.

Once the DCU assembly is performed (refer to § 9.3), the DCU EM/QM1 functional tests are performed at Sap according to the following flow chart :

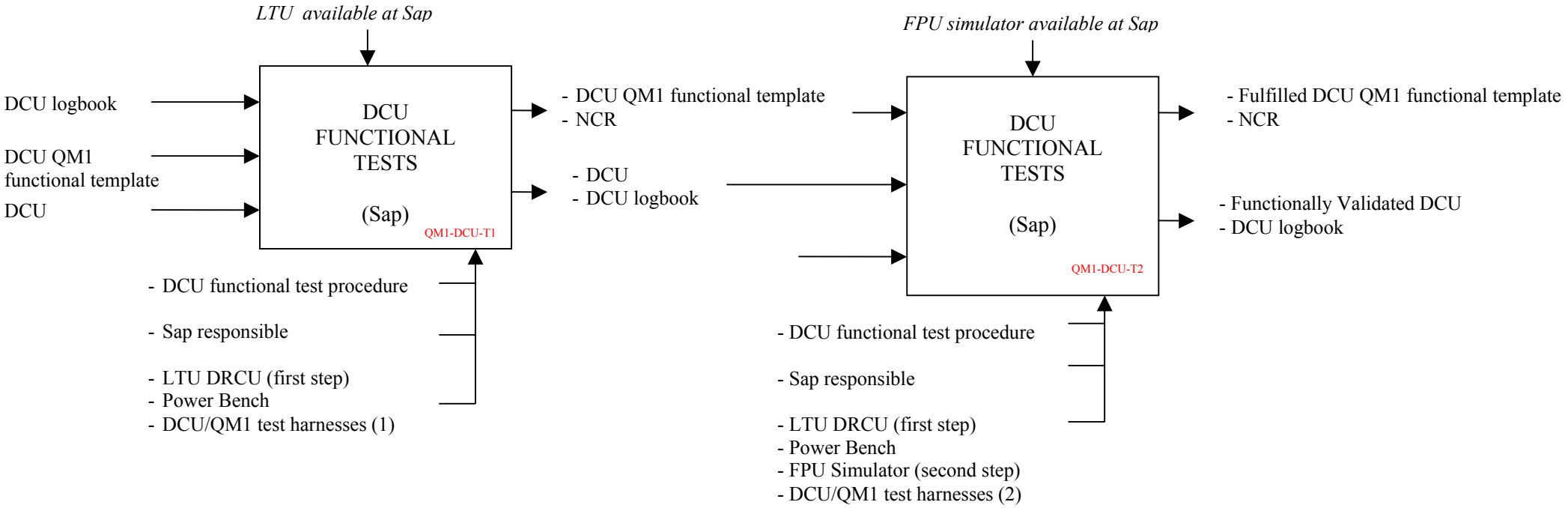


Diagram 11.2.1-3 DCU QM1 functional tests at Sap

These functional tests as well as the resources required for each test will be detailed in further AIV documents.

As the functional tests are performed and the cryostat FPU JPL tested and available in Sap, we perform simplified performance tests on DCU :

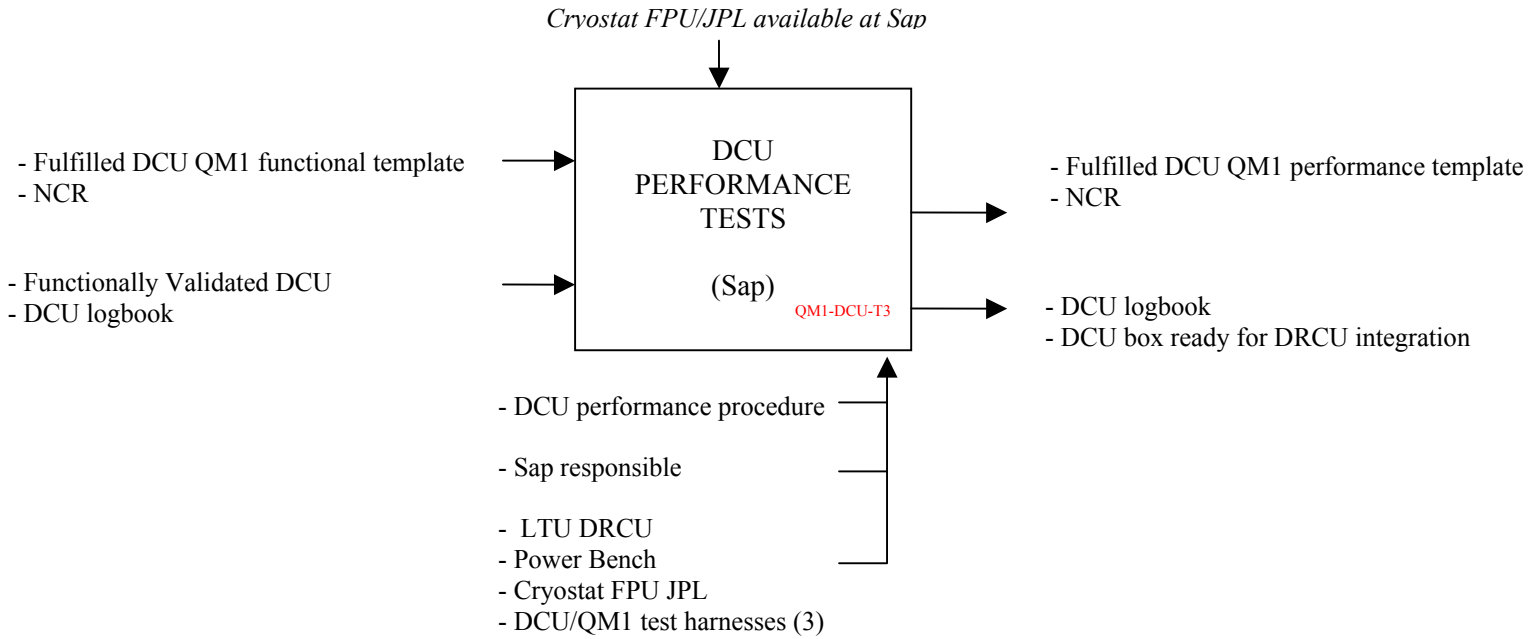


Diagram 11.2.1-4 DCU QM1 functional tests at Sap

These performance tests as well as the resources required for each test will be detailed in further AIV documents.

11.2.2 SCU QM1

The SCU is designed by SEDI under Sap's responsibility. The first paragraph below details the AIV steps performed at SEDI.

11.2.2.1 SEDI activities

Before the SCU reception in Sap, the following AIV activities are performed at DAPNIA/SEDI :

- Boards functional and performance tests,
- Boards assembly to constitute the SCU sub unit,
- SCU sub unit functional and performance tests using dedicated EGSE.

These steps are detailed in the following flow chart :

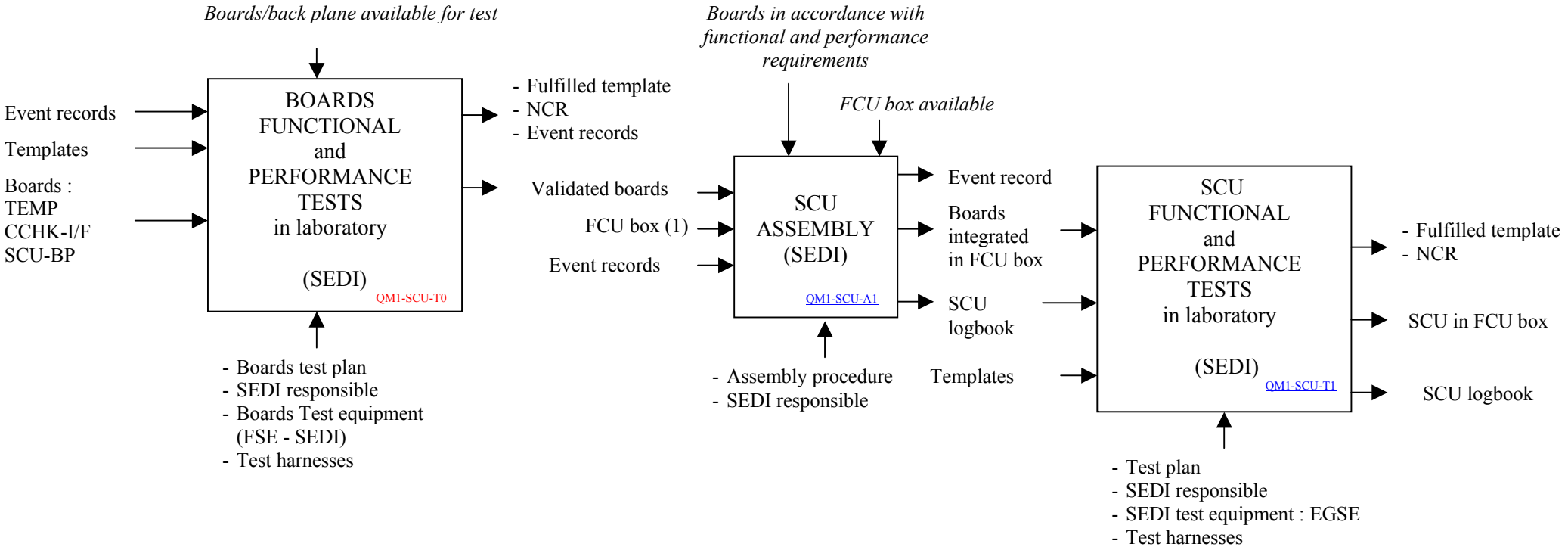


Diagram 11.2.2-1 SCU QM1 AIV activities at SEDI

11.2.2.2 Sap activities

Once received at Sap, the SCU QM1 functional tests are performed according to the following flow chart :

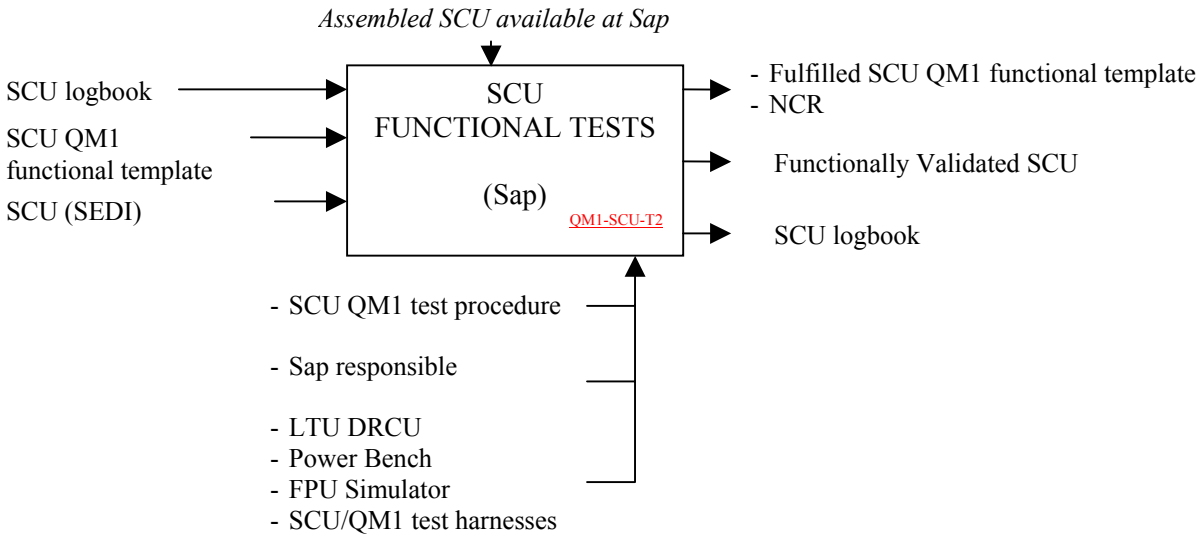


Diagram 11.2.2-2 SCU QM1 functional tests

As a matter of facts, the SCU being already validated at SEDI, these tests will validate the Sap test configuration (LTU, FPU simulator, Power Bench …). Therefore, these tests will be deduced from those performed by SEDI using the EGSE.

11.2.3 MCU QM1

Before the MCU assembly in FCU unit, the following action is performed under LAM's responsibility at Sap. The corresponding MCU flow chart is the following :

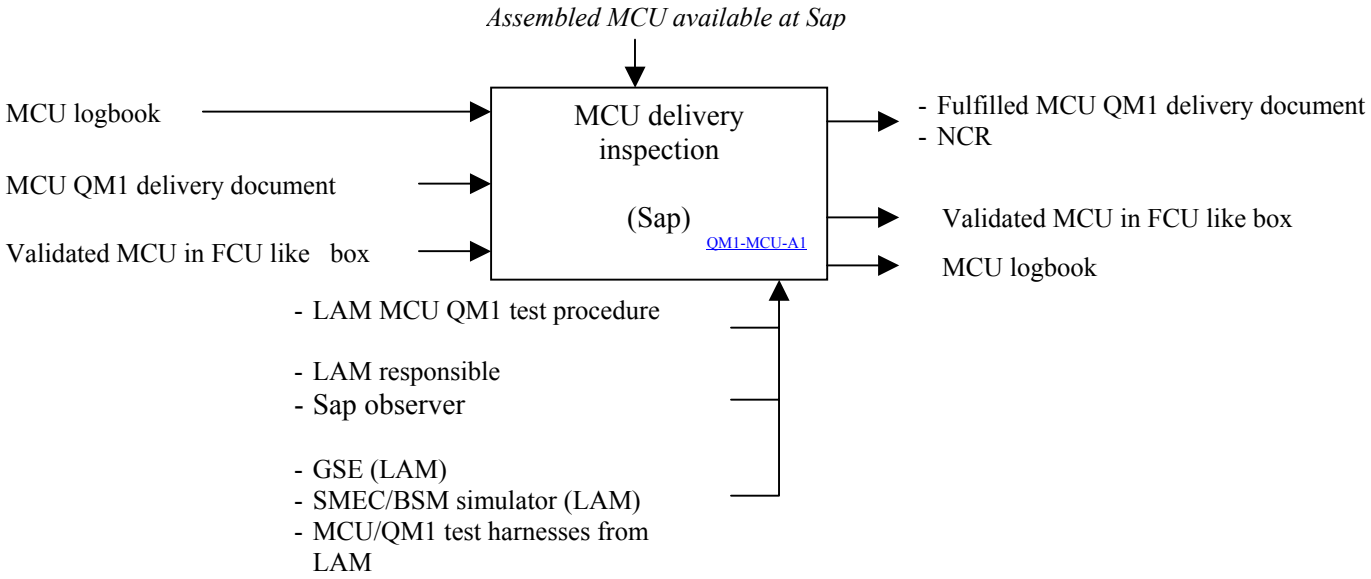


Diagram 11.2.3-1 MCU QM1 delivery inspection

As a matter of facts, the MCU being already validated at LAM, the AIV action required at Sap consists in some TBD verifications and inspections.

11.2.4 FCU QM1 assembly and test

The FCU QM1 assembly and functional tests are performed according to the following flow chart :

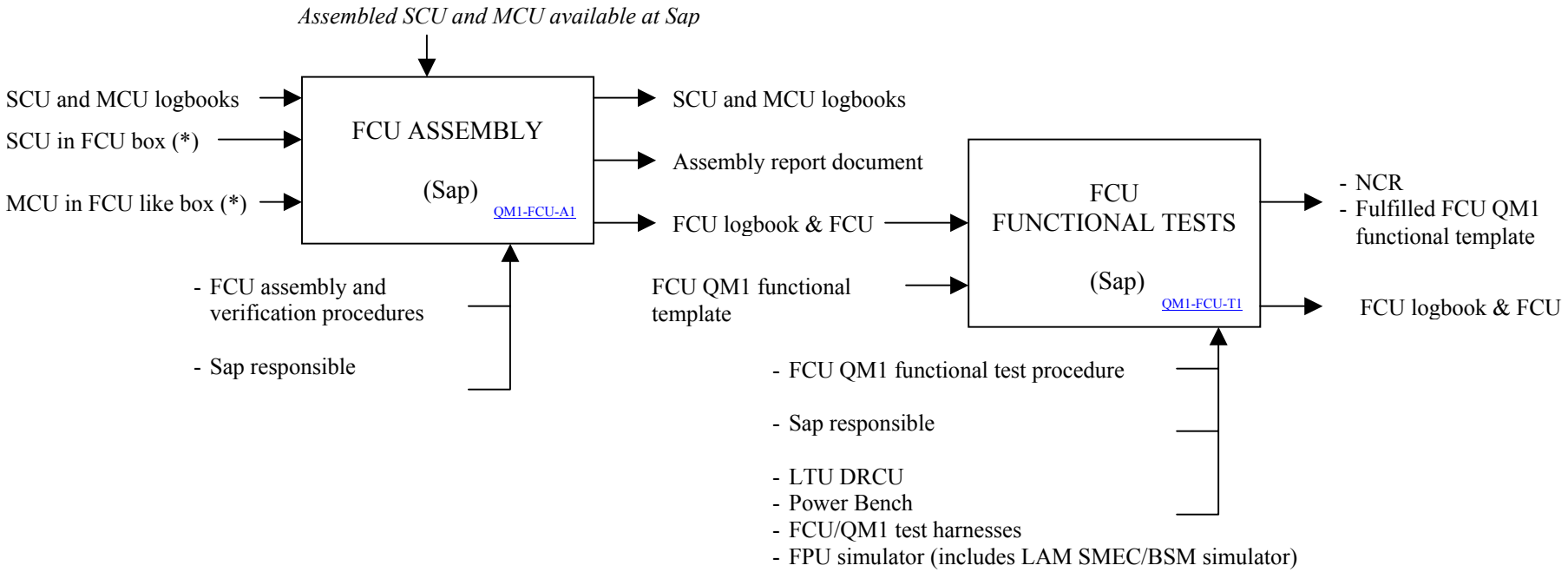


Diagram 11.2.4-1 FCU QM1 assembly and functional tests

These functional tests as well as the resources required for each test will be detailed in further AIV documents.
(*) MCU will be removed from its FCU like box to be mounted on the SCU FCU box.

11.2.5 DRCU : DCU QM1/FCU QM1 integration and test

The DRCU QM1 performance tests are performed at Sap according to following flow chart :

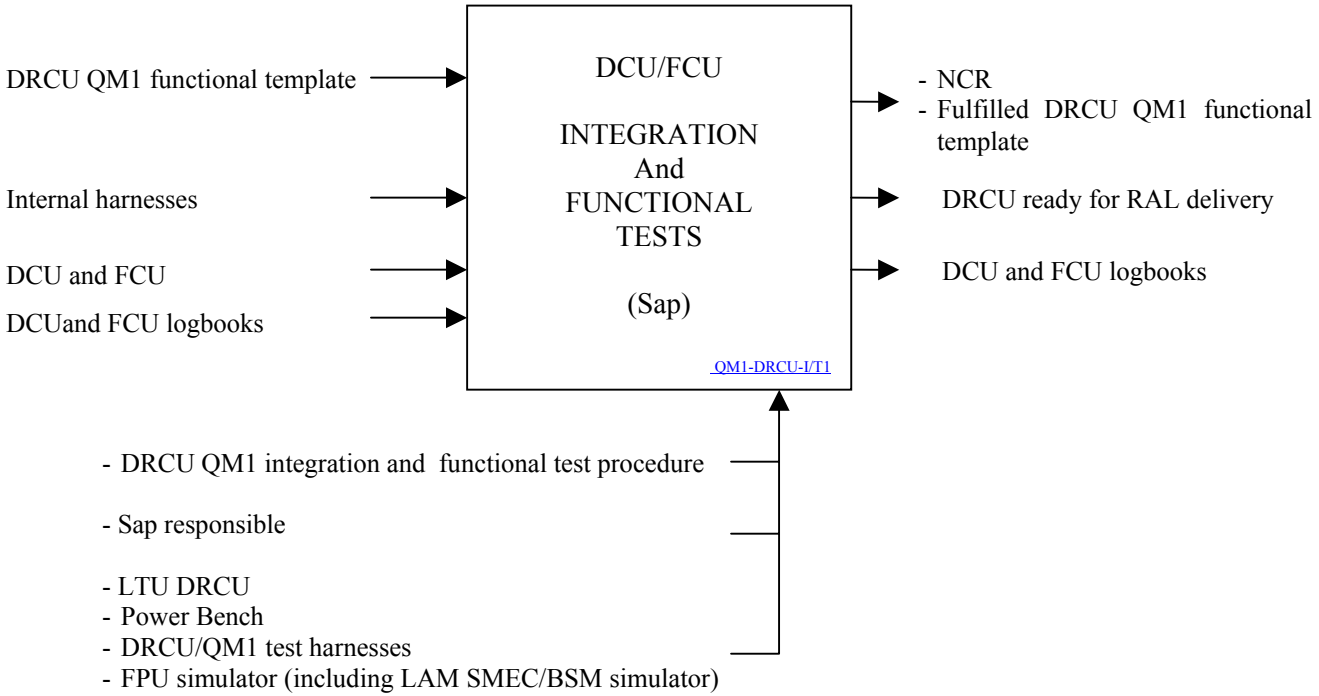


Diagram 11.2.5-1 DRCU QM1 functional tests

We here notice that the integration and functional tests steps are gathered in on action for these are processed successively, the integration being only realized to perform the functional tests.

11.2.6 DRCU : DCU/FCU QM1 packing/shipping

Once the DRCU QM1 is tested, it is packed to be delivered to RAL :

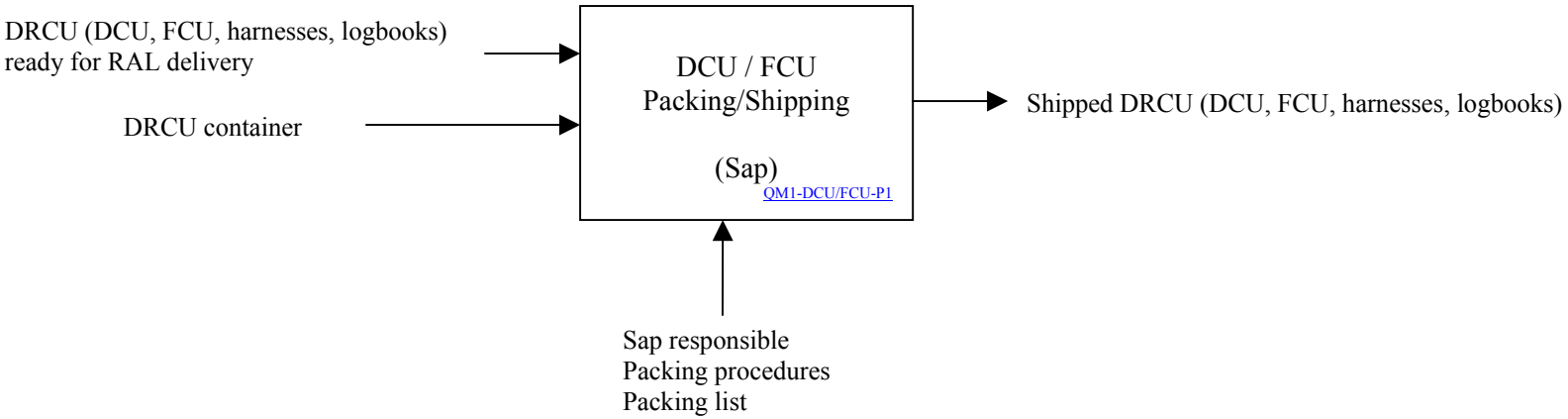


Diagram 11.2.6-1 DCU/FCU QM1 Packing/Shipping

Together with the DRCU, the QM1 Power Bench will be delivered to RAL; associated specific AIV activities will then be planned.

11.3 Representation of the AIV activities for the QM2

11.3.1 DCU QM2

Once the FSE are validated, the following AIV steps for DCU QM2 can be performed :

The DCU is pre-assembled under subcontractor's responsibility as described in the following flow chart :

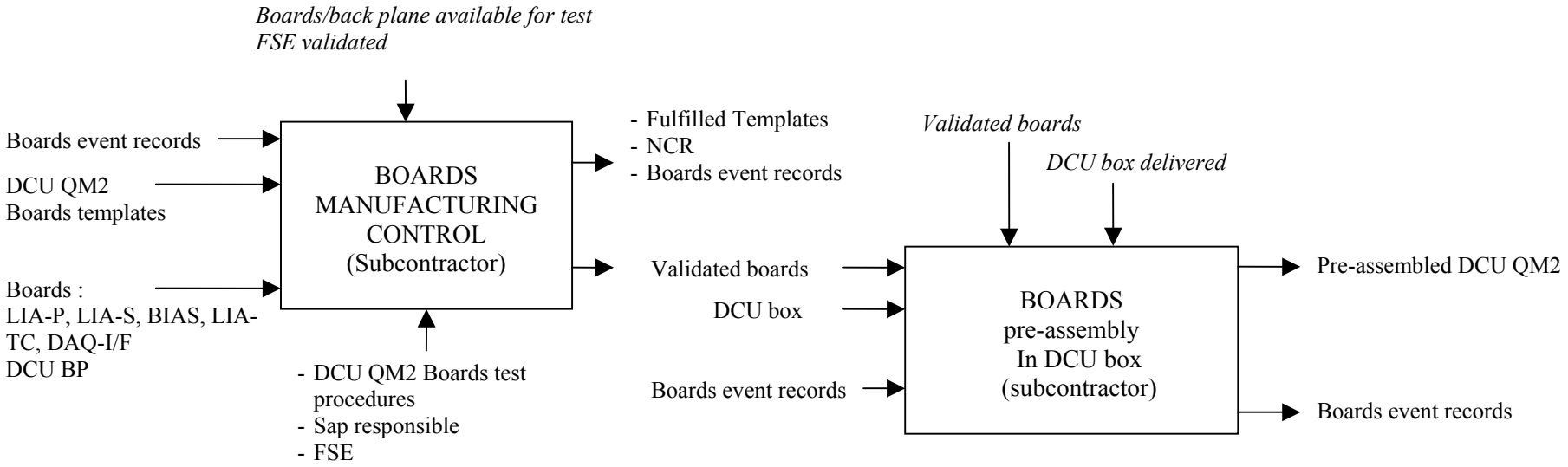


Diagram 11.3.1-1 DCU QM2 pre-assembly activities

At Sap, we receive boards pre-assembled in the DCU box. Assembly procedures will be performed in Sap after visual inspection of the pre-assembled DCU.

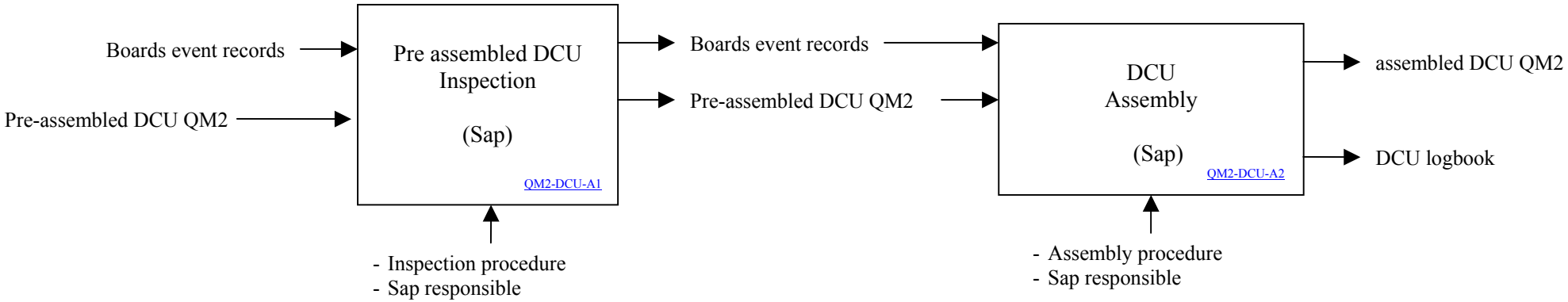


Diagram 11.3.1-2 DCU QM2 assembly activities

The functional and performance tests are then performed at Sap as described in the following flow chart :

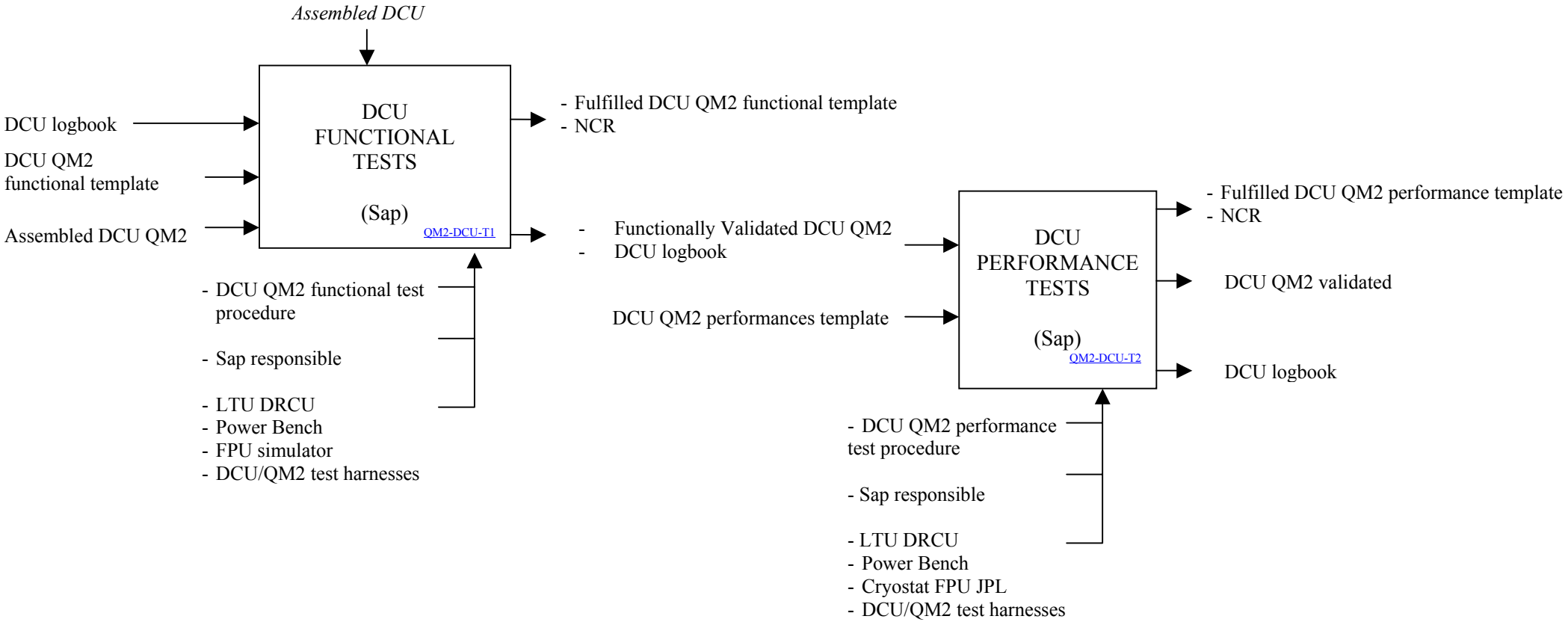
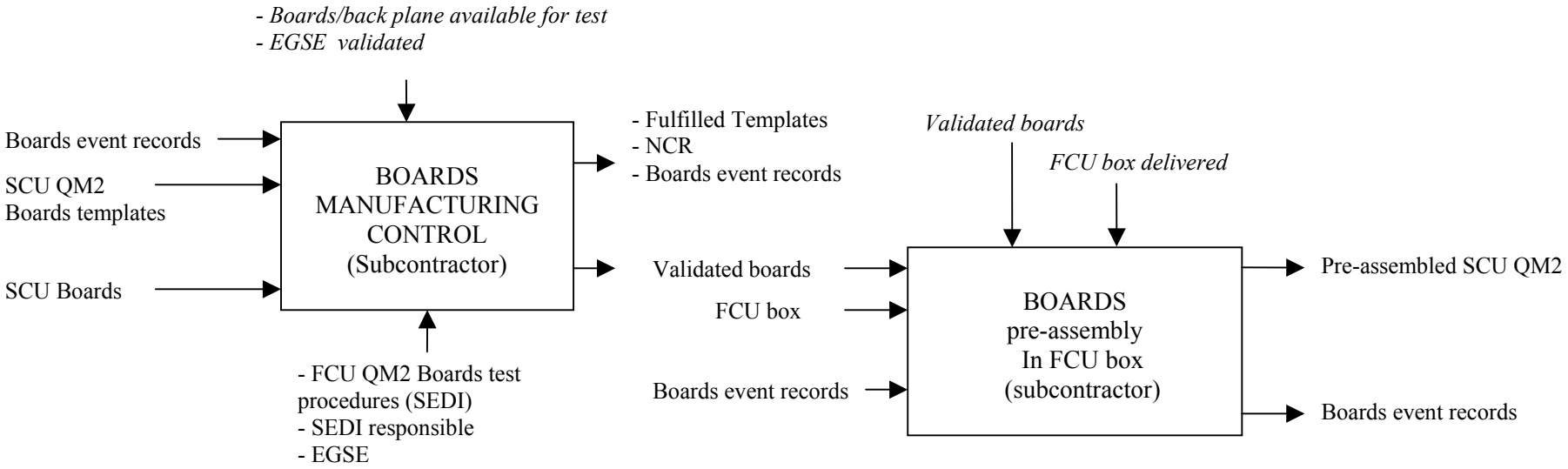


Diagram 11.3.1-3 DCU QM2 functional and performance tests

These functional and performance tests as well as the resources required for each test will be detailed in further AIV documents.

11.3.2 SCU QM2

As for the DCU, the SCU is pre-assembled under sub contractor's responsibility.



At Sap, we receive SCU boards pre-assembled in the FCU box. Assembly procedures will be performed in Sap after visual inspection of the pre-assembled SCU. When the SCU is received pre-assembled from subcontractor, the following actions are performed :

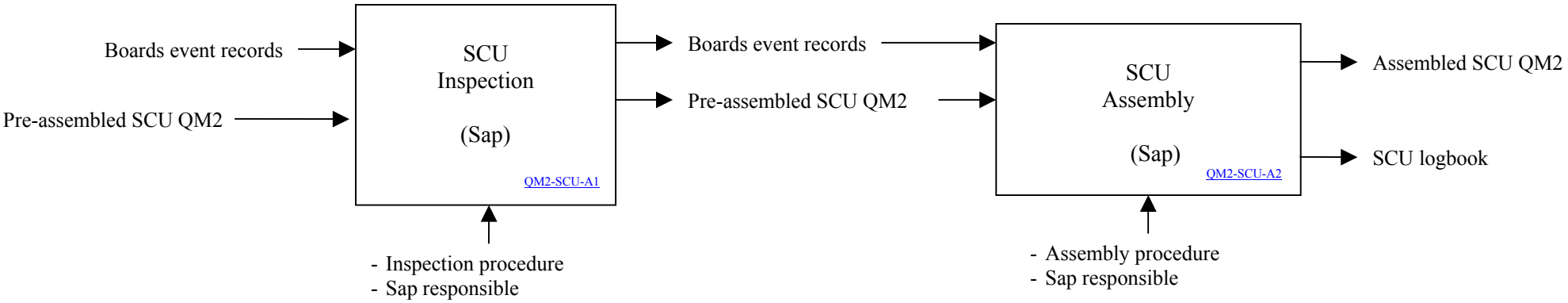


Diagram 11.3.2-1 SCU QM2 assembly

The AIV activities for SCU QM2 functional and performance tests are described in the following flow charts.

The performance tests will be performed using the SEDI dedicated EGSE :

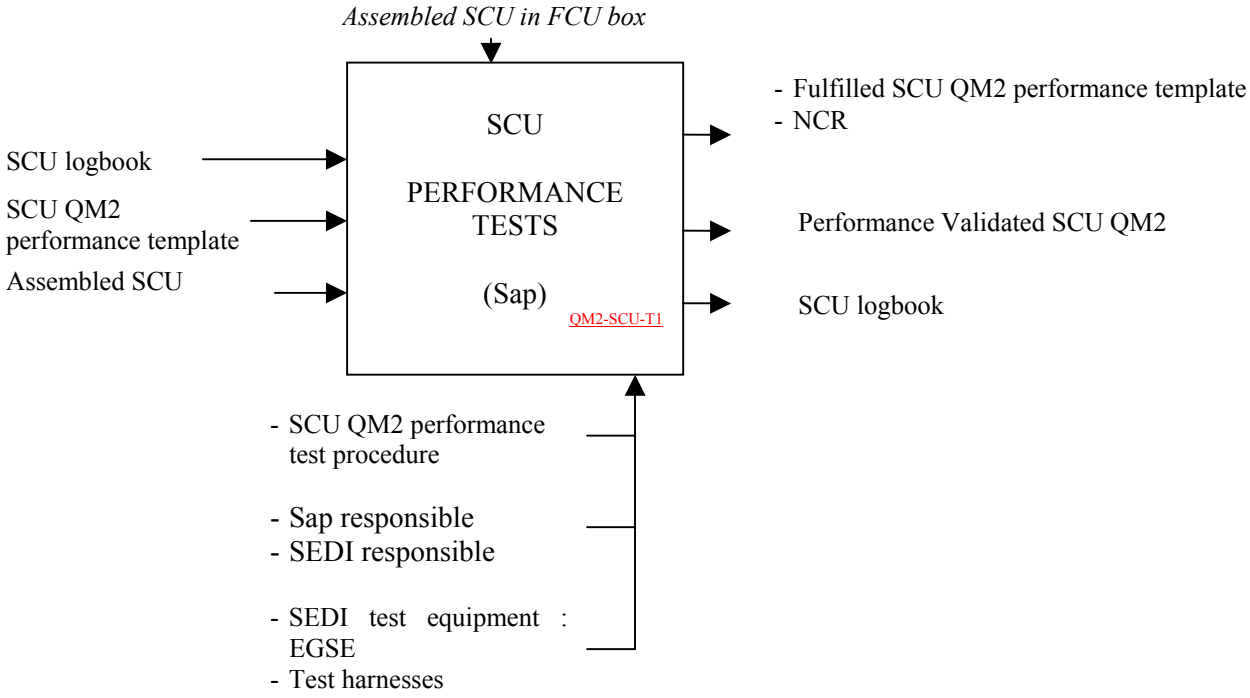


Diagram 11.3.2-2 SCU QM2 performance tests

The functional tests, derived from the tests performed will the SEDI EGSE will be performed using the LTU and FPU simulator :

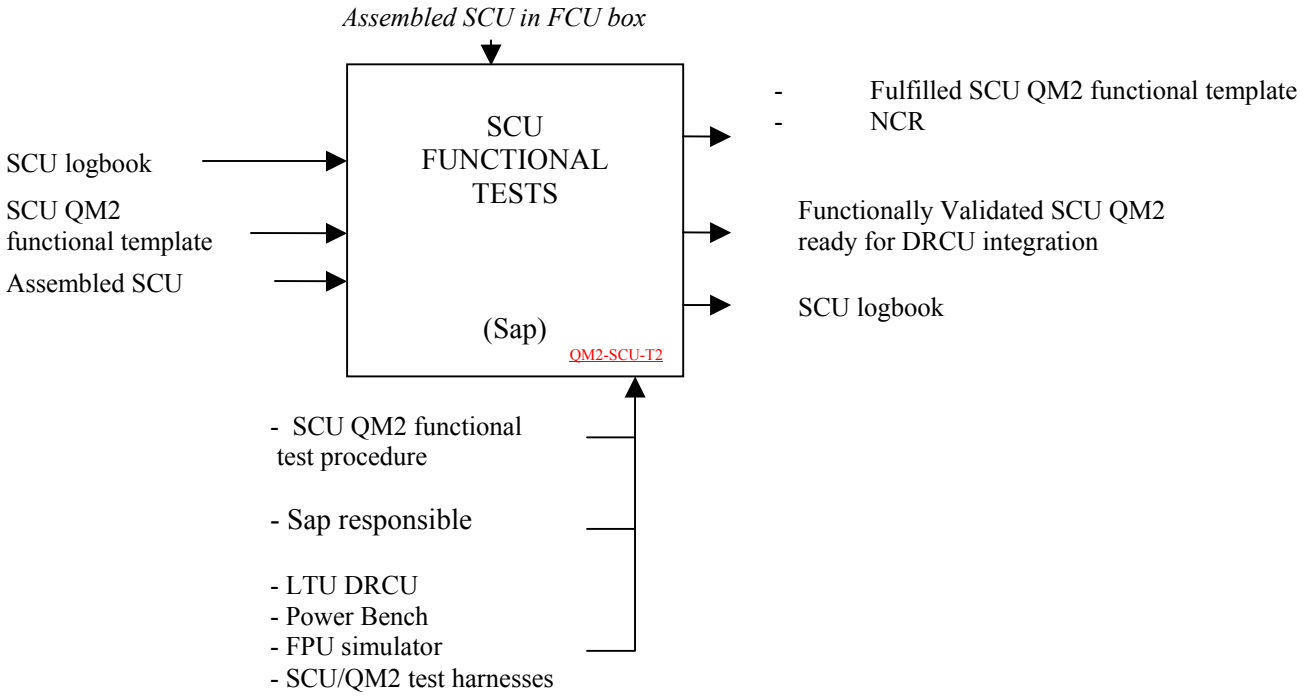


Diagram 11.3.2-3 SCU QM2 functional tests

Note : In that case, the performance tests will be restricted to noise measurements (TBC).

These functional and performance tests as well as the resources required for each test will be detailed in further AIV documents.

11.3.3 MCU QM2

Before the MCU assembly in FCU unit, the following action is performed under LAM's responsibility at Sap. The corresponding MCU flow chart is the following :

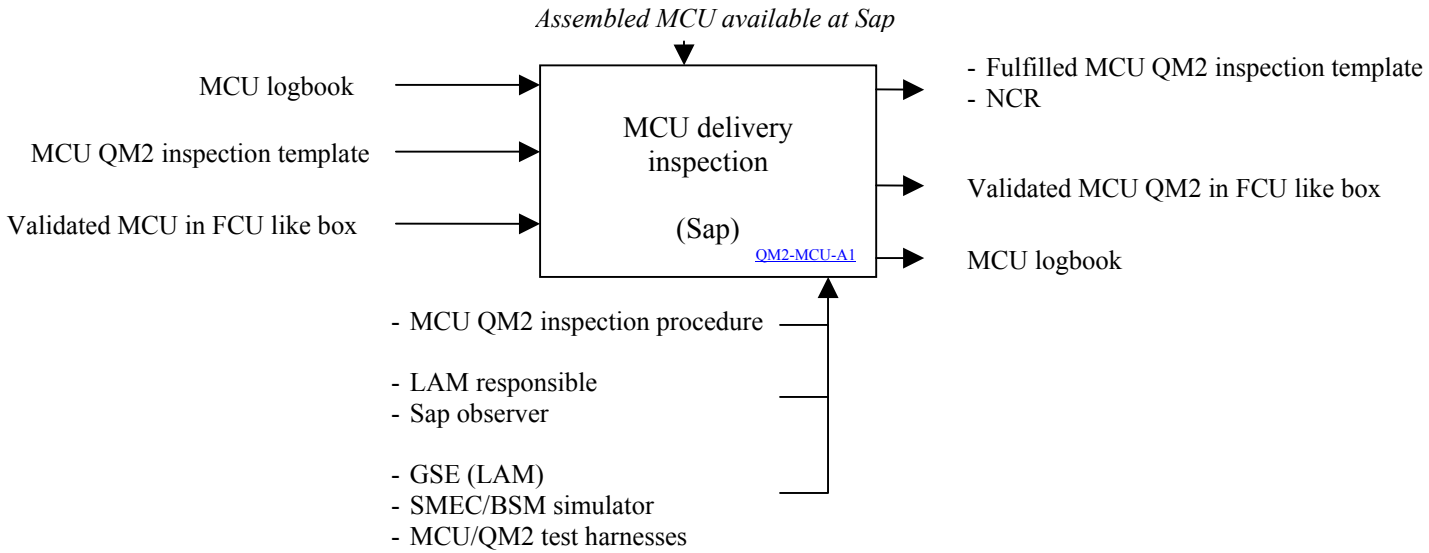


Diagram 11.3.3-1 MCU QM2 delivery inspection

As a matter of facts, the MCU being already validated at LAM, the AIV action required at Sap consists in some TBD verifications and inspections.

11.3.4 FCU QM2

The FCU QM2 assembly and functional tests are performed at Sap as described in the following flow chart :

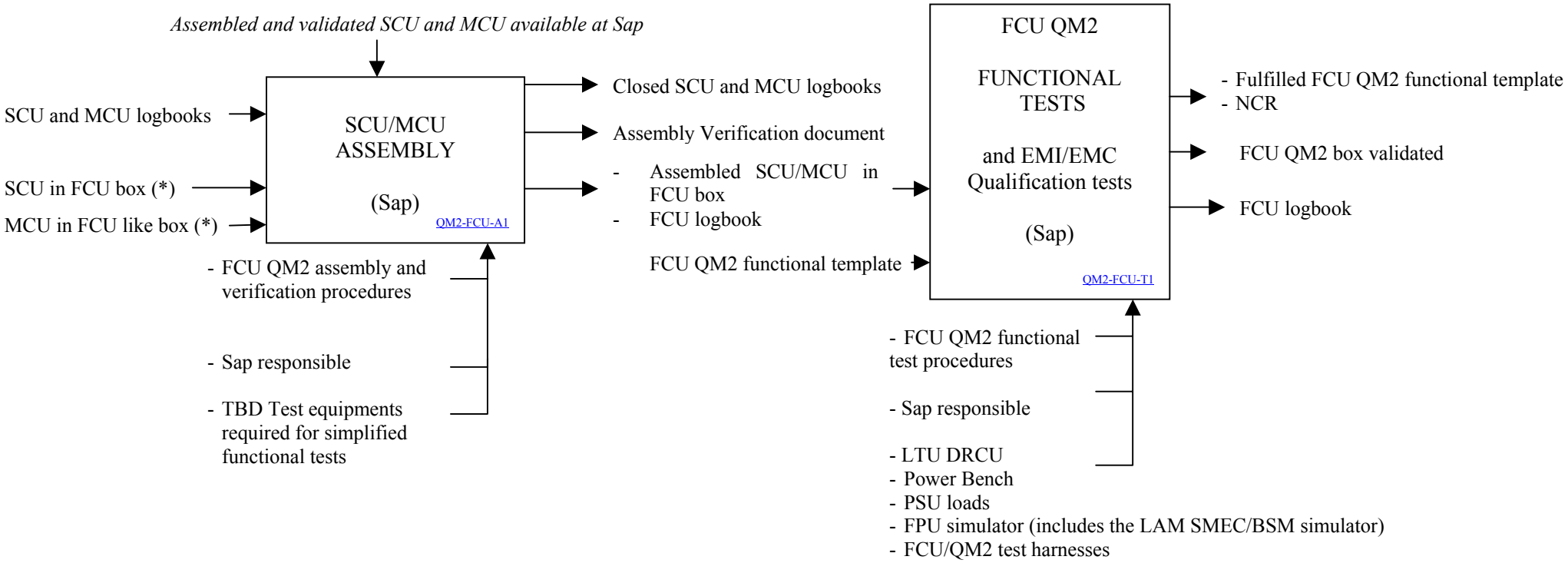


Diagram 11.3.4-1 FCU QM2 functional tests

(*) MCU will be removed from its FCU like box to be mounted on the SCU FCU box.
These functional tests as well as the resources required for each test will be detailed in further AIV documents.

11.3.5 DRCU QM2 functional tests

The DRCU QM2 is functionally tested without the PSU EM or STM as described in the following flow chart :

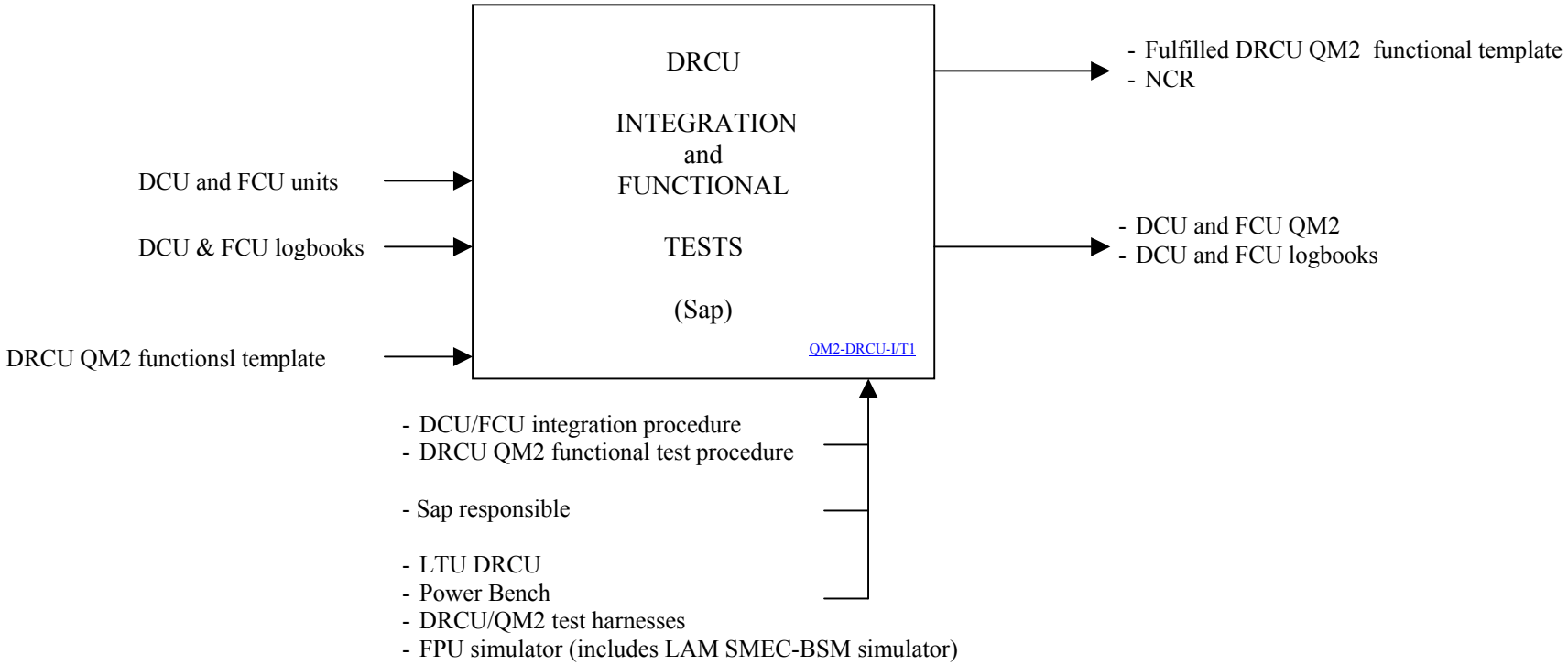


Diagram 11.3.5-1 DRCU QM2 functional tests

These performance tests as well as the resources required for each test will be detailed in further AIV documents.
After the DRCU functional tests are performed, the DCU and FCU units are separated.

11.3.6 DRCU QM2 performance tests

Before to proceed to DRCU performance tests, we assemble the PSU EM to the FCU QM2. The AIV activities for DRCU QM2 / PSU EM are then described in the following flow chart :

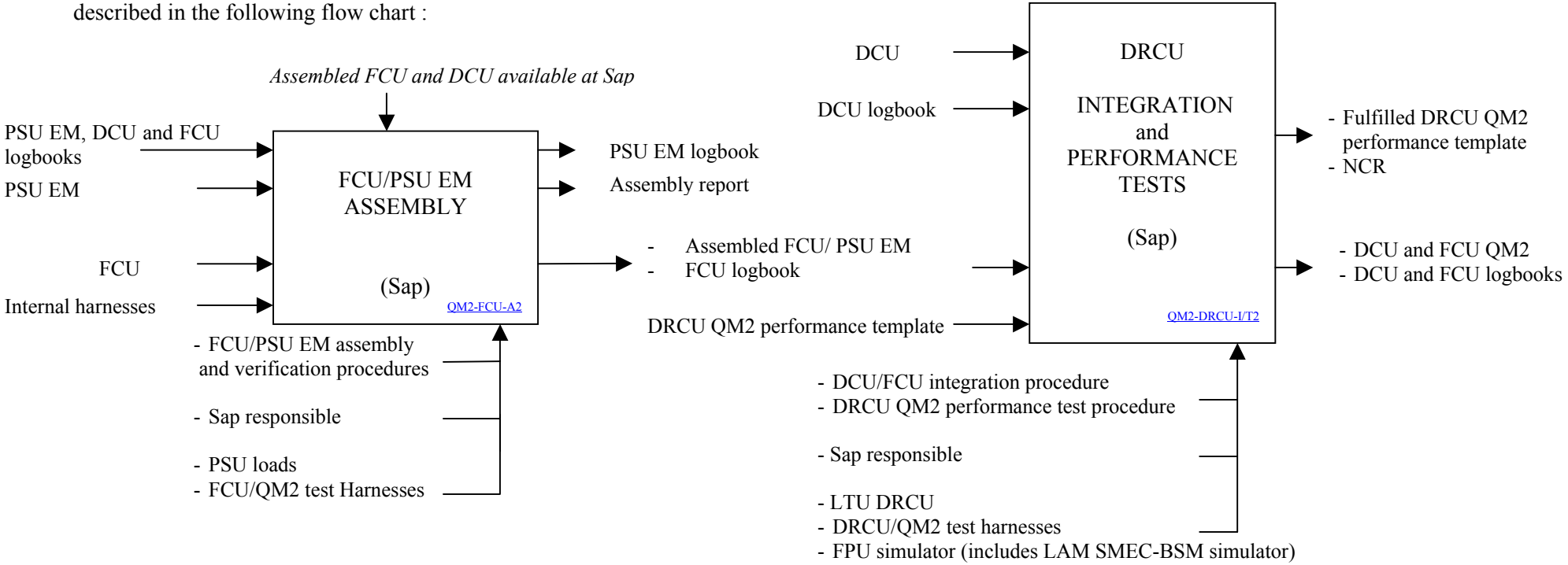


Diagram 11.3.6-1 DRCU QM2 performance tests

These performance tests as well as the resources required for each test will be detailed in further AIV documents.
After the DRCU performance tests are performed, the DCU and FCU units are separated.

11.3.7 FCU QM2 qualification tests

Before to proceed to FCU qualification tests, we assemble the PSU STM to the FCU QM2. The AIV activities for FCU QM2/PSU STM are the described in the following flow chart :

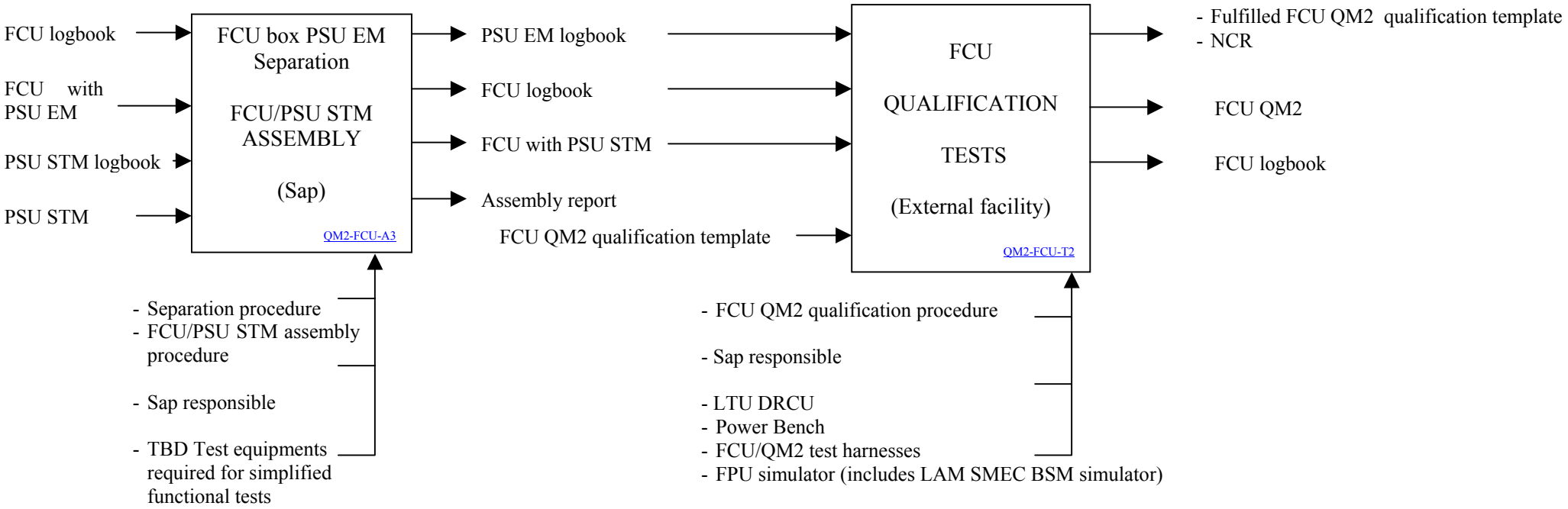


Diagram 11.3.7-1 FCU QM2 qualification tests

The qualification tests consist in environment tests performed on FCU unit. Vibration, thermal and shock tests will be realized with the FCU/PSU STM configuration. FCU EMI/EMC tests will be performed in the same configuration as the one used for FCU performance tests described in § 11.3.4 (using the PB). These qualification tests as well as the resources required for each test will be detailed in further AIV documents.

11.3.8 DCU QM2 qualification tests

The AIV qualification activities for DCU QM2 are described in the following flow chart :

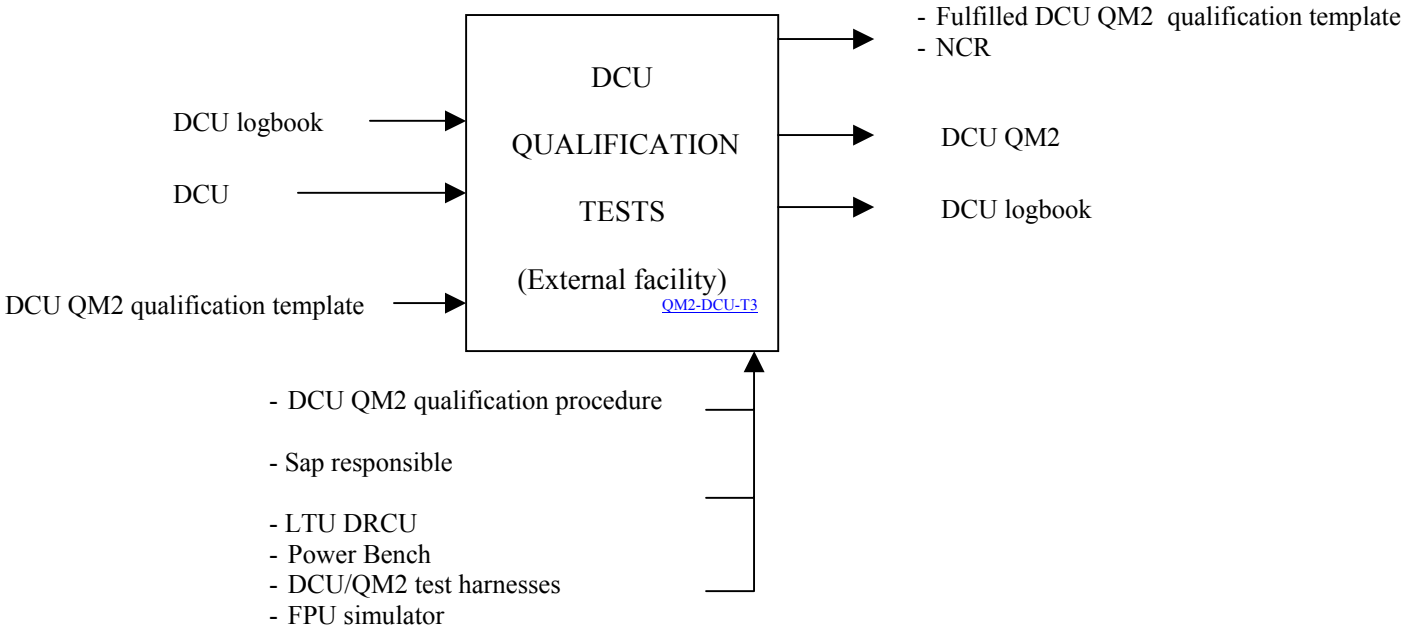


Diagram 11.3.8-1 DCU QM2 qualification tests

The qualification tests consist in environment tests performed on DCU unit. Vibration, thermal, EMI/EMC and shock tests will be realized. These qualification tests as well as the resources required for each test will be detailed in further AIV documents.

11.3.9 DCU/FCU QM2 Packing/Shipping

Once the DRCU QM2 is tested, it is packed to be delivered to RAL :

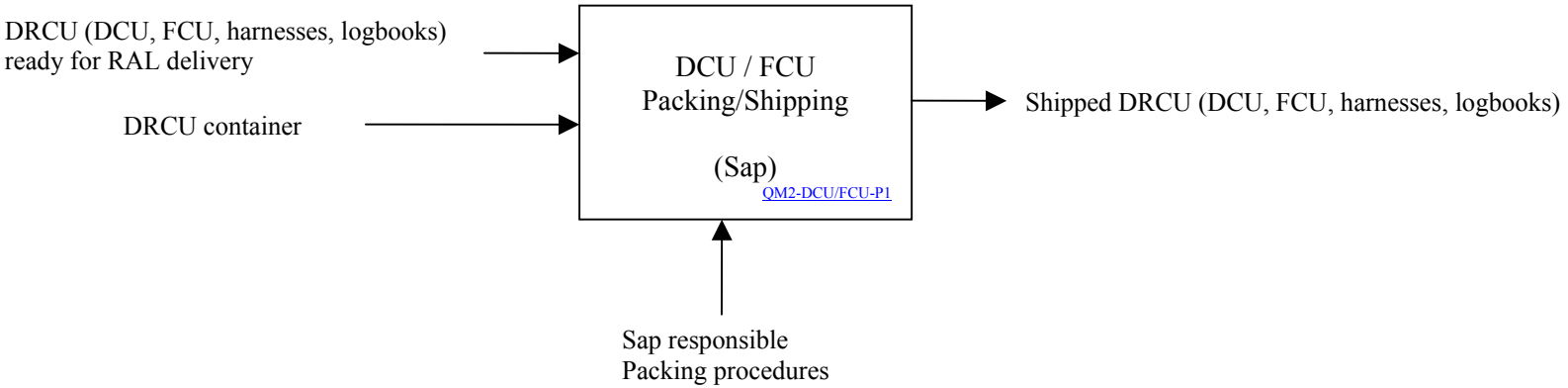


Diagram 11.3.9-1 DCU/FCU QM2 Packing/Shipping

Together with the DRCU, the QM2 Power Bench will be delivered to RAL, associated specific AIV activities will then be planned.

11.4 Representation of the AIV activities for the FM

For the Flight Model (FM), the following AIV activities are required :

11.4.1 DCU FM

Using the validated FSE designed for the QM2, the following steps will be performed to validate the DCU functions.

The DCU is pre-assembled under sub contractor's responsibility as described in the following flow chart :

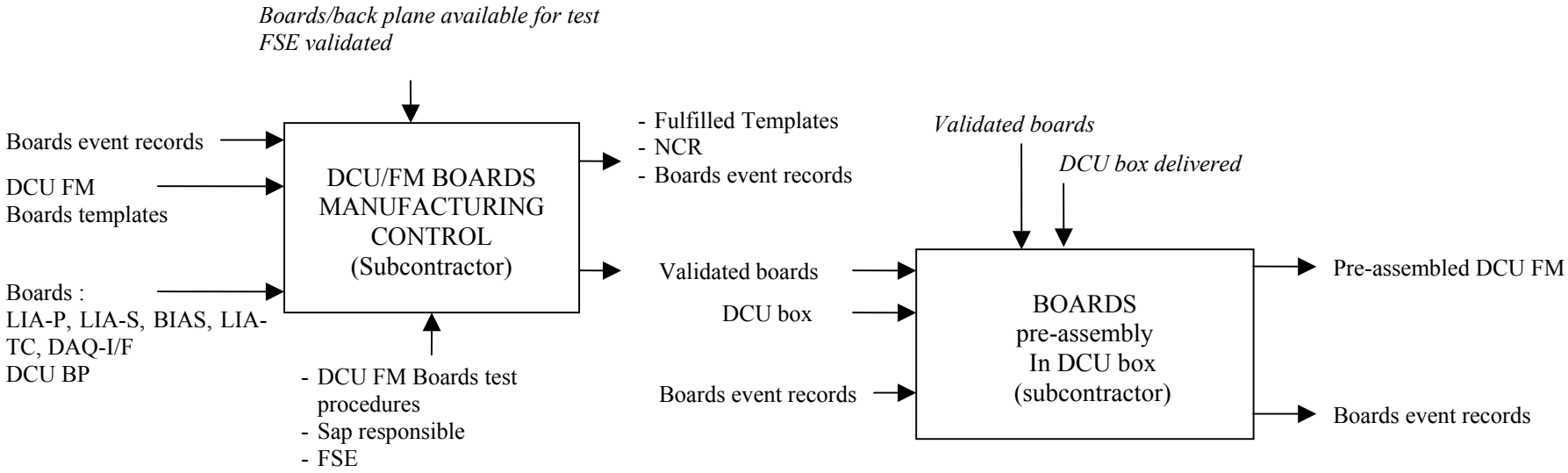


Diagram 11.4.1-1 DCU FM pre-assembly activities

At Sap, we receive boards pre-assembled in the DCU FM box. Assembly procedures will be performed in Sap after visual inspection of the pre-assembled DCU.

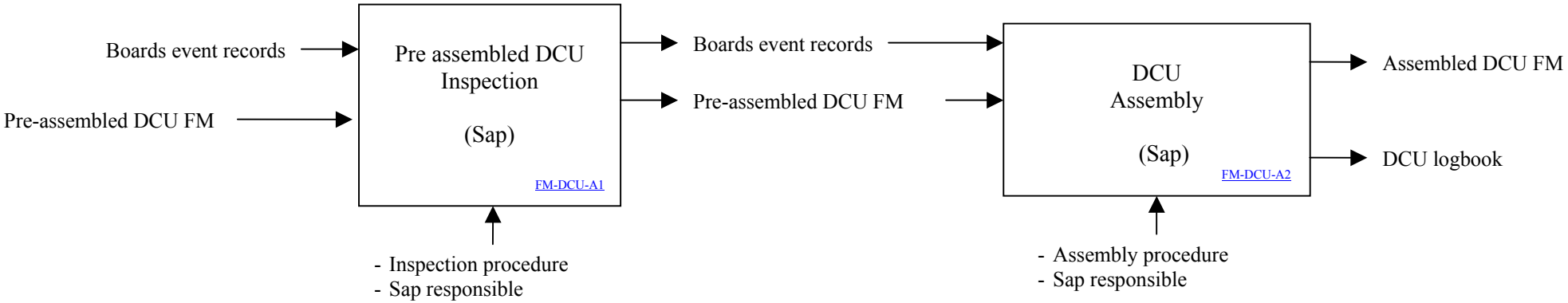


Diagram 11.4.1-2 DCU FM assembly activities

The functional and performance tests are then performed at Sap as described in the following flow chart :

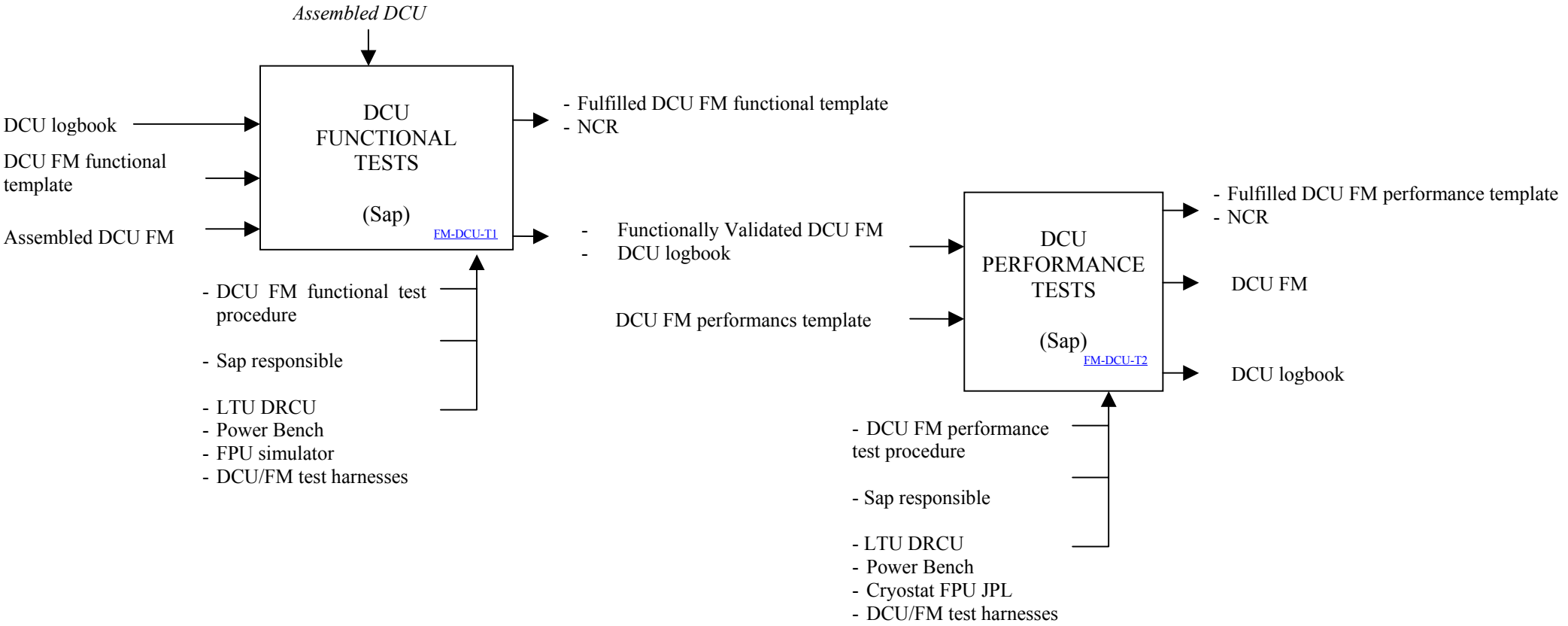


Diagram 11.4.1-3 DCU FM functional and performance tests

As for QM2, the DCU boards are validated and the DCU is pre-assembled in the DCU box by the subcontractor. Once delivered to Sap, the assembly is performed under Sap's responsibility and functional/performance tests are performed. These tests as well as the resources required for each test will be detailed in further AIV documents.

11.4.2 SCU FM

At Sap, we receive SCU boards pre-assembled by the subcontractor in the FCU box (the actions described in Diagram 11.3.1-1 can be transposed to those performed on SCU by the subcontractor). Assembly procedures will be performed in Sap after visual inspection of the pre-assembled SCU. When the SCU is received pre-assembled from subcontractor, the following actions are performed :

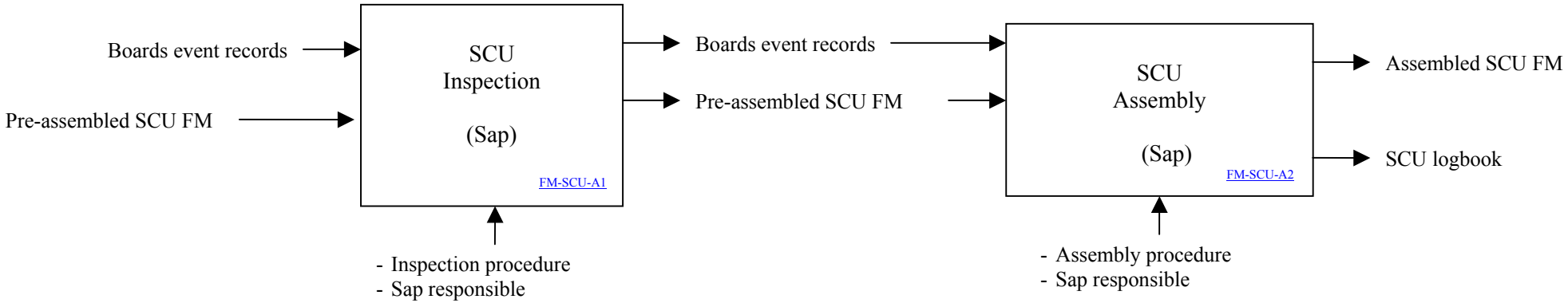


Diagram 11.4.2-1 SCU FM assembly

The AIV activities for SCU FM functional and performance tests are described in the following flow charts.

The performance tests will be performed using the SEDI dedicated EGSE :

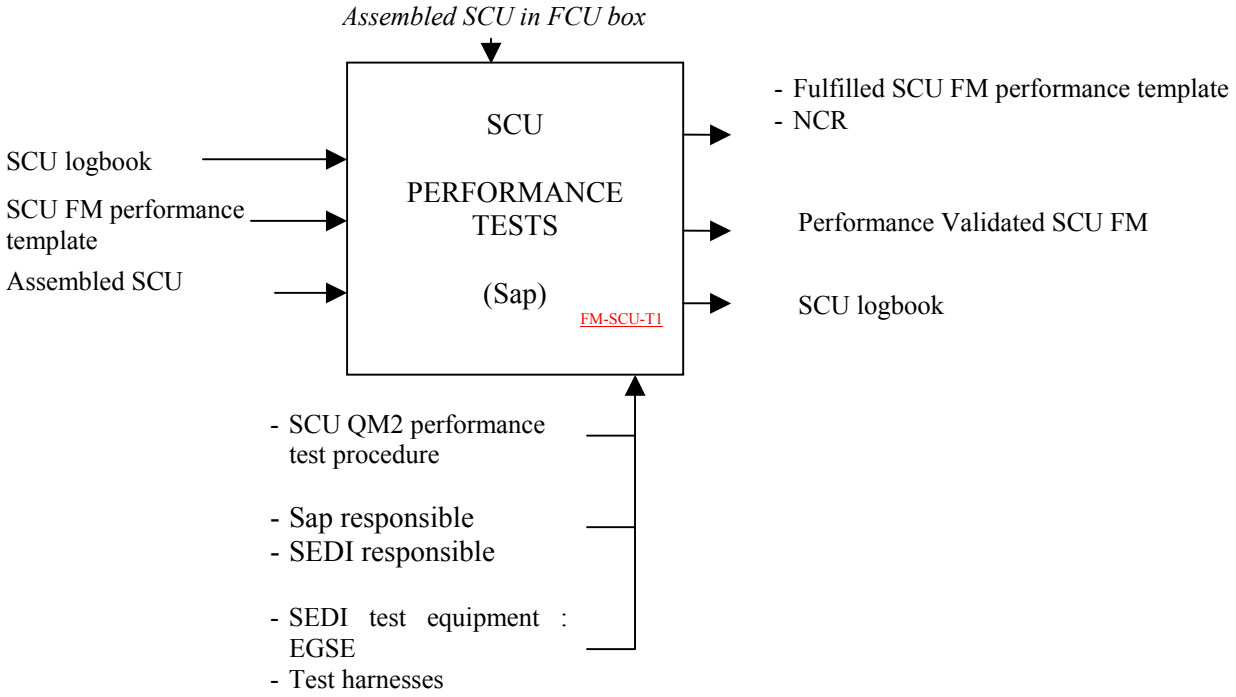


Diagram 11.4.2-2 SCU QM2 performance tests

Notes :

- *The performance tests will include noise measurements (TBC),*
- *The PB has to be designed to cope with FM requirements.*

The functional tests, derived from the tests performed will the SEDI EGSE will be performed using the LTU and FPU simulator :

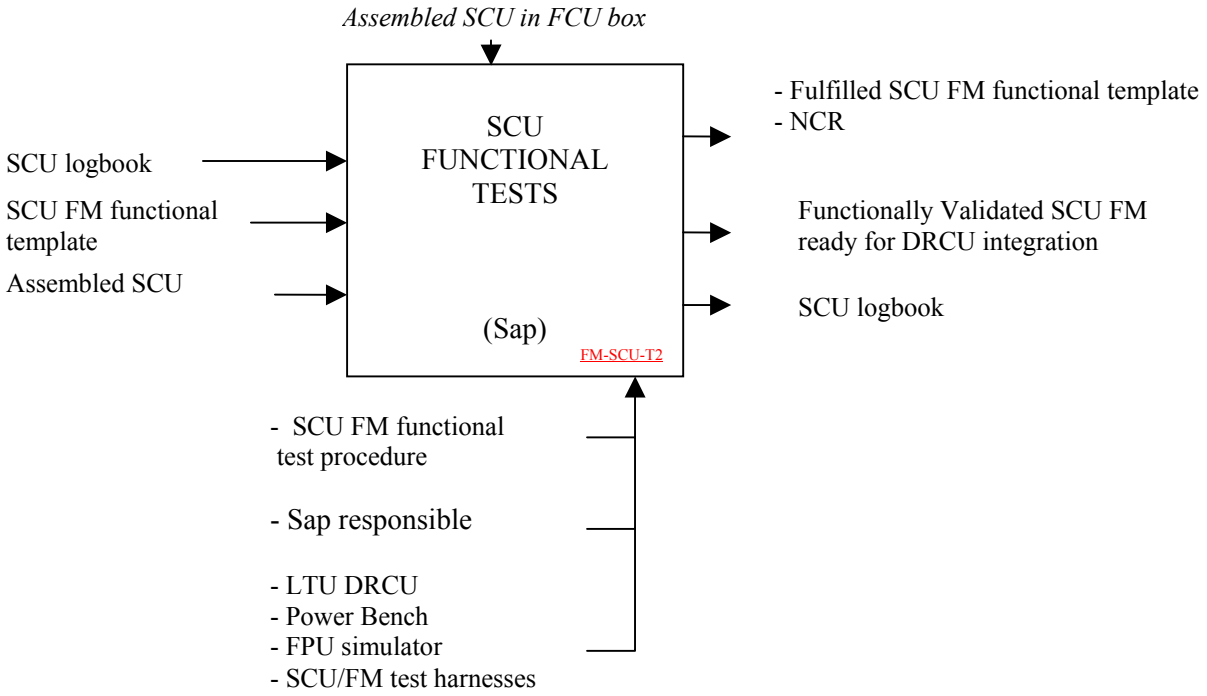


Diagram 11.4.2-3 SCU QM2 functional tests

Note : In that case, the performance tests will be restricted to noise measurements (TBC).

These functional and performance tests as well as the resources required for each test will be detailed in further AIV documents.

11.4.3 MCU FM

Before the MCU assembly in FCU unit, the following action is performed under LAM's responsibility at Sap. The corresponding MCU flow chart is the following :

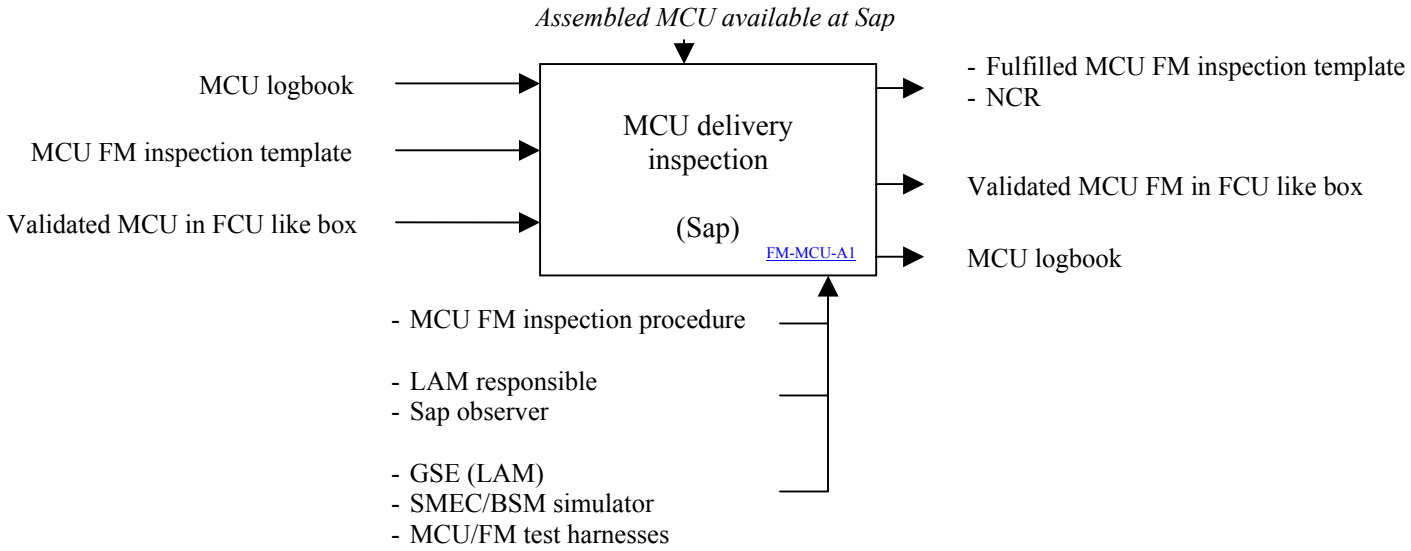


Diagram 11.4.3-1 MCU FM delivery inspection

As a matter of facts, the MCU being already validated at LAM, the AIV action required at Sap consists in some TBD verifications and inspections. The principle of these AIV activities for MCU FM are the same as those described for QM2.

11.4.4 FCU FM

The AIV activities for FCU FM consist in FCU assembly and functional tests. These are described in the following flow chart :

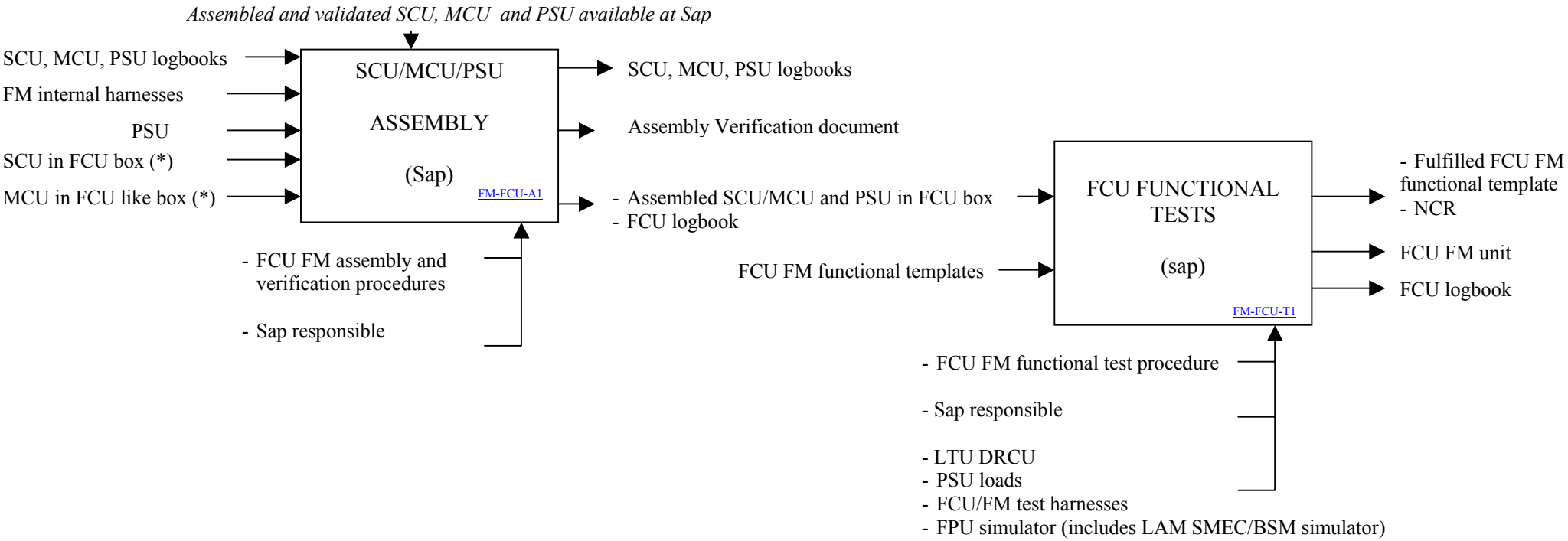


Diagram 11.4.4-1 FCU FM functional tests

(*) MCU will be removed from its FCU like box to be mounted on the SCU FCU box.
These functional tests as well as the resources required for each test will be detailed in further AIV documents.

11.4.5 DRCU FM

The DRCU FM functional and performance tests are performed at Sap as described in the following flow chart :

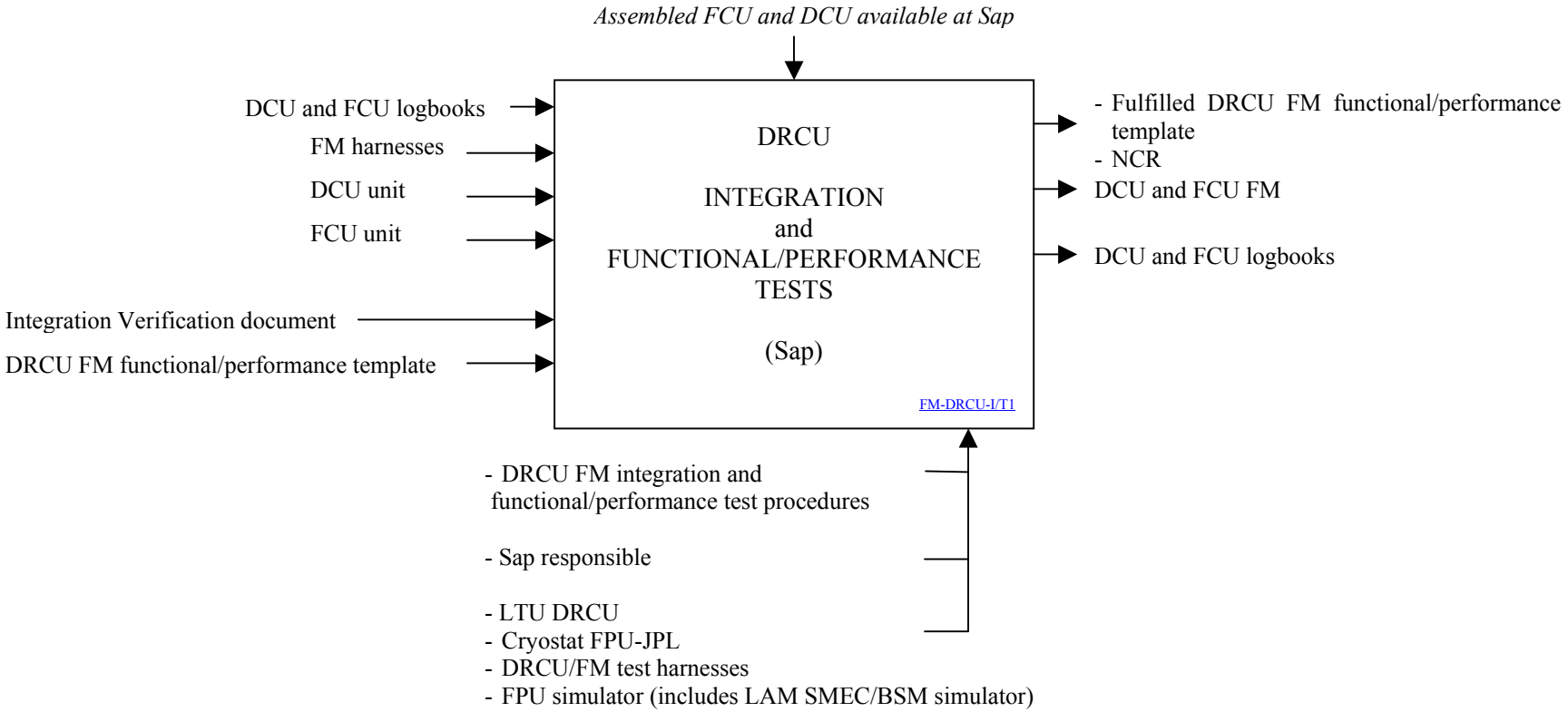


Diagram 11.4.5-1 DRCU FM functional/performance tests

These functional/performance tests as well as the resources required for each test will be detailed in further AIV documents. After the DRCU performance tests are performed, the DCU and FCU units are separated.

11.4.6 DCU FM acceptance tests

The AIV flow chart for DCU FM acceptance tests is given below :

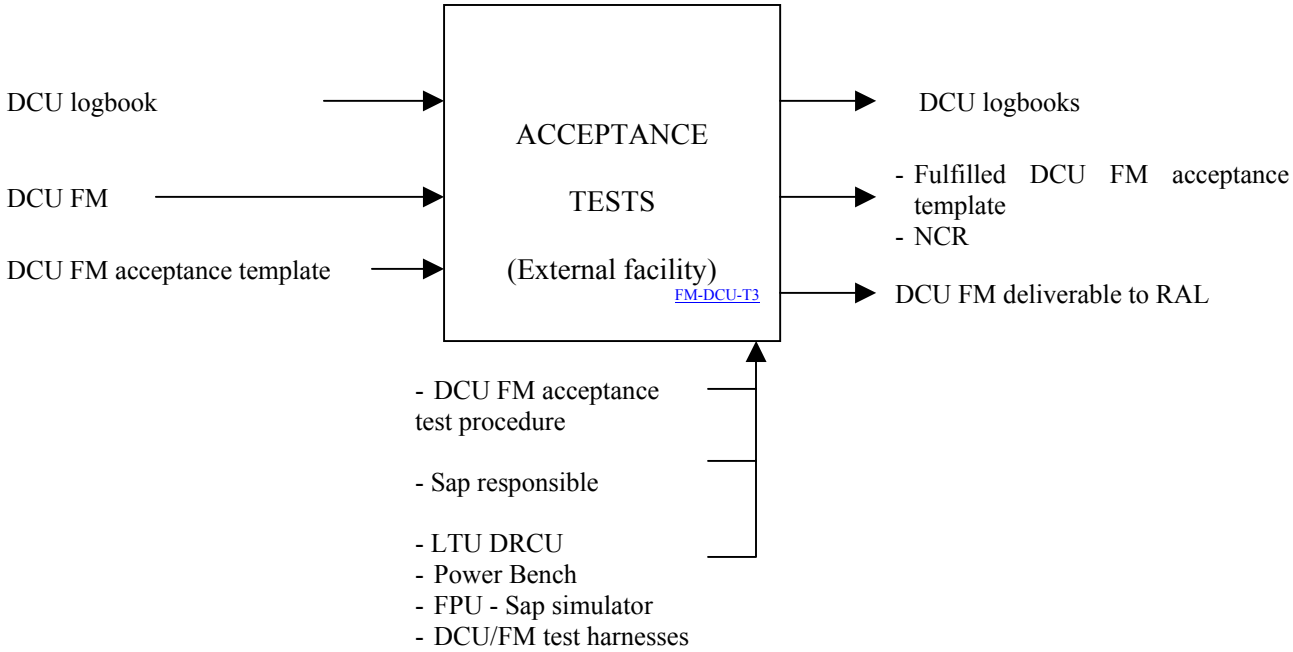


Diagram 11.4.6-1 DCU FM acceptance tests

These acceptance tests as well as the resources required for each test will be detailed in further AIV documents.

11.4.7 FCU FM acceptance tests

The AIV flow chart for FCU FM acceptance tests is given below :

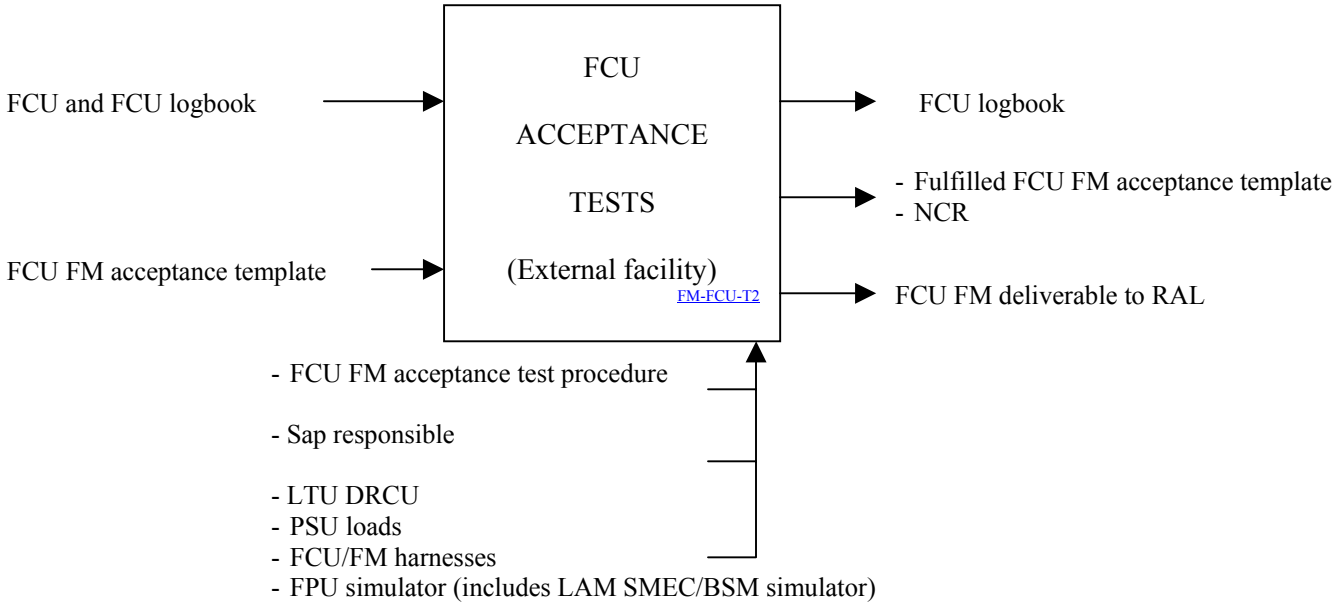


Diagram 11.4.7-1 FCU FM acceptance tests

These acceptance tests as well as the resources required for each test will be detailed in further AIV documents.

11.4.8 DCU / FCU FM packing/shipping

Once the DRCU FM is tested, it is packed to be delivered to RAL :

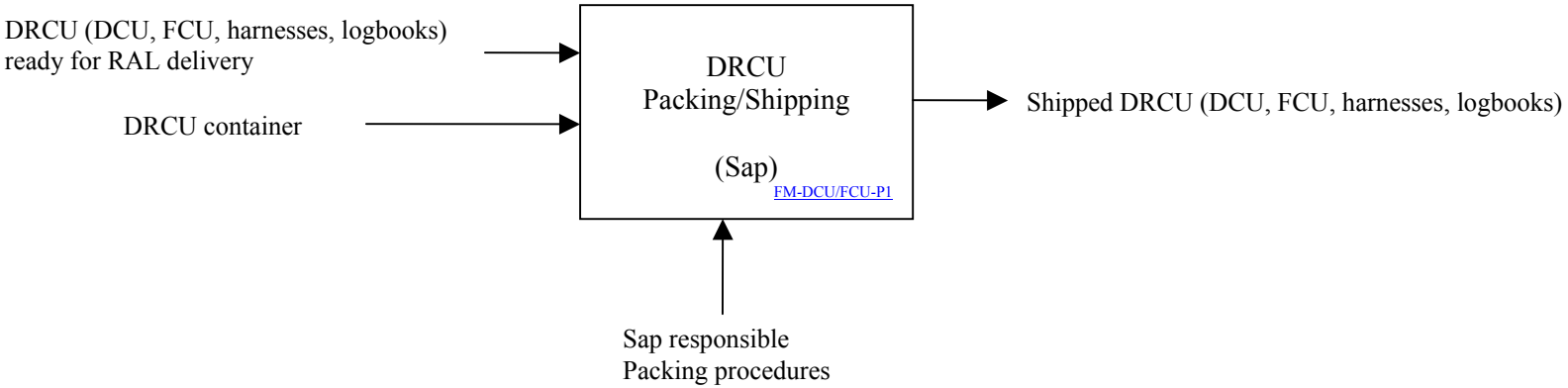


Diagram 11.4.8-1 DCU/FCU FM Packing/Shipping

12 PSU activities

12.1 AIV activities for the various PSU models

The PSU EM, PSU STM and PSU FM are designed by subcontractor under Sap's responsibility. They undergo individual unitary tests. They will be delivered to SAp by the manufacturer.

After the delivery, Sap will perform the following sequence before the assembly with FCU :

1. Incoming inspection:
   - Visual inspection of the boxes to verify:
   - Identification of the box and the connectors
   - Integrity and surface treatment status after transportation
   - Verification of the delivered documentation

2. Incoming tests.
   A functional test shall be executed to verify the functionality of the PSU after delivery

The thereafter diagrams represent the AIV activities concerning the various PSU models :

12.2 Flow chart of the AIV activities for the various PSU models

The activities performed by the subcontractor are not detailed in this document.

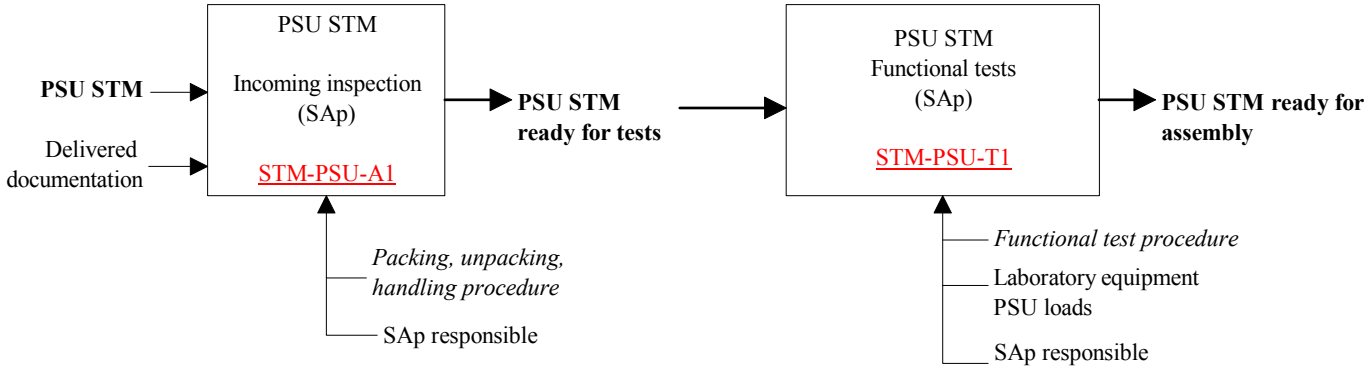


Diagram 12.2-1 - PSU STM activities

The STM functional tests are simple electrical verifications of resistor values.

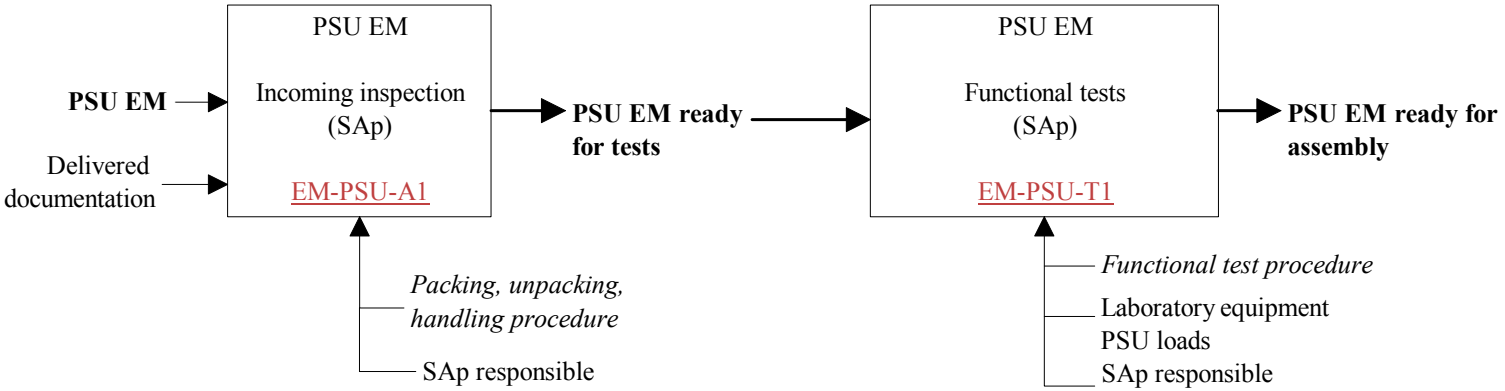


Diagram 12.2-2 - PSU EM activities

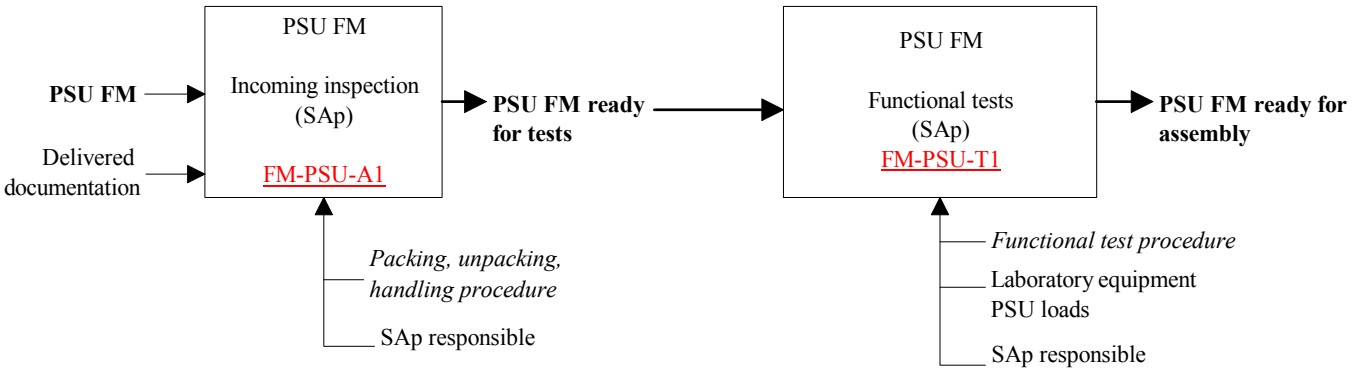


Diagram 12.2-3 - PSU FM activitie

13 Power supply environment test configurations

The Power Bench is designed under Sap's responsibility. It undergoes individual unitary tests. Reception tests will then be planned by the AIV group for the FM Power Bench.

The FCU power supply environment test configurations are summarized in the following table:

	FCU QM1	FCU QM2	FCU FM
Functional tests	Power bench	Power bench	PSU FM PSU loads
Vibrations tests	-	Power Bench / PSU STM	PSU FM PSU loads
Thermal tests	-	Power Bench / PSU STM	PSU FM PSU loads
EMI / EMC tests	-	Power Bench	PSU FM PSU loads
Physical properties	-	-	PSU FM

Table 13-1 FCU power supply test configurations

We here recall that, during environment (vibration and thermal vacuum) tests of the STM and FCU QM2, the PSU STM will be mounted under FCU box. FCU QM2 EMI/EMC tests will be performed without the PSU STM. For these tests, we will not use the PSU EM but the power bench.

The DCU power supply environment test configurations is always the Power Bench as indicated in the following table:

	DCU QM1	DCU QM2	DCU FM
Functional / Performance tests	Power bench	Power Bench	Power bench
Vibrations tests	-	Power Bench	Power bench
Thermal tests	-	Power Bench	Power bench
EMI / EMC tests	-	Power Bench	Power bench
Physical properties	-	-	Power bench

Table 13-2 DCU power supply test configurations

The DRCU power supply environment test configurations are summarized in the following table:

	DRCU QM1	DRCU QM2	DRCU FM
Functional tests	Power bench	Power Bench	PSU FM
Performance tests	-	PSU EM	PSU FM

Table 13-3 DRCU power supply test configurations

14 Test equipment

The tests equipment consists in specifically designed facilities (LTU DRCU for example) and dedicated laboratory equipment (Electronic laboratory for example), that is the environment in which the tests are performed.

The LTU is designed to pilot the functional and performance tests performed on units (DCU, FCU) or integrated DRCU. It is then associated with the detector simulator (FFU simulator). The LTU is also used for qualification and acceptance tests id est, during environment tests (EMI/EMC, Vibration, Thermal vacuum).

The FPU will be developed by CEA/SIS. Depending on the level of achievement of the FPU, this latter may include the SMEC/BSM simulator from LAM to simulate FPU mechanisms.

The table below summarizes the test equipment required for the HERSCHEL SPIRE AIV actions under Sap's responsibility.

Action Name MODEL-ELEMENT-ACTION	**Action Type**	**Test equipment**	**Test Facilities**
QM1-DCU-A1	Assembly	TBD Test equipments required for simplified functional tests	Sap SPIRE laboratory ⇨ Mechanic ⇨ Electric
QM1-DCU-T0	Laboratory tests	- Test equipment (generator …) - DCU/EM connectors	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric
QM1-DCU-T1	Functional tests	- LTU DRCU - Power Bench - DCU/QM1 test harnesses	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric
QM1-DCU-T2	Functional tests	- LTU DRCU - Power Bench - FPU Simulator - DCU/QM1 test harnesses	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric
QM1-DCU-T3	Performance Tests	- LTU DRCU - Power Bench - Cryostat FPU JPL - DCU/QM1 test harnesses	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric
QM1-SCU-A1	Inspection		Sap SPIRE laboratory
QM1-SCU-A2	Assembly		Sap SPIRE laboratory
QM1-SCU-T1	Performance tests	- SEDI EGSE - FPU Simulator	SEDI laboratory ⇨ Electronic ⇨ Electric
QM1-SCU-T2	Functional tests	- LTU DRCU - Power Bench - FPU Simulator - SCU/QM1 test harnesses	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric
QM1-MCU-A1	Inspection and Functional tests	- GSE (LAM) - SMEC/BSM Simulator - MCU/QM1 test harnesses	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric

QM1-FCU-A1	Assembly	TBD Test equipments required for simplified functional tests	Sap SPIRE laboratory ⇨ Mechanic ⇨ Electric
QM1-FCU-T1	Functional Tests	- LTU DRCU - Power Bench - QM1 test harnesses - FPU simulator (includes LAM SMEC/BSM simulator)	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric
QM1-DRCU-I/T1	Integration and functional tests	- LTU DRCU - Power Bench - QM1 test harnesses - FPU simulator (including LAM SMEC/BSM simulator)	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric
QM2-DCU-A1	Inspection		Sap SPIRE laboratory
QM2-DCU-A2	Assembly	TBD Test equipments required for simplified functional tests	Sap SPIRE laboratory ⇨ Mechanic ⇨ Electric
QM2-DCU-T1	Functional tests	- LTU DRCU - Power Bench - FPU Simulator - DCU/QM2 test harnesses	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric
QM2-DCU-T2	Performance Tests	- LTU DRCU - Power Bench - Cryostat FPU JPL - DCU/QM2 test harnesses	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric
QM2-SCU-A1	Inspection		Sap SPIRE laboratory
QM2-SCU-A2	Assembly	TBD Test equipments required for simplified functional tests	Sap SPIRE laboratory ⇨ Mechanic ⇨ Electric
QM2-SCU-T1	Performance tests	- SEDI EGSE - FPU Simulator	SEDI laboratory ⇨ Electronic ⇨ Electric
QM2-SCU-T2	Functional tests	- LTU DRCU - Power Bench - FPU Simulator - SCU/QM2 test harnesses	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric
QM2-MCU-A1	Inspection and Functional tests	- GSE (LAM) - SMEC/BSM Simulator - MCU/QM2 test harnesses	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric
QM2-FCU-A1	Assembly	TBD Test equipments required for simplified functional tests	Sap SPIRE laboratory ⇨ Mechanic ⇨ Electric
QM2-FCU-T1	Functional tests and EMI/EMC Qualification	- LTU DRCU - Power Bench - PSU loads - FCU/QM2 test harnesses - FPU simulator (including LAM SMEC/BSM simulator)	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric Intespace (or equivalent) facilities ⇨ EMI/EMC
QM2-DRCU-I/T1	Integration and Functional tests	- LTU DRCU - Power Bench - FCU/QM2 test harnesses	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric

		- FPU simulator (including LAM SMEC/BSM simulator)	
QM2-FCU-A2	Assembly	- PSU loads - FCU/QM2 test Harnesses	Sap SPIRE laboratory ⇨ Mechanic ⇨ Electric
QM2-DRCU-I/T2	Integration and performance tests	- LTU DRCU - DRCU/QM2 test harnesses - FPU simulator (including LAM SMEC/BSM simulator)	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric
QM2-FCU-A3	Assembly	TBD Test equipments required for simplified functional tests	Sap SPIRE laboratory ⇨ Mechanic ⇨ Electric
QM2-FCU-T2	Qualification tests	- LTU DRCU - Power Bench - FCU/QM2 test harnesses - FPU simulator (including LAM SMEC/BSM simulator)	Intespace (or equivalent) facilities ⇨ Vibration ⇨ Thermal vacuum ⇨ Shock
QM2-DCU-T3	Qualification tests	- LTU DRCU - Power Bench - DCU/QM2 test harnesses - FPU simulator (including LAM SMEC/BSM simulator)	Intespace (or equivalent) facilities ⇨ Vibration ⇨ Thermal vacuum ⇨ Shock ⇨ EMI/EMC
FM-DCU-A1	Inspection		Sap SPIRE laboratory ⇨ Mechanic ⇨ Electric
FM-DCU-A2	Assembly	TBD Test equipments required for simplified functional tests	Sap SPIRE laboratory
FM-DCU-T1	Functional tests	- LTU DRCU - Power Bench - FPU Simulator - DCU/FM test harnesses	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric
FM-DCU-T2	Performance Tests	- LTU DRCU - Power Bench - Cryostat FPU JPL - DCU/FM test harnesses	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric
FM-SCU-A1	Inspection		Sap SPIRE laboratory
FM-SCU-A2	Assembly	TBD Test equipments required for simplified functional tests	Sap SPIRE laboratory ⇨ Mechanic ⇨ Electric
FM-SCU-T1	Performance tests	- SEDI EGSE - FPU Simulator	SEDI laboratory ⇨ Electronic ⇨ Electric
FM-SCU-T2	Functional tests	- LTU DRCU - Power Bench - FPU Simulator - SCU/FM test harnesses	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric
FM-MCU-A1	Inspection and Functional tests	- GSE (LAM) - SMEC/BSM Simulator - MCU/FM test harnesses	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric
FM-FCU-A1	Assembly	TBD Test equipments required for simplified functional tests	Sap SPIRE laboratory ⇨ Mechanic ⇨ Electric

FM-FCU-T1	Functional tests	- LTU DRCU - PSU loads - FCU/FM test harnesses - FPU simulator (including LAM SMEC/BSM simulator)	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric
FM-DRCU-I/T1	Integration, functional and performance tests	- LTU DRCU - Cryostat FPU-JPL - DRCU/FM test harnesses - FPU simulator (including LAM SMEC/BSM simulator)	Sap SPIRE laboratory ⇨ Electronic ⇨ Electric
FM-DCU-T3	Acceptance tests	- LTU DRCU - Power Bench - FPU Simulator - DCU/FM test harnesses	Intespace (or equivalent) facilities ⇨ Vibration ⇨ Thermal vacuum ⇨ Shock ⇨ EMI/EMC ⇨ MICD
FM-FCU-T2	Acceptance tests	- LTU DRCU - PSU loads - FPU Simulator - FCU/FM test harnesses	Intespace (or equivalent) facilities ⇨ Vibration ⇨ Thermal vacuum ⇨ Shock ⇨ EMI/EMC ⇨ MICD

Table 14-1 Test equipment

15 AIV Test documentation

This paragraph deals with the content of the test documentation to be provided and fulfilled for and during each test action.

All items must appear in the test procedure, the content of which is given thereafter :

Test Procedure

The Test procedure must contain the following items :

1. Test procedure identification
   Description of the AIV action
   (example, DCU QM1 performance tests at Sap)
2. Introduction
   - List of elements and physical characteristics to be tested
     (example : DCU, electronic properties)
   - References to other reference documents
     (example : quality plan)
3. Elements to be tested
   Their identification and description with reference to appropriate documents (STB, design documents and so on …)
   (example : DCU with reference to "HERSCHEL/SPIRE DRCU Subsystem specification")
4. Properties to be tested
   These will be described with reference to the test conception specifications
   (example, DCU EMI/EMC tests with reference to EMI/EMC tests specifications)
5. Method
   - Description of the activities, techniques, tools that will be used during tests. This description will be accurate enough to evaluate :
     - The necessary resources (material, human, qualifications)
     - The required time for the activities
6. Test acceptance criterion
7. Test suspension criterion
8. Preliminary actions
   Description of the actions required to prepare the test
9. Environment
   Description of the tools, software, hardware, safety elements required for the test

10. **Detailed Test procedures**
    This part of the main "test procedure" document shall contain

    a. Test specification and conception
       Detail of the elements to be tested and the method used

    b. Test patterns identification
       Description of input data, output data, nominal behaviors, environment …

    c. Test procedures specifications
       This is the main point of the document : it details the test steps

    d. Report associated with the elements to be tested
       Identification of the les elements (versions) and required documents

11. Identification of documents
    The documents listed below may be separate documents or part of the main test plan :

    a. **Logbooks** of involved elements
       This is the document in which the main actions performed on an element are reported

    b. **Templates**
       This is the test report document that includes

       i. description of the activities performed, results

       ii. Test data report : input data, output data, observed results

       iii. Miscellaneous tools required for the test (not planned before)

    c. **Non Conformity Report (NCR)** : list of activities, resulting anomalies

12. Test Responsible
    Identification of the human resources for each company involved in the test and for each test activity

13. Risks
    Identification of the risks

14. Approvals
    Identification of the responsible that have to approve the plan.

16 Conclusion

This document consists in overview of then AIV activities required for all SPIRE DRCU models. The main AIV steps have been described using SADT diagrams, the necessary resources and equipment listed in chapter 14 and the documents to be written to fulfill the tests detailed in chapter 15.

The forthcoming documents will then detail, for each identified AIV step, the tests performed, the tests environment, equipments and resources as well as the input/output documents.

The tests procedures will be written from the requirements associated with each unit. Cross matrixes shall be used to ensure that all functions and performances are tested.

The test harness configurations will also be studied so as to gather and organize the tests considering the DRCU harness connections.

Appendix A : Functional tests

This appendix lists the functional tests to be performed on DCU unit. At this stage, this list in given as an illustration of the functional tests and is not exhaustive.

- Reception and decoding of the low level commands
- Detector bias generation
- Bolometer signal processing
- Bolometer signal digitisation
- JFET box amplifier biasing
- JFET box heaters biasing
- Sequencer protocol (bias and clock generation)
- Housekeeping Read-out
- Cryo-cooler control
- Data acquisition
- Data processing
- Data transmission to (LTU)

Appendix B : Performance tests

This appendix lists the performance tests to be performed on DCU unit. At this stage, this list in given as an illustration of the functional tests and is not exhaustive.

- Noise measurements and identification,
- Linearity,
- stability,
- Cross talk.