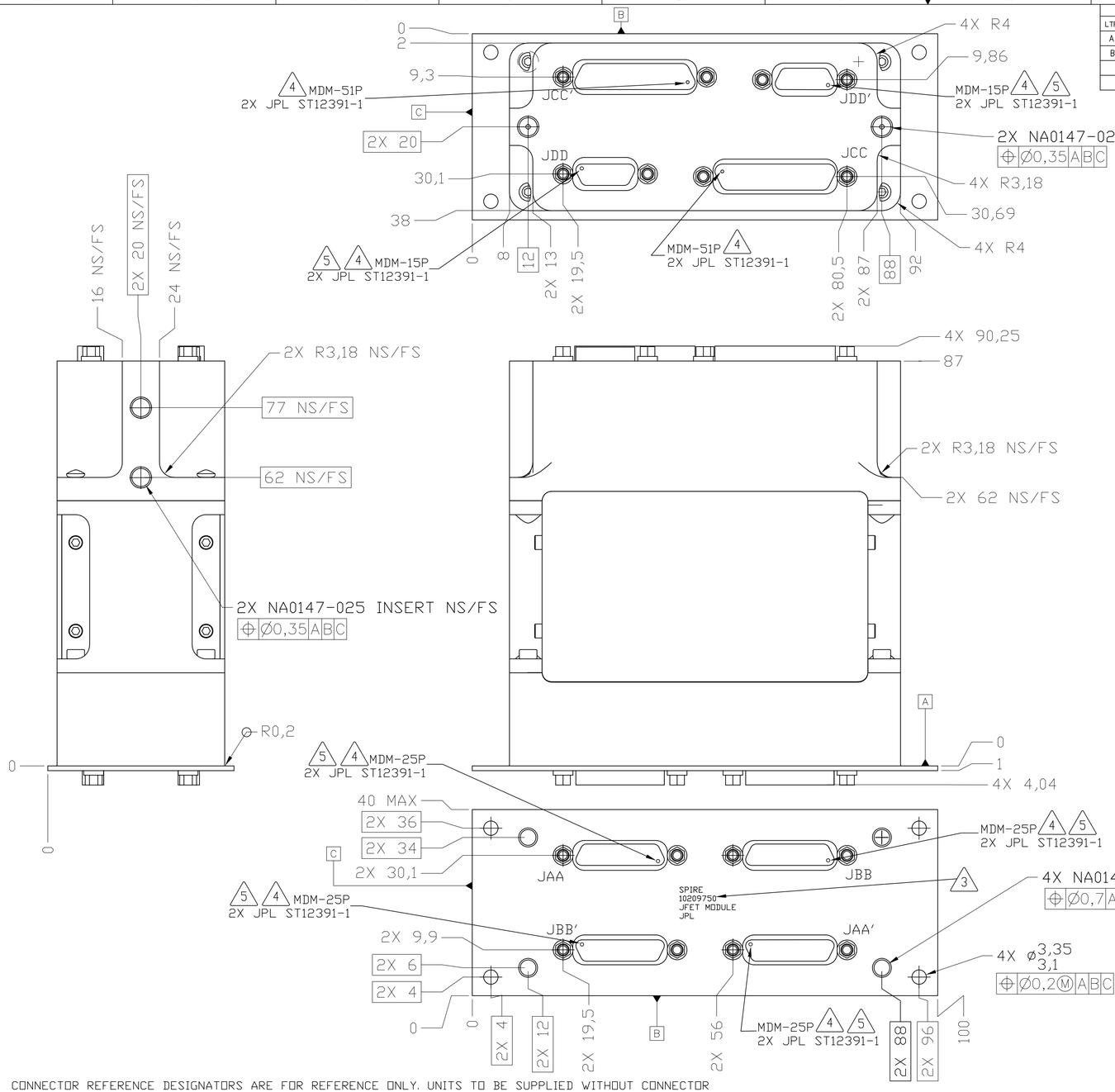
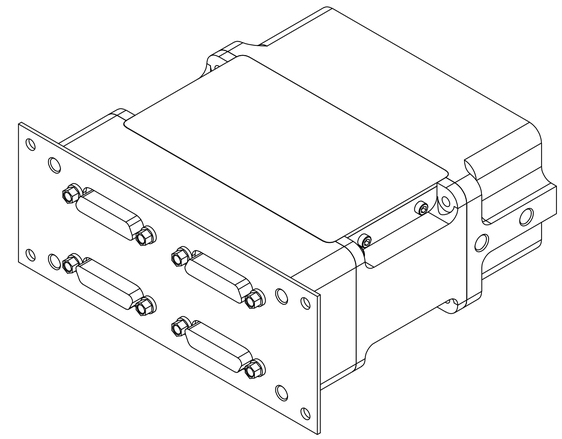
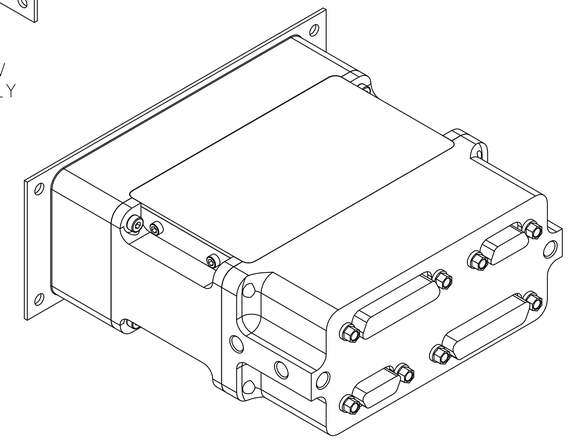
REVISIONS													
LTR	ZONE	DESCRIPTION		DWN	CHK	STRUCT	MATL	THRM CONT		ENGR	DSGN SUPV	DATA MGT	RELEASE DATE
A		INITIAL RELEASE	CODE B	SEE TITLE BLOCK									
B		SHEET 1: DELETED CONNECTOR OUTLINES; SHEET 2: UPDATED TABLES											





GENERAL VIEW
REFERENCE ONLY
SCALE: NONE



GENERAL VIEW
REFERENCE ONLY
SCALE: NONE

6. CONNECTOR REFERENCE DESIGNATORS ARE FOR REFERENCE ONLY. UNITS TO BE SUPPLIED WITHOUT CONNECTOR REFERENCE DESIGNATORS. FLIGHT REFERENCE DESIGNATORS WILL APPEAR ON JFET RACKS.

5 FILTER TYPE IS PT(3300/5000 PICOFARAD).

4 CONNECTOR CUT OUTS SIZED TO ALLOW PROPER MATING OF SOCKET CONNECTORS.

3 ASSEMBLY NUMBER, NAME, TITLE, DASH NUMBER, AND REV LETTER TO APPEAR AS SHOWN IN THIS AREA.

2. THIS IS THE INTERFACE CONTROL DRAWING FOR THE JFET MODULE ASSEMBLY, JPL PART NUMBER 10209750, REFERENCE DESIGNATION TBD. JPL DRAWING NUMBER 10209750 SHALL CONTAIN THE FOLLOWING NOTE: THIS ASSEMBLY MEETS THE INTERFACE REQUIREMENTS OF JPL INTERFACE CONTROL DRAWING 10209722.

1. THIS TECHNICAL DATA IS EXPORT CONTROLLED UNDER U.S. LAW AND IS BEING TRANSFERRED BY JPL TO PPARC PURSUANT TO THE NASA / PPARC LETTER OF AGREEMENT WHICH ENTERED INTO FORCE ON DECEMBER 2, 1999. THIS TECHNICAL DATA IS TRANSFERRED TO PPARC FOR USE EXCLUSIVELY ON THE NASA/PPARC SPIRE ON FIRST COOPERATIVE PROJECT, MAY NOT BE USED FOR ANY OTHER PURPOSE, AND SHALL NOT BE RE-TRANSFERRED OR DISCLOSED TO ANY OTHER PARTY WITHOUT THE PRIOR WRITTEN APPROVAL OF NASA.

NOTES: UNLESS OTHERWISE SPECIFIED

INTERFACE DRAWING ? John Deddeh 2003.02.1 0 09:50:26 Z ? ? Douglas Griffin Signature Not Verified Digitally signed by Douglas Griffin DN: cn=Douglas Griffin, o=RAL, ou=SSTD, c=GB Date: 2003.02.11 12:21:19 Z Reason: I have reviewed this document Location: Chilton, Didcot, OX11 0QX

PARTS LIST

QTY REQD	ITEM NO	REF DES	CAGE NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	MATERIAL OR NOTE	ZONE

MATERIAL

METRIC

THIRD ANGLE PROJECTION

NEXT ASSEMBLY: SPIRE

USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS

LINEAR TOLERANCES:

0–6	± 0.1
OVER 6–30	± 0.2
OVER 30–120	± 0.3
OVER 120–315	± 0.5
OVER 315–1000	± 0.8
OVER 1000	± 1.2

ANGULAR TOLERANCES: ± 0.5°

MACHINE FINISH (MICROMETERS) 32

DO NOT SCALE DRAWING

INTERPRET DWG PER ANSI Y14.100M

CONTRACT NO 960939

APPD _____ DATE _____

DWN D CRUMB 01/09/02

CHK

STRUCT

MATL

THRM CONT

ENGR

DSGN SUPV

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
PASADENA, CA 91109

RELEASED THROUGH EDMG

JFET MODULE, INTERFACE DRAWING

SIZE	CAGE NO		REV
A1	23835	10209722	B
SCALE 2:1		UNCLASSIFIED	SHEET 1 OF 2

REV 2/00

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A1 10209722

JAA JFET OUTPUT 1B	
PIN #	PIN PURPOSE
1	SIGNAL M+
2	SIGNAL N+
3	SIGNAL P+
4	SIGNAL R+
5	SIGNAL S+
6	SIGNAL T+
7	SIGNAL U-
8	SIGNAL V-
9	SIGNAL W-
10	SIGNAL X-
11	SIGNAL Y-
12	SIGNAL Z-
13	FPU GND
14	SIGNAL M-
15	SIGNAL N-
16	SIGNAL P-
17	SIGNAL R-
18	SIGNAL S-
19	SIGNAL T-
20	SIGNAL U+
21	SIGNAL V+
22	SIGNAL W+
23	SIGNAL X+
24	SIGNAL Y+
25	SIGNAL Z+

JBB JFET OUTPUT 1A	
PIN #	PIN PURPOSE
1	SIGNAL A+
2	SIGNAL B+
3	SIGNAL C+
4	SIGNAL D+
5	SIGNAL E+
6	SIGNAL F+
7	SIGNAL G-
8	SIGNAL H-
9	SIGNAL I-
10	SIGNAL J-
11	SIGNAL K-
12	SIGNAL L-
13	FPU GND
14	SIGNAL A-
15	SIGNAL B-
16	SIGNAL C-
17	SIGNAL D-
18	SIGNAL E-
19	SIGNAL F-
20	SIGNAL G+
21	SIGNAL H+
22	SIGNAL I+
23	SIGNAL J+
24	SIGNAL K+
25	SIGNAL L+

JAA' JFET OUTPUT 2A	
PIN #	PIN PURPOSE
1	SIGNAL M+'
2	SIGNAL N+'
3	SIGNAL P+'
4	SIGNAL R+'
5	SIGNAL S+'
6	SIGNAL T+'
7	SIGNAL U-'
8	SIGNAL V-'
9	SIGNAL W-'
10	SIGNAL X-'
11	SIGNAL Y-'
12	SIGNAL Z-'
13	FPU GND'
14	SIGNAL M-'
15	SIGNAL N-'
16	SIGNAL P-'
17	SIGNAL R-'
18	SIGNAL S-'
19	SIGNAL T-'
20	SIGNAL U+'
21	SIGNAL V+'
22	SIGNAL W+'
23	SIGNAL X+'
24	SIGNAL Y+'
25	SIGNAL Z+'

JBB' JFET OUTPUT 2B	
PIN #	PIN PURPOSE
1	SIGNAL A+'
2	SIGNAL B+'
3	SIGNAL C+'
4	SIGNAL D+'
5	SIGNAL E+'
6	SIGNAL F+'
7	SIGNAL G-'
8	SIGNAL H-'
9	SIGNAL I-'
10	SIGNAL J-'
11	SIGNAL K-'
12	SIGNAL L-'
13	FPU GND'
14	SIGNAL A-'
15	SIGNAL B-'
16	SIGNAL C-'
17	SIGNAL D-'
18	SIGNAL E-'
19	SIGNAL F-'
20	SIGNAL G+'
21	SIGNAL H+'
22	SIGNAL I+'
23	SIGNAL J+'
24	SIGNAL K+'
25	SIGNAL L+'

JCC JFET INPUT 1	
PIN #	PIN PURPOSE
1	BIAS V+
2	BIAS V-
3	SIGNAL Y+
4	SIGNAL W-
5	SIGNAL V+
6	SIGNAL T+
7	SIGNAL S-
8	SIGNAL P+
9	SIGNAL N-
10	SIGNAL L-
11	SIGNAL K+
12	SIGNAL I-
13	SIGNAL H+
14	SIGNAL F+
15	SIGNAL E-
16	SIGNAL C+
17	SIGNAL B-
18	SIGNAL A-
19	BIAS GND
20	SIGNAL Z+
21	SIGNAL X-
22	SIGNAL W+
23	SIGNAL U-
24	SIGNAL T-
25	SIGNAL R+
26	SIGNAL P-
27	SIGNAL M+
28	SIGNAL L+
29	SIGNAL J-
30	SIGNAL I+
31	SIGNAL G-
32	SIGNAL F-
33	SIGNAL D+
34	SIGNAL C-
35	SIGNAL A+
36	SIGNAL Z-
37	SIGNAL Y-
38	SIGNAL X+
39	SIGNAL V-
40	SIGNAL U+
41	SIGNAL S+
42	SIGNAL R-
43	SIGNAL N+
44	SIGNAL M-
45	SIGNAL K-
46	SIGNAL J+
47	SIGNAL H-
48	SIGNAL G+
49	SIGNAL E+
50	SIGNAL D-
51	SIGNAL B+

JDD JFET SERVICE 1	
PIN #	PIN PURPOSE
1	Vss
2	V+
3	H+
4	V-
5	V-
6	H+
7	V+
8	Vss
9	BIAS GND
10	Vdd
11	H-
12	CHASSIS GND
13	H-
14	Vdd
15	BIAS GND

JDD' JFET SERVICE 2	
PIN #	PIN PURPOSE
1	Vss'
2	V+'
3	H+'
4	V-'
5	V-'
6	H+'
7	V+'
8	Vss'
9	BIAS GND'
10	Vdd'
11	H-'
12	CHASSIS GND'
13	H-'
14	Vdd'
15	BIAS GND'

JCC' JFET INPUT 2	
PIN #	PIN PURPOSE
1	BIAS V+'
2	BIAS V-'
3	SIGNAL Y+'
4	SIGNAL W-'
5	SIGNAL V+'
6	SIGNAL T+'
7	SIGNAL S-'
8	SIGNAL P+'
9	SIGNAL N-'
10	SIGNAL L-'
11	SIGNAL K+'
12	SIGNAL I-'
13	SIGNAL H+'
14	SIGNAL F+'
15	SIGNAL E-'
16	SIGNAL C+'
17	SIGNAL B-'
18	SIGNAL A-'
19	BIAS GND'
20	SIGNAL Z+'
21	SIGNAL X-'
22	SIGNAL W+'
23	SIGNAL U-'
24	SIGNAL T-'
25	SIGNAL R+'
26	SIGNAL P-'
27	SIGNAL M+'
28	SIGNAL L+'
29	SIGNAL J-'
30	SIGNAL I+'
31	SIGNAL G-'
32	SIGNAL F-'
33	SIGNAL D+'
34	SIGNAL C-'
35	SIGNAL A+'
36	SIGNAL Z-'
37	SIGNAL Y-'
38	SIGNAL X+'
39	SIGNAL V-'
40	SIGNAL U+'
41	SIGNAL S+'
42	SIGNAL R-'
43	SIGNAL N+'
44	SIGNAL M-'
45	SIGNAL K-'
46	SIGNAL J+'
47	SIGNAL H-'
48	SIGNAL G+'
49	SIGNAL E+'
50	SIGNAL D-'
51	SIGNAL B+'

SIZE	CAGE NO		REV
A1	23835	10209722	B
SCALE NONE	UNCLASSIFIED	SHEET 2 OF 2	

REV 2/00

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A1 10209722