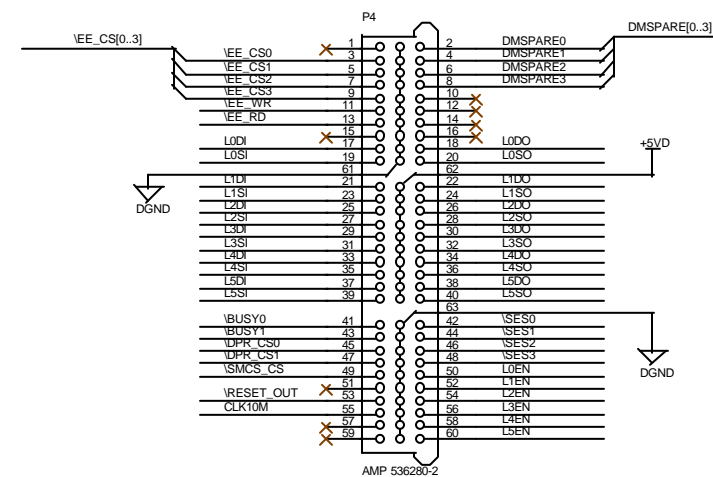
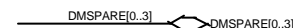
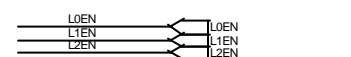
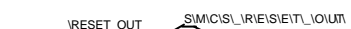
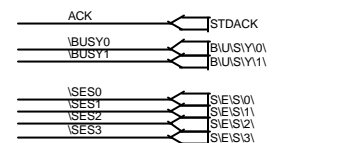
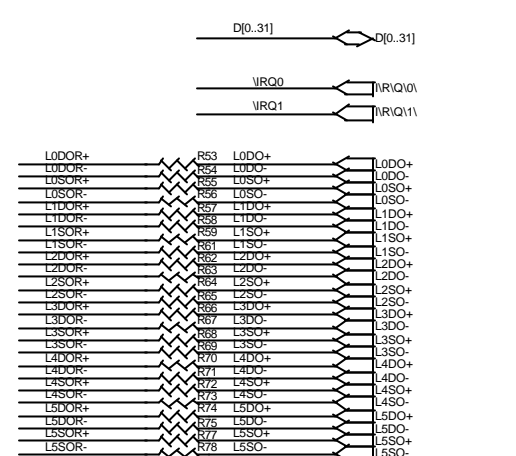
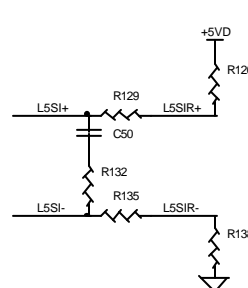
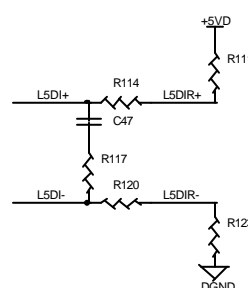
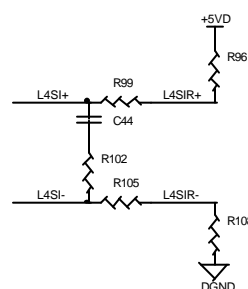
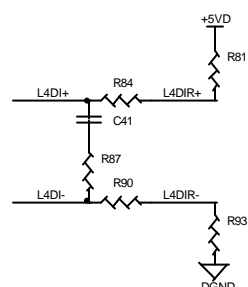
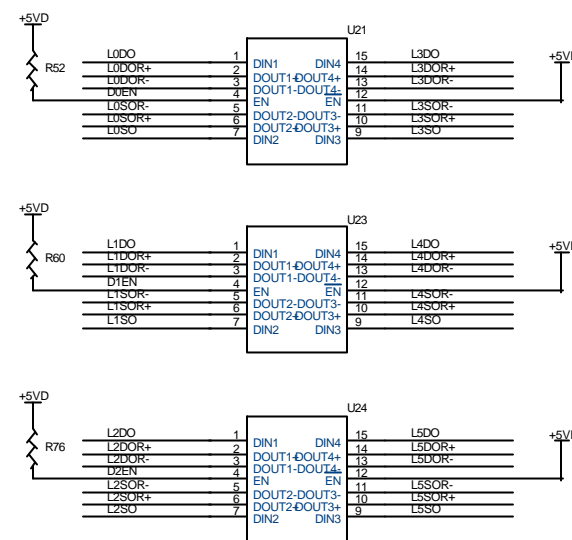
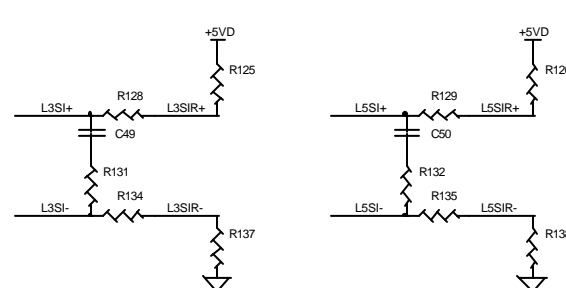
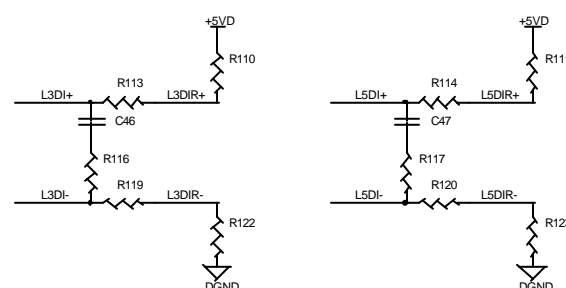
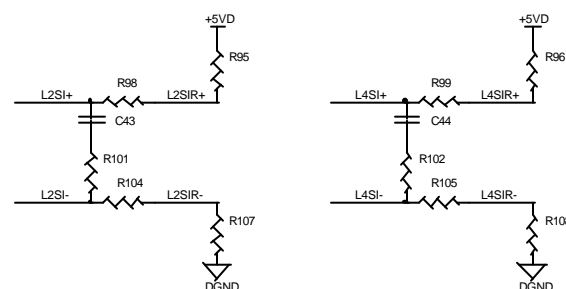
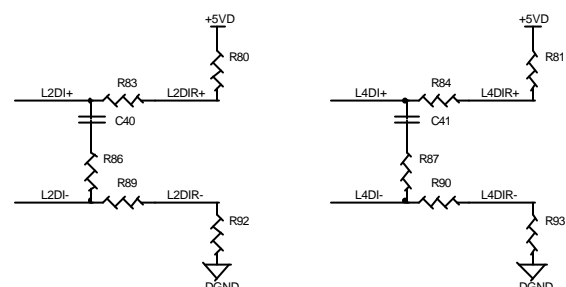
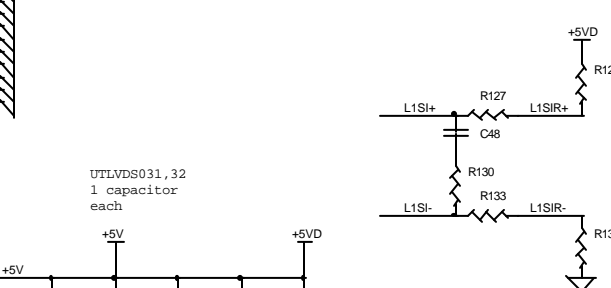
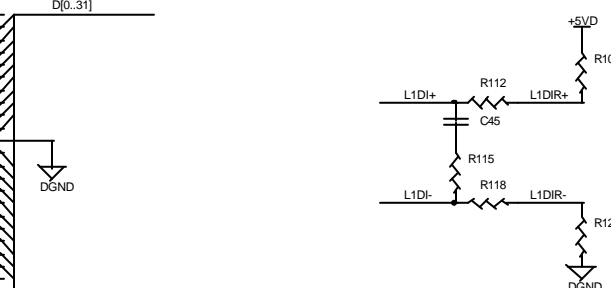
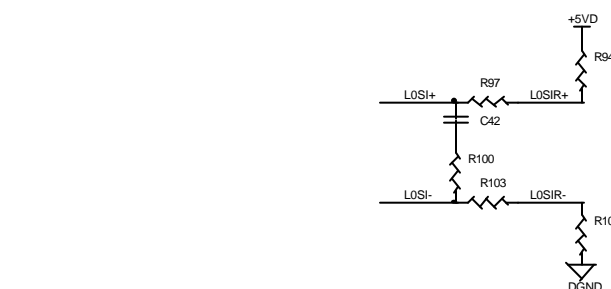
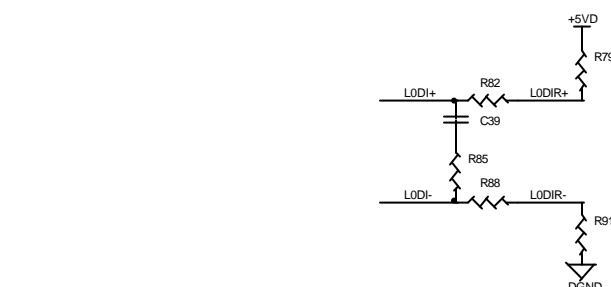
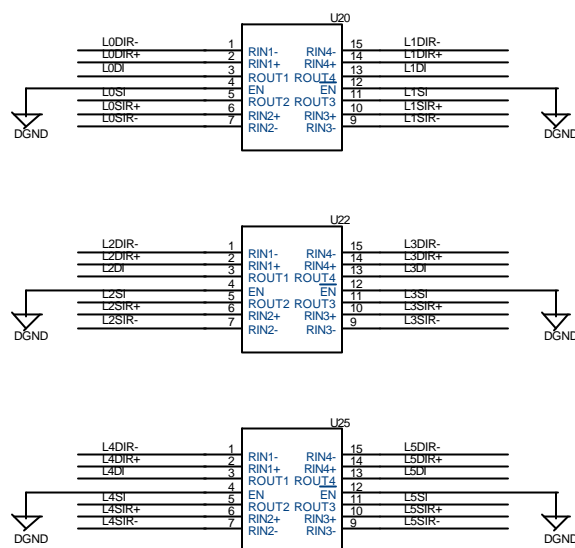
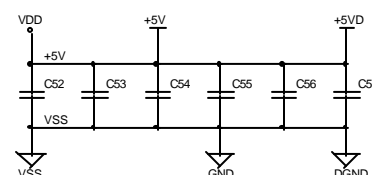
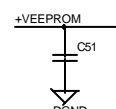
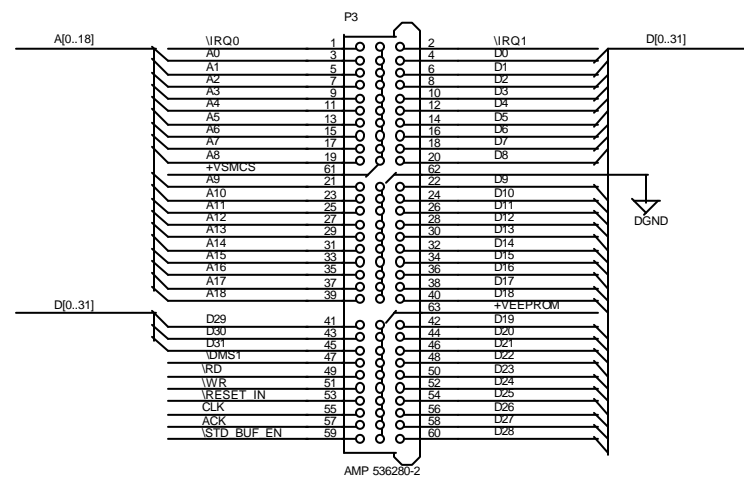
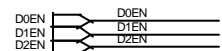
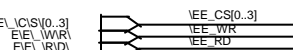
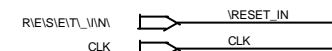
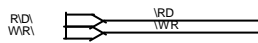
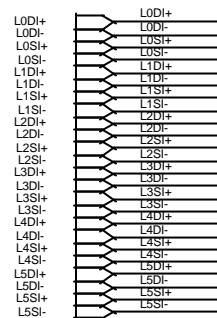
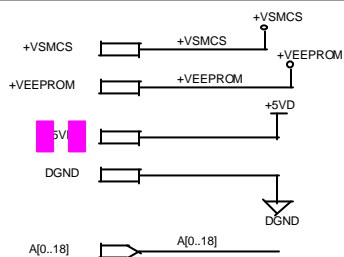



UTLVDS031,32
VDD: 16
VSS: 8

KEEP, R85-C39, R86-C40, R100-C42,
R101-C43, R115-C45, R130-C48 AS NEAR
AS POSSIBLE TO THE RESPECTIVE RECEIVER
(UTLVDS032) MAX. 10mm OF PCB TRACE

PCB TRACES BETWEEN U20, U21, U22, U23,
U24, U25 AND CONNECTOR P2 MUST BE AS
SHORT AS POSSIBLE



/									
REV.	DATE	DRAWN	CHECK	ENG.	PLASS	C. dC.	CHANGE AUTHORITY		
CUSTOMER				EFFECTIVITY		CARLO GAVAZZI SPACE			
DRAWING TITLE		HSO/FIRST-DPU CPU BOARD DM Mezzanine I/F				SCALE		GEN. TEL.	
								GEN. RA.	
HIGHER ASSEMBLY				DRAWING NUMBER				SHEET OF	
DPU-EM-110.000				DPU-EM-110.020				5 OF 8	