CARLO GAVAZZI SPACE S.p.A.

FIRST DPU

DOCUMENT TYPE : SPECIFICATION **DRD :**

TITLE: PAYLOAD & SPACECRAFT INTERFACE BOARD SPECIFICATION

DOCUMENT No: DPU-SP-CGS-002 **PAGE:** 1 **OF** 34

ISSUE No: 1 **DATE:** 11/12/2000

PREPARED BY: L. TUNESI

APPROVED BY:

THIS DOCUMENT IS SUBJECT TO THE APPROVAL OF:

	YES	NO		
Product Assurance	X		Approval Signature	Date
Configuration Control	X		Approval Signature	Date
Project Control		X	Approval Signature	Date
Engineering	X		Approval Signature	Date
Managing Director		X	Approval Signature	Date
CGS Program Manager	X		Approval Signature	Date

	YES	NO		
Higher Level Contractor	X		Approval Signature	Date
Customer		X	Approval Signature	Date

Data Management		
	Signature	Date

DOCUMENT CHANGE RECORD				
ISSUE N°	**DATE**	**CHANGE AUTHORITY**	**PAGES AFFECTED**	**REMARKS**
1	11/12/2000			

LIST OF VALID PAGES

PAGE	ISSUE N°	PAGE	ISSUE N°	PAGE	ISSUE N°	PAGE	ISSUE N°	PAGE	ISSUE N°
1-34	1								

TABLE OF CONTENTS

LIST OF ACRONYMS

AD#	Applicable Document number #
ASI	Agenzia Spaziale Italiana
ATP	Authorization to proceed
CGS	Carlo Gavazzi Space SpA
CNR	Consiglio Nazionale delle Ricerche
CPP	Coordinated Part Procurement
DPU	Data Processing Unit
DDC	Data Device Corporation
DPR	Dual Port Ram
EDAC	Error Detector And Corrector
EEPROM	Electrically Erasable Programmable Read Only Memory
EF	Empty FIFO
EM	Engineering Model
EPROM	Erasable Programmable Read Only Memory
EQM	Engineering Qualification Model
FIRST	Far Infra-Red and Sub-millimeter Telescope
FF	Full FIFO
FM	Flight Model
FPGA	Field Programmable Gate Array
FS	Flight Spare
FSDL	Fast Science Data Link
HF	Half Full FIFO
HIFI	Heterodyne Instrument for First
IFSI	Istituto per la Fisica dello Spazio Interplanetario
I/F	Interface
LSL	Low Speed Link
OBDH	On Board Data Handling
PA	Product Assurance
PACS	Photoconductor Array Camera and Spectrometer

PCB	Printed Circuit Board
PROM	Programmable Read Only Memory
PL	Payload
RAM	Random Access Memory
RD#	Reference Document number #
SEU	Single Event Upset
S/C	Spacecraft
SPIRE	Spectral and Photometric Imaging Receiver

1 SCOPE

The aim of the present document is to define the specifications of the PL I/F board to be used in the Data Processing Units, developed in the framework of the First program.

This document shall be the basis on which the PL I/F board will be designed.

2 APPLICABLE DOCUMENTS

[AD1]: CNR.IFSI.2000TR01 "Documento di Specifiche Tecniche per il Contratto delle Data Processing Units del Satellite First dell'ESA" IFSI (Issue: 1 - 15/09/2000)

[AD2]: Technical proposal CGS (Ref. S9-030 November 99)

[AD3]: "Allegato Tecnico al Contratto ASI"

3 REFERENCE DOCUMENTS

[RD1]: Radiation Tolerant 32/40-BIT IEEE Floating Point DSP Microprocessor Data Book Temic REV E October 05, 1998

[RD2]: First CPU Board Specification DPU-SP-CGS-001, Carlo Gavazzi Space Issue 1 date 12/10/2000

[RD3]: Space Level MIL-STD-1553 BC/RT/MT Advanced Communication Engine Terminal BU-61582 Data Book ILC Data Device Corporation 1995

[RD4]: MIL-STD-1553 BC/RT/MT Advance Communication Engine (ACE) Data Book ILC Data Device Corporation

[RD5]: ACE/Mini-ACE Series BC/RT/MT Advanced Communication Engine Integrated 1553 Terminal… User's Guide ILC Data Device Corporation, june 1999, REV J-2

4 BOARD CHARACTERISTICS

The PL I/F board is based on the Actel 8000 gates RH1280 FPGA. The main characteristics of the board are the following:

- ✓ MIL-STD-1553 RT-mode serial interface up to 400KHz (burst mode) for the connection to the spacecraft
- ✓ 16MHz square wave oscillator onto the board (for the 1553 terminal unit)
- ✓ Four Fast Science Data Link (FSDL) ports up to 2.5MHz for the HIFI and SPIRE payloads interfacing
- ✓ Low Speed Link at 312.5KHz towards 7 sub-systems, for commands sending
- ✓ eight, not conditioned, 0-5V, single ended, analog inputs
- ✓ 32-bit parallel system bus
- ✓ Software interface implemented by registers mapped on the parallel bus address space
- ✓ AMP connector for test purpose (EM version only)

5 MECHANICAL CONSTRAINTS

The PL I/F function is implemented through two Printed Circuit Boards (TBC) named:

- ✓ Main board
- ✓ Mezzanine board (TBC)

The mechanical constraints of the two boards are shown in the Table 1 and Table 2 while the weight of the overall PL I/F function is specified in the Table 3

Main board size:	Double Euro (160mm x 233.35mm)
Overall thickness:	28 mm (6mm solder side, 20mm comp. side, 2 mm PCB max)
Card retainers:	Calmark series 260
Board connectors (connection to back plane):	90°, male, DIN41612 type
Board connectors (connection to mezzanine):	AMP 536280-2

Table 1 Main board constraints

Mezzanine size:	TBD
Mezzanine connectors:	AMP 536279-2
Mechanical fastening:	Fixation on main board and stiffening bar with six screws

Table 2 Mezzanine board constraints

Overall weight (max):	480g (TBC)

Table 3 PL I/F board weight

Due to critical allocation of the components on the board, components are mounted on both sides of the PCB.

6 ENVIRONMENTAL CONSTRAINTS AND POWER SUPPLY

The constraints are summarised in the following tables:

Operating temperature:	-30 ÷ +55 °C
Non operating temperature:	-50 ÷ +85 °C
Total dose:	≤ 10 Krad
SEU rate:	≤ 1 error/year

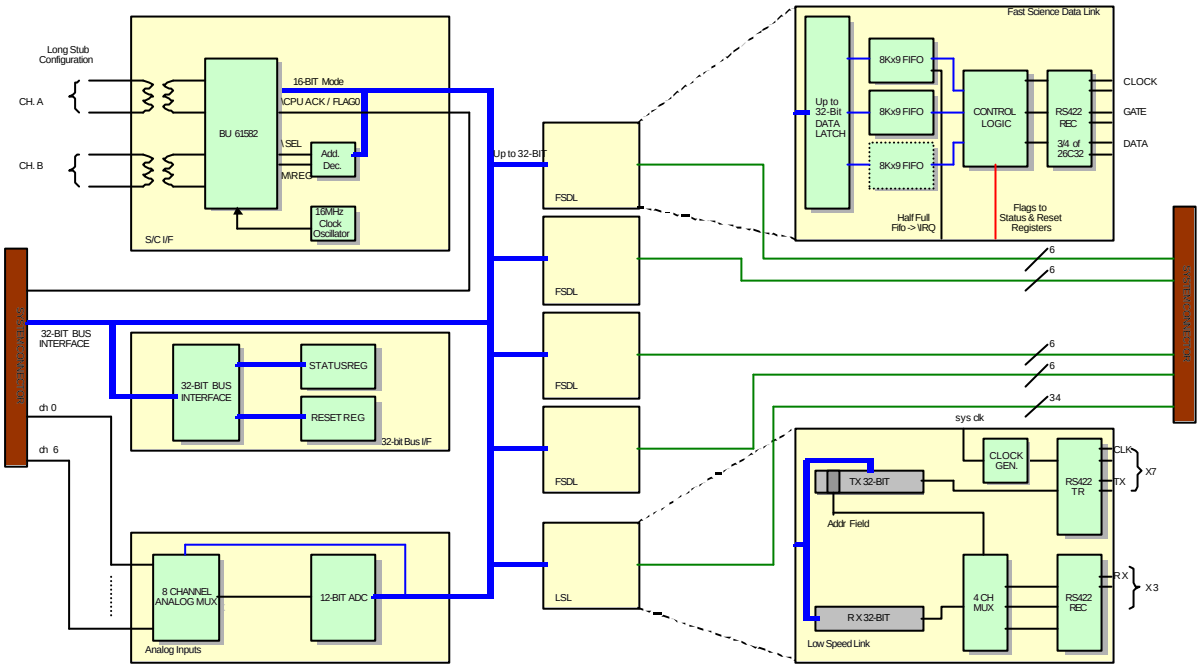
Table 4 Environmental constraints

Power supply:	5V ± 0.5V +15V ± 1.5V -15V ± 1.5V
Maximum continuous supply current	1.5A
Peak current:	2A

Table 5 Power supply

7 FUNCTIONAL DESCRIPTION

The block diagram of the PL I/F board is shown in the Picture 1



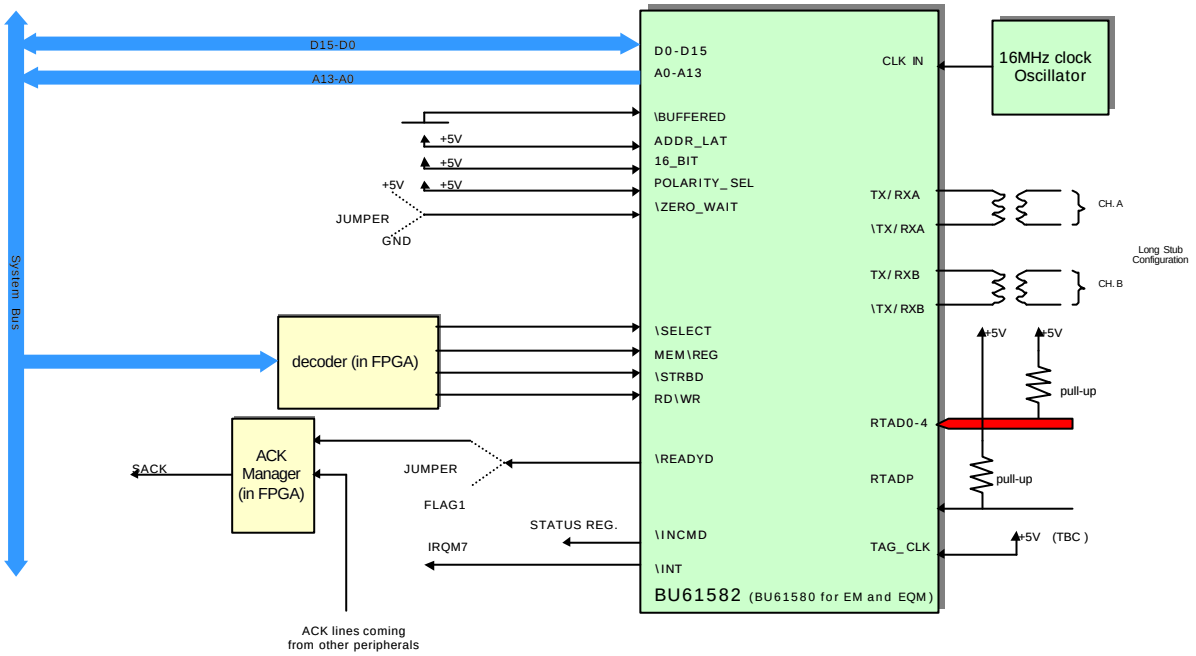
Picture 1 PL I/F board block diagram

The dashed parts of the block diagram (third FIFO in the FSDL interface) are mounted only for HIFI configuration.

In the next paragraphs each block will be described in detail.

7.1 Spacecraft Interface

The spacecraft interface is the MIL-STD-1553B standard serial link at 100Kbit/s up to 400Kbit/s (burst mode). This interface is realised with a dedicated hybrid circuit, made by DDC.



Picture 2: MIL-STD-1553 interface

For the EM and EQM models shall be mounted the commercial version, named BU-61580. For the flight models (FM, FS) the BU-61582, the radiation hardened version of the BU-61580 terminal, shall be mounted.

This very useful terminal integrates dual transceivers, protocol, memory management and processor interface logic, 16Kx16-bit (4Kx16-bit for the commercial version) of Dual Port RAM and a Time Tag Register used to allow the software to manage the "on board time". The timer rollover generates an interrupt to be used to increment the software time registers. The clock of the Time Tag Register implies the time resolution. The programmable resolution is 2, 4, 8, 16, 32 or 64µs per LSB.

The terminal unit is used in 16-bit buffered mode [RD5].

7.1.1 CLOCK GENERATION

The DDC chip needs a square wave clock @16MHz; in order to easily generate this signal, a VECTRON qualified oscillator shall be used. All the other peripherals shall work with dedicated clocks generated by the 20MHz system clock.

7.1.2 SOFTWARE INTERFACE

In two different system bus spaces are mapped the S/C interface registers and the interface memory (see Table 15). The registers are the following:

Address	Register	Size [bit]	Direction
0x4000	Interrupt mask register	16	read/write
0x4001	Configuration register #1	16	read/write
0x4002	Configuration register #2	16	read/write
0x4003	Start/Reset register	16	write
0x4003	BC/RT Command Stack Pointer register	16	read
0x4004	BC Control Word/RT Subaddress Control Word register	16	read/write
0x4005	Time Tag register	16	read/write
0x4006	Interrupt Status register	16	read
0x4007	Configuration register #3	16	read/write
0x4008	Configuration register #4	16	read/write
0x4009	Configuration register #5	16	read/write
0x400A	Data Stack Address register	16	read/write
0x400B	BC Frame Time Remaining register	16	read/write
0x400C	BC Time Remaining to Next Message register	16	read/write
0x400D	BC Frame Time/RT Last Command/MT Trigger Word register	16	read/write
0x400E	RT Status Word register	16	read
0x400F	RT BIT Word register	16	read
0x4010	Test Mode register 0	16	
0x4011	Test Mode register 0	16	
0x4012	Test Mode register 0	16	
0x4013	Test Mode register 0	16	
0x4014	Test Mode register 0	16	
0x4015	Test Mode register 0	16	
0x4016	Test Mode register 0	16	
0x4017	Test Mode register 0	16	

Address	Register	Size [bit]	Direction
0x4018	Reserved	16	--
0x4019	Reserved	16	--
0x401A	Reserved	16	--
0x401B	Reserved	16	--
0x401C	Reserved	16	--
0x401D	Reserved	16	--
0x401E	Reserved	16	--
0x401F	Reserved	16	--

Table 6: MIL-STD-1553 registers

The registers are described in detail in [RD3].

For the data exchange, a 16Kx16-bit (4Kx16-bit for EM and EQM version) internal Dual Port RAM is used and it is mapped according to Table 7.

Address	Peripheral	Size [bit]	Direction
0x0000 ÷ 0x3FFF	Buffer RAM	16	read write

Table 7: S/C interface buffer memory

The \INCMD hardware flag is mapped on the board status register (see Table 19) whereas the \SSFLAG pin is not connected.

7.1.3 HARDWARE INTERFACE

A hardware reset, acting on the MSTCLR pin of the terminal, shall be mapped in the reset register of the board.

This terminal unit is mapped as slow peripheral (\CS7) of the system bus; in order to adjust the timing, an acknowledge management mode is foreseen [RD5]. Two configurations (settable via jumper) are possible to manage this timing:

1. non zero wait state mode

2. zero wait state mode

The non zero wait state mode allows direct interface to the system bus: the terminal stops the DSP until the data are available on the output bus of the unit. In the zero wait state mode, the processor can clear its strobe before the completion of access to the unit internal RAM or registers. In this case it is necessary to connect and polling the

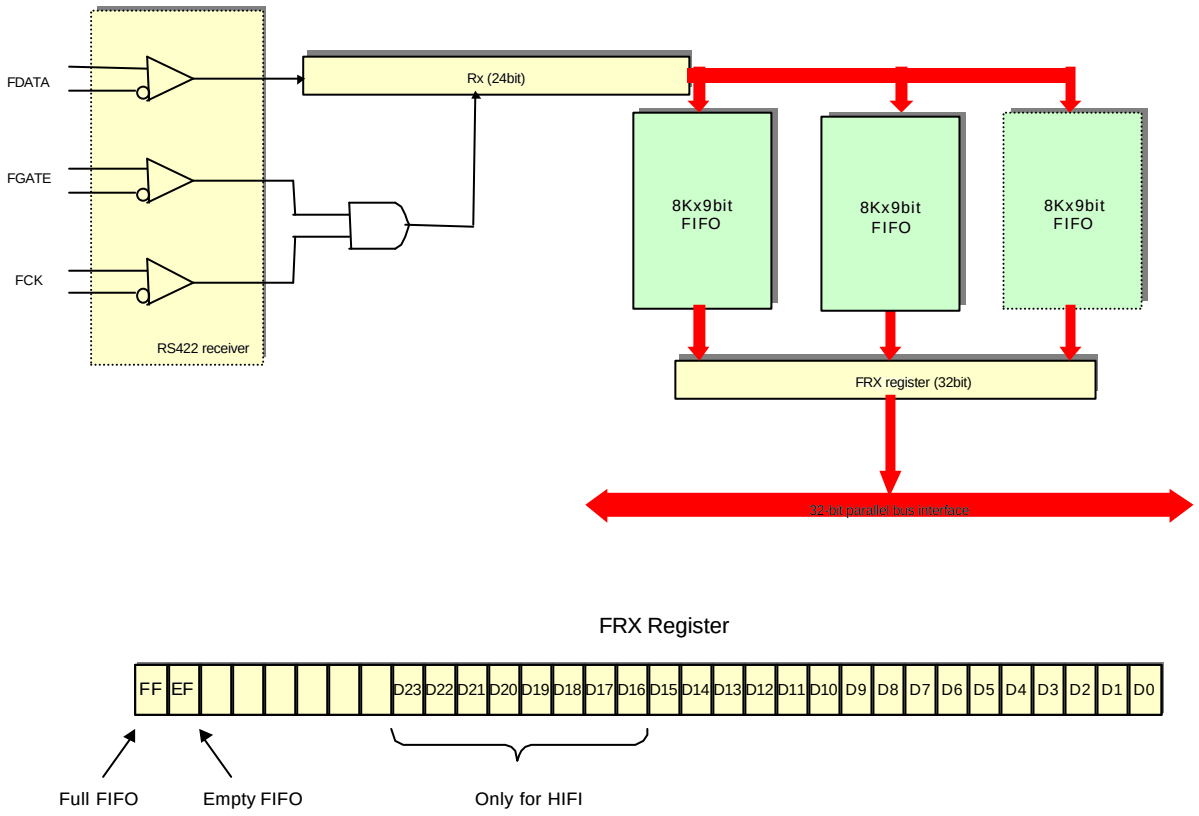
\READYD line to FLAG1, for the completion of the transfer [RD3]. The suggested configuration is the first one.

7.1.4 INTERFACE TO MIL-STD-1553 BUS

The interface to MIL-STD-1553 bus is the transformer coupled configuration (long stub). Two isolation transformers (one per section) are present on the board. Since the terminal unit is powered at ±15V, the transformers have a turns ratio of 2:1.

7.2 Fast Science Data Link Interfaces

The four Fast Science Data Links are implemented to receive data from HIFI and SPIRE; the conceptual scheme is presented in the following picture:

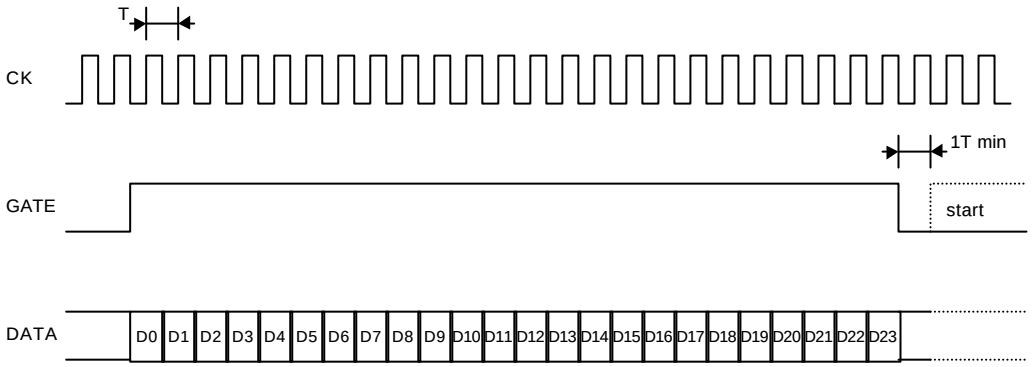


Picture 3: Fast Science Data Link diagram

HIFI interfaces the DPU with four FSDL links (connection with HRS-V/H and WBS-V/H) only three links are necessary for the SPIRE (connection with DRE, MCE, SCE).

All the signals (FDATA, FCK, FGATE) are generated on the sub-unit side. The interface can receive data with clock frequencies up to 2.5MHz and the size of the data is dependent to the payload. HIFI uses 24-bit and the total FIFO configuration is necessary (up to 32-bit); on the contrary SPIRE uses 16-bit and two FIFO banks per link are mounted.

The timings are shown in Picture 4



Picture 4: FSDL timings

The gate signal is active (high) during the transmission of each data word. The gate signal shall be inactive (low) for, at least, one clock cycle between successive data word transfers. The gate and data signals change state on the falling edge of the clock signal.

7.2.1 INTERRUPT GENERATION

When the FIFO reaches the half quantity of data, an edge mode (150ns) interrupt is generated; each FSDL provides a dedicated interrupt line (see Table 8).

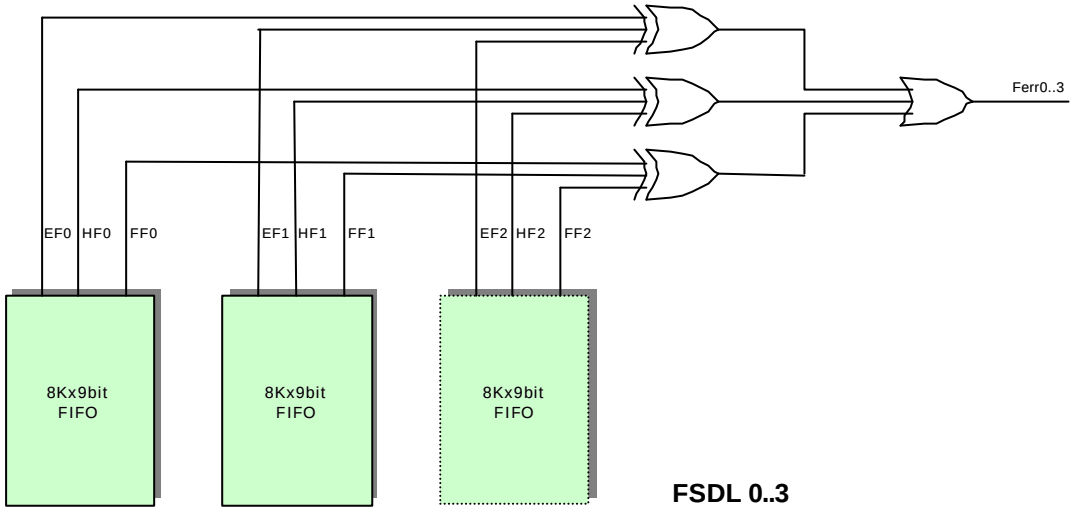
IRQM#	Peripheral
3	Bus interface (FSDL 0)
4	Bus interface (FSDL 1)
5	Bus interface (FSDL 2)
6	Bus interface (FSDL 3)

Table 8: FSDL interrupts

7.2.2 FIFO FLAGS

In the status register (see paragraph 7.6.1) the empty FIFO (EF), half full FIFO (HF) and full FIFO (FF) of each link are mapped; an echo of the gate signals (ACQ) are present in the status register to inform the system about the receiving data from the payload. An echo of the empty and full FIFO flags is directly in the SRX registers of each FSDL interface (see Picture 3).

Four fifo error flags (one per link) are mapped in the status register to inform that a misalignment is occurred. The hardware implementation is shown in Picture 5



Picture 5 FIFO error flag generation

In the reset register (see paragraph 7.6.1) four FIFO resets are mapped to clear the memories.

7.2.3 SOFTWARE INTERFACE

Address	Register name	Size [bit]	Direction
0x0	FRX_register	32	read

Table 9: FSDL registers

The 24 bit (16 for SPIRE) shall be mapped on the lowest space of the system data bus.

If the software accesses the registers when the FIFO are empty (EF flag asserted on the status register), the loaded value is not significant.

7.3 Low Speed Link Interface

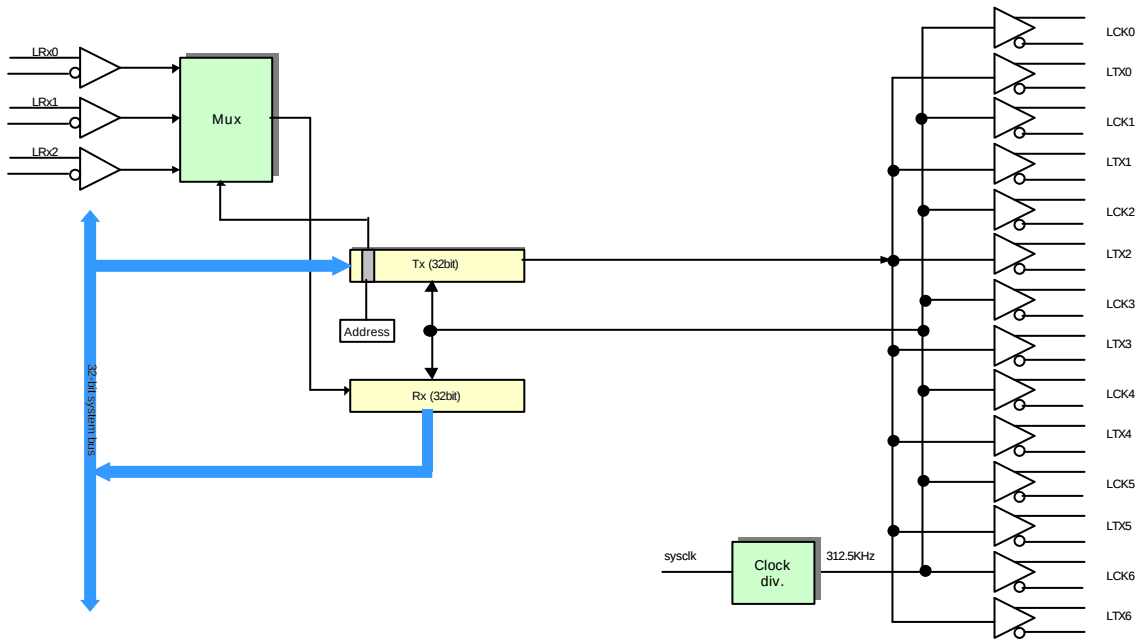
This command/housekeeping interface is applicable to both HIFI and SPIRE payloads; in particular it has to interface the LSU, LCU, FCU, HR-H, HR-V, WBE-H and WBE-V sub-units of HIFI, whereas DRE, MCE, SCE are the sub-units of SPIRE connected to this link.

The signals constituting the links are: clock line (LCK), transmitter line (LTX) and receiver line (LRX). LCK and LTX have to be generated by the board and LRX arrives from the sub-units. The LTX and LRX signals change state on the falling edge of the clock signal.

The clock is fixed at 312.5KHz and it is generated dividing the system clock by 64 (with a FPGA divider block).

Only three LRX lines are present, both for HIFI (LSU, LCU, FCU) and SPIRE; they have dedicates RS422 receivers and are selected, for the acquisition, by a MUX.

A schematic view of the board-side interface is the following:



Picture 6: Low Speed Link Interface

By this interface it is possible to send commands or housekeeping requests; some differences between the two payloads will be discussed: two different FPGA projects allow the implementation of the two configurations.

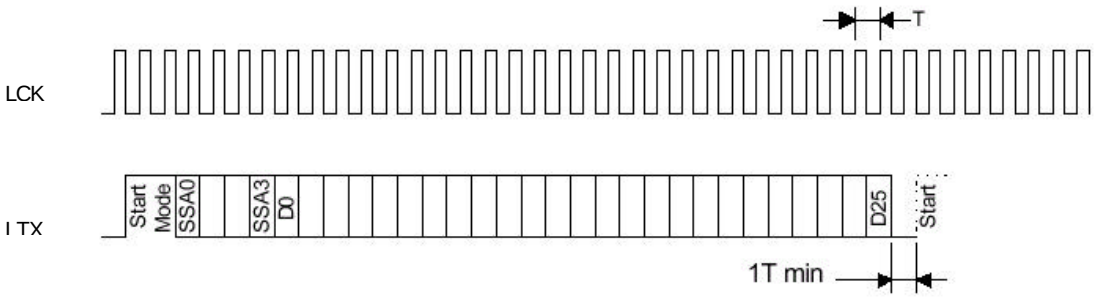
All the data formats shall be performed by software. In particular, for what concern the HIFI housekeeping request, the programmer must adds 16 high bits LSB to normalise the word in 32-bit format.

7.3.1 INTERFACE FOR HIFI

The command protocol and timing diagram is shown in Picture 7. Each command consists of: one start bit (high), one mode bit (high), four subsystem address bits and 26 data bits. The subsystem addresses are hamming coded, according to Table 10. No answers from the sub-units are foreseen in command protocol.

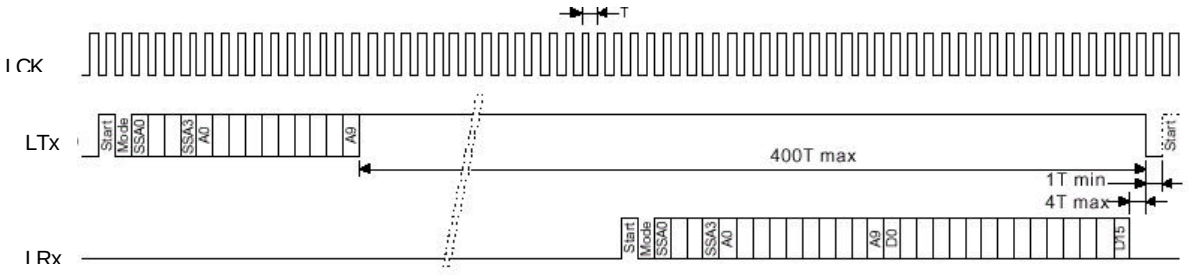
AS0-AS3	Unit
0000	LSU
0011	FCU
0101	HRH
0110	HRV
1001	WBE-H
1010	WBE-V
1100	LCU
1111	Broadcast command

Table 10: Subsystem addresses



Picture 7: HIFI command protocol

A housekeeping request consist of: one start bit (high), one mode bit (low), four subsystem address bits, and an envelope. The address bits identify the requested housekeeping parameter. The envelope shall be active (high) until the full housekeeping response has been received, in any case it goes inactive (low) after 400 clock-cycles (hardware timeout). If the DPU has to transmit a command, when the housekeeping envelope is still active, the housekeeping request shall be aborted by setting the envelope into the inactive state.

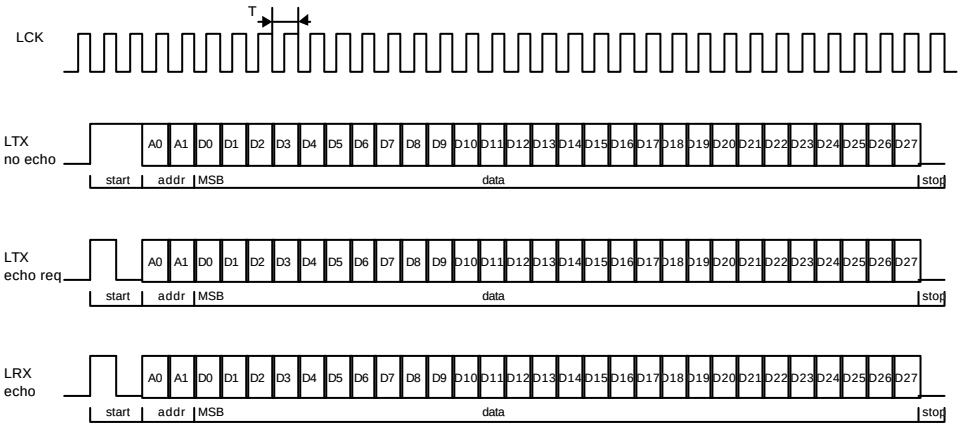


Picture 8: HIFI housekeeping request command protocol

A command or housekeeping request shall not start within one clock-cycle after the previous command has terminated or the housekeeping envelope has gone to the inactive state.

7.3.2 INTERFACE FOR SPIRE

The command and acknowledge (echo or parameters) protocol is shown in Picture 9



Picture 9: SPIRE command protocol

Each command or acknowledge word is composed by: one start bit (high), one mode bit (low for echo request, high for command sending without answers), two subsystem address bits, 28 data bits.

Mode bit	Ack
0	yes
1	no

Table 11: Mode bit pattern definition

A1	A0	Subsystem
0	0	DRE
0	1	MCE
1	0	SCE
1	1	Broadcast command

Table 12: subsystem addresses

Each command shall not start within one clock-cycle after the previous command has terminated (stop bit).

When a command with acknowledge request is received, the subsystem responds by transferring a command acknowledge word (echo or parameter) on the LRX interface line. The DPU receives then the answer, from the selected sub-unit. Successive answers, generated by other commands, will be overwritten on the same register.

7.3.3 SOFTWARE INTERFACE

The software interface is realised with three registers, as mentioned in Table 13

Address	Register name	Size [bit]	Direction
0x0	LTX_register	32	read/write
0x1	LRX_ register	32	read
0x2	Lstatus_register	32	read

Table 13: LSL registers

The command a/o the housekeeping request have to be written in the LTX register in 32-bit format, only when the "TX busy" flag of the Lstatus register (see Table 14) is not asserted. The "TX busy flag" is asserted when the interface is engaged in a command sending.

When a write cycle starts (only for HIFI), a previous housekeeping request, not terminated, shall be aborted and a new transmission will start. In this case the "HK aborted" flag of the Lstatus register will assert.

The echo/housekeeping datum (when the mode-bit of the TX command is low) is latched in the LRX register, then the "data ready" flag is asserted. The LRX register (and the "data ready" flag) shall be HW reset after a CPU read-access of this register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used	**HK aborted (HIFI only)**	**Timeout (HIFI only)**	**HK pending (HIFI only)**	**Data ready**	**TX Busy**

Table 14: Lstatus register

The D3, D4 bits of the Lstatus register will be reset after a Lstatus reading cycle; in any case a new writing of the LTX register will reset the D1, D2, D3 of the same register.

In the board reset register a LSL reset flag clears whole the interface aborting every command sending, parameter waiting and clearing all the Lregisters.

7.4 32-bit bus Interface

The bus interface is implemented with buffer and transceiver devices, to match the bus electrical specifications and to be able to receive the following lines:

- ✓ 24 address lines
- ✓ 32 data lines
- ✓ 7 chip select lines (actives low)
- ✓ 1 read line (active low)
- ✓ 1 write line (active low)

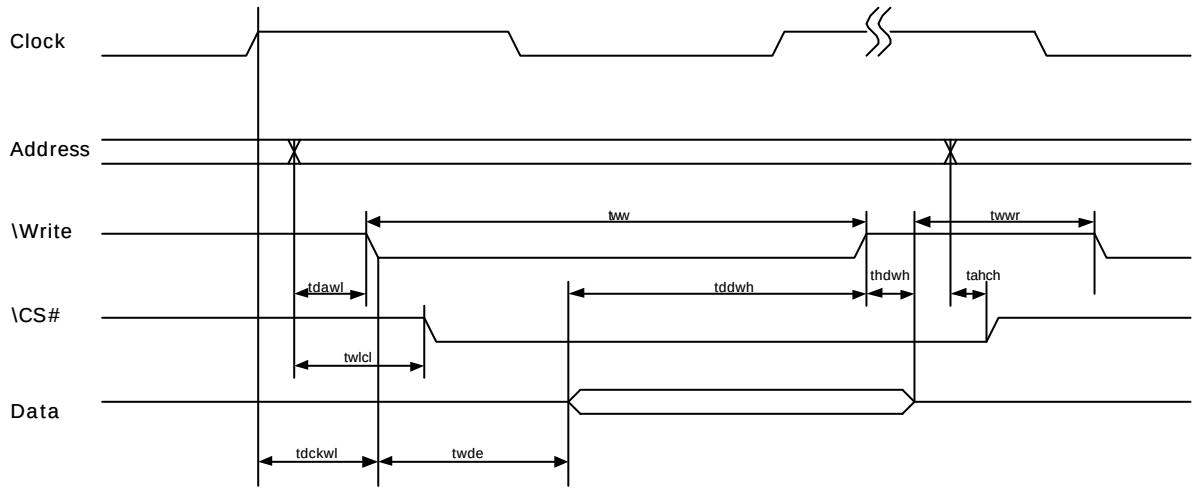
- ✓ 1 system clock (20MHz)
- ✓ 1 asynchronous reset line (active low)

The bus interface has to drive:

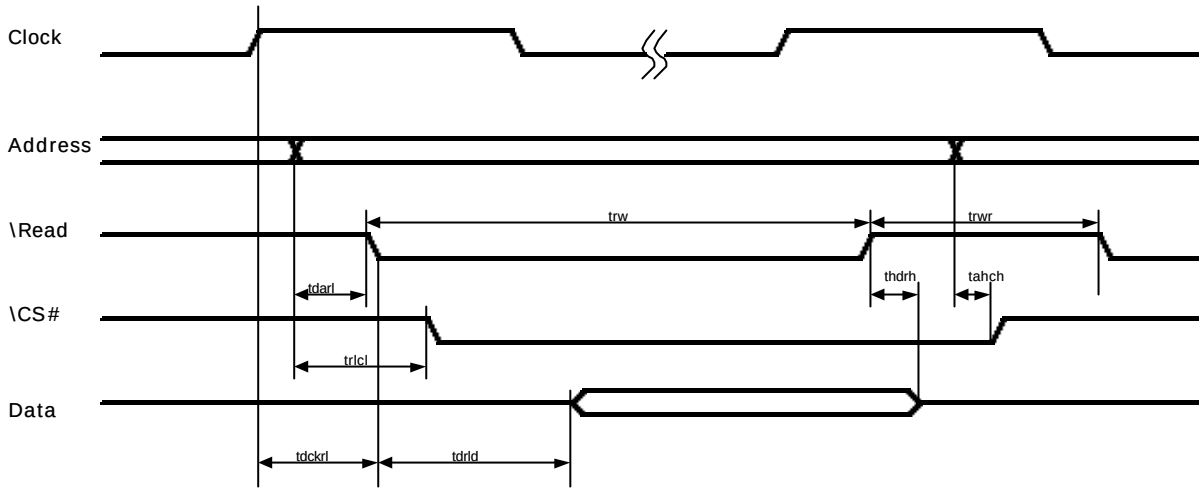
- ✓ 5 interrupt lines
- ✓ 32 data lines
- ✓ 1 acknowledge line (active high)

The timing of the bus is derived from the ADSP21020 data bus; the number of wait states, associated to each chip select, is reported in the [RD2]. The 32 bits shall be mapped in the bits D8-D39 of the DSP data bus.

The Picture 10 and Picture 11 show respectively, the write and read cycles for the peripherals on the bus space.



Picture 10: Bus write cycle



Picture 11: Bus read cycle

The timing values are reported in the [RD2].

For what concern the internal peripherals, the chip select lines, coming from the bus, manage them according to the following table:

\Chip select	Peripheral
0	FSDL 0
1	FSDL 1
2	FSDL 2
3	FSDL 3
4	Low Speed Link
5	Board Registers
6	Not used
7	MIL-STD-1553 Dual Port Ram (16KW)
7	MIL-STD-1553 Registers (see Table 6)
7	Analog Inputs (see Table 16)

Table 15: map of the board into the system bus space

In case of successive accesses to the same memory area (same chip select), the \CS lines remain asserted until a different memory area is addressed; this means that is not mandatory to have chip select signal edges on a bus cycle.

7.5 Analog Inputs

This section provides 8 single-ended, 0÷5V, not conditioned analog inputs, each one having 10KΩ 100pF RC filter.

7.5.1 ANALOG INPUT INTERFACES

The analog input interface is implemented with an ADC chain, composed by the following stages:

- ✓ 8 analog input channels, each one with a 10KΩ 100pF RC filter
- ✓ a 8-channel analog multiplexer (HS508) that selects the channel
- ✓ an amplifier implemented with a OP27 operational amplifier that adapts the signal to the ADC span
- ✓ an AD584 voltage reference that provides a high precision voltage reference to the ADC chain, allowing a reference for possible software compensation of errors (thermal drift, gain variations, ageing, offset and so on) and for calibration verification purposes
- ✓ an AD574, 12-bit, 35μs ADC that receives the start conversion signal from the control stage of the FPGA and, after about 35μs, provides a data ready signal to the FPGA
- ✓ a 12-bit latch, implemented on the FPGA, that stores the converted value until the CPU reading

7.5.2 SOFTWARE INTERFACE

The analog input stage is addressed by a dedicated chip select line of the system bus. The set of registers are showed in the following table:

Address	Register name	Size [bit]	Direction
0x8000	MSEL_reg	3	read/write
0x8001	MDATA_reg	13	read

Table 16: analog input registers

The MDATA_reg contains the 12-bit converted data and a "ready" flag (MSB) that indicates when the data is ready (active high).

By writing a multiplexer selection in the MSEL_reg, the multiplexer shall select the line to be converted and the control block shall manage the conversion, after a delay of about 15µs, for the stabilisation of the signal. When the conversion will finished (about 35µs conversion time), the "ready" bit of the MDATA_reg will assert and the converted value will be present in this register. After the reading, the MDATA_reg shall be reset by the control block of the FPGA.

The analog input #7 is reserved: a half scale voltage reference is connected to this input to provide a reference for the calibration phase.

7.6 Control Logic

The control logic is implemented with an Actel RH 1280 FPGA; it manages all the peripherals and realises the interface between the system bus and the peripherals.

7.6.1 BOARD REGISTERS

Address	Register name	Size [bit]	Direction
0x0	Reset register	32	read/write
0x1	Status register	32	read

Table 17: board registers

The reset register allows single peripheral resets (except for the control logic) and the global software reset (see paragraph 7.7). Each flag must be asserted (high) to generate a reset and it must be de-asserted (low) by another writing.

These flags are mapped, according to the following table:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SW reset	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	**LSL reset**	**MIL1553 reset**	**FSDL3 reset**	**FSDL2 reset**	**FSDL1 reset**	**FSDL0 reset**

Table 18: Reset register

The Status register reports all the status of the peripherals, the following table shows the map of the register:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ACQ3	FF3	HF3	EF3	ACQ2	FF2	HF2	EF2	ACQ1	FF1	HF1	EF1	ACQ0	FF0	HF0	EF0

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	1553 \INCMD	Ferr3	Ferr2	Ferr1	Ferr0

Table 19: Status register

7.7 Board Reset

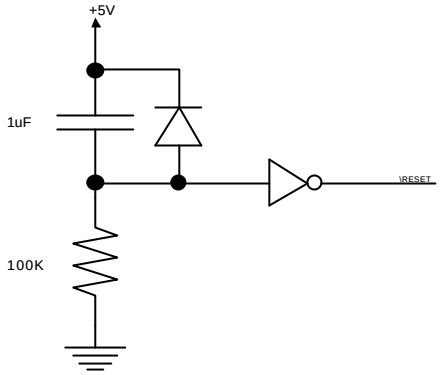
Three possible actions can globally reset the board:

1. power-on reset
2. hardware reset with the system reset line (\SYSRESETIN) driven by the CPU board
3. software reset, asserting the global reset bit in the reset register

When the CPU asserts the reset line (hardware reset) the whole board is reset (also the blocks of the FPGA control logic) whereas a software reset causes the reset of all the devices except for the control logic block.

7.7.1 POWER-ON RESET

The board is equipped with a power-on reset network to clear all the circuits at power-on.



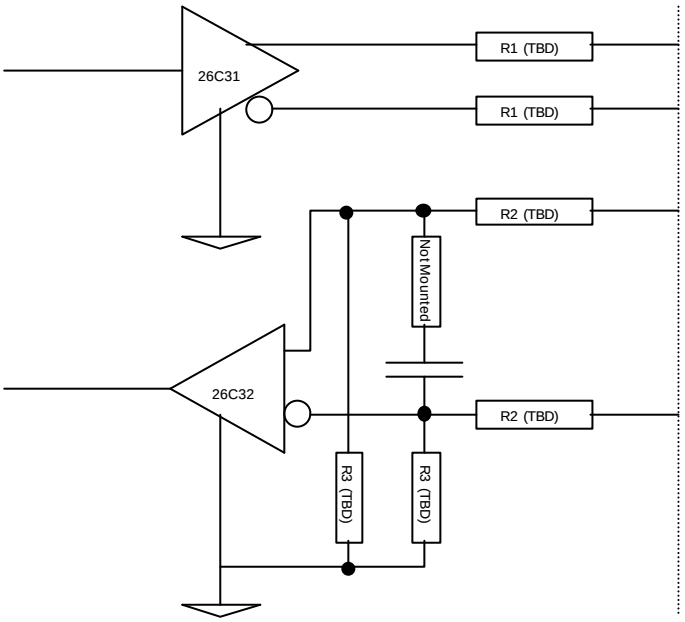
Picture 12: power-on reset network

7.8 Latchup Protection

Due to the high level of latchup immunity of the selected components (>100MeV/mg cm^2), no latchup protection is implemented on PL I/F board. Anyway, different supply sections are foreseen on the board itself, to increase flexibility of the current protection philosophy of the system. Actually, all the power supply sections are joined on the motherboard to supply the PL I/F board with single 5V, +15V -15V power lines.

8 ELECTRICAL INTERFACES

All the interfaces FSDL, and LSL are in RS422 electrical standard format. The interfaces employ balanced differential line drivers and receivers, type 26C31, 26C32, to provide good common mode rejection and reasonable isolation characteristics. In the Picture 13 are shown the driving and receiving networks:



Picture 13: RS422 electrical interface

The parasitic capacitance of the 26C32 input lines (to ground) shall be <20pF, this restricts the length of the PCB traces between the input resistors and the 26C32 inputs.

All the data have to be transferred with the MSB first.

9 PIN FUNCTION

The pin function of the PL I/F board is shown in the Table 20 and Table 21.

Pin #	Signal	Pin #	Signal	Pin #	Signal
1	+5VD	33	+5VD	65	+5VD
2	+VFIFO	34	+5VBU61582	66	+VFPGA
3	D0	35	D1	67	D2
4	D3	36	D4	68	D5
5	D6	37	D7	69	D8
6	D9	38	D10	70	D11
7	D12	39	D13	71	D14
8	D15	40	D16	72	D17
9	D18	41	D19	73	D20
10	D21	42	D22	74	D23
11	D24	43	D25	75	D26
12	D27	44	D28	76	D29
13	D30	45	D31	77	\WR
14	A0	46	A1	78	A2
15	A3	47	A4	79	A5
16	A6	48	A7	80	A8
17	DGND	49	SACK	81	DGND
18	A9	50	A10	82	A11
19	A12	51	A13	83	A14
20	A15	52	A16	84	A17
21	A18	53	A19	85	A20
22	A21	54	A22	86	A23
23	\CS0	55	\CS1	87	\CS2
24	\CS3	56	\CS4	88	\CS5
25	RESERVED	57	\CS7	89	\RD
26	IRQM3	58	IRQM4	90	IRQM5
27	IRQM6	59	IRQM7	91	SYSCLK
28	\SYSRESETIN	60	RESERVED	92	SYSCLK
29	-15VA	61	-15VA	93	-15VA
30	AGND	62	AGND	94	AGND
31	+15VA	63	+15VA	95	+15VA
32	DGND	64	DGND	96	DGND

Table 20 PL I/F board: P1 pin function

Pin #	Signal	Pin #	Signal	Pin #	Signal
1	+5VD	33	RESERVED	65	+5VD
2	FCK0+	34	FGATE0+	66	FDATA0+
3	FCK0-	35	FGATE0-	67	FDATA0-
4	FCK1+	36	FGATE1+	68	FDATA1+
5	FCK1-	37	FGATE1-	69	FDATA1-
6	FCK2+	38	FGATE2+	70	FDATA2+
7	FCK2-	39	FGATE2-	71	FDATA2-
8	FCK3+	40	FGATE3+	72	FDATA3+
9	FCK3-	41	FGATE3-	73	FDATA3-
10	AINP0	42	AINP1	74	AINP2
11	AGND	43	AGND	75	AGND
12	AINP3	44	AINP4	76	AINP5
13	AGND	45	AGND	77	AGND
14	AINP6	46	NOT USED	78	NOT USED
15	AGND	47	AGND	79	AGND
16	RTAD0	48	RTAD2	80	RTAD4
17	RTAD1	49	RTAD3	81	RTADP
18	LCK0+	50	LTX0+	82	LRX0+
19	LCK0-	51	LTX0-	83	LRX0-
20	LCK1+	52	LTX1+	84	LRX1+
21	LCK1-	53	LTX1-	85	LRX1-
22	LCK2+	54	LTX2+	86	LRX2+
23	LCK2-	52	LTX2-	84	LRX2-
24	LCK3+	53	LTX3+	85	NOT USED
25	LCK3-	54	LTX3-	86	NOT USED
26	LCK4+	58	LTX4+	90	SCTX/RXA+
27	LCK4-	59	LTX4-	91	SCTX/RXA-
28	LCK5+	60	LTX5+	92	SCTX/RXB+
29	LCK5-	61	LTX5-	93	SCTX/RXB-
30	LCK6+	62	LTX6+	94	NOT USED
31	LCK6-	63	LTX6-	95	FLAG1
32	DGND	64	DGND	96	DGND

Table 21 PL I/F board: P2 pin function