NOTES:

UTLVDS031,32
VDD: 16
VSS: 8

KEEP, R85-C39, R86-C40, R100-C42, R101-C43, R115-C45, R130-C48 AS NEAR AS POSSIBLE TO THE RESPECTIVE RECEIVER (UTLVDS032) MAX. 10mm OF PCB TRACE

PCB TRACES BETWEEN U20, U21, U22, U23, U24, U25 AND CONNECTOR P2 MUST BE AS SHORT AS POSSIBLE

+VSMCS
+VEEPROM
+5VD
DGND
A[0..18]
L0DI+ L0DI- L0SI+ L0SI- L1DI+ L1DI- L1SI+ L1SI- L2DI+ L2DI- L2SI+ L2SI- L3DI+ L3DI- L3SI+ L3SI- L4DI+ L4DI- L4SI+ L4SI- L5DI+ L5DI- L5SI+ L5SI-
R\D\ W\R\ → \RD \WR
R\E\S\E\T_\I\N\ → \RESET_IN
CLK → CLK
CLK10M → CLK10M
D\P\R_\C\S\0\ → \DPR_CS0
D\P\R_\C\S\1\ → \DPR_CS1
S\M\C\S_\C\S\ → \SMCS_CS
D\M\S\1\ → \DMS1
E\E_\C\S\[0..3] → \EE_CS[0..3]
E\E_\W\R\ → \EE_WR
E\E_\R\D\ → \EE_RD
S\T\D_\B\U\F_\E\N → \STD_BUF_EN
D0EN D1EN D2EN → D0EN D1EN D2EN

U20
L0DIR- L0DIR+ L0DI L0SI L0SIR+ L0SIR-
RIN1- RIN1+ ROUT1 EN ROUT2 RIN2+ RIN2-
RIN4- RIN4+ ROUT4 EN ROUT3 RIN3+ RIN3-
L1DIR- L1DIR+ L1DI L1SI L1SIR+ L1SIR-
DGND

U22
L2DIR- L2DIR+ L2DI L2SI L2SIR+ L2SIR-
RIN1- RIN1+ ROUT1 EN ROUT2 RIN2+ RIN2-
RIN4- RIN4+ ROUT4 EN ROUT3 RIN3+ RIN3-
L3DIR- L3DIR+ L3DI L3SI L3SIR+ L3SIR-
DGND

U25
L4DIR- L4DIR+ L4DI L4SI L4SIR+ L4SIR-
RIN1- RIN1+ ROUT1 EN ROUT2 RIN2+ RIN2-
RIN4- RIN4+ ROUT4 EN ROUT3 RIN3+ RIN3-
L5DIR- L5DIR+ L5DI L5SI L5SIR+ L5SIR-
DGND

U21
+5VD R52
L0DO L0DOR+ L0DOR- D0EN L0SOR- L0SOR+ L0SO
DIN1 DOUT1-DOUT4+ EN DOUT2-DOUT3- DIN2
DIN4 DOUT1+DOUT4- EN DOUT2+DOUT3+ DIN3
L3DO L3DOR+ L3DOR- L3SOR- L3SOR+ L3SO
+5VD

U23
+5VD R60
L1DO L1DOR+ L1DOR- D1EN L1SOR- L1SOR+ L1SO
DIN1 DOUT1-DOUT4+ EN DOUT2-DOUT3- DIN2
DIN4 DOUT1+DOUT4- EN DOUT2+DOUT3+ DIN3
L4DO L4DOR+ L4DOR- L4SOR- L4SOR+ L4SO
+5VD

U24
+5VD R76
L2DO L2DOR+ L2DOR- D2EN L2SOR- L2SOR+ L2SO
DIN1 DOUT1-DOUT4+ EN DOUT2-DOUT3- DIN2
DIN4 DOUT1+DOUT4- EN DOUT2+DOUT3+ DIN3
L5DO L5DOR+ L5DOR- L5SOR- L5SOR+ L5SO
+5VD

+5VD R79 L0DI+ R82 L0DIR+ C39 R85 L0DI- R88 L0DIR- R91 DGND
+5VD R80 L2DI+ R83 L2DIR+ C40 R86 L2DI- R89 L2DIR- R92 DGND
+5VD R81 L4DI+ R84 L4DIR+ C41 R87 L4DI- R90 L4DIR- R93 DGND
+5VD R94 L0SI+ R97 L0SIR+ C42 R100 L0SI- R103 L0SIR- R106 DGND
+5VD R95 L2SI+ R98 L2SIR+ C43 R101 L2SI- R104 L2SIR- R107 DGND
+5VD R96 L4SI+ R99 L4SIR+ C44 R102 L4SI- R105 L4SIR- R108 DGND
+5VD R109 L1DI+ R112 L1DIR+ C45 R115 L1DI- R118 L1DIR- R121 DGND
+5VD R110 L3DI+ R113 L3DIR+ C46 R116 L3DI- R119 L3DIR- R122 DGND
+5VD R111 L5DI+ R114 L5DIR+ C47 R117 L5DI- R120 L5DIR- R123 DGND
+5VD R124 L1SI+ R127 L1SIR+ C48 R130 L1SI- R133 L1SIR- R136 DGND
+5VD R125 L3SI+ R128 L3SIR+ C49 R131 L3SI- R134 L3SIR- R137 DGND
+5VD R126 L5SI+ R129 L5SIR+ C50 R132 L5SI- R135 L5SIR- R138 DGND

D[0..31] → D[0..31]
\IRQ0 → \I\R\Q\0\
\IRQ1 → \I\R\Q\1\
L0DOR+ L0DOR- L0SOR+ L0SOR- L1DOR+ L1DOR- L1SOR+ L1SOR- L2DOR+ L2DOR- L2SOR+ L2SOR- L3DOR+ L3DOR- L3SOR+ L3SOR- L4DOR+ L4DOR- L4SOR+ L4SOR- L5DOR+ L5DOR- L5SOR+ L5SOR-
R53 R54 R55 R56 R57 R58 R59 R61 R62 R63 R64 R65 R66 R67 R68 R69 R70 R71 R72 R73 R74 R75 R77 R78
L0DO+ L0DO- L0SO+ L0SO- L1DO+ L1DO- L1SO+ L1SO- L2DO+ L2DO- L2SO+ L2SO- L3DO+ L3DO- L3SO+ L3SO- L4DO+ L4DO- L4SO+ L4SO- L5DO+ L5DO- L5SO+ L5SO-
ACK → STDACK
\BUSY0 \BUSY1 → B\U\S\Y\0\ B\U\S\Y\1\
\SES0 \SES1 \SES2 \SES3 → S\E\S\0\ S\E\S\1\ S\E\S\2\ S\E\S\3\
\RESET_OUT → S\M\C\S_\R\E\S\E\T_\O\U\T\
L0EN L1EN L2EN → L0EN L1EN L2EN
DMSPARE[0..3] → DMSPARE[0..3]

P3
A[0..18] A0 A1 A2 A3 A4 A5 A6 A7 A8 +VSMCS A9 A10 A11 A12 A13 A14 A15 A16 A17 A18
D[0..31] D29 D30 D31 \DMS1 \RD \WR \RESET_IN CLK ACK \STD_BUF_EN
\IRQ0 \IRQ1 D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 +VEEPROM D19 D20 D21 D22 D23 D24 D25 D26 D27 D28
D[0..31]
DGND
AMP 536280-2

P4
\EE_CS[0..3]
\EE_CS0 \EE_CS1 \EE_CS2 \EE_CS3 \EE_WR \EE_RD L0DI L0SI L1DI L1SI L2DI L2SI L3DI L4DI L4SI L5DI L5SI \BUSY0 \BUSY1 \DPR_CS0 \DPR_CS1 \SMCS_CS \RESET_OUT CLK10M
DMSPARE0 DMSPARE1 DMSPARE2 DMSPARE3 L0DO L0SO L1DO L1SO L2DO L2SO L3DO L3SO L4DO L4SO L5DO L5SO \SES0 \SES1 \SES2 \SES3 L0EN L1EN L2EN L3EN L4EN L5EN
DMSPARE[0..3]
+5VD
DGND
AMP 536280-2

UTLVDS031,32
1 capacitor
each
+VEEPROM C51 DGND
VDD +5V C52 C53 C54 C55 C56 C57 VSS VSS GND DGND

REV.	DATE	DRAWN	CHECK	ENG.	PR.ASS	C. of C.	CHANGE AUTORITY
/							

CUSTOMER ID
EFFECTIVITY
CARLO GAVAZZI SPACE
DRAWING TITLE
HSO/FIRST-DPU
CPU BOARD
DM Mezzanine I/F
SCALE
GEN. TOL.
GEN. RA
HIGHER ASSEMBLY: DPU-EM-110.000
DRAWING NUMBER: DPU-EM-110.020
SHEET OF: 5 8