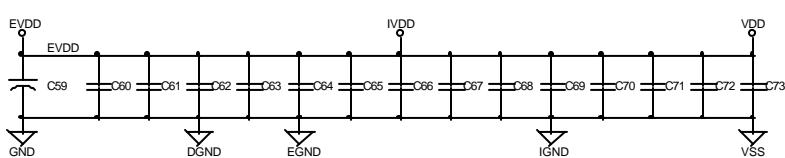
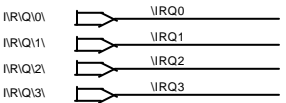
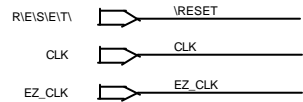
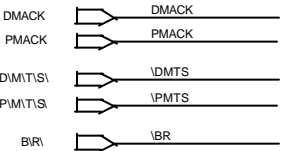
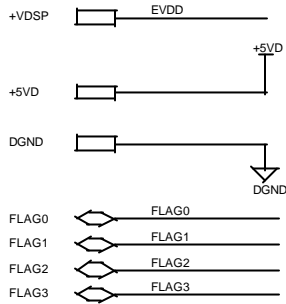
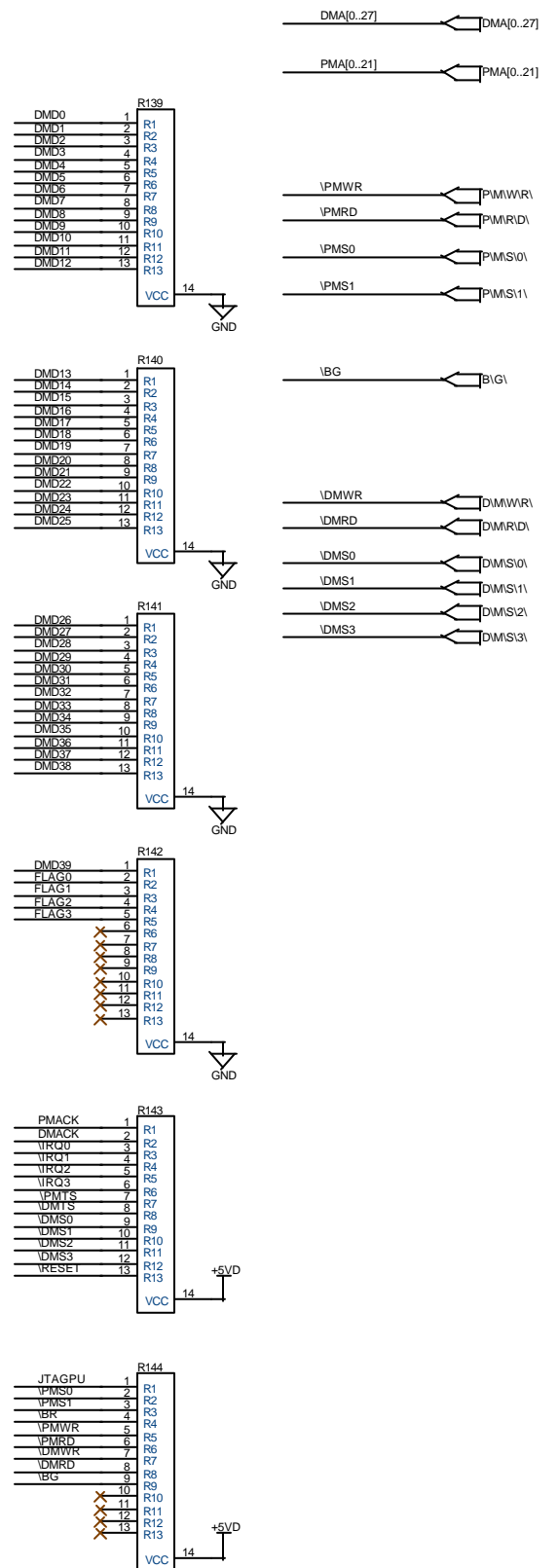
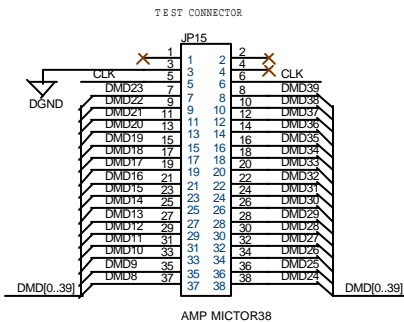
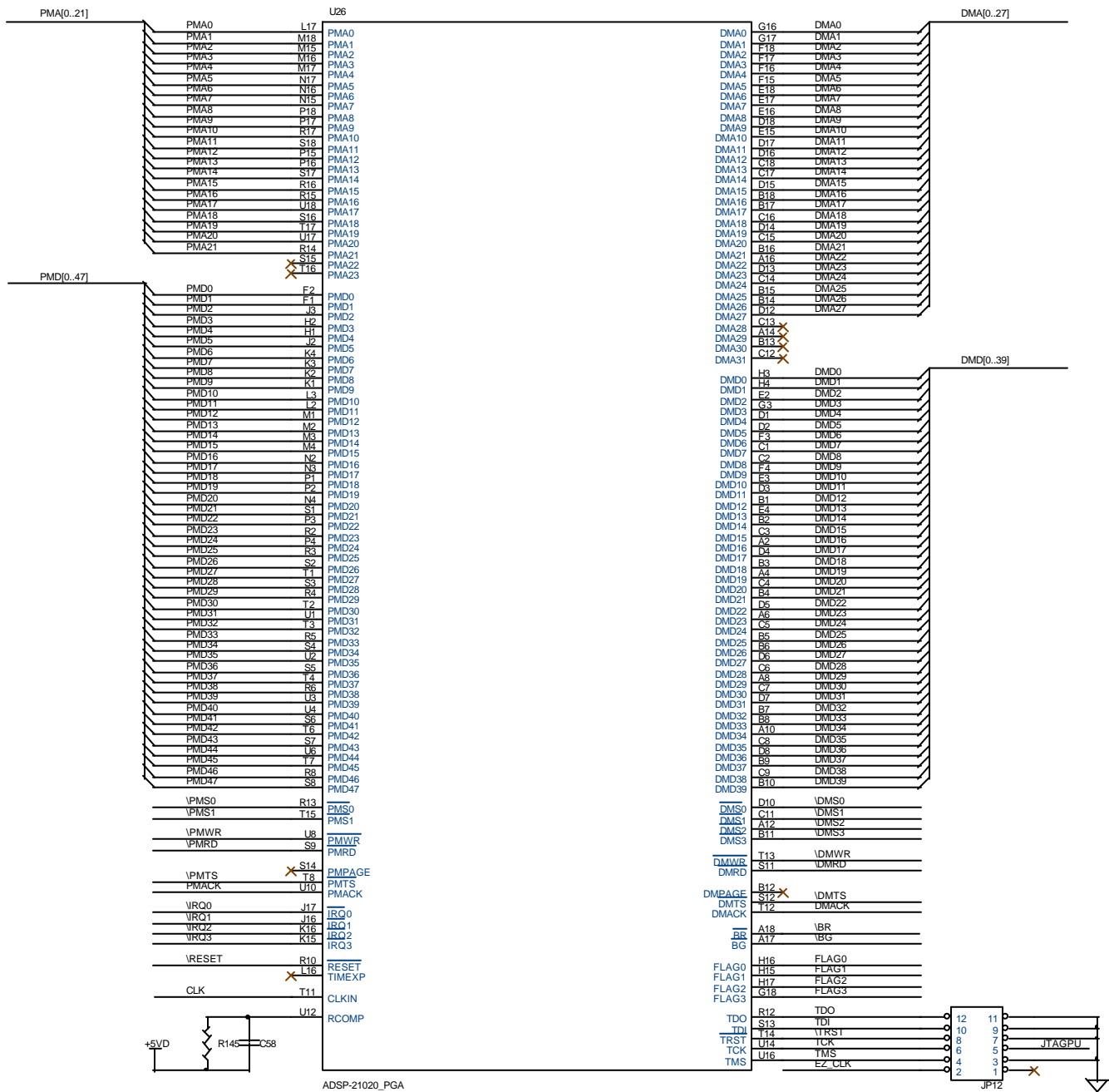


NOTES:
ADSP21020
EVDD: A5, A9, A13, J1, J18, N1, N18, U9, U13, K18
IVDD: D9, J4, J15, R9
EGND: H18, A3, A7, A11, A15, E1, G1, L1, L18, R1,
R18, T18, U5, U7, U11, U15
IGND: D11, G4, L4, L15, R7, R11

ADSP21020
IT MUST BE POWERED BY +VCORE LINE



FILTER CAPACITORS:
DSP: 1 capacitor near each IVDD and EVDD pin



/							
REV.	DATE	DRAWN	CHECK	ENG.	FRASS	C.d.C.	CHANGE AUTHORITY
CUSTOMER				EFFECTIVITY		CARLO GAVAZZI SPACE	
DRAWING TITLE HSO/FIRST-DPU CPU BOARD DSP_FGA				SCALE		GEN. TEST. RA	
HIGHER ASSEMBLY DPU-EM-110.00-0				DRAWING NUMBER DPU-EM-110.020		SHEET OF 6 8	