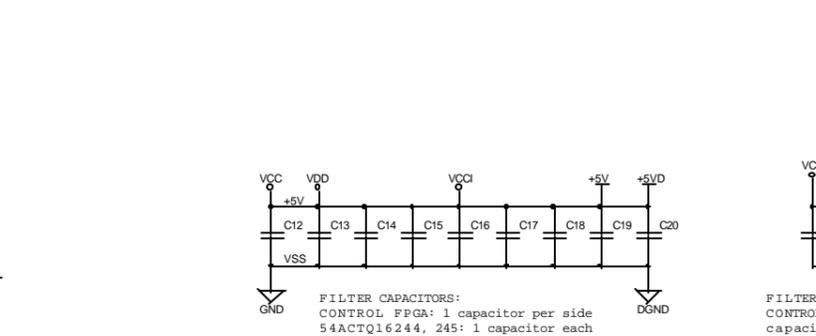
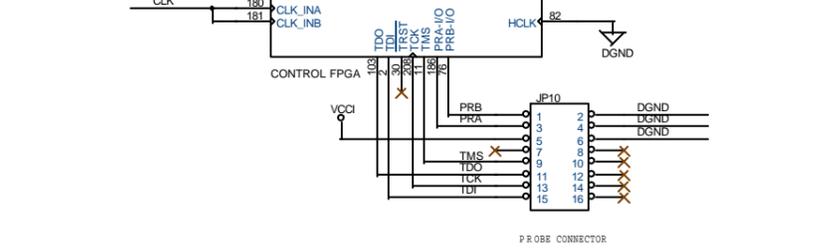
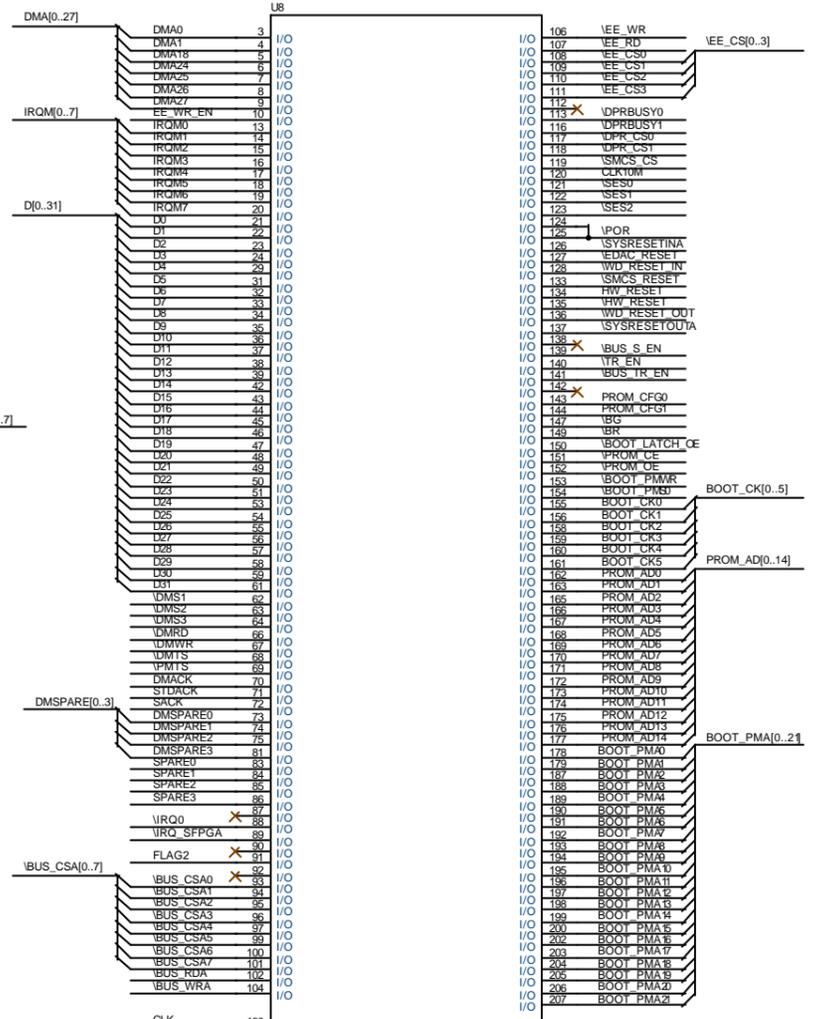
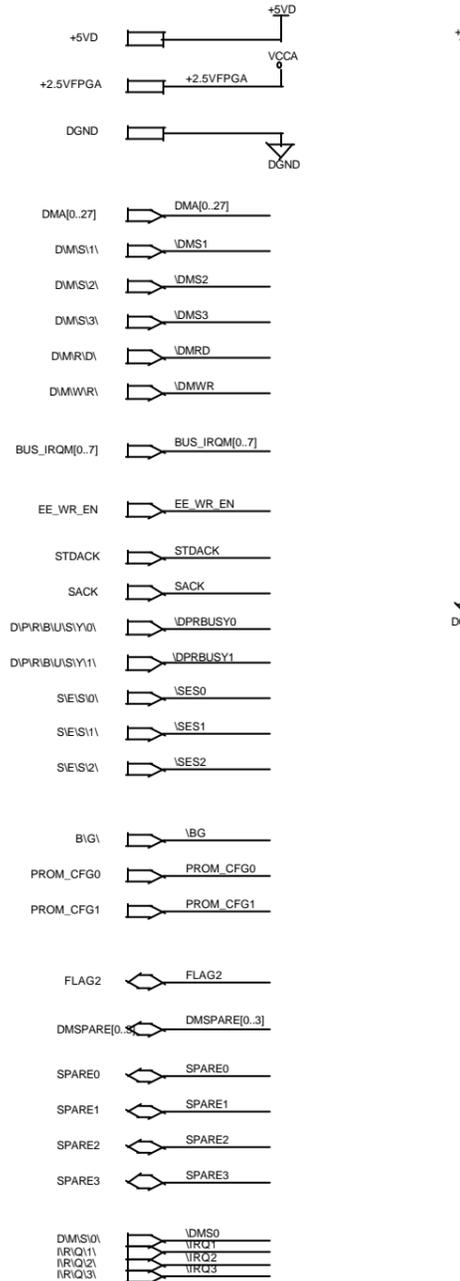
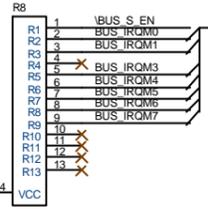
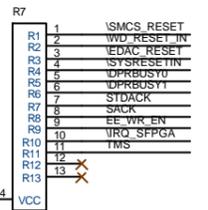


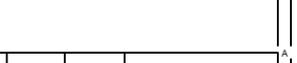
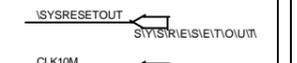
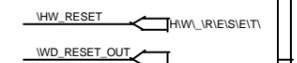
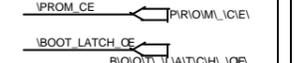
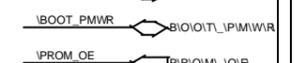
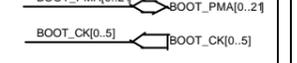
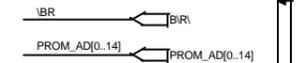
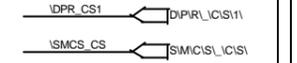
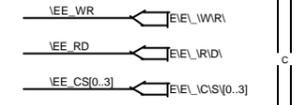
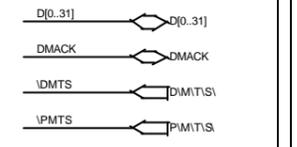
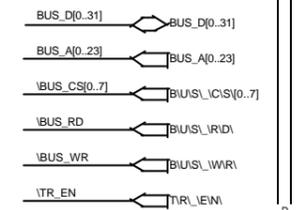
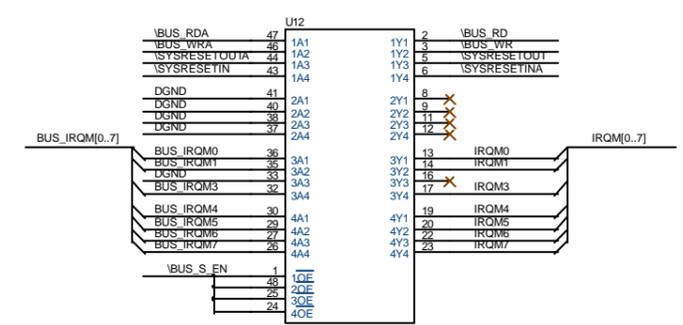
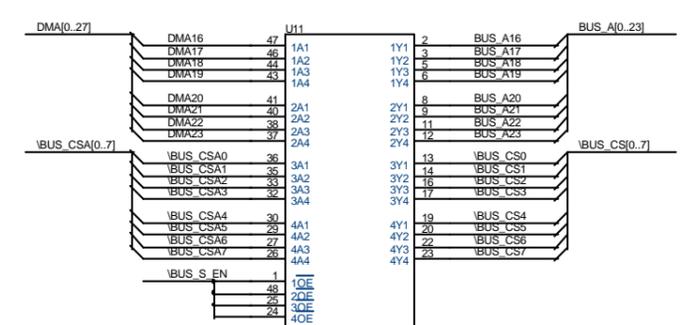
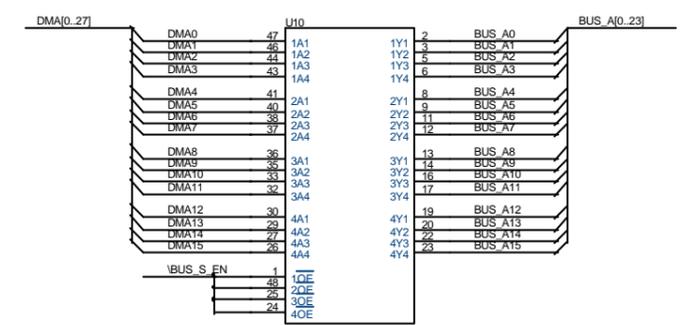
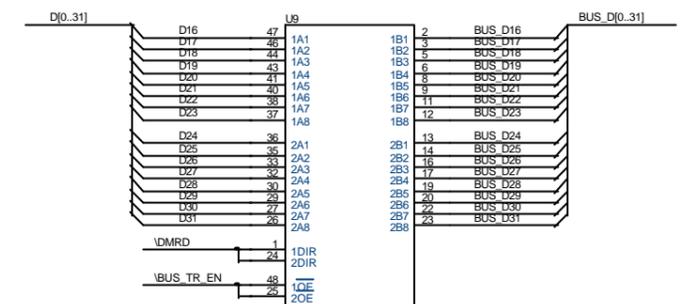
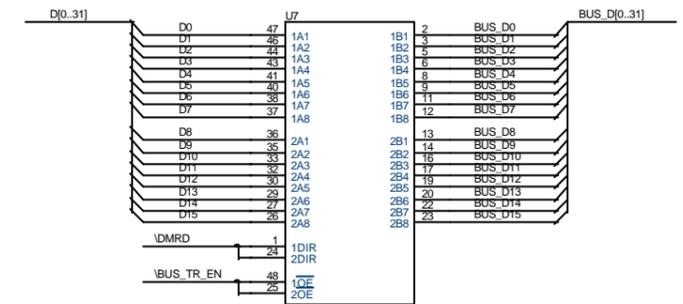
NOTES:
 54ACTQ16244/245
 VCC: 7, 18, 31, 42
 GND: 4, 10, 15, 21, 28, 34, 39, 45

KEEP THE PROBE CONNECTOR AS NEAR AS POSSIBLE TO THE CONTROL FPGA

CONTROL FPGA (RT54S32S)
 VCCI (+5V): 12, 40, 60, 98, 115, 148, 164, 201
 VCCA (+2.5VFPGA): 27, 41, 78, 114, 130, 145, 184
 GND: 1, 26, 28, 52, 77, 79, 105, 129, 131, 146, 157, 183, 185



FILTER CAPACITORS:
 CONTROL FPGA: 1 capacitor per side
 54ACTQ16244, 245: 1 capacitor each



REV.	DATE	DRAWN	CHECK	ENG.	FRASS	C. d.C.	CHANGE/REVISION
CUSTOMER				EFFECTIVITY		CARLO GAVAZZI SPACE	
DRAWING TITLE						SCALE	GEN. REL.
HSO/FIRST-DPU						GEN. REL.	GEN. REL.
CPU BOARD						CARLO GAVAZZI	
Control Block							
HIGH-ASSEMBLY				DRAWING NUMBER		SHEET OF	
DPU-EM-110.000				DPU-EM-110.020		3 8	