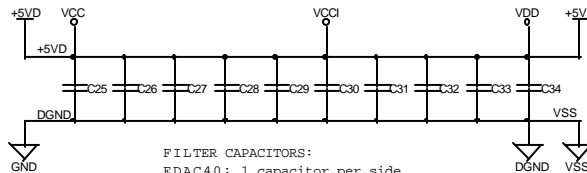
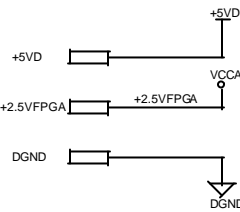


NOTES:

UT9Q512
VDD: 9, 27
VSS: 10, 28
NC: 19, 36

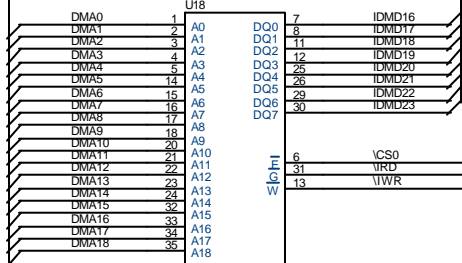
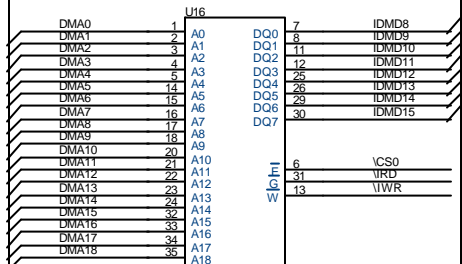
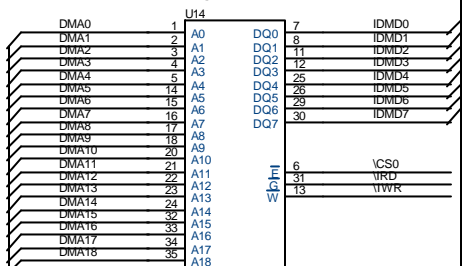
KEEP THE PROBE
CONNECTOR AS NEAR
AS POSSIBLE TO THE
CONTROL FPGA

EDAC40 (RT54SX32S)
VCCI (+5V): 12, 40, 60, 98, 115,
148, 164, 201
VCCA: (+2.5VFPGA): 27, 41, 78, 114,
130, 145, 184
GND: 1, 26, 28, 52, 77, 79, 105,
129, 131, 146, 157, 183, 185

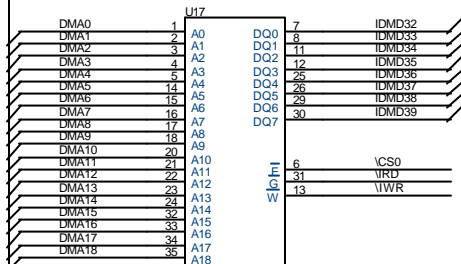
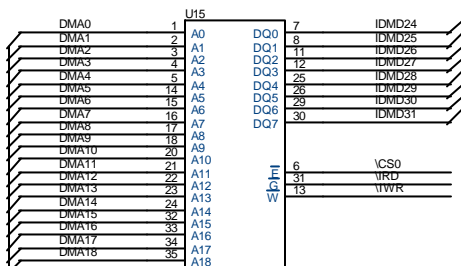


FILTER CAPACITORS:
EDAC40: 1 capacitor per side
UT9Q512: 1 capacitor each

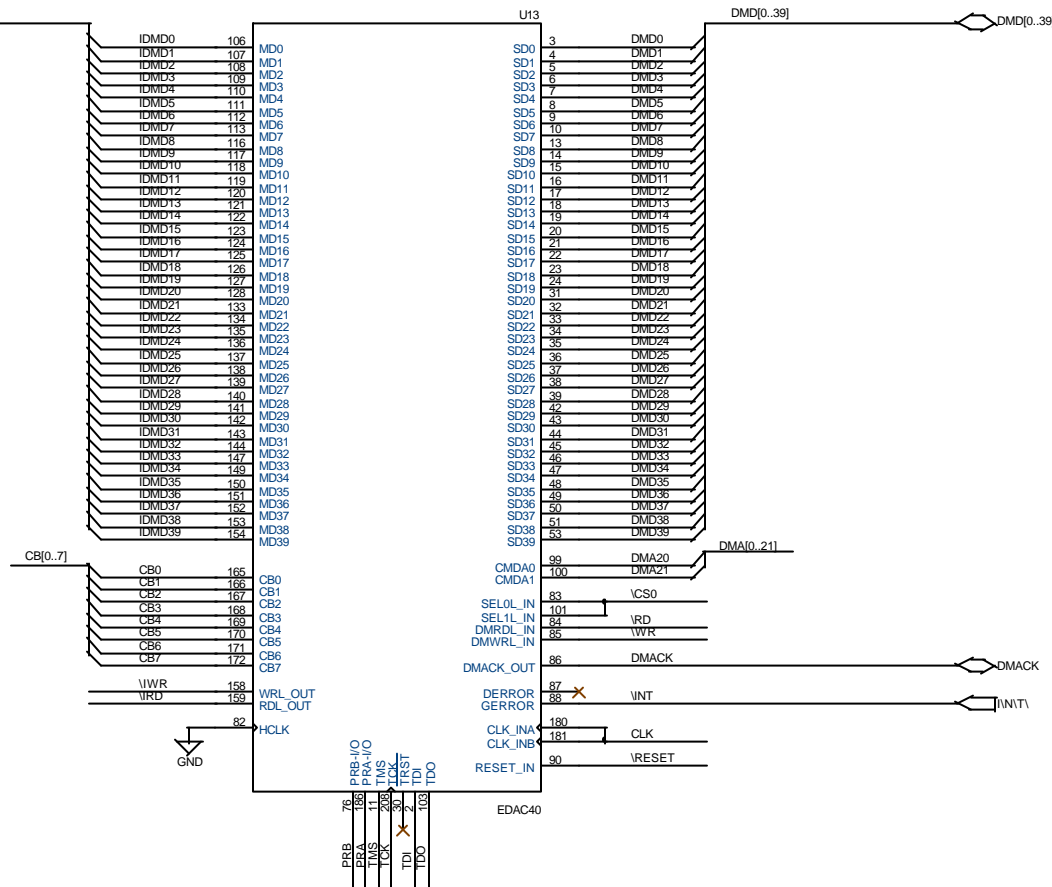
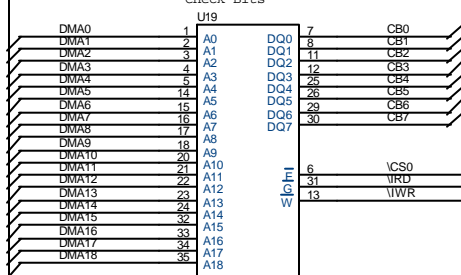
Bench for Extended
Floating Point



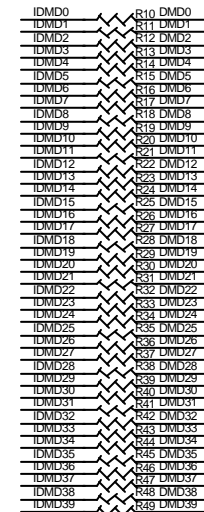
IDMD[0..39]



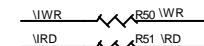
Bench for EDAC
Check Bits



If EDAC is present, do
not mount



If EDAC is present, do
not mount



REV	DATE	DRAWN	CHECK	ENG	FRASE	C.d.C.	CHANGEAURITY
CUSTOMER				EFFECTIVITY		CARLO GAVAZZI SPACE	
DRAWING TITLE				SCALE		GEN. TOL. GEN. FA.	
HIGHER ASSMBLY				DRAWING NUMBER		SHEET OF	
DPU-EM-110.00-0				DPU-EM-110.020		4 8	