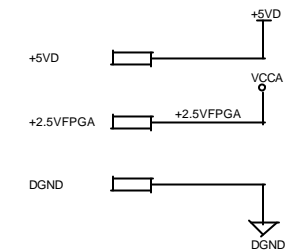


NOTES:

UT9Q512
VDD: 9, 27
VSS: 10, 28
NC: 19, 36

KEEP THE PROBE
CONNECTOR AS NEAR
AS POSSIBLE TO THE
CONTROL FPGA

EDAC48 (RT54SX32S)
VCCI (+5V): 12, 40, 60, 98, 115,
148, 164, 201
VCCA: (+2.5VFPGA): 27, 41, 78, 114,
130, 145, 184
GND: 1, 26, 28, 52, 77, 79, 105,
129, 131, 146, 157, 183, 185



WRI WVR

RDI VRD

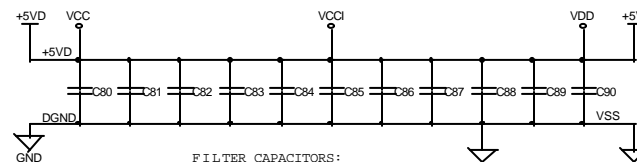
CS0A VCS0

CS1A VCS1

CLK CLK

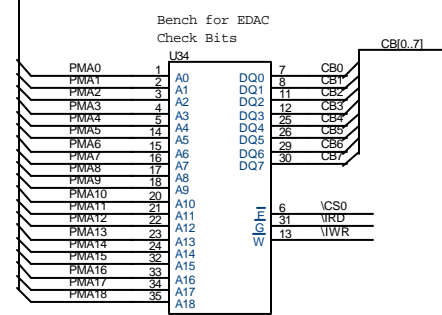
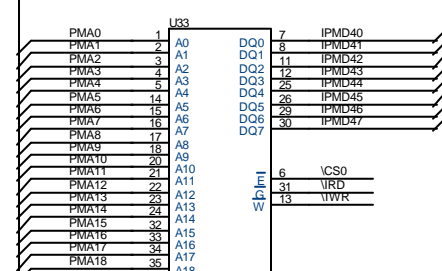
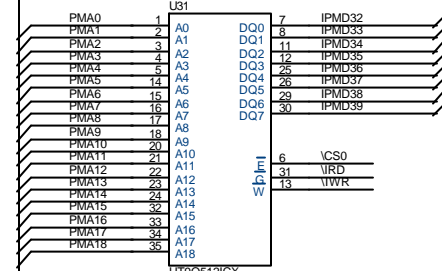
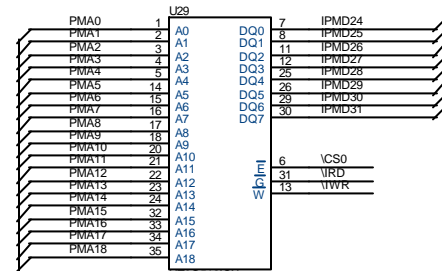
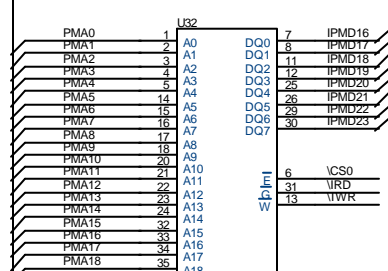
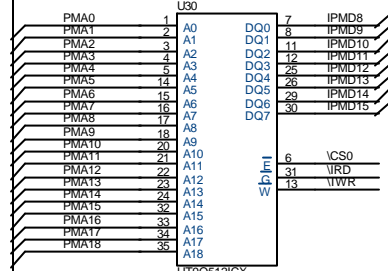
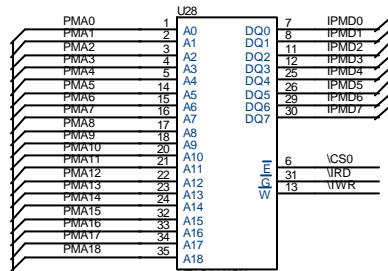
R/E/S/E/T VRESET

PMA[0..21] PMA[0..21]



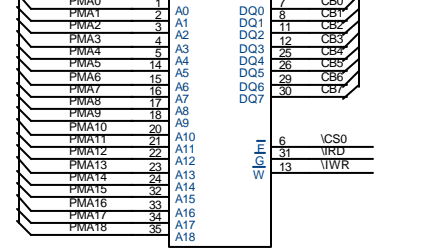
FILTER CAPACITORS:
EDAC48: 1 capacitor per
side
UT9Q512: 1 capacitor each

IPMD[0..47]

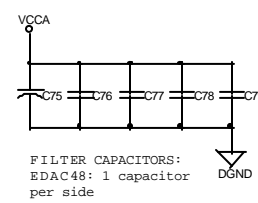


Bench for EDAC
Check Bits

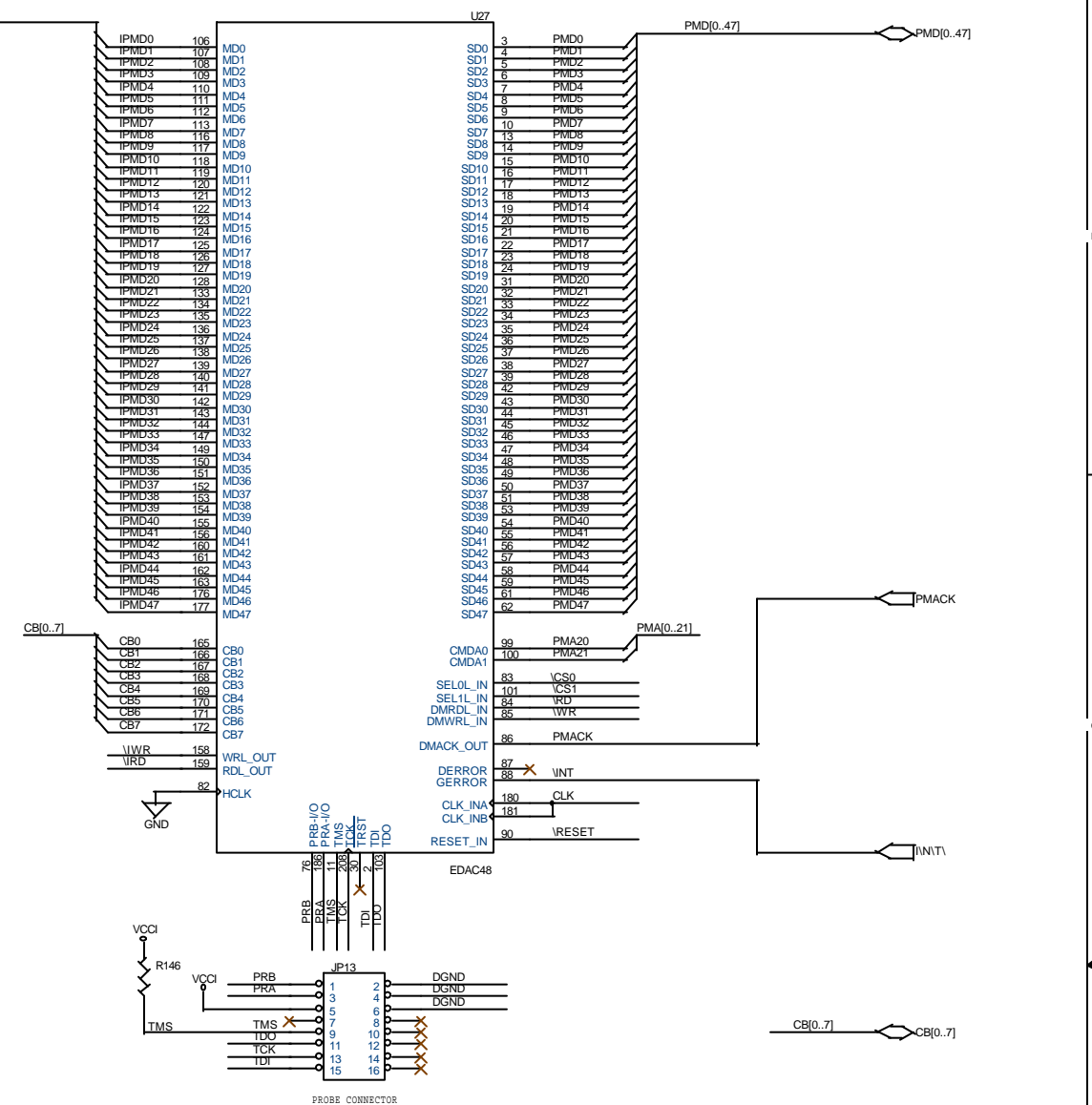
U34



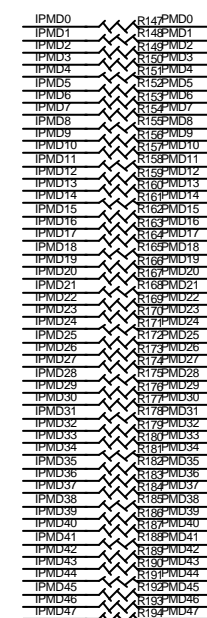
UT9Q512ICX NOT MOUNTED



FILTER CAPACITORS:
EDAC48: 1 capacitor
per side



If EDAC is present, do
not mount



WVR R189WR
VRD R189RD
If EDAC is present, do
not mount

REV.	DATE	DRAWN	CHECK	ENG.	FRASS	C. d.C.	CHANGE AUTHORITY
/							
CUSTOMER				EFFECTIVITY			
DRAWING TITLE				SCALE			
HSO/FIRST-DPU				GEN. TEL.			
CPU BOARD				GEN. RA			
Program Memory							
HIGHER ASSEMBLY				DRAWING NUMBER			
DPU-EM-110.000				DPU-EM-110.020			
				SHEET OF			
				8 8			