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1 LIST OF ACRONYMS

AD#	Applicable Document Number
BB	Broadband
CE	Conducted Emission
CS	Conducted Susceptibility
DPU	Data Processing Unit
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
FIRST	Far Infra-Red and Sub-millimeter Telescope
FPU	Focal Plane Unit
GND	Ground
HIFI	Heterodyne Instrument for First
HK	House Keeping
ICD	Interface Control Document
ICU	Instrument Control Unit
IID	Instrument Interface Document
I/F	Interface
LCL	Latching Current Limiter
OCP	Over-Current Protection
OVP	Over-Voltage Protection
NA	Not Applicable
NB	Narrowband
PA	Product Assurance
PACS	Photoconductor Array Camera and Spectrometer
PDU	Power Distribution Unit
PL	Payload
RD#	Reference Document Number
RE	Radiated Emission
RS	Radiated Susceptibility
RTN	Return Line
S/C	Spacecraft
SPIRE	Spectral and Photometric Imaging receiver
TBC	To Be Confirmed
TBD	To Be Determined
TM/TC	Telemetry & Tele-command

2 SCOPE

Scope of this document is to define the general requirements of the DC/DC board which shall be used to supply the Data Processing Unit (DPU) of the Payload Instruments HIFI, PACS and SPIRE to be developed in the framework of the FIRST program.

For the payload experiment HIFI only, the DC/DC board, besides the supply of the DPU, shall provide supplying voltages for the HIFI instrument itself. In this case the DC/DC board shall be called, in this document, as “DPU+PL version”.

The DC/DC board devoted to supply the DPU unit only, shall be called, in this document, as “DPU version”.

The design of the DC/DC board shall be compliant to this document.

3 DOCUMENTS

The following documents were utilized to write this document:

3.1 Applicable Documents

[AD1]: CNR.IFSI.2000TR01 "Documento di Specifiche Tecniche per il Contratto delle Data Processing Units del Satellite First dell'ESA" IFSI (Issue: 1 - 15/09/2000)

[AD2]: Technical proposal CGS (Ref. S9-030 November 99)

[AD3]: “Allegato Tecnico al Contratto ASI"

[AD4]: Product Assurance Plan for the FIRST DPU (DPU-PL-CGS-001 Issue 1 Jan. 2001)

3.2 Reference Documents

[RD1] - FIRST/Planck Instrument Interface Document Part A. (Ref. SCI-PT-IIDA-04624 Issue-Rev. No. : 1/1)

[RD2] - FIRST/Planck Instrument Interface Document Part B - Instrument “HIFI” (Ref. SCI-PT-IIDB/HIFI-02125 Issue-Rev No. : 1/0)

4 MECHANICAL CONSTRAINTS

The DC/DC board shall be located within the DPU.
The DC/DC board is implemented through one Printed Circuit Board.
The mechanical constraints are specified in Table 4-1; the weight of the overall board is specified in Table 4-2

Size (DPU+PL version)	Double Euro (160mm x 233.35mm)
Size (DPU version)	Double Euro (160mm x 233.35mm)
Overall thickness: (both versions)	38mm
Card retainers:	Calmark series 260
Connectors (connection to back plane):	90°, male, DIN41612 type

Table 4-1 Board constraints

Overall Weight (DPU+PL version)	≈1000gr TBC
Overall Weight (DPU version)	≈750gr TBC

Table 4-2 Board weight

5 ENVIRONMENTAL CONSTRAINTS

The DC/DC board shall be designed to be compatible with the environmental constraints summarized in the following Table 5-1 and to survive the limit mechanical environment at DPU box interface described in Table 5-2:

Board operating temperature:	-25 ÷ +45 °C
Board non operating temperature:	-35 ÷ +85 °C
Total dose:	≤ 10 Krad

Table 5-1 Thermal and radiation Environmental constraints

Random environment for each perpendicular axis	
Freq	level g^2/Hz
10	0.02
100	0.15
300	0.15
2000	0.001
	8gRMS (70 sec)
Quasistatic environment	
Quasistatic environment for in plane axes	1.6 [g]
Quasistatic environment for out of plane axis	6.8 [g]

Table 5-2 Limit Mechanical environmental constraints at DPU box interface

Note: The above mentioned temperature ranges are valid only if components with appropriate extended temperature range are utilized.
Note: the above mentioned limit loads at box interface are valid for a DPU box first global frequency >120 Hz.

6 FUNCTIONAL REQUIREMENTS

The DC/DC board must provide a set of supply voltages for to the DPU internal electronics of the payload experiments HIFI, PACS and SPIRE. For the payload experiment HIFI only, the DC/DC board must provide a further external set of supply voltages for the HIFI/FCU unit.

Therefore the board must provide, considering the DPU+PL version, the following two sets of output voltages:

⇒ "DPU-Outputs" to supply the DPU internal electronics

⇒ "PL-Outputs" to supply the payload instrument HIFI/FCU unit.

The PL-Outputs shall be divided in two types of outputs; the first type are regulated outputs while the second type are unregulated outputs.

In the DPU version only the DPU-Outputs shall be provided.

DPU-Outputs and PL-Outputs shall be isolated from primary power side and from each other as described in paragraph 9.

The input power line voltage (28V) shall be distributed by the S/C PDU through a Latching Current Limiter (LCL).

The switching frequency of the power cell/cells shall be synchronized with an external signal.

The DC/DC board shall switch on automatically when the input voltage is within the range established in Table 8-1.

In Figure 6-1 the DC/DC board functional diagram is shown (DPU+PL version).

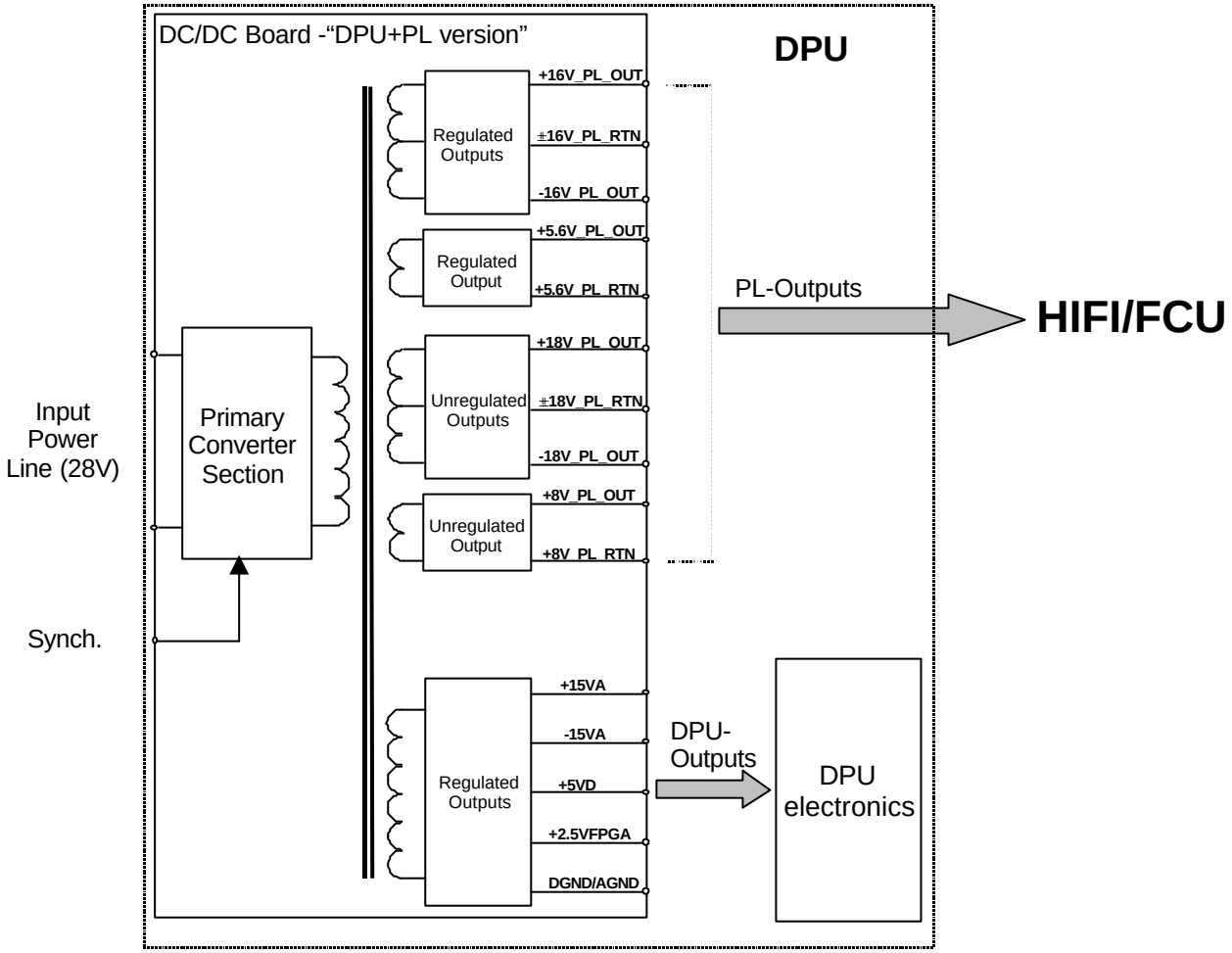

Figure 6-1 DC/DC Board functional diagram ("DPU+PL version")

7 OUTPUT ELECTRICAL REQUIREMENTS

Maximum overall output power of the DC/DC board in the DPU+PL version shall be 44 W ± 20%.
Maximum overall output power of the DC/DC board in the DPU version shall be 23W ± 20%.

The conversion efficiency shall be at least 70% at maximum output power.
Power from the DC/DC board to the HIFU/FCU unit will be switched by devices mounted into the FCU. Therefore the DC/DC board (with reference to the "DPU+PL version") shall be designed taking into account voltage transients / load variations that can arise from the ON/OFF switching of downstream loads.

7.1 DPU-Outputs Requirements

The DPU-Outputs are regulated and the electrical requirements are reported in the following Table 7-1:

Output	V_{min} [V]	V_{max} [V]	I_{min} [mA]	I_{max} [mA]	Ripple [mV_{PP}]	Spikes [mV_{PP}]
+5VD	4.75	5.25	1000	3500	200	100
+15VA	14.25	15.75	TBD	100	400	200
-15VA	-15.75	-14.25	TBD	250	400	200
+2.5VFPGA	2.375	2.625	TBD	200	200	100

Table 7-1 DPU-Outputs Requirements

V_{min} is the minimal output voltage delivered when the outlet is loaded with a current in the range from I_{min} to I_{max}.
V_{max} is the maximal output voltage delivered when the outlet is loaded with a current in the range from I_{min} to I_{max}.
I_{min} is the minimum continuous load current for which the output voltage shall be in the range from V_{min} and V_{max}.
I_{max} is the maximum continuous load current for which the output voltage shall be in the range from V_{min} and V_{max}.
Ripple and spikes shall be measured with a representative dummy load, the dummy load shall sink a DC load current of I_{max} in parallel with a 20µF capacitance in series with a 10Ω resistance. Spikes measurements shall be performed with a 50MHz BW Oscilloscope. For ripple measurements, a 2MHz BW limitation shall be introduced. Measurements shall be performed in differential mode.
In the following Figure 7-1 the meaning of ripple and spikes peak to peak envelopes is shown.

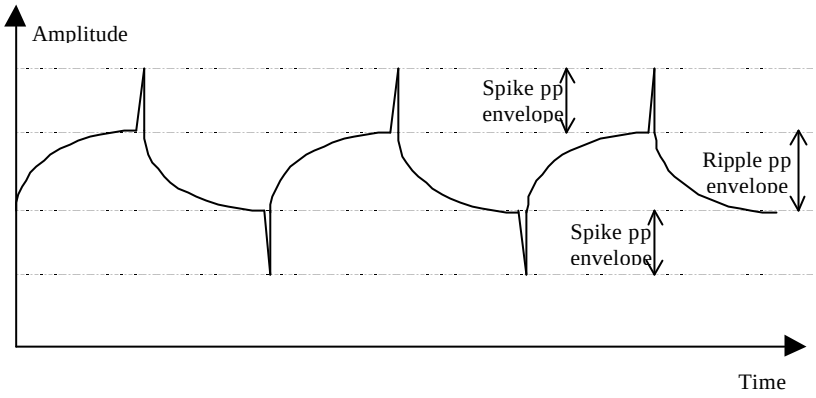

Figure 7-1

To simulate the inrush current of the load connected to each DPU-Output a 100µF capacitor with no significant series impedance can be used.

7.1.1 DPU-Outputs Protections

The following protections shall be implemented on the DC/DC board DPU-outputs:

⇒ Over-voltage protection (OVP) on, +5VD outlet. (Set at 5.5V TBC)
⇒ Over-current protection on +5VD, +15VA and -15VA outlets as reported in the following Table 7-2:

Outlet	Threshold Current [mA]
+5VD	4000±10% TBC
+15VA	200±10% TBC
-15VA	500±10% TBC

Table 7-2

Each protection intervention will shutdown the DC/DC board.

7.2 PL-Outputs Requirements

7.2.1 Regulated PL-Outputs Requirements

In the following Table 7-3 the electrical requirements of the Regulated PL-Outputs are reported:

Output	V_{min} [V]	V_{max} [V]	I_{min} [mA]	I_{max} [mA]	Ripple [mV_{PP}]	Spikes [mV_{PP}]
+5.6V_PL_OUT	+5.5	+5.8	0	240	140	100
+16V_PL_OUT	+15.6	+16.4	0	190	140	100
-16V_PL_OUT	-16.4	-15.6	0	150	140	100

Table 7-3 Regulated PL-Outputs Requirements

V_{min} is the minimal output voltage delivered when the outlet is loaded with a current in the range as indicated by I_{min} and I_{max}.

V_{max} is the maximal output voltage delivered when the outlet is loaded with a current in the range as indicated by I_{min} and I_{max}.

I_{min} is the minimum continuous load current for which the output voltage shall be in the range from V_{min} and V_{max}.

I_{max} is the maximum continuous load current for which the output voltage shall be in the range from V_{min} and V_{max}.

Ripple and spikes shall be measured with a representative dummy load, the dummy load shall sink a DC load current of I_{max} in parallel with a 20µF capacitance in series with a 10Ω resistance. Spikes measurements shall be performed with a 50MHz BW Oscilloscope. For ripple measurements, a 2MHz BW limitation shall be introduced. Measurements shall be performed in differential mode.

In Figure 7-1 the meaning of ripple and spikes peak to peak envelopes is shown.

7.2.1.1 Regulated PL-Outputs Protections

The following protections shall be implemented on the DC/DC board Regulated PL-Outputs:

⇒ Over-voltage protection (OVP) with crow-bar on the +5.6V_PL_OUT, +16V_PL_OUT and -16V_PL_OUT outputs.

The over-voltage protection characteristics are summarized in the following Table 7-4

Output	Threshold Voltage [V]	I_{clamp} [A]	V_{lim} [V]
+5.6V_PL_OUT	+6.5±5%	-2…+2	-0.7…+7
+16V_PL_OUT	+17.2±5%	-2…+2	-0.7…+18
-16V_PL_OUT	-17.2±5%	-2…+2	-18…+0.7

Table 7-4

I_{clamp} is the maximum current that the over-voltage protection should be able to handle (crowbar). The voltage on the output shall be within V_{lim} range when I_{clamp} is injected.

Note: in case of short circuit between output “hot lines” with current injection (within the range of I_{clamp}) from one line into the other, the output voltage shall be limited within the range established in the V_{lim} column.

⇒ Current limitation (CL) on the +5.6V_PL_OUT, +16V_PL_OUT and -16V_PL_OUT outlets.

The current limitation values are reported in the following Table 7-5.

Output	I_{lim} [mA]
+5.6V_PL_OUT	285±5%
+16V_PL_OUT	285±5%
-16V_PL_OUT	285±5%

Table 7-5

I_{lim} is also the maximum output current for inrush currents when downstream electronics is switched ON.

To simulate the inrush current of the load connected to each Regulated PL-Output a 100µF capacitor with no significant series impedance can be used.

Each protection intervention will shutdown the DC/DC board.

7.2.2 Unregulated PL-Outputs Requirements

In the following Table 7-6 the electrical requirements of the Unregulated PL-Outputs are reported:

Output	V_{min} [V]	V_{max} [V]	I_{min} [mA]	I_{max} [mA]	Ripple [mV_{PP}]	Spikes [mV_{PP}]
+8V_PL_OUT	+7	+9	0	350	850	200
+18V_PL_OUT	+17	+20	0	330	1400	200
-18V_PL_OUT	-17	-20	0	230	1400	200

Table 7-6 Unregulated PL-Outputs Requirements

V_{min} is the minimal output voltage delivered when the outlet is loaded with a current in the range as indicated by I_{min} and I_{max}.

V_{max} is the maximal output voltage delivered when the outlet is loaded with a current in the range as indicated by I_{min} and I_{max}.

I_{min} is the minimum continuous load current for which the output voltage shall be in the range from V_{min} and V_{max}.

I_{max} is the maximum continuous load current for which the output voltage shall be in the range from V_{min} and V_{max}.

Ripple and spikes shall be measured with a representative dummy load, the dummy load shall sink a DC load current of I_{max} in parallel with a 20µF capacitance in series with a 10Ω resistance. Spikes measurements shall be performed with a 50MHz BW Oscilloscope. For ripple measurements, a 2MHz BW limitation shall be introduced. Measurements shall be performed in differential mode.

In Figure 7-1 the meaning of ripple and spikes peak to peak envelopes is shown.

To simulate the inrush current of the load connected to each Unregulated PL-Output a 100µF capacitor with no significant series impedance can be used.

7.2.2.1 Unregulated PL-Outputs Protections

The following protections shall be implemented on the DC/DC board Unregulated PL-Outputs:

⇒ Over-voltage protection (OVP) on the +8V_PL_OUT, +18V_PL_OUT and -18V_PL_OUT outlets as reported in the following Table 7-7:

Outlet	Threshold Voltage [V]
+8V_PL_OUT	10±1
+18V_PL_OUT	22±2
-18V_PL_OUT	-22±2

Table 7-7

⇒ Over-current protection (OCP) on the +8V_PL_OUT, +18V_PL_OUT and -18V_PL_OUT outlets as reported in the following Table 7-8:

Outlet	Threshold Current [mA]
+8V_PL_OUT	600±100
+18V_PL_OUT	600±100
-18V_PL_OUT	500±100

Table 7-8

Each protection intervention will shutdown the DC/DC board.

8 INTERFACE REQUIREMENTS

8.1 Input Power Supply

Power is switched and distributed from the main bus of the spacecraft to the DC/DC board through a protected line by means of a Latching Current Limiter (LCL). The characteristics of the LCL are TBD.

Use of fuses shall be avoided.

8.1.1 Input Voltage Range

Line	Minimum Voltage [V]	Maximum Voltage [V]
Power Bus	26	29

Table 8-1 Input Voltage Range

The DC/DC board shall safely survive any standing or fluctuating voltage in the full range from 0V to the Maximum Voltage.

8.1.2 Input Voltage Transients

The DC/DC board shall operate with nominal performance when subject to a transient superimposed on the steady state voltage of ± 2.5V with a time constant of 2 ms.

8.1.3 Input Voltage Ripple and Spikes

The DC/DC board shall operate with nominal performance when subject to the following

Input voltage ripple and spikes:

- 140mVpp ripple
- 240mVpp Commutation spikes.

8.1.4 Power Bus Impedance

The Power Bus Impedance mask is shown in the following Figure 8-1

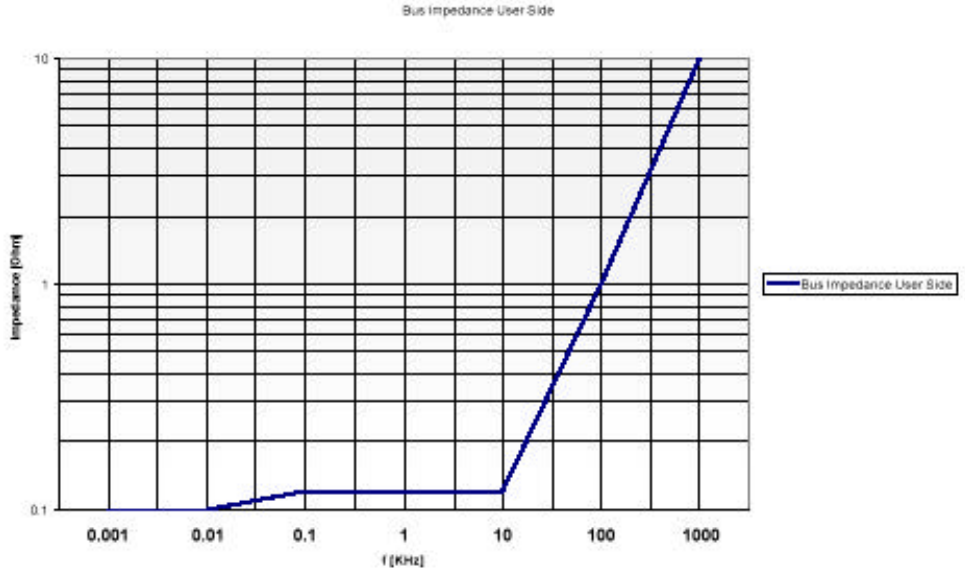

Figure 8-1

The DC/DC board input impedance shall be 6dB higher than the power bus impedance mask.

8.2 Inrush Current

DC/DC board inrush current due to DC/DC board switch-on shall be limited to 1.5 times the DC/DC input peak current, specified as 1.2 times the nominal current. The duration of the inrush peak shall not exceed 0.5ms. The rate of change (slope) of the inrush current shall not exceed 50mA/µsec.

8.3 Input Current Transitions

The instantaneous rate of change (dI/dt) of the DC/DC board input current shall not exceed 50mA/µsec. Pulse repetition frequency shall not exceed 1Hz unless confined to the limits of admissible ripple current.

8.4 Input Protections

The DC/DC board shall be protected against Input Under-voltages (24V), Input Over-voltages (32V) and Input Over-current (set at 3A TBC for the DPU+PL version and 1.5A TBC for the DPU version).

Each protection intervention shall shutdown the DC/DC board.

8.5 Telemetries / Telecommands

The DC/DC board shall provide the telemetries described in the following Table 8-2:

Telemetry	Function	Accuracy	Type	Scale	Reference
INCUR_MNT	Input current monitor	±10%	Analog Isolated	0A ⇒ 0V MNT 1.8A ⇒ 5V MNT	RTN_MNT0
+5V_MNT	+5VD voltage monitor	±5%	Voltage monitor Single Ended	0V ⇒ 0V MNT 6V ⇒ 5V MNT	RTN_MNT1
+15V_MNT	+15VA voltage monitor	±5%	Voltage monitor Single Ended	0V ⇒ 0V MNT 18V ⇒ 5V MNT	RTN_MNT2
-15V_MNT	-15VA voltage monitor	±5%	Voltage monitor Single Ended	0V ⇒ 0V MNT 18V ⇒ 5V MNT	RTN_MNT3
+TEMP_MNT	Temperature monitor	±5%	Temperature Monitor Single Ended	-50°C ⇒ 0V MNT +80°C ⇒ 5V MNT	RTN_MNT4

Table 8-2 Telemetries

Note: RTN_MNT0, RTN_MNT1, RTN_MNT2, RTN_MNT3 and RTN_MNT4 shall be connected, into the DC/DC board, to DPU-Outputs Return line.

No telecommands are foreseen, the DC/DC board shall switch-on automatically when the input voltage is within the range established in Table 8-1

8.6 Synchronization

The DC/DC converter/s within the board shall be synchronized through two external signals (nominal and redundant). The sinch. frequency shall be 131.072 kHz, in the absence of both clock signals the converter shall be free running at a nominal frequency of 110kHz±10% TBC.

9 GROUNDING AND ISOLATION

9.1 Grounding

The power inlet shall not be connected to the chassis.
A connection to bond stud point shall be provided through dedicated pins in the DC/DC board connector (see Table 12-1). DPU-Outputs shall be connected to the chassis while PL-Outputs use the connection to bond stud for high frequency noise filtering.

9.2 Output Power Lines Isolation

DPU-Outputs and PL-Outputs shall be isolated from each other.

PL-Outputs shall have four distinct and isolated power return lines as reported in the following Table 9-1:

Output	Power Return Line
+16V_PL_OUT & -16V_PL_OUT	±16V_PL_RTN
+5.6V_PL_OUT	+5.6V_PL_RTN
+18V_PL_OUT & -18V_PL_OUT	±18V_PL_RTN
+8V_PL_OUT	+8V_PL_RTN

Table 9-1 Power Return Lines

DPU-Outputs shall have two isolated power return lines as reported in the following Table 9-2.

Output	Power Return Line
+5VD	DGND
+15VA & -15VA	AGND

Table 9-2

The Power return lines DGND and AGND shall be connected into the DC/DC board

When the output power return lines are disconnected from ground, the isolation between the output power return lines and the DC/DC board chassis shall be at least 1MΩ shunted by not more than 50nF (exclusive of PL-Outputs filters).

9.3 Isolation between Input Power Line and Output Power Lines

Output lines shall maintain an isolation of at least 1MΩ shunted with a capacity less than 5nF with respect to primary power return line before any grounding of the secondary reference is made.

To reduce the capacitive coupling from primary side to secondary side of the DC/DC board, a static shield into the converter transformer shall be foreseen.

10 EMC REQUIREMENTS

10.1 Conducted Emission on Input Power Line

10.1.1 CE on Input Power Line, Frequency Domain, Differential Mode, NB

Narrow-Band conducted emission Differential Mode in the frequency range 30Hz÷50MHz generated by the DC/DC board on the input power line shall not exceed the following adjustable limit:

A) For Nominal DC input current less than 1A, use the curve in Figure 10-1

B) For Nominal DC input current greater than 1A, increase the level (in dBμA) of the curve in Figure 10-1 by 10*Log[I (A)]. I(A) is the nominal input current in Ampere.

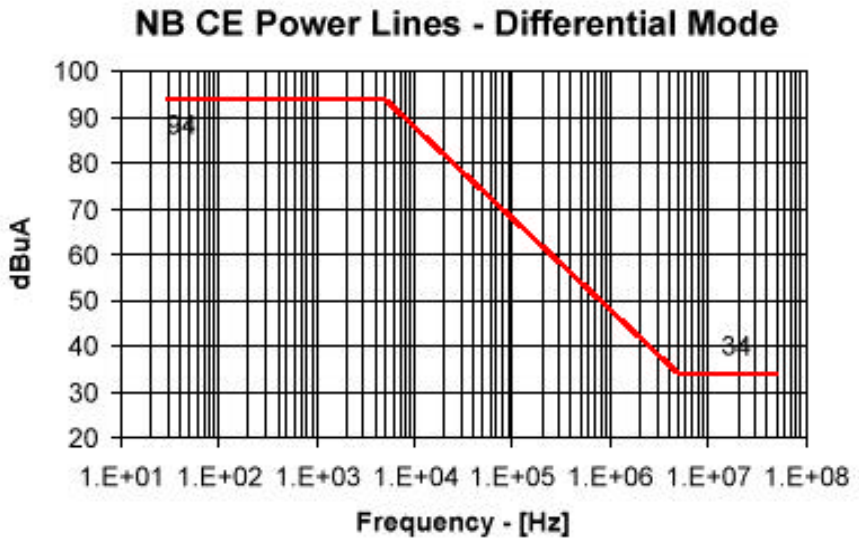

Figure 10-1

10.1.2 CE on Input Line, Frequency Domain, Common Mode, NB

Narrow-Band conducted emission Common Mode in the frequency range 10kHz ÷50MHz generated by the DC/DC board on the input power line shall not exceed the following adjustable limit:

⇒ For nominal DC input current less than 1A, use the curve of Figure 10-2 as shown.

⇒ For nominal DC input current greater than 1A, increase the level (in dBμA) of the curve in Figure 10-2 by 10*log[I(A)]. I(A) is the nominal input current in Ampere.

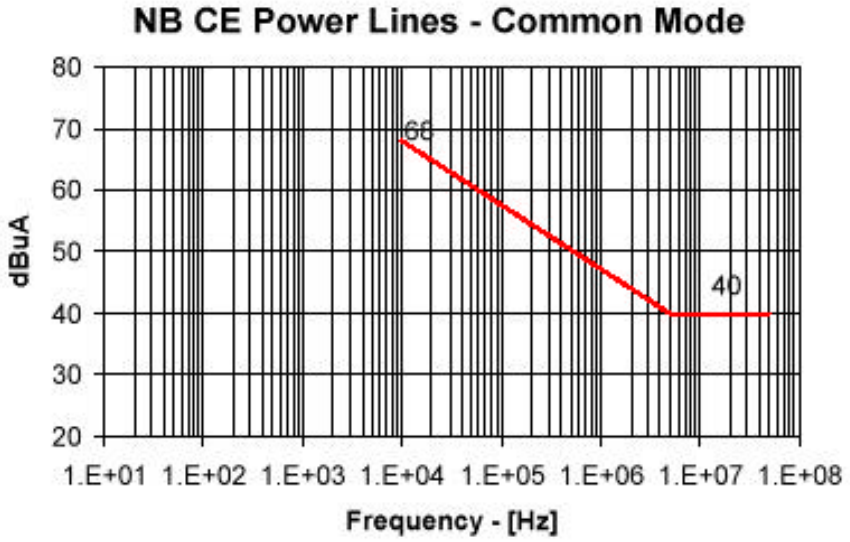

Figure 10-2

10.1.3 Current Ripple, Time Domain, Differential Mode

Differential mode, time domain current ripple and spikes on the input power line of the DC/DC board shall not exceed the following adjustable limits:

A) For nominal DC input current less than 1A:
Ripple: less than 20mApp.
Spikes, including ripple: less than 60mApp.

B) For nominal DC input current greater than 1A:
Ripple: multiply 20mApp by a factor √I(A), I(A) is the nominal input current in Ampere.
Spikes, including ripple: multiply 60mApp by a factor √I(A), I(A) is the nominal input current in Ampere.

Ripple and spikes shall be measured on both the primary and return lines with at least 50MHz bandwidth.

10.2 Conducted Susceptibility from Input Power Line

10.2.1 CS from Input Power Line, Differential Mode, Steady State

The DC/DC board shall not exhibit any malfunction, degradation of performance or deviation beyond the tolerance indicated in the electrical specification when sinusoidal voltages with amplitude specified in Figure 10-3 are injected into the input power leads in the frequency range 30Hz÷50MHz:

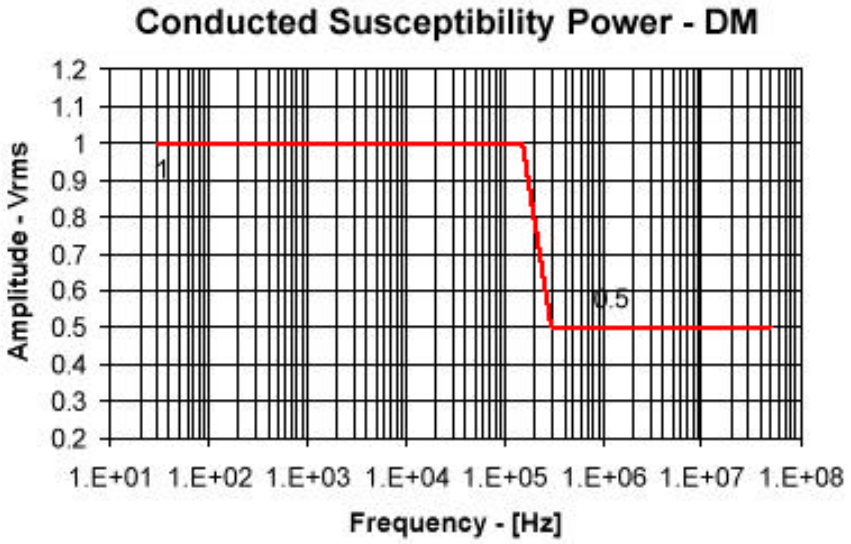

Figure 10-3

The frequency sweep rate shall not be faster than 5 min/decade.

In the frequency range 50kHz – 50MHz, the applied sinusoidal voltage shall be 1kHz amplitude modulated (30% AM).

The requirement shall be considered to have been met when:

1) Frequency range 30Hz – 50kHz

The specified test voltage level cannot be generated but the injected current has reached 3 Arms and the subsystem equipment is still operating without malfunctions within its specified tolerances.

2) Frequency range 50kHz – 50MHz

A power source of 1 Watt, 50Ω impedance cannot develop the required voltage at the equipment power input terminals and the subsystem equipment is still operating without malfunctions within its specified tolerances.

10.2.2 CS from Input Power Line, Common Mode, Steady State

The DC/DC board shall not exhibit any malfunction, degradation of performance or deviation beyond the tolerance indicated in the electrical specification when sinusoidal common mode currents are injected in both the input power leads via Bulk Current Injection (BCI).

The injection shall be in accordance with the following adjustable limit:

A) For nominal DC input current less than 1A, use the curve of Figure 10-4 as shown.

B) For nominal DC input current greater than 1 A, increase the level (in dBμA) of the curve in Figure 10-4 by 10*Log[I(A)].

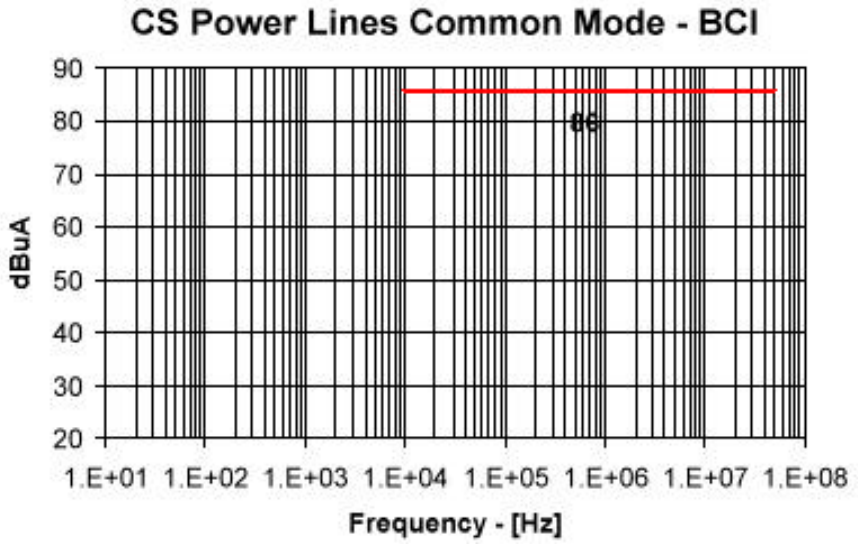

Figure 10-4

10.2.3 CS Common Mode Voltage- Steady State

The DC/DC board shall not exhibit any malfunction, degradation of performance or deviation beyond the tolerance indicated in the electrical specification when sinusoidal voltages with $2V_{pp}$ amplitude are applied between the subsystem equipment signal reference and the ground plane in the frequency range 50kHz –50MHz. The sweep rate shall not be faster than 5min/decade.

10.2.4 CS Common Mode Voltage Transients

The DC/DC converter shall not exhibit any malfunction, degradation of performance or deviation beyond the tolerance indicated in the electrical specification when transient voltages typically shaped as shown in Figure 10-5 are applied between the equipment signal reference and the ground plane. With reference to Figure 10-5, the peak amplitude shall be calibrated to ±3V and Td shall be between 150ns and 250ns when the source having output impedance of 50W is connected to a 50W resistor. Then the source is applied to the equipment after it is detached from the ground plane. The pulse repetition frequency of the waveform shall range from 5Hz to 10Hz and the test duration shall be at least 3 minutes.

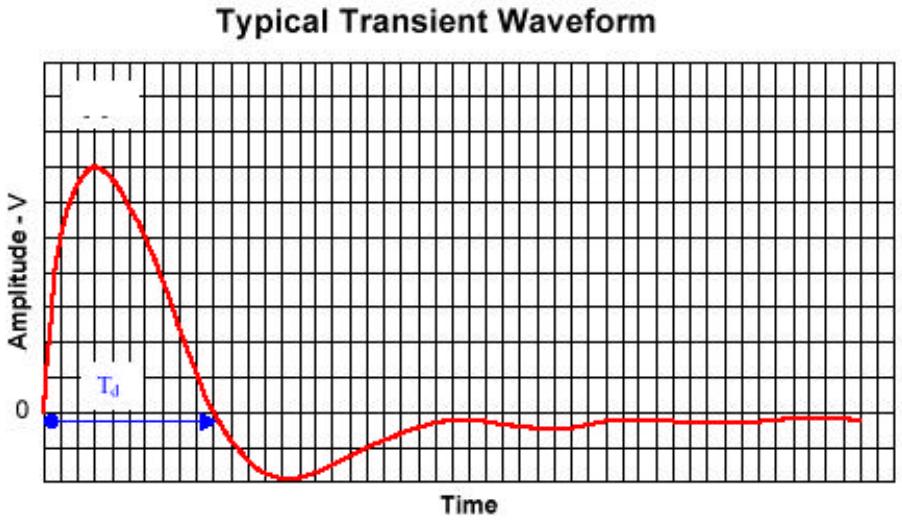

Figure 10-5

10.2.5 CS from Input Power Line – Transients due to Switching

The DC/DC board shall not exhibit any malfunction, degradation of performance or deviation beyond the tolerance indicated in the electrical specification when transient voltages typically shaped as shown in Figure 10-5 are applied to the DC/DC board input power leads. With reference to Figure 10-5 the peak amplitude shall be ±2.5V and T_d shall be 700µs±10%. The pulse repetition frequency of the waveform shall range from 5Hz to 10Hz and the test duration shall be at least 5 minutes.

10.3 Conducted Emissions on PL-Output Lines

To avoid problems arising from common mode disturbances on the output lines, use of a common mode filter on the output lines shall be foreseen.

10.4 Arc Discharge Susceptibility

No malfunction, degradation of performance or deviation beyond the tolerance indicated in the electrical specification shall occur when the DC/DC board input line is exposed to a repetitive electrostatic conducted arc discharge of at least 5.6mJ energy/15kV.

11 EEE PARTS SELECTION CRITERIA

EEE parts will be selected according to the following criteria:

⇒ ESA-SCC qualified part list
⇒ MIL-QML

Quality level shall be:

Discrete semiconductors	MIL-PRF-19500 JANS ESA-SCC level B
Microcircuits	MIL-PRF-38510 class S MIL-PRF-38535 class V and/or T ESA-SCC level B
Transformers and Inductors	ESA-SCC level C or ER-MIL level R
Passive Parts	ESA-SCC level C ; ER-MIL level R
Relays, Crystals	ESA-SCC level C or equivalent
Connectors	ESA-SCC level C or equivalent
Cables	ESA-SCC level C

12 PIN FUNCTION

The pin function of the DC-DC Converter board is shown in Table 12-1 and Table 12-2.

Pin #	Signal	Pin #	Signal	Pin #	Signal
1	+5VD	33	+5VD	65	+5VCORE
2	+VEEPROM	34	+2.5VFPGA	66	+5VCORE
3	+VFIFO	35	+5VBU61582	67	NOT USED
4	NOT USED	36	+VIFMEZZ	68	NOT USED
5	NOT USED	37	NOT USED	69	NOT USED
6	NOT USED	38	NOT USED	70	NOT USED
7	NOT USED	39	NOT USED	71	NOT USED
8	NOT USED	40	NOT USED	72	NOT USED
9	NOT USED	41	NOT USED	73	NOT USED
10	NOT USED	42	NOT USED	74	NOT USED
11	NOT USED	43	NOT USED	75	NOT USED
12	NOT USED	44	NOT USED	76	NOT USED
13	NOT USED	45	NOT USED	77	NOT USED
14	NOT USED	46	NOT USED	78	NOT USED
15	NOT USED	47	NOT USED	79	NOT USED
16	NOT USED	48	NOT USED	80	NOT USED
17	DGND	49	NOT USED	81	DGND
18	BONDING	50	BONDING	82	BONDING
19	BONDING	51	BONDING	83	BONDING
20	NOT USED	52	NOT USED	84	NOT USED
21	NOT USED	53	NOT USED	85	NOT USED
22	NOT USED	54	NOT USED	86	NOT USED
23	NOT USED	55	NOT USED	87	NOT USED
24	NOT USED	56	NOT USED	88	NOT USED
25	NOT USED	57	NOT USED	89	NOT USED
26	NOT USED	58	NOT USED	90	NOT USED
27	NOT USED	59	NOT USED	91	NOT USED
28	NOT USED	60	NOT USED	92	NOT USED
29	-15VA	61	-15VA	93	-15VA
30	AGND	62	AGND	94	AGND
31	+15VA	63	+15VA	95	+15VA
32	DGND	64	DGND	96	DGND

Table 12-1 DC-DC Converter board: P1 pin function

Note: +VEEPROM, +VFIFO, +5VBU61582, +5VCORE and +5VD shall be connected, into the DC/DC board, to the +5VD outlet.

Pin #	Signal	Pin #	Signal	Pin #	Signal
1	+28V	33	+28V	65	+28V
2	NOT USED	34	NOT USED	66	NOT USED
3	+28V_RTN	35	+28V_RTN	67	+28V_RTN
4	NOT USED	36	NOT USED	68	NOT USED
5	SYNCH_MAIN+	37	SYNCH_MAIN+	69	SYNCH_MAIN+
6	SYNCH_MAIN-	38	SYNCH_MAIN-	70	SYNCH_MAIN-
7	SYNCH_RED+	39	SYNCH_RED+	71	SYNCH_RED+
8	SYNCH_RED-	40	SYNCH_RED-	72	SYNCH_RED-
9	NOT USED	41	NOT USED	73	NOT USED
10	INCUR_MNT	42	+5V_MNT	74	+15V_ MNT
11	RTN_MNT0	43	RTN_MNT1	75	RTN_MNT2
12	-15V_MNT	44	+TEMP_MNT	76	AINP5
13	RTN_MNT3	45	RTN_MNT4	77	RTN_MNT5
14	AINP6	46	NOT USED	78	NOT USED
15	RTN_MNT6	47	AGND	79	AGND
16	NOT USED	48	NOT USED	80	NOT USED
17	NOT USED	49	NOT USED	81	NOT USED
18	NOT USED	50	NOT USED	82	NOT USED
19	NOT USED	51	NOT USED	83	NOT USED
20	NOT USED	52	NOT USED	84	NOT USED
21	NOT USED	53	NOT USED	85	NOT USED
22	+16V_PL_OUT	54	+16V_PL_OUT	86	+16V_PL_OUT
23	-16V_PL_OUT	55	-16V_PL_OUT	87	-16V_PL_OUT
24	±16V_PL_RTN	56	±16V_PL_RTN	88	±16V_PL_RTN
25	+5.6V_PL_OUT	57	+5.6V_PL_OUT	89	+5.6V_PL_OUT
26	+5.6V_PL_RTN	58	+5.6V_PL_RTN	90	+5.6V_PL_RTN
27	+18V_PL_OUT	59	+18V_PL_OUT	91	+18V_PL_OUT
28	-18V_PL_OUT	60	-18V_PL_OUT	92	-18V_PL_OUT
29	±18V_PL_RTN	61	±18V_PL_RTN	93	±18V_PL_RTN
30	+8V_PL_OUT	62	+8V_PL_OUT	94	+8V_PL_OUT
31	+8V_PL_RTN	63	+8V_PL_RTN	95	+8V_PL_RTN
32	NOT USED	64	NOT USED	96	NOT USED

Table 12-2 DC-DC Converter board: P2 pin function