NOTES:

KEEP THE PROBE CONNECTOR AS NEAR AS POSSIBLE TO THE CONTROL FPGA

UT9Q512
VDD: 9, 27
VSS: 10, 28
NC: 19, 36

EDAC40 (RT54SX32S)
VCCI (+5V): 12, 40, 60, 98, 115, 148, 164, 201
VCCA: (+2.5VFPGA): 27, 41, 78, 114, 130, 145, 184
GND: 1, 26, 28, 52, 77, 79, 105, 129, 131, 146, 157, 183, 185

+5VD
VCCA
+2.5VFPGA
DGND
\WR
\RD
\CS0
CLK
\RESET
DMA[0..21]
IDMD[0..39]
CB[0..7]

Bench for Extended Floating Point

U14 — UT9Q512ICX NOT MOUNTED
U15 — UT9Q512ICX
U16 — UT9Q512ICX
U17 — UT9Q512ICX
U18 — UT9Q512ICX

Bench for EDAC Check Bits

U19 — UT9Q512ICX NOT MOUNTED

U13 — EDAC40

JP11 — PROBE CONNECTOR

If EDAC is present, do not mount

R9 VCCI

R10 DMD0
R11 DMD1
R12 DMD2
R13 DMD3
R14 DMD4
R15 DMD5
R16 DMD6
R17 DMD7
R18 DMD8
R19 DMD9
R20 DMD10
R21 DMD11
R22 DMD12
R23 DMD13
R24 DMD14
R25 DMD15
R26 DMD16
R27 DMD17
R28 DMD18
R29 DMD19
R30 DMD20
R31 DMD21
R32 DMD22
R33 DMD23
R34 DMD24
R35 DMD25
R36 DMD26
R37 DMD27
R38 DMD28
R39 DMD29
R40 DMD30
R41 DMD31
R42 DMD32
R43 DMD33
R44 DMD34
R45 DMD35
R46 DMD36
R47 DMD37
R48 DMD38
R49 DMD39

If EDAC is present, do not mount

R50 \WR
R51 \RD

C25 C26 C27 C28 C29 C30 C31 C32 C33 C34

FILTER CAPACITORS:
EDAC40: 1 capacitor per side
UT9Q512: 1 capacitor each

C35 C36 C37 C38

FILTER CAPACITORS:
EDAC40: 1 capacitor per side

REV.	DATE	DRAWN	CHECK	ENG.	PR.ASS.	C. of C.	CHANGE AUTORITY
/							

CUSTOMER ID
E.F. RECTIFY
CARLO GAVAZZI SPACE

DRAWING TITLE
HSO/FIRST-DPU
CPU BOARD
Data Memory

SCALE
GEN. TOL.
GEN. RA.

HIGHER ASSEMBLY
DPU-EM-110.000

DRAWING NUMBER
DPU-EM-110.020

SHEET 4 OF 8