DPU/ICU

Derating and Worst Case Analysis

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Acronyms

AD	Architectural Design
ASI	Italian Space Agency
ATP	Acceptance Test Plan
AVM	Avionic Model
BSW	Basic SW
CDR	Critical Design Review
CGS	Carlo Gavazzi Space
CIDL	Configuration Item Data List
CSL	Configuration Status List
CNR	Consiglio Nazionale delle Ricerche
CPP	Co-ordinated Parts Procurement Board
CPU	Control Processing Unit
CDMS	Central Data Management System
CDMU	Central Data Management Unit
CQM	Cryogenic Qualification Model
DCU	Detector Control Unit
DDD	Detailed Design Document
DPU	Digital Processing Unit
EEPROM	Electrically Erasable Programmable Read Only Memory
EMC	Electro Magnetic Compatibility

EMI	Electro Magnetic Interference
ESA	European Space Agency
FIRST	Far InfraRed and Submillimeter Telescope
HK	HouseKeeping
HW	HardWare
IBDR	Instrument Baseline Design Review
ICD	Interface Control Document
ICDR	Instrument Critical Design Review
ICU	Instrument Control Unit
IHDR	Instrument Hardware Design Review
IFSI	Istituto di Fisica dello Spazio Interplanetario
ISVR	Instrument Science Verification Review
LCU	Local oscillator Control Unit
LVDS	Low Voltage Differential Signal
MCU	Mechanism Control Unit
NA	Not Applicable
OBS	On-Board Software
OBSM	On Board Software Management
PA	Product Assurance
PDU	Power Distribution Unit
PROM	Programmable Read Only Memory
PUS	Packet Utilisation Standard
S/C	SpaceCraft

SCC	SpaceCraft Components
SEU	Single Event Upset
SPIRE	Spectral and Photometric Imaging Receiver
S/S	SubSystem
SPR	Software Problem Report
SSD	Software Specification Document
SVM	Service Module
SW	Software
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
TV	Thermal Vacuum
WBS	Work Breakdown Structure
WCA	Worst Case Analysis

1 SCOPE

The Istituto di Fisica per lo Spazio Interplanetario (IFSI) of the Italian Consiglio Nazionale delle Ricerche (CNR) is responsible for the design and manufacturing of the three Digital Processing Units/Instrument Control Unit for the three instruments to be flown on board of the ESA satellite Herschel (ex FIRST): HIFI, PACS and SPIRE.

The design, manufacturing, electrical and functional tests of the DPU/ICU boards and the Basic Software in PROM, are implemented by Carlo Gavazzi Space (CGS) under a contract with ASI. IFSI is responsible of the mechanical box, the box connectors, the electrical-mechanical integration, the environmental tests and the On Board Software.

The purpose of this document is to assess the derating concepts and the Worst Case Analysis used during the design of the DPU/ICU.

It has to be noted that all DPU/ICU electronic components will be purchased through the Co-ordinated Parts Procurement Agency set up by ESA and contracted to Tecnologica (Sevilla, Spain) and TOP-REL (Rome, Italy).

2 DOCUMENTS

2.1 APPLICABLE DOCUMENTS

AD	Name
01	Herschel/Planck Instrument Interface Document, part A
02	Herschel/Planck Instrument Interface Document, part B, Instrument PACS
03	Herschel/Planck Instrument Interface Document, part B Instrument HIFI
04	Herschel/Planck Instrument Interface Document, part B Instrument SPIRE
05	DPU/ICU PA Plan
06	PACS PA Plan
07	HIFI PA Plan
08	SPIRE PA Plan

2.2 Reference documents

Reference Document	Name
01	Derating Requirements Applicable to Electronic, Electrical and Electro-mechanical Components for ESA Space Systems (ESA PSS-01-301)
02	Declared Components, Materials and Processes Lists
03	PACS FMECA
04	HIFI FMECA
05	SPIRE FMECA
06	PAD for CGS made inductors
07	PAD for CGS made transformers
08	RFA for CGS made inductors
09	RFA for CGS made transformers
10	CPU Board Design
11	CPU Board Piggy-Back Design
12	Interface Board Design
13	DC/DC Converter Board Design
14	Mother-Board Design

3 Analysis of the "internal" electronics

For "internal electronics" it is meant all the electronics of the following boards, excluding the electrical interfaces with the spacecraft that will be dealt with in the following section:

- CPU board
- I/F board
- DC/DC Converter Board
- Motherboard.

According to a general statement in the contract ASI-CGS, all design activities are in agreement with the ESA applicable directives, e.g. as per REF 01.

3.1 CPU Board Derating and Worst Case Analysis

The whole CPU Board is powered with 5 V, the core of the FPGA RT54SX32S is powered with 2.5 V. The differences between the CPU boards for HIFI and SPIRE with respect to the PACS one is the presence on the PACS mezzanine board of the ATMEL chip TSS901ESBMV implementing 3 STD 1355 links and the relevant LVDS drivers/receivers. Hence from the point of view of the following analysis there is no difference in the CPU boards for the 3 instruments.

3.1.1 Capacitors Derating and WCA

As can be seen from REF 02 the capacitors of the CPU board are of the following types:

-chip ceramic capacitors: 50 V 10%
-Tantalum capacitors: 30 V 10% or 60V 10%

The required derating is 50% for chip ceramic capacitors: actual derating is 10 times.
The required derating is 60% for tantalum capacitors: actual derating is 6 or 12 times, respectively, with respect to 30 V or 60 V tantalum capacitors.

WCA: the delta C variations, a 50% drop in initial minimum insulation resistance, a 100% increase of the initial maximum leakage current are well within the selected capacitors rated values.

3.1.2 Resistors derating and WCA

As can be seen from REF 02 the resistors of the CPU board are of the following types:

-chip resistors: 0.1 W , 1%, 50 V, 200 ppm/C°
-network resistors: 0.325 W 5%

The required derating is 80% for voltage, 50% for power for chip resistors.
The actual voltage derating is 10 times.
The power derating is such that the minimum allowed resistor directly connected between 5V and GND is 500 OHM. By checking REF 10 and REF 11 it is clear that this is not the case.

WCA: the worst case for all chip resistors is during thermal vacuum at about 70 C°, in this condition, by allowing a 2% reduction in resistance and taking into account the delta °C variations, a minimum resistance of 517 OHM directly connected between 5V and GND is allowed. By checking the schematics shown in REF 10 and REF 11 it is clear that this is not the case.

3.2 I/F Board Derating and Worst Case Analysis

The I/F Board is powered with 5 V, the core of the FPGA RT54SX32S is powered with 2.5 V; the analogue electronics and the DDC chip BU-61582F1 implementing the STD 1553B are powered with +15 V and – 15 V (the DDC chip also with +5 V). The differences between the I/F boards for HIFI and SPIRE with respect to the PACS one is the absence on the PACS I/F board of the FIFOs and the balanced line drivers and receivers as the internal I/F to/from subsystems is made in PACS, as already written, via the ATMEL chip TSS901ESBMV implementing 3 STD 1355 links and the relevant LVDS drivers/receivers. Hence from the point of view of the following analysis there is no difference in the I/F boards for the 3 instruments.

3.2.1 Capacitors Derating and WCA

As can be seen from REF 02 the capacitors of the CPU board are of the following types:

-chip ceramic capacitors: 50 V 10%
-chip ceramic capacitors: 100 V 10%

-Tantalum capacitors: 50 V 10%

The required derating is 50% for chip ceramic capacitors: actual derating is 10 times for capacitors connected to + 5 V, and it is more than 3 times for those connected to + - 15 V.

The required derating is 60% for tantalum capacitors: actual derating is 10 times for capacitors connected to + 5 V, and it is more than 3 times for those connected to + - 15 V.

WCA: the delta C variations, a 50% drop in initial minimum insulation resistance, a 100% increase of the initial maximum leakage current are well within the selected capacitors rated values.

3.2.2 Resistors derating and WCA

As can be seen from REF 02 the resistors of the I/F board are of the following types:

-chip resistors: 0.1 W , 1%, 50 V, 200 ppm/C°
-metal film resistors 0.125 W 0.1% 200 V 5ppm
-network resistors: 0.325 W 5%.

The required derating is 80% for voltage, 50% for power for chip resistors.
The actual voltage derating:

- for chip resistors is 10 times at +5 V, more than 3 times at +-15 V;
- for metal film resistors is 40 times at +5 V, more than 10 times at +-15 V.

The power derating is such that the minimum allowed resistor directly connected between 5V and GND is 500 OHM and from +-15 V and GND is 4500 OHM. By checking the schematics shown in REF 12 it is clear that this is not the case.

WCA: the worst case for all resistors is during thermal vacuum at about 70 C°, in this condition, by allowing a 2% reduction in resistance and taking into account the delta °C variations, a minimum resistance of 517 OHM directly connected between 5V and GND and of 4650 OHM between +-15 V and GND are allowed. By checking the schematics shown in REF 12 it is clear that this is not the case.

3.3 DC/DC Converter Board Derating and Worst Case Analysis

The circuits of the DC/DC Board powered with 28 V are:

- the soft start circuitry,
- the Under Voltage Protection,
- the "power" switching section.

The switching control section is powered with 15 V.

The differences between the DC/DC boards for PACS and SPIRE with respect to the HIFI one is the absence on the PACS and SPIRE board of 3 regulated and 3 unregulated additional voltages used to power the HIFI subsystem FCU. The general concept of the different output voltages is always the same and so we can consider that there are no relevant differences among the three DC/DC converters, two of them (i.e. PACS and SPIRE) actually identical in design and implementation.

3.3.1 Capacitors Derating and WCA

As can be seen from REF 02 the capacitors of the DC/DC board are of the following types:

- chip ceramic capacitors: 50 V 10%
- chip ceramic capacitors: 100 V 10%
- Tantalum capacitors: 50 V 10%
- Tantalum capacitors: 60 V 10%

Looking at the schematics in REF13, page 2 of 6, one can see that capacitor C6 in series with C16, and capacitor C19 in series with C21 are connected to the input lines. The capacitors are identical and of 3.3 nF, 50 V 10%, so the nominal derating is greater than 3 times.

The capacitors directly connected to Power GND and to + 28 V are C10, C11, C12 and C13, all tantalum 8.2 uF 60 V: derating greater than 2 times; the capacitors C14 and C15 are also connected to Power GND and to 28 V: they are .1uF 100 V and their derating is larger than 3 times; capacitors C4 in series with C17 and the like C5 in series with C18 are .47uF and 50 V, their derating is larger than 3 times.

Looking at the schematics in REF13, page 3 of 6, one can see the remaining capacitors directly connected to Power GND and to 28 V in the switching transformer: C134, C136, C137, and C144 all tantalum 8.2 uF 60 V: derating greater than 2 times; the capacitors C129 and C147 are .1uF 100 V and their derating is larger than 3 times.

The required derating is 50% for chip ceramic capacitors: actual derating is 10 times for capacitors connected to + 5 V, and it is more than 3 times for those connected to + - 15 V.

The required derating is 60% for tantalum capacitors: actual derating is 10 times for capacitors connected to + 5 V, and it is more than 3 times for those connected to + - 15 V.

WCA: the delta C variations, a 50% drop in initial minimum insulation resistance, a 100% increase of the initial maximum leakage current are well within the selected capacitors rated values.

3.3.2 Resistors derating and WCA

As can be seen from REF 02 the resistors of the DC/DC board are of the following types:

-chip resistors: 0.25 W , 1%, 50 V, 200 ppm/C°
-metal film resistors 0.125 W, 0.1%, 200 V 5ppm
-low valued resistors: 1 W 1%

The required derating is 80% for voltage, 50% for power for chip resistors.
The actual voltage derating:

- for chip resistors is 10 times at +5 V, more than 3 times at +-15 V;
- for metal film resistors is 40 times at +5 V, more than 10 times at +-15 V.
- at least 2 chip resistors are in series if connected to Power GND and to + 28 V, so their derating is larger than 3 times.

The power derating is such that the minimum allowed resistor directly connected between 5V and GND is 500 OHM and from +-15 V and GND is 4500 OHM. By checking REF 13 it is clear that this is not the case.

WCA: the worst case for all chip resistors is during thermal vacuum at about 70 C°, in this condition, by allowing a 2% reduction in resistance and taking into account the delta °C variations, a minimum resistance of 517 OHM directly connected between 5V and GND and of 4650 OHM between +-15 V and GND are allowed. By checking REF 13 it is clear that this is not the case.

3.3.3 Transformers and inductances

All transformers and inductances are designed in agreement with REF 01 with respect to:

- the voltage applied, to be considered for insulation properties (REF 06 and 08);
- the current flowing, to be considered for the transformer/inductance core selection and wire gauge selection (REF 06 and 08).

WCA: no degradation is foreseen for the Worst Case Analysis for transformers, chokes, coils, motor windings components characteristics (section 3.3, page 8 of REF 01).

3.4 Motherboard Derating

The Motherboard is purely passive and there is no derating and WCA analyses to be applied, as the PCB itself will be designed and manufactured according to ESA approved Flight quality rules both for the materials and for the technology design rules.

4 Analysis of the electrical interfaces with the spacecraft

The interfaces of the DPU/ICU with the spacecraft are:

- mechanical,
- thermal
- electrical.

Only the electrical interfaces will be dealt with in the following and these can be splinted in two:

- Power interface
- Telemetry and Telecommand interface.

4.1 Power interface derating and Worst Case Analysis

The DPU/ICU power interface with the spacecraft is shown in the following figure.
It is to be recalled that in a single DPU/ICU box there will be two completely separated units with one ON while the other is OFF in cold redundancy state. The spacecraft decides which unit is ON by powering it via the 28 V lines.

The interfaces with the S/C power system are:

a) the wires from the spacecraft PDU to DPU/ICU connector(s);
b) the power connector pins;
c) the common mode transformer located in the DC/DC converter board.

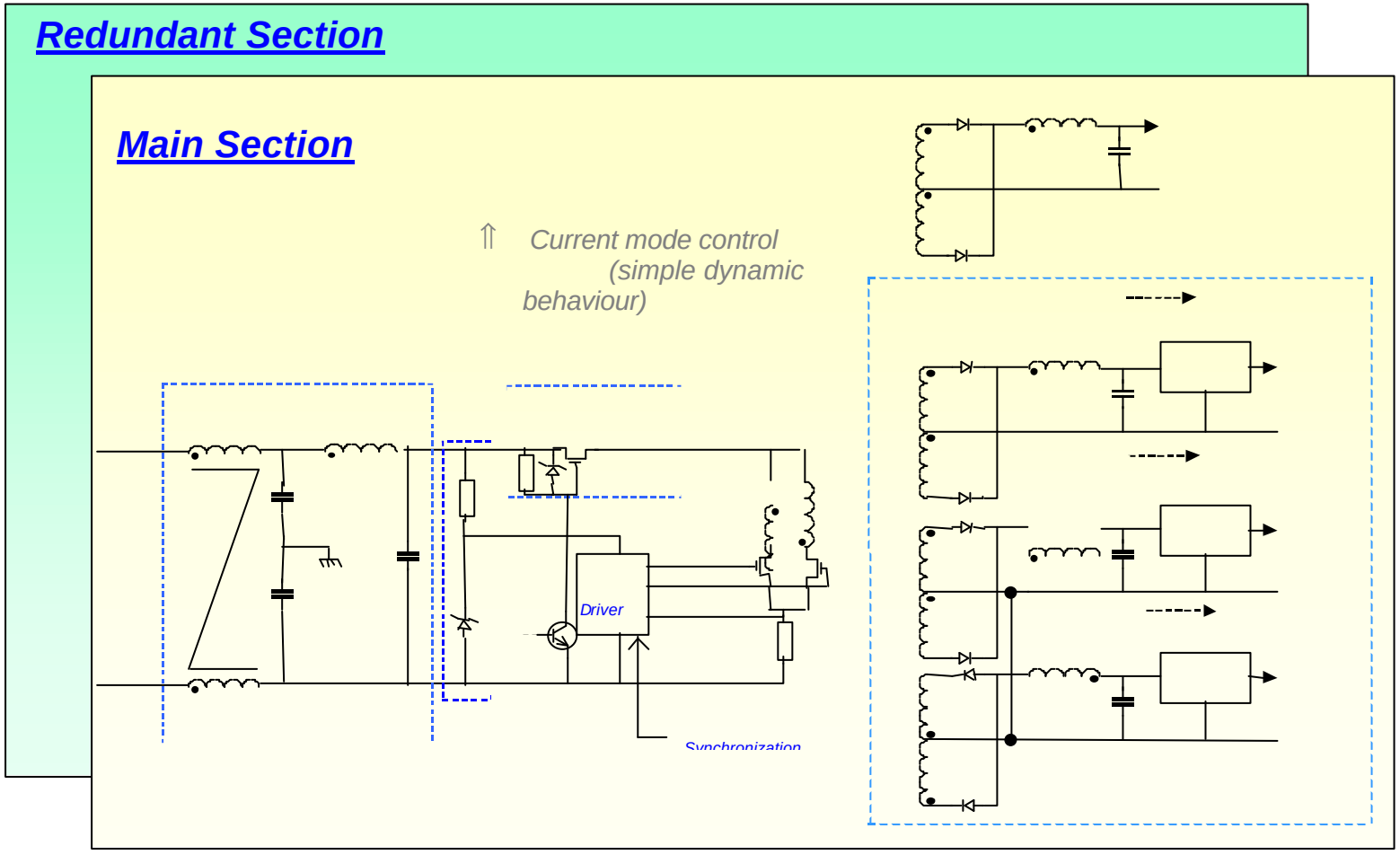
a) The wires from the PDU to DPU/ICU are not considered here as they are S/C provided.

b) There are 2 power connector pins for +28 V and 2 power connector pins for 28 V return. The maximum steady current is less than 1 A for PACS and SPIRE and less than 2 A for HIFI, when HIFI is fully operational. The 2 pins are well beyond the 50% required derating as each connector pin is rated 5 A.

WCA: no degradation is foreseen for the Worst Case Analysis for the connectors components characteristics (section 3.6, page 11 of REF 01).

c) The common mode transformer is designed in agreement with REF 01 with respect to:
- the voltage applied, to be considered for insulation properties (REF 06 and 08);
- the current flowing, to be considered for the transformer core selection and wire gauge selection (REF 06 and 08).

WCA: : no degradation is foreseen for the Worst Case Analysis for transformers, chokes, coils, motor windings components characteristics (section 3.3, page 8 of REF 01).


Redundant Section
Main Section
⇑ Current mode control (simple dynamic behaviour)
Driver
Synchronization

4.2 Spacecraft Interface Derating and Worst Case Analysis

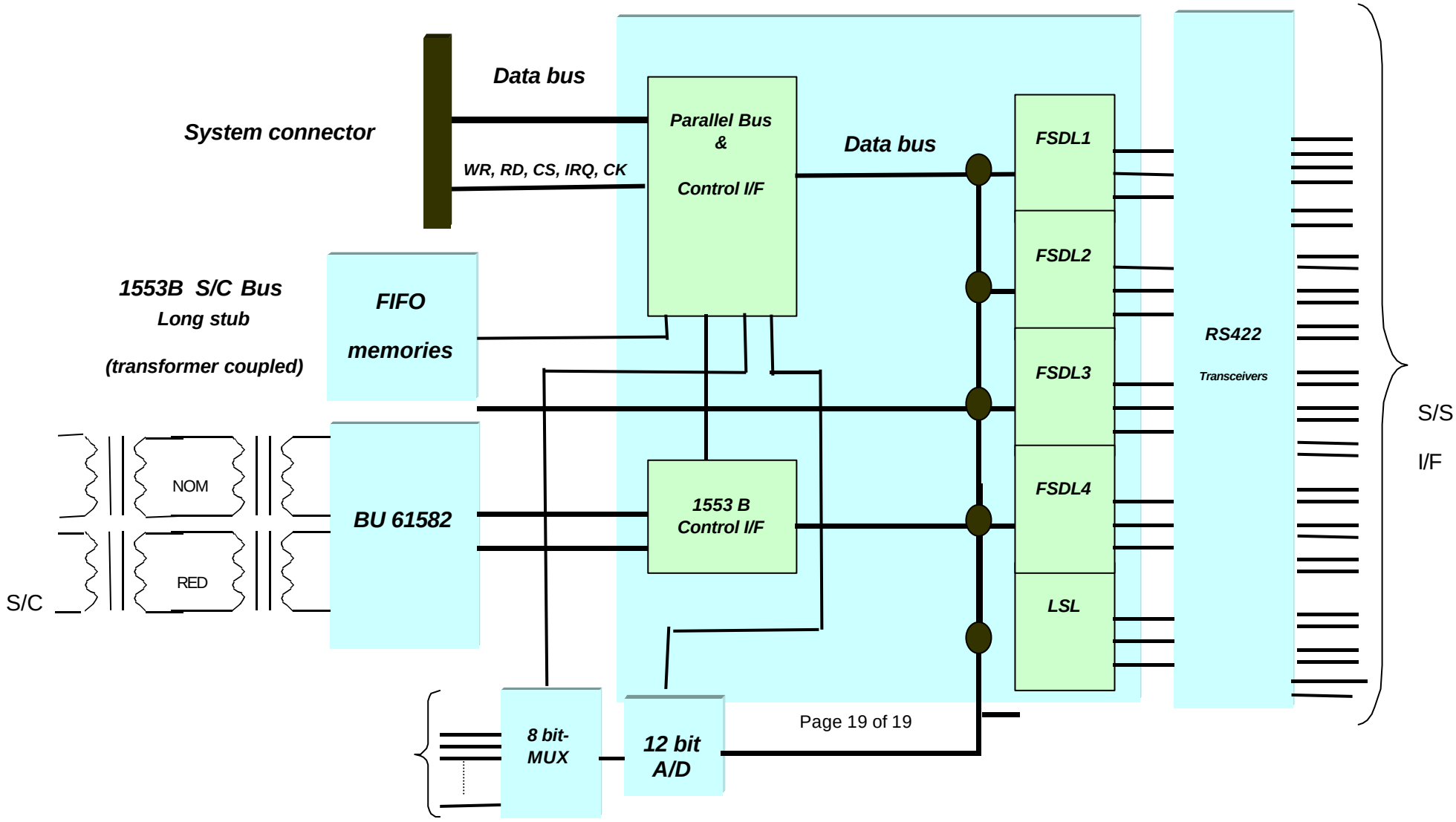
In the following figure the spacecraft interface circuitry is shown as part of the interface board. The interface is based on the MIL STD 1553B, that is on the spacecraft side (acting as Bus Controller) there is a bus on which are serially transmitted telecommands and serially received the telemetry from the instruments (acting as Remote Terminals).

The chosen configuration is "long stub" and the electrical interface is implemented via a suitable transformer. It is to be noted that there are a Prime ("A") and Redundant (B") connections to the Prime CDMS, and the same applies for the Redundant CDMS and the Redundant DPU/ICU.

There are no derating and/or WCA rules to be followed in the cabling from CDMU (S/C responsibility) and the pertinent DPU/ICU box connectors, as the current flowing via the sockets is well below the rated 5 A (28 Vpp on 75 OHM).

The transformer used to interface with the spacecraft 1553B bus in the "long stub" configuration is just designed by BTC to this purpose and recommended by DDC (the manufacturer of the special hybrid device that implements the 1553B standard). The transformer characteristics (type HLP6002) are then such as to be selected and be put in the Co-ordinated Parts Procurement Agency. No further analysis is then carried out about this component and thus this has to be considered "passed" as far as the derating criteria are concerned.

WCA: this interface has to be considered compliant not only because the transformers are purchased via the Co-ordinated Parts Procurement Agency, but also because no degradation is foreseen for the Worst Case Analysis for transformers, chokes, coils, motor windings components characteristics (section 3.3, page 8 of REF 01).


Data bus
System connector
WR, RD, CS, IRQ, CK
Parallel Bus
&
Control I/F
Data bus
FSDL1
FSDL2
FSDL3
FSDL4
LSL
RS422
Transceivers
S/S
I/F
1553B S/C Bus
Long stub
(transformer coupled)
FIFO
memories
NOM
RED
S/C
BU 61582
1553 B
Control I/F
8 bit-
MUX
12 bit
A/D