NOTES:

UT9Q512
VDD: 9, 27
VSS: 10, 28
NC: 19, 36

KEEP THE PROBE
CONNECTOR AS NEAR
AS POSSIBLE TO THE
CONTROL FPGA

EDAC48 (RT54SX32S)
VCCI (+5V): 12, 40, 60, 98, 115,
148, 164, 201
VCCA: (+2.5VFPGA): 27, 41, 78, 114,
130, 145, 184
GND: 1, 26, 28, 52, 77, 79, 105,
129, 131, 146, 157, 183, 185
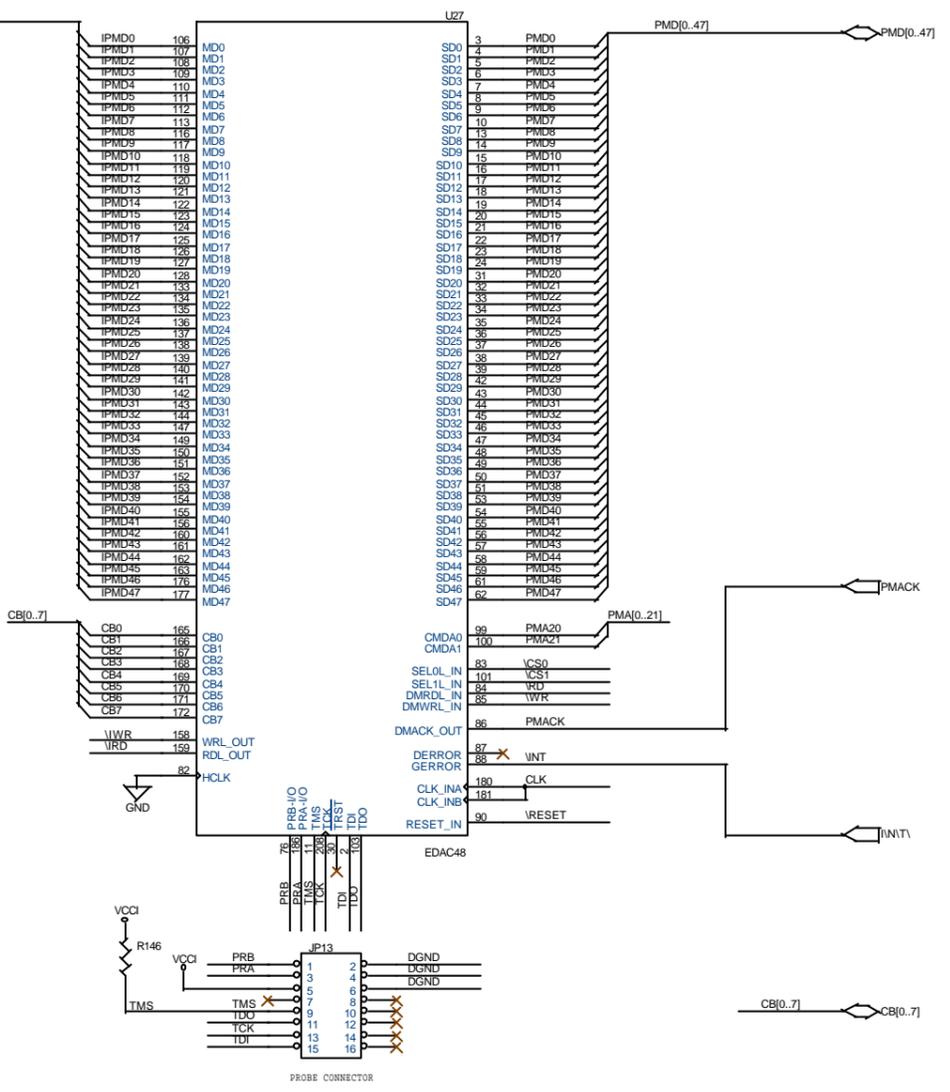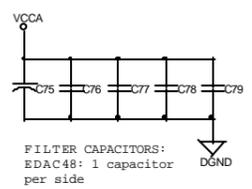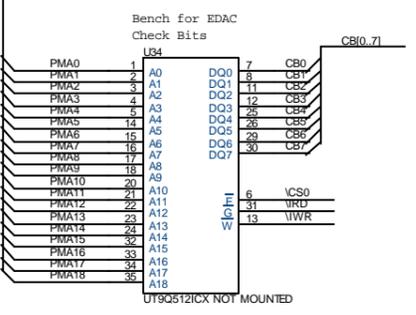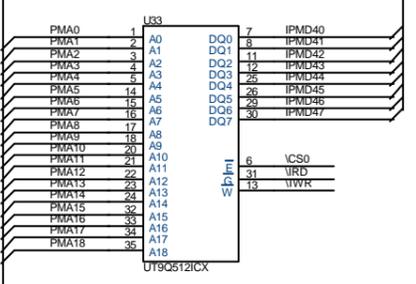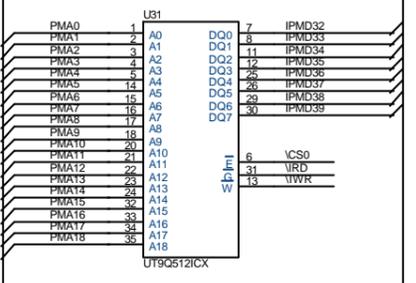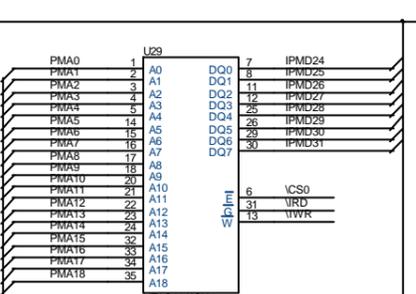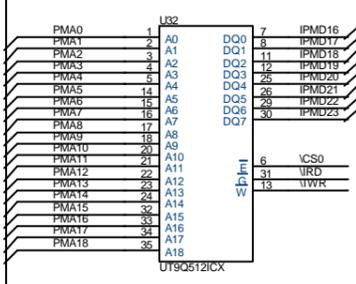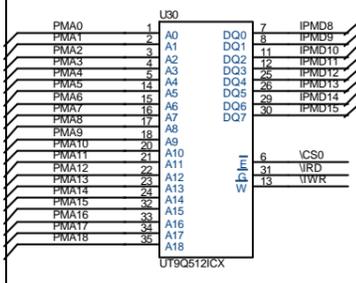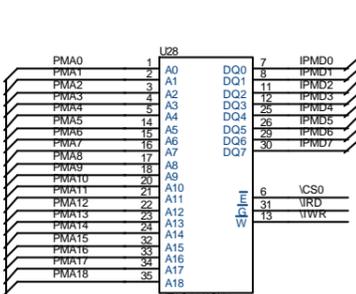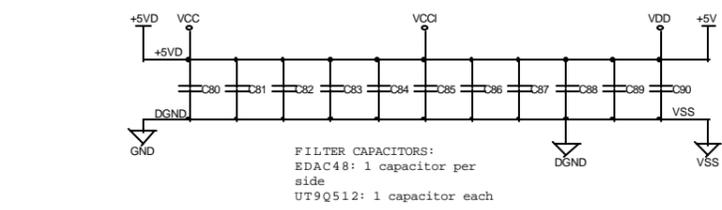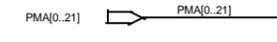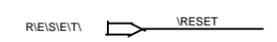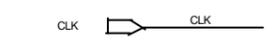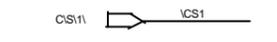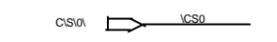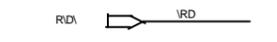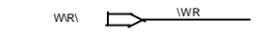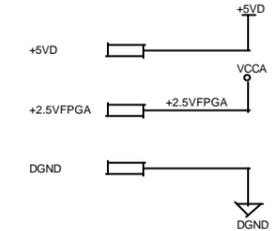
If EDAC is present, do
not mount
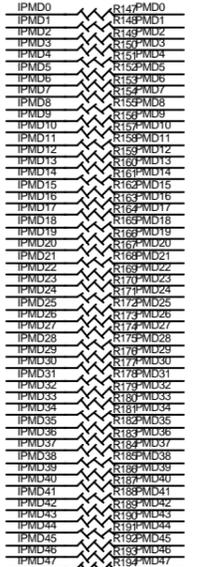
Bench for EDAC
Check Bits

FILTER CAPACITORS:
EDAC48: 1 capacitor per
side
UT9Q512: 1 capacitor each

FILTER CAPACITORS:
EDAC48: 1 capacitor
per side

If EDAC is present, do
not mount

CARLO GAVAZZI SPACE

DRAWING TITLE
HSO/FIRST-DPU
CPU BOARD
Program Memory

HIGHER ASSEMBLY
DPU-EM-110.000

DRAWING NUMBER
DPU-EM-110.020

SHEET OF
8   8