NOTES:

54ACTQ16244/245
VCC: 7, 18, 31, 42
GND: 4, 10, 15,
21, 28, 34, 39, 45

KEEP THE PROBE
CONNECTOR AS NEAR AS
POSSIBLE TO THE
CONTROL FPGA

CONTROL FPGA (RT54SX32S)
VCCI (+5V): 12, 40, 60, 98, 115,
148, 164, 201
VCCA: (+2.5VFPGA): 27, 41, 78, 114,
130, 145, 184
GND: 1, 26, 28, 52, 77, 79, 105,
129, 131, 146, 157, 183, 185

+5VD
+2.5VFPGA
DGND
DMA[0..27]
D\M\S\1\
D\M\S\2\
D\M\S\3\
D\M\R\D\
D\M\W\R\
BUS_IRQM[0..7]
EE_WR_EN
STDACK
SACK
D\P\R\B\U\S\Y\0\
D\P\R\B\U\S\Y\1\
S\E\S\0\
S\E\S\1\
S\E\S\2\
B\G\
PROM_CFG0
PROM_CFG1
FLAG2
DMSPARE[0..3]
SPARE0
SPARE1
SPARE2
SPARE3
D\M\S\0\
I\R\Q\1\
I\R\Q\2\
I\R\Q\3\
CLK
P\O\R\
S\Y\S\R\E\S\E\T\I\N\
E\D\A\C_\R\E\S\E\T\
W\D_\R\E\S\E\T_\I\N\
S\M\C\S_\R\E\S\E\T\

R7: \SMCS_RESET, WD_RESET_IN, \EDAC_RESET, \SYSRESETIN, \DPRBUSY0, \DPRBUSY1, STDACK, SACK, EE_WR_EN, \IRQ_SFPGA, TMS
R8: \BUS_S_EN, BUS_IRQM0, BUS_IRQM1, BUS_IRQM3, BUS_IRQM4, BUS_IRQM5, BUS_IRQM6, BUS_IRQM7 → BUS_IRQM[0..7]

U8
DMA[0..27]: DMA0, DMA1, DMA18, DMA24, DMA25, DMA26, DMA27
IRQM[0..7]: EE_WR_EN, IRQM0, IRQM1, IRQM2, IRQM3, IRQM4, IRQM5, IRQM6, IRQM7
D[0..31]: D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27, D28, D29, D30, D31
DMSPARE[0..3]: DMSPARE0, DMSPARE1, DMSPARE2, DMSPARE3
BUS_CSA[0..7]: \BUS_CSA0, \BUS_CSA1, \BUS_CSA2, \BUS_CSA3, \BUS_CSA4, \BUS_CSA5, \BUS_CSA6, \BUS_CSA7
\BUS_RDA, \BUS_WRA
CLK: CLK_INA, CLK_INB
\DMS1, \DMS2, \DMS3, \DMRD, \DMWR, \DMACK, STDACK, \PMTS, SACK, \IRQ0, \IRQ_SFPGA, FLAG2, SPARE0, SPARE1, SPARE2, SPARE3
EE_WR, \EE_RD, \EE_CS0, \EE_CS1, \EE_CS2, \EE_CS3 → \EE_CS[0..3]
\DPRBUSY0, \DPRBUSY1, \DPR_CS0, \DPR_CS1, \SMCS_CS, CLK10M, \SES0, \SES1, \SES2, \POR, \SYSRESETINA, \EDAC_RESET, \WD_RESET_IN, \SMCS_RESET, HW_RESET, \HW_RESET, \WD_RESET_OUT, \SYSRESETOUTA, \BUS_S_EN, \TR_EN, \BUS_TR_EN, PROM_CFG0, PROM_CFG1, \BG, \BR, \BOOT_LATCH_OE, \PROM_OE, \PROM_CE, \BOOT_PMWR, \BOOT_PMS0, BOOT_CK0, BOOT_CK1, BOOT_CK2, BOOT_CK3, BOOT_CK4, BOOT_CK5 → BOOT_CK[0..5]
PROM_AD0, PROM_AD1, PROM_AD2, PROM_AD3, PROM_AD4, PROM_AD5, PROM_AD6, PROM_AD7, PROM_AD8, PROM_AD9, PROM_AD10, PROM_AD11, PROM_AD12, PROM_AD13, PROM_AD14 → PROM_AD[0..14]
BOOT_PMA0, BOOT_PMA1, BOOT_PMA2, BOOT_PMA3, BOOT_PMA4, BOOT_PMA5, BOOT_PMA6, BOOT_PMA7, BOOT_PMA8, BOOT_PMA9, BOOT_PMA10, BOOT_PMA11, BOOT_PMA12, BOOT_PMA13, BOOT_PMA14, BOOT_PMA15, BOOT_PMA16, BOOT_PMA17, BOOT_PMA18, BOOT_PMA19, BOOT_PMA20, BOOT_PMA21 → BOOT_PMA[0..21]
PRA-I/O, PRB-I/O, TDO, TDI, TRST, TCK, TMS, HCLK

CONTROL FPGA

JP10 (PROBE CONNECTOR): PRB, PRA, TMS, TDO, TCK, TDI, VCCI, DGND
PROBE CONNECTOR

JP14 (TEST CONNECTOR): CLK, \IRQ3, \IRQ2, \IRQ1, \IRQ0, IRQM2, \DMACK, \HW_RESET, \EDAC_RESET, \WD_RESET, CLK, \DMS3, \DMS2, \DMS1, \DMS0, \DMRD, \DMWR, DMA15, DMA14, DMA13, DMA12, DMA11, DMA10, DMA9, DMA8, DMA7, DMA6, DMA5, DMA4, DMA3, DMA2, DMA1, DMA0, DMA[0..27]
AMP MICTOR38

U7: D[0..31], \DMRD, \BUS_TR_EN, BUS_D[0..31]
U9: D[0..31], \DMRD, \BUS_TR_EN, BUS_D[0..31]
U10: DMA[0..27], \BUS_S_EN, BUS_A[0..23]
U11: DMA[0..27], \BUS_CSA[0..7], \BUS_S_EN, BUS_A[0..23], BUS_CS[0..7]
U12: \BUS_RDA, \BUS_WRA, \SYSRESETOUTA, \SYSRESETINA, BUS_IRQM[0..7], \BUS_S_EN, \BUS_RD, \BUS_WR, \SYSRESETOUT, IRQM[0..7]

BUS_D[0..31]
BUS_A[0..23]
BUS_CS[0..7]
\BUS_RD
\BUS_WR
\TR_EN
D[0..31]
DMACK
\DMTS
\PMTS
\IRQ_SFPGA
\IRQ0
\EE_WR
\EE_RD
\EE_CS[0..3]
\DPR_CS0
\DPR_CS1
\SMCS_CS
\BR
PROM_AD[0..14]
BOOT_PMA[0..21]
BOOT_CK[0..5]
\BOOT_PMS0
\BOOT_PMWR
\PROM_OE
\PROM_CE
\BOOT_LATCH_OE
HW_RESET
\HW_RESET
\WD_RESET_OUT
\SYSRESETOUT
CLK10M

VCC, VDD, +5V, VCCI, +5VD
C12, C13, C14, C15, C16, C17, C18, C19, C20
VSS
GND
FILTER CAPACITORS:
CONTROL FPGA: 1 capacitor per side
54ACTQ16244, 245: 1 capacitor each

VCCA
C21, C22, C23, C24
DGND
FILTER CAPACITORS:
CONTROL FPGA: 1
capacitor per side

REV.	DATE	DRAWN	CHECK	ENG.	PR.ASS	C. dIC.	CHANGEAUTORITY
/							

CUSTOMERID
EFFECTIVITY
CARLO GAVAZZI SPACE
DRAWINGTITLE: HSO/FIRST-DPU
CPU BOARD
Control Block
SCALE
GEN. TOL.
GEN. PA.
HIGHERASSEMBLY: DPU-EM-110.000
DRAWINGNUMBER: DPU-EM-110.020
SHEET OF: 3 8