SPIRE

DPU AIV and TEST PLAN

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Prepared by: Renato Orfei Date: 14 February 2002

Agreed PA: Riccardo Cerulli

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A. Di Giorgio		
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5.2	Updated AIV flow

Acronyms

AD	Architectural Design
ATP	Acceptance Test Plan
AVM	Avionic Model
CIDL	Configuration Identification Document List
CSL	Configuration Status List
CNR	Consiglio Nazionale delle Ricerche
CPP	Coordinated Parts Procurement
CPP	Coordinated Parts Procurement Board
CPU	Control Processing Unit
CDMS	Central Data Management System
CDMU	Central Data Management Unit
CQM	Cryogenic Qualification Model
DCU	Detector Control Unit
DDD	Detailed Design Document
DPU	Digital Processing Unit
EEPROM	Electrically Erasable Programmable Read Only Memory
EMC	Electro Magnetic Compatibility
EMI	Electro Magnetic Interference
ESA	European Space Agency
FIRST	Far InfraRed and Submillimeter Telescope

HK	HouseKeeping
HW	HardWare
IBDR	Instrument Baseline Design Review
ICD	Interface Control Document
ICDR	Instrument Critical Design Review
ICU	Instrument Control Unit
IHDR	Instrument Hardware Design Review
IFSI	Istituto di Fisica dello Spazio Interplanetario
ISVR	Instrument Science Verification Review
MCU	Mechanism Control Unit
NA	Not Applicable
OBS	On-Board Software
PA	Product Assurance
PDU	Power Distribution Unit
PROM	Programmable Read Only Memory
S/C	SpaceCraft
SCC	SpaceCraft Components
SCU	Subsystem Control Unit
SEU	Single Event Upset
SPIRE	Spectral and Photometric Imaging Receiver
S/S	SubSystem
SVM	Service Module
SW	Software

TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
TV	Thermal Vacuum
WBS	Work Breakdown Structure

1 INTRODUCTION

1.1 GENERAL

The content of this plan is based on the DPU model philosophy and the DPU subsystem specification AD-05, the DPU product tree, the pertinent instrument level AIV plan and consistent with the interface documents AD-01, AD-02 and AD15.

The subsystem that is delivered for integration and tests at instrument level consists of an electronic box called DPU and of the On Board Software both appropriate for each of the delivered models.

The deliverables are detailed and scheduled in the DPU/ICU Subsystem Development Plan AD-06.

It is recalled that the design, manufacturing, electrical and functional tests of the DPU boards, the basic SW (switch-on and emergency) are implemented by Carlo Gavazzi Space under a contract with ASI. IFSI is responsible of the mechanical box, the box connectors, the electrical-mechanical integration, the environmental tests and the On Board Software.

1.2 SCOPE

The document describes the baseline regarding integration, test organisation, test description, test control and a test matrix for the DPU subsystem. It contains references to the procedures used.

There will be the following deliverable models of the DPU subsystem (AD-06):

AVM subsystem

EQM subsystem

FM subsystem

In addition there will be various flight spare boards for the three Herschel instruments to cover possible failures as indicated in AD-06.

The letters AVM, EQM and FM identify these models respectively.

This document concentrates on the integration and testing of the various models.

1.3 OBJECTIVES

- Verification by means of testing of the DPU subsystem with respect to the subsystem specification, including operational procedures;
- Establish an integration sequence for the units;
- Identification of test activities at unit level ;
- Show the reviews, (e.g. a TRRB before environmental tests)
- Identify the procedures for the various tests

Test description and control sheets are presented in the different test procedures: (Reference Document RD -01– RD-08).

2 DOCUMENTS

2.1 APPLICABLE DOCUMENTS

AD	Name
01	Herschel/Planck Instrument Interface Document, part A
02	Herschel/Planck Instrument Interface Document, part B-Instrument SPIRE
03	SPIRE Instrument Model Approach
04	SPIRE Instrument Specification
05	Herschel SPIRE DPU Subsystem Specification Document
06	Herschel DPU/ICU Subsystem Development Plan
07	DPU/ICU P.A.Plan
08	SPIRE Interface Control Document
09	SPIRE Instrument Development and Verification Plan
10	SPIRE PA Plan
11	Environmental Specification
12	Herschel PS-ICD
13	F/P CDMS Interface Test Requirements Specifications
14	Cleanliness specification
15	SPIRE OBS URD
16	Herschel DPU/ICU Spacecraft Interface Acceptance Test Plan

2.2 Reference documents

Reference Document	Name
RD1	CPU Board Test Procedure
RD2	Interface Board Test Procedure
RD3	DC/DC Board Test Procedure
RD3	DPU/ICU Spacecraft Interface Acceptance Test Plan
RD4	SPIRE Operational modes test procedure

3 MANAGEMENT AND ORGANISATION

The DPU subsystem shall be verified against the requirements contained in AD-04 and the applicable documents contained therein. Two organisations are involved in the DPU production: CGS and IFSI, with different responsibilities as outlined in 3.2 and different activities stated in 1.1.

3.1 Description of the test article

The DPU under test is described in document AD-05

3.2 Responsibilities

It is understood that after the acceptance of the boards at CGS, the responsibility of the following activities stays with IFSI, with CGS helping and solving all HW problems that might be found and the SW problems that might be found only related to the switch-on and emergency procedures.

The responsibilities of persons during the tests will be defined in the relevant test procedures. QA personnel can witness all tests and especially those on EQM, FM and spare parts.

3.2.1 Test reviews

Each integration test at instrument level will be closed by a test review. Before each environmental test at instrument level a TRRB is held. After environmental testing of the subsystem, there will be a TRB.

3.2.2 Criteria for failure definition

Pass/fail criteria are part of each individual Test Procedure. The proper levels for acceptance are considered at Test Procedure Level.

3.2.3 Non conformance

Non conformances will be issued if the test or its results deviate from criteria identified in AD-01, 02, 04 and 05 of this plan including its relevant procedures. NCRs will be classified and processed in accordance with the document referenced SRON-U/HIFI/PR/1999-007. Major non conformances will be issued against deviations with respect to AD–05 and AD-04.

3.2.4 Reporting

All test results will be documented in a logbook copied in dedicated test reports and will be available for review. A summary test report will be issued for each model and will be part of the dedicated End Item Data Package (EIDP).

3.3 Test procedures

Test procedures will be generated for all test steps as identified. They will be applied as a mandatory guidance for performing the test and will be applied as a test log, NCR identification etc.

The test procedures will contain as a minimum:

- a step by step identification of the test
- pass and fail criteria
- test criteria
- environmental conditions
- instrument handling
- responsibilities
- test facility requirements
- data requirements, including data archiving and data analysis as appropriate.

4 TEST ENVIRONMENT

4.1 Facility

For the normal AVM and EQM DPU testing there are no special requirements for pressure, humidity and clean room class. Normal ambient conditions will be sufficient and normal precautions to avoid ESD should be applied. The AVM will be even less stringent with respect to the EQM and obviously FM. In fact the FM will be bolt on an aluminium plate and inside a protective box, with holes to access the connectors savers, and a 100000 class clean room will be required in order for the DPU not to be contaminated and in turn contaminate other subsystems.

The environmental tests like vibrations, thermal vacuum EMC will be carried out at TBD facilities following the specifications of AD-01.

4.2 Test Set up

4.2.1 Tests at Carlo Gavazzi Space

The tests at CGS are described in AD-17, they are aiming at demonstrating that the boards and the PROM SW are working and performing as expected. The test set-up will allow to carry out the foreseen tests both at single board and at integrated boards levels.
The tests will be dedicated to:

- CPU board;
- I/F board;
- DC/DC converters board
- Basic SW performance.

4.2.2 In house test set up: first step

The general in house first step test set up is shown in the following figure 4.1. It is partly a repetition of the tests carried out at CGS premises but with the Herschel CDMS simulator and the IFSI power supply, followed by low level tests of the SW. In brackets it is shown the institution providing the relevant hardware. All the boards are integrated together, i.e. the CPU board, the I/F board and the DC/DC converter boards are connected to the motherboard and from the motherboard the cabling to the box connectors is in place.

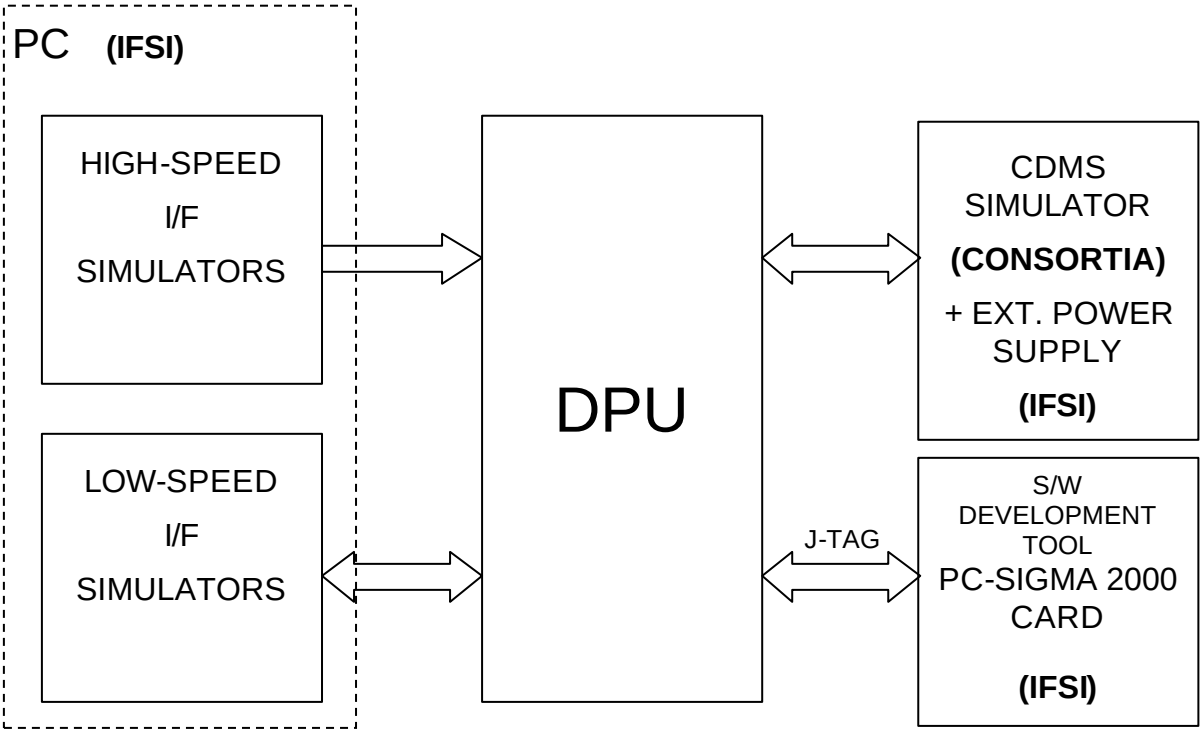

PC (IFSI)
HIGH-SPEED I/F SIMULATORS
LOW-SPEED I/F SIMULATORS
DPU
CDMS SIMULATOR
(CONSORTIA)
+ EXT. POWER SUPPLY
(IFSI)
J-TAG
S/W DEVELOPMENT TOOL
PC-SIGMA 2000 CARD
(IFSI)

Figure 4-1

This test set up is used during preliminary tests at subsystem level to test:

- hardware interfaces functions to/from spacecraft (STD-1553 B HW I/F) (AD-16);
- hardware interface functions to/from subsystems (both types of serial links);
- low level test software to/from spacecraft (STD-1553 B basic protocol) (AD-16);
- low level driving/receiving software to/from subsystems (addressing, data transmission and reception) .

It is underlined that as far as the STD-1553B tests are concerned the HW properties guaranteed by the interface hybrid chip will not be tested (see AD-16).

The test and debugging software can be loaded into the DPU through the J-TAG connector provided on the CPU board.

The same test set up can be used for all DPU models for preliminary tests and for debugging purposes.

4.2.3 In house test set up: second step

In the following figure 4.2 the set up is shown of the in house second step, the main difference from step 1 being the SPIRE (Consortia) provided EGSE.

The purpose of this second set up is to test:

- the transfer layer protocol software;
- the on board software as far as possible, taking into account that the IFSI subsystem simulators will be very simple, their design principle being only aiming at testing the hardware interface and the basic command reception and data transmission.
- for all models, after transport from IFSI to the instrument integrating place or test facility to check the subsystem integrity.

The J-TAG link is still foreseen for a cross-check of the EGSE software uploading facility and for debugging purposes.

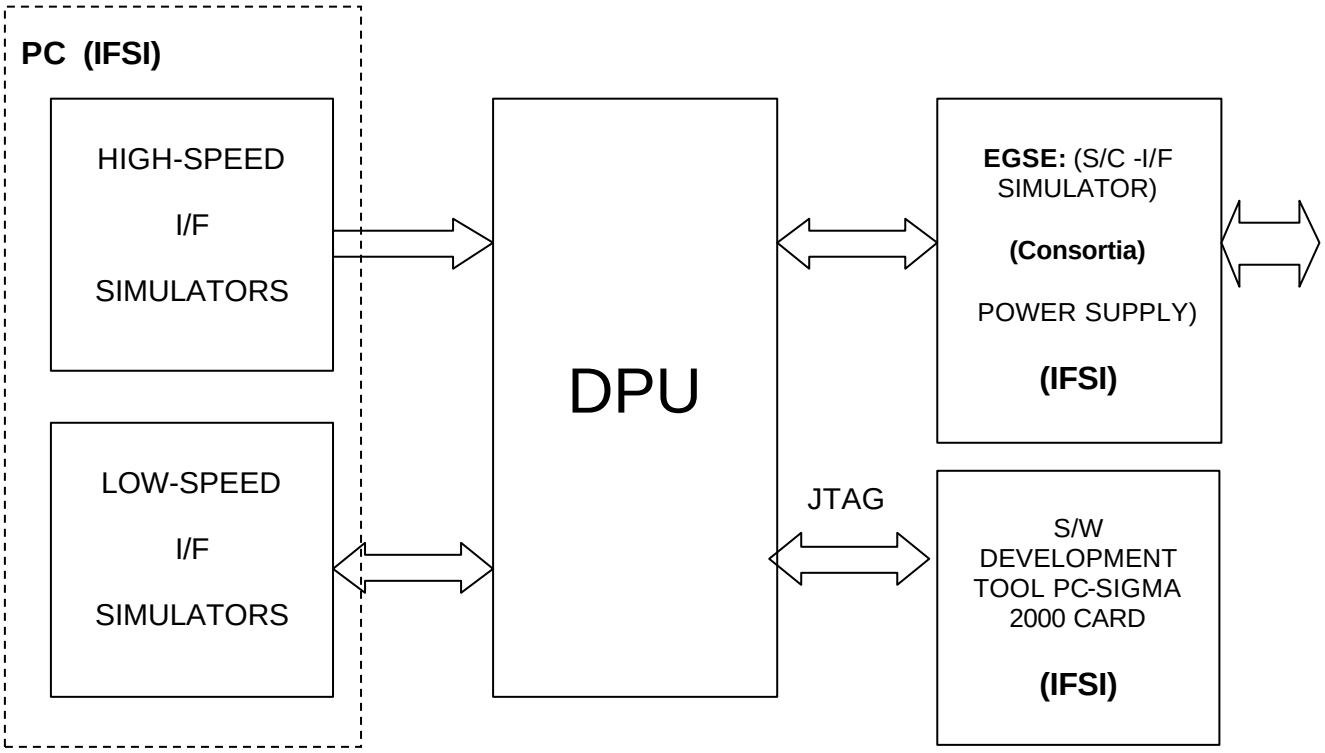

PC (IFSI)
HIGH-SPEED I/F SIMULATORS
LOW-SPEED I/F SIMULATORS
DPU
EGSE: (S/C -I/F SIMULATOR)
(Consortia)
POWER SUPPLY)
(IFSI)
JTAG
S/W DEVELOPMENT TOOL PC-SIGMA 2000 CARD
(IFSI)

Figure 4-2

4.2.4 Instrument level integration tests

In the following figure 4.3 the DPU integrated together with the SPIRE (Consortia) EGSE and subsystems, or their simulators, is shown. This is the only configuration in which the full on board software test will be carried out for models EQM and FM and in which the full on board software test could be carried out for the AVM if the subsystems, or the subsystems simulators, can appropriately answer the DPU commands, send back HK and science data. It is also to be noted that the J-TAG connection is not used any longer as the facility to load new software through the telecommand link should be fully operational.

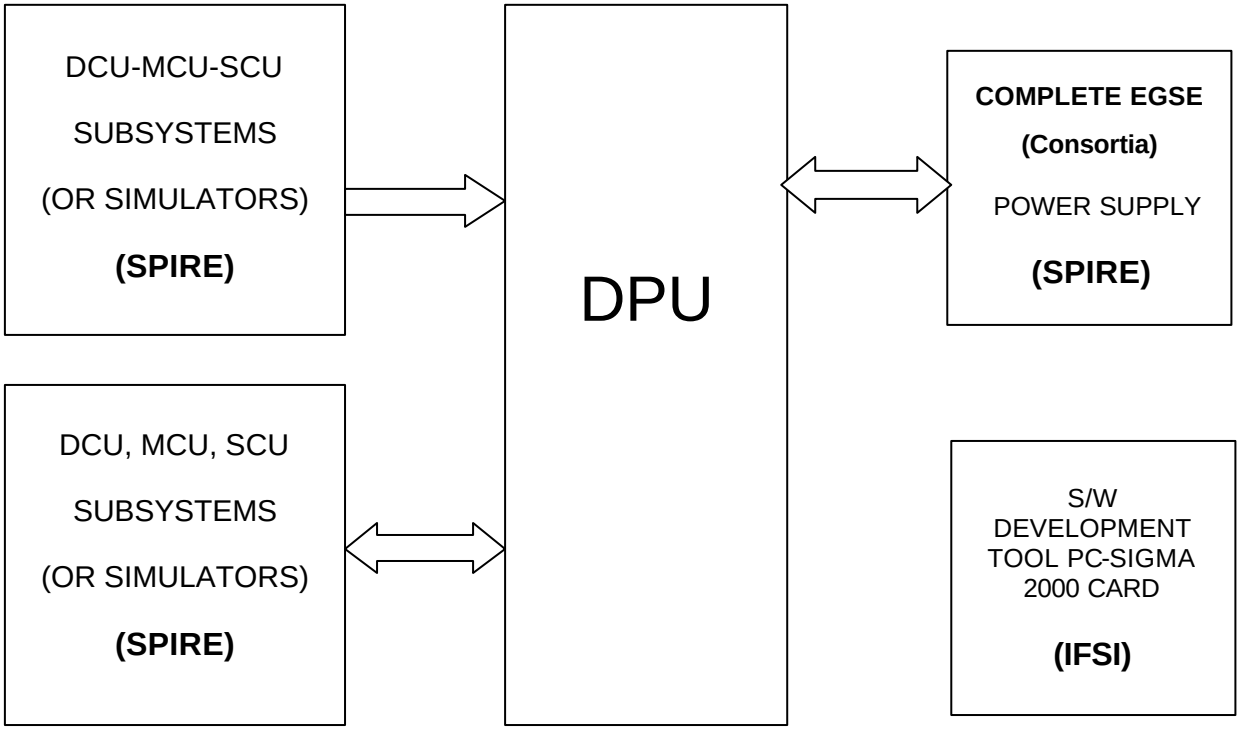


Figure 4-3

4.2.5 Test Parameters Tolerances

The parameters read out from the DPU are analogue and digital. The analogue parameters are:

- DPU temperature
- DPU voltages

The accuracy of the analogue channels will be within 5% (TBC).

The digital parameters will be shown in one or more digital words (TBD) showing the DPU status.

No accuracy percentage can be attributed to the digital status word.

4.2.6 Test Apparatus Accuracy

The high speed and low speed simulators made by IFSI, will follow, as far as the hardware is concerned, the requirements of the DPU sections in the SPIRE Interface Control Document (AD-12).

5 ASSEMBLY, INTEGRATION AND TESTING (AIT)

The following list of tests applies (AD-17):

- Physical properties (dimensions, mass, mechanical interfaces, alignment, CoG, MoI (computed));
- Electrical tests: electrical interfaces with S/C and subsystems and FCU DC/DC converter tests;
- Functional tests;
- Software tests;
- Vibration Tests;
- Thermal vacuum;

- EMC tests;
- Visual inspection;

Thermal vacuum:

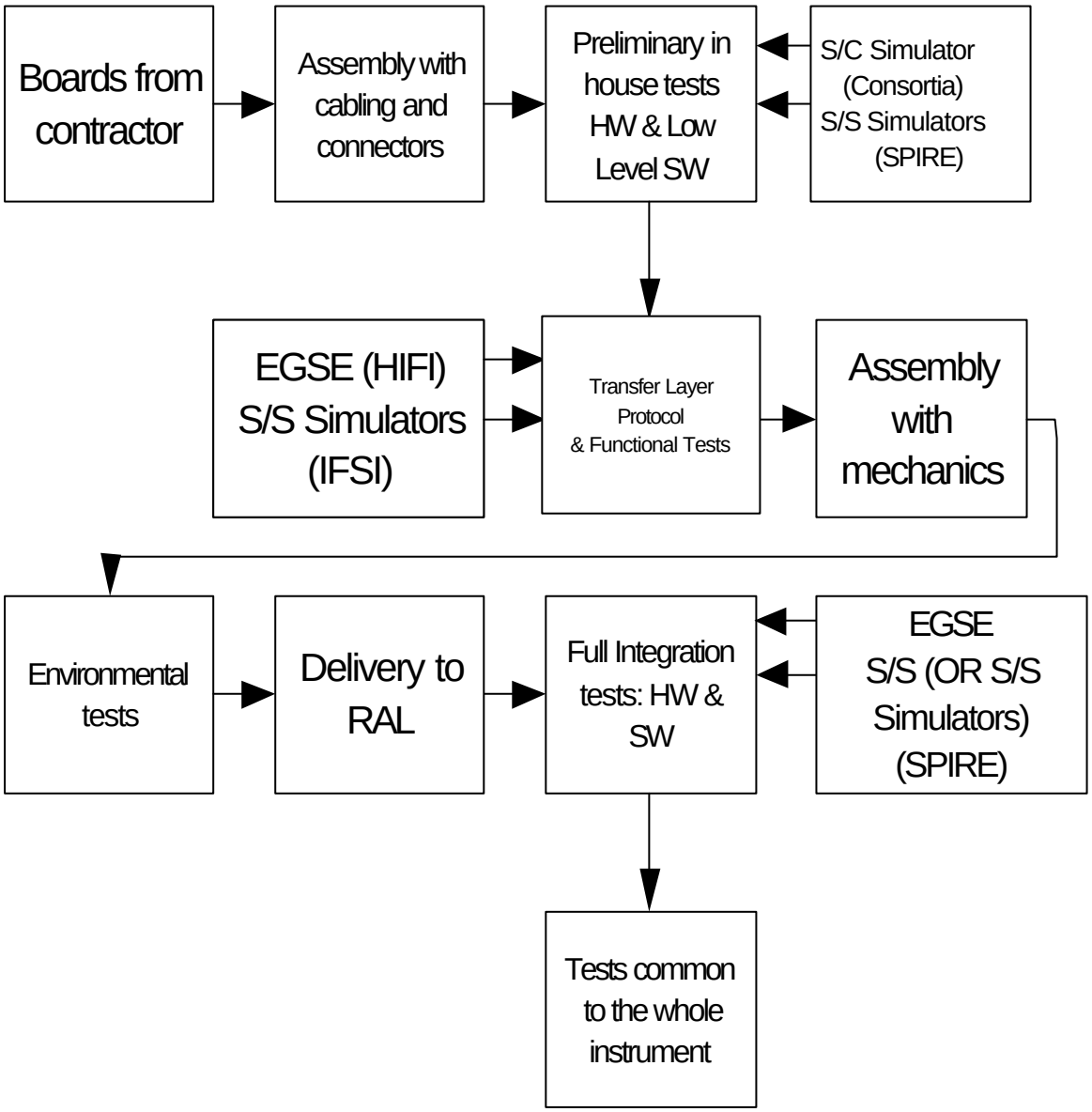
Whenever the DPU subsystem is switched on during any environmental test, the OBS will be running and controlling the instrument. If one or more parameters are out of warning limits, the OBS autonomous functions should send a warning in telemetry to be interpreted by the EGSE and made evident to the operator. The EGSE/check-out software should be such that an alarm is given if pre-set emergency limits have been exceeded; the instrument must then be switched off. Monitoring data should automatically be archived so that trends can be identified later. A full functional test will be performed before and after each environmental test, a subset of the functional test will be performed at certain moments during the testing. This is clearly indicated in the applicable test procedures.

5.1.1 DPU subsystem test matrix

SUBSYSTEM TEST MATRIX	DPU	Instrument Specification
Functional Tests		
1. Electrical I/F	FT-x	AD-01, AD-8
2. Command I/F	FT-x	AD-02
3. Functional reproducibility	NA	
Thermal behaviour	**NA**	
1. Temperature levels (during cooldown)	NA	
2. Thermal response on dissipation	NA	
Operational procedures		
1. Start-up and shutdown procedures	OP-x	RD-01
2. Monitoring procedures	OP-x	RD-01
3. Tuning procedures	NA	
4. Calibration procedures	NA	
5. Instrument modes	OP-x	RD-08
6. Synchronization	OP-x	AD-01
7. Data handling	OP-x	AD-01 AD-05
Performance tests	NA	See para. 6.6

5.2 AIT flow

The detailed assembly, integration and test flow is presented in Fig. 5.1



A full functional test will at least be performed at the beginning and at the end of each environmental test.

Each test is closed with a test review.

6 TESTS PLAN DESCRIPTION

The tests planned and described in the following aim at verifying that the DPU meets the requirements for which it was designed and manufactured.

All units, AVM, EQM, FM and FS will undergo the planned tests, but as far as the environmental tests are concerned, the Qualification Units will undergo the vibration and thermal vacuum tests at qualification levels while the flight units (FM and FS) will be submitted to vibration and thermal vacuum tests only at acceptance levels.

The following matrix shows the tests the various models will undergo.

TYPE OF TEST	**AVM**	**EQM**	**FM**	**FS**
Functional Test	X	X	X	X (note2)
Performance Test	X	X	X	X (note2)
Interface Drawing Verification	X *	X	X	NA
Electrical Interface Tests	X	X	X	X
Vibrations Tests	NA	Q	A	A
Thermal-.Vacuum Test	NA	Q	A	A
Radiation tolerance	NA	NA	note 1	note 1
EMI / EMC	NA (note 4)	Q (note 3)	Partly (TBD)	NA
ESD	NA	X	NA	NA

(* NA but implemented also for AVM).
X = a test is carried out.**Q** = Qualification levels and duration. **A** = Acceptance levels and duration.

Items that will be in the Interface Drawing:

- Box dimensions and envelope.
- Mass; Moment of Inertia; Centre of Gravity
- Feet and connectors positions..
- Flatness of the mounting surface.
- Box and connectors identification.
- Connectors definitions.
- Box surface treatment including α and ε values (*NA for AVM).

Note 1: Radiation is included in EEE component selection and S/C sector analysis.
Note 2: Tests on PCB level only.
Note 3: Meaningful EMI/EMC tests should be carried out with subsystems or subsystems simulators.
Note 4: on the AVM only conducted emission tests will be carried out.

7 Test Types

The following tests are foreseen:

- Metrological tests
- Electrical tests
- Performance tests
- Vibration tests
- Thermal Vacuum tests
- EMC/EMI tests
- Functional tests

7.1 Metrological Tests

The DPU box shall comply with the physical characteristics shown in the Interface Control Drawing in AD3.

The parameters to be measured are:

- Mass
- Dimensions
- Centre of Gravity (COG)
- Moment Of Inertia (MOI)
- Baseplate and Feet Flatness
- Bonding Strap Position
- Connectors Positions
- Connectors Identification Position

NOTE: The Moment Of Inertia will not be measured but derived by analysis.

7.2 Electrical Tests

The different models AVM, EQM, FM and FS are specified to be electrically identical, as far as the hardware interfaces with S/C and subsystems are concerned, and functionally identical.

The AVM will contain only one computer unit while the remaining models will be fully hardware redundant containing two computer units.

As far as the On Board Software is concerned, the AVM OBS can be upgradable and so will be the EQM. Of course the AVM OBS will be checked up to the level of the subsystems implementation or to the level of the subsystems simulators implementation.

In order for the OBS to be tested the interface between the DPU, as Remote Terminal, and the S/C simulator, as Bus Controller, will be carried out in agreement with AD9.

The electrical tests that will be carried out at CGS premises are the following:

7.2.1 Tests on the CPU Board (RD1)

1. DSP and Program Memory
2. Data Memory
3. 32-Bit Internal Bus
4. Interval Timer & Interrupt Manager
5. Watch-dog
6. EEPROM
7. Check power consumption

7.2.2 Tests on the I/F Board (RD2)

1. Check absence of short circuit to power supply
2. Check digital ground to analogue ground insulation
3. Check power consumption
4. Check Power-On reset generation
5. Check external Hardware Reset generation
6. Check control Logic
7. Check Fast Science Data Link Interfaces
8. Check Low Speed Link Interfaces
9. Check Analogue Inputs
10. Check MIL-STD-1553 Clock Generation
11. Check MIL-STD-1553 Interface
12. Check Control Logic Status Register

7.2.3 TEST SW PACKAGE MENUS

7.2.3.1 MAIN MENU

1 HW Reset Board
2 Reset Board
3 FSDL Interfaces
4 LSL Interfaces
5 Analogue Inputs
6 MIL-STD-1553 Interface
7 Status Register

7.2.3.2 RESET BOARD

1 FSDL0 Reset
2 FSDL1 Reset
3 FSDL2 Reset
4 FSDL3 Reset
5 MIL-STD-1553 Reset
6 LSL Reset
7 Software Reset
8 Return to the Main Menu

7.2.3.3 FSDL Interfaces

1 Reset all FSDL Interfaces
2 Send Single Datum
3 Send Single Data Packet
4 Send half FIFO Data Packet
5 Read Single Datum
6 Read All Data

7.2.3.4 LSL Interfaces

1 Reset LSL Interface
2 Send Single Datum without Echo
3 Send Single Datum with Echo
4 Read Data
5 Read Status Register
6 Timeout Check

7 Abort Check
8

7.2.3.5 Analogue Inputs

No Sub-menus are present

7.2.3.6 MIL-STD-1553 Interface

See RD3

7.2.3.7 Status Register

No Sub-menus are present

7.2.4 Tests on the DC/DC Converter for DPU

See RD4

7.2.5 Electrical Test Objectives at IFSI

The main parameters to be checked are:

- Voltage levels for the DPU and for the FCU
- Noise on voltage levels both for DPU and for FCU
- Converter efficiency of the DC/DC for DPU
- Converter efficiency of the DC/DC for FCU
- Inrush current
- Conducted emission on power lines
- Conducted susceptibility on power lines and signal lines
- Total power drain

- Interface signal timing to/from S/C (repeated as there is a different CDMS I/F simulator)
- Pin functions
- Isolation and Grounding

Some of the above tests are part of the EMC/EMI environmental tests and their results will be contained in the EMC/EMI test report.

7.2.6 Test Set-Up

To meet the objectives described in section 3.2.6 the test set-up will ensure:

- Isolation and grounding
- Input and output impedances
- Signal level and duration
- Rise and fall times

The measurements will be carried-out under nominal power supply generation/drain and environmental conditions, but they will be repeated at the extremes of the operational conditions to verify the electrical performance.

7.3 Performance tests

Performance tests shall be carried-out to exercise all hardware and software functions in:

- normal environmental conditions
- marginal power supply conditions
- thermal vacuum conditions

7.3.1 Test objectives

The tests shall be carried-out to exercise all hardware and software functions, including non destructive negative conditions, to verify the correct response of the equipment.

The tests shall be carried-out in normal conditions, during thermal vacuum test steps and after vibrations.

7.3.2 Test set-up

At subsystem level the DPU performance will be tested by means of the CDMS simulator, the EGSE and with IFSI subsystems simulator. The subsystems simulators are very simple and at basic levels (see AD7) to mainly test the hardware to/from the HIFI subsystems.

At integrated SPIRE instrument the DPU performance will be tested by means of the SPIRE EGSE and the subsystems simulators or the subsystems units.

7.4 Vibration tests

The vibration tests will include:

- a low level sinusoidal vibration for resonance frequencies research
- sinusoidal vibration at qualification level for the EQM or at acceptance levels for the FM and FS
- random vibration at qualification level for the EQM or at acceptance levels for the FM and FS

The pertinent vibration levels are shown in AD2 sections 9.5.3.3.2 and 9.5.3.4.

7.4.1 Test Objectives

The tests shall demonstrate the capability of the DPU to withstand the stress induced by vibrations during the launch phase without degradation of performances.

The resonance research will indicate the frequencies at which the maximum stresses will be induced by the vibrations to the structure and to all devices internal to the box.

7.4.2 Test set-up

A rigid interface flange between the DPU and the shaker is required having the appropriate interface holes.

The EGSE and subsystems simulators are required to verify that after vibrations, at subsystem level, no damage was sustained.

7.5 Thermal Vacuum tests

7.5.1 Test objectives

Thermal vacuum (TV) tests are carried-out to check that:

- The thermal design is correct
- no assembly defects exist as they are emphasised by the combined effects of thermal cycling and heat dissipation.

The pertinent TV requirements are shown in AD2 section 9.5.4.

7.5.2 Test set-up

Meaningful TV tests at subsystem level, in order to check also the OBS performance, require the interconnection with the HIFI subsystems (or the S/S simulators) and with the FPU (or FPU simulator), together with the HIFI EGSE in order to allow thorough performance testing checks to be carried-out as required during thermal cycling and/or soaking phases.

TV tests only at unit level will be carried-out, with the EGSE and subsystems simulators but only low level software functionalities will be tested.

7.6 EMC/EMI tests

7.6.1 Test objectives

The EMC/EMI tests have to be carried out to verify the compatibility of the instrument subsystems with the electromagnetic environment of Herschel.

At unit level the meaningful tests that will be carried out are:

- conducted emission on power lines
- conducted susceptibility on power lines
- conducted susceptibility on signal lines (CM)
- CM tests on power lines
- CM tests on signal lines
- radiated emission
- radiated susceptibility (susceptibility thresholds, if any, assessed only on dedicated software routines)
- radiated ESD susceptibility tests
- conducted ESD susceptibility tests

7.6.2 Test set-up

For the various EMC/EMI tests the suggested set-up is shown in the relevant subsections of section 9.5.6 of AD2, i.e.:

- section 9.5.6.12 for conducted emission tests
- section 9.5.6.13 for conducted susceptibility tests
- section 9.5.6.14 for radiated emission tests
- section 9.5.6.15.1 for radiated ESD susceptibility tests
- section 9.5.6.15.2 for conducted ESD susceptibility tests

7.7 Functional tests

The following functional tests will be foreseen in order to check the performance of the DPU at various levels:

- GO/NO-GO test
- Short functional test
- Functional test

7.7.1 GO/NO-GO test

The GO/NO-GO test will be performed every time a quick assessment of the vitality of the DPU unit is required. It will consist in a check of the current drain at the nominal power supply voltage and of the DPU HK content. It can be carried-out with the DPU, the FCU load simulator, the EGSE. The performance assessment is just limited to the good health of the DPU itself and the HK content should reflect the situation of all subsystems being missing.

7.7.2 Short functional test

The short functional test will be performed together with the subsystems (or their simulators) and the HIFI EGSE and will consist in the full procedure of the default settings of all the subsystems following the switch on procedure up to a pre-defined stand-by mode. The check of the whole HK content will provide information of the good health of the DPU and its interfaces (HW and SW) with the instrument subsystems.

7.7.3 Functional test

The functional test will be performed with the full integrated instrument in such conditions as to allow scientific measurements in order to check all OBS functionalities in the various operating modes, the various settings and including the autonomous functions. The SPIRE EGSE will be used to assess the performance of the DPU OBS.