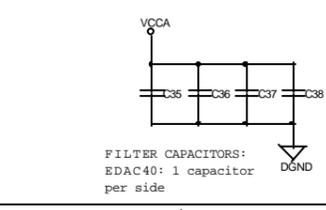
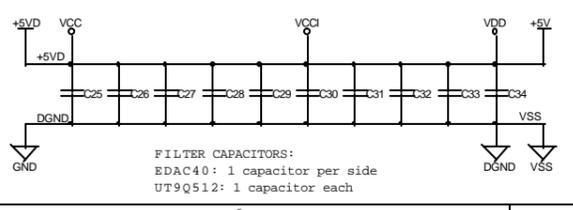
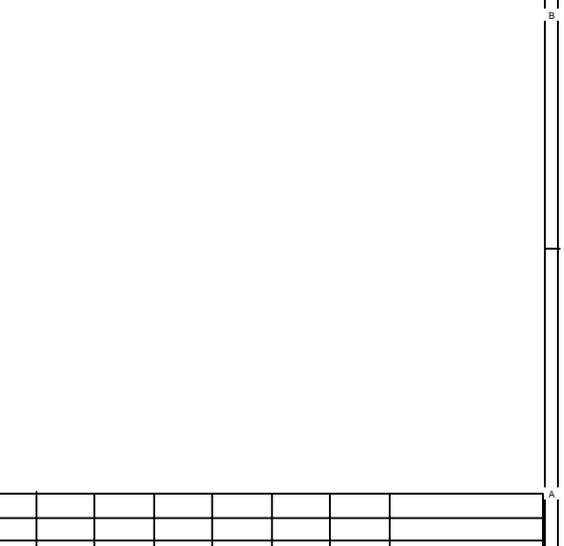
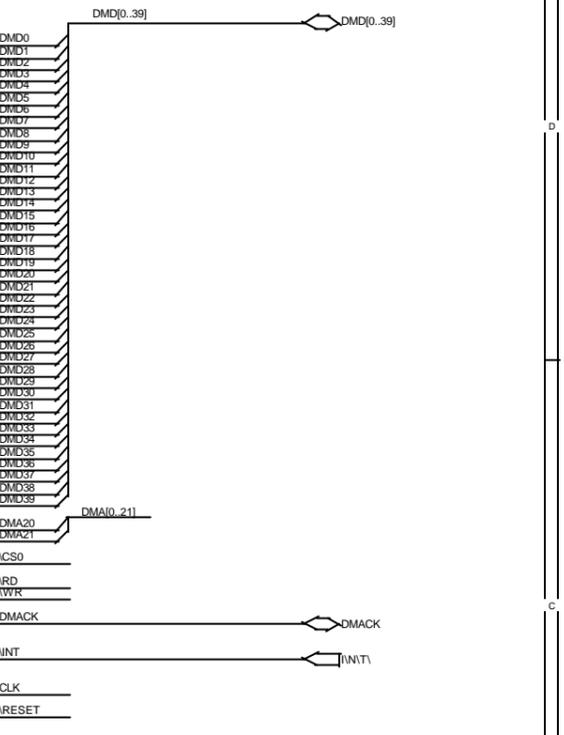
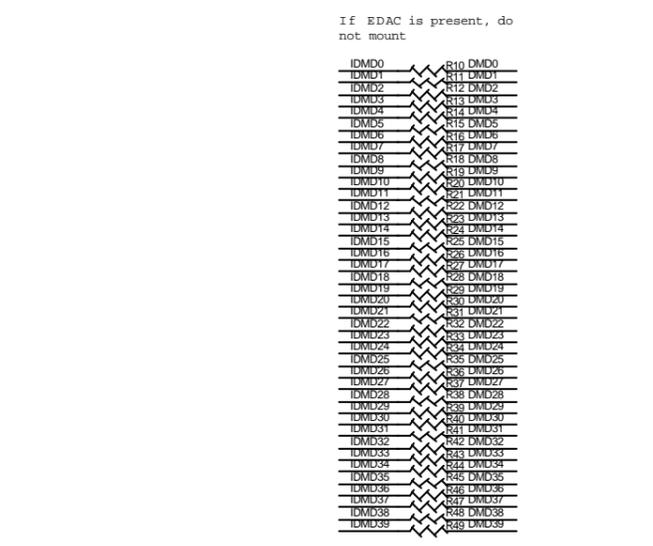
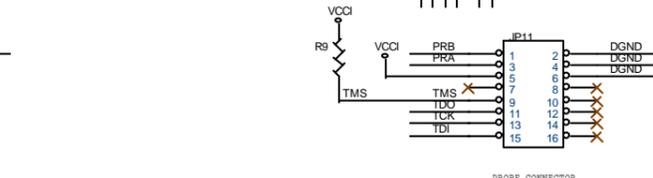
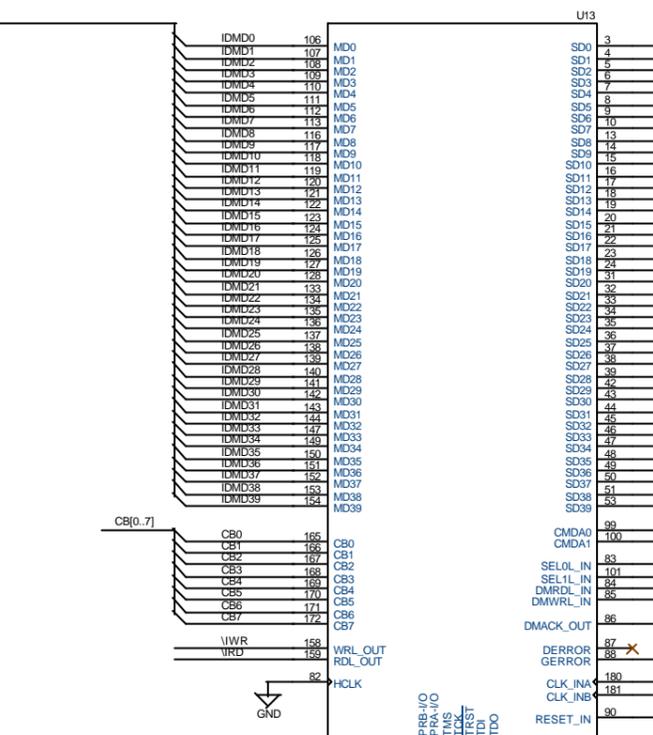
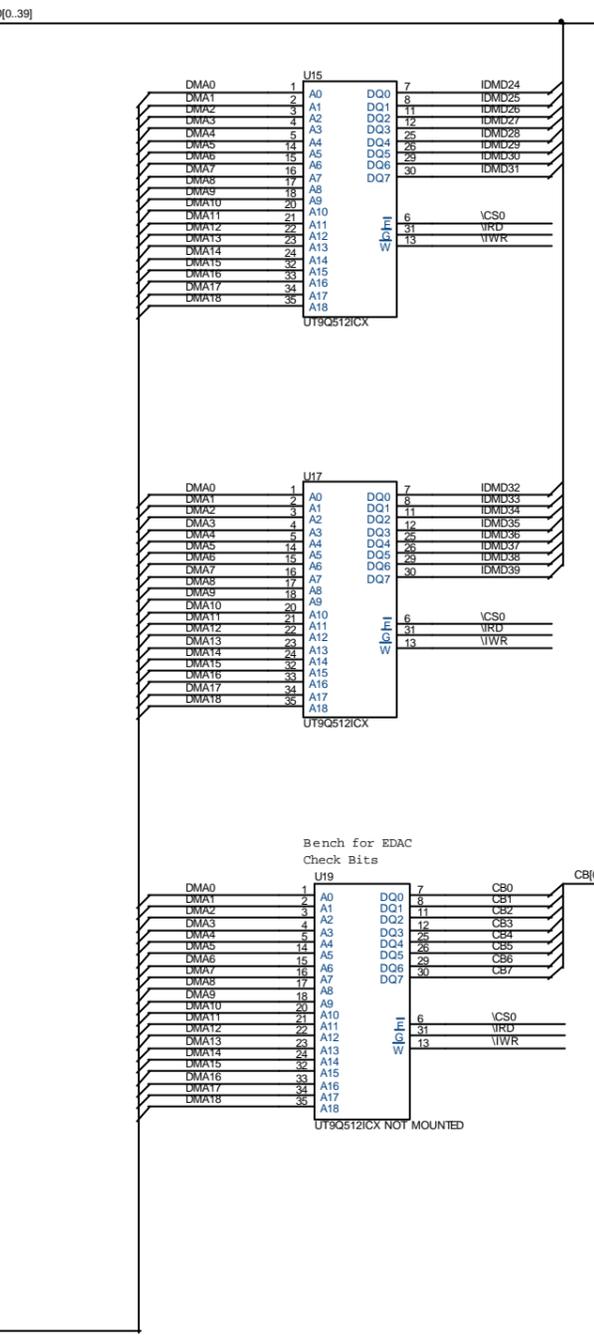
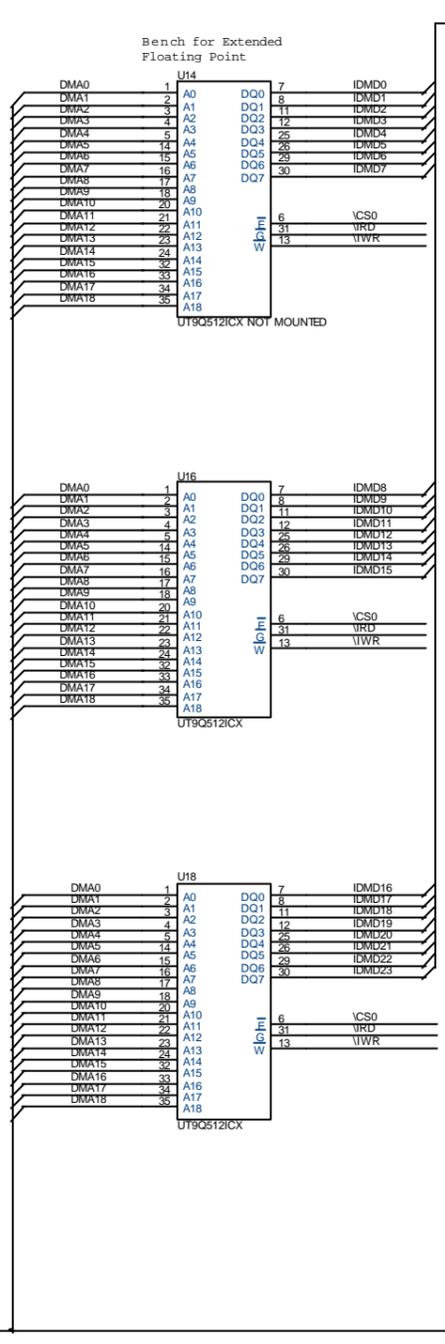
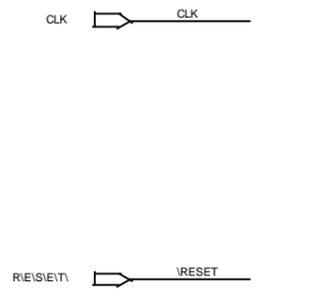
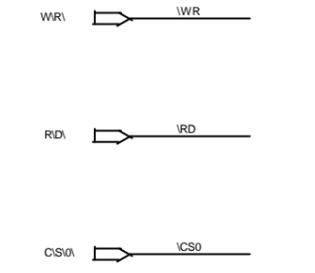
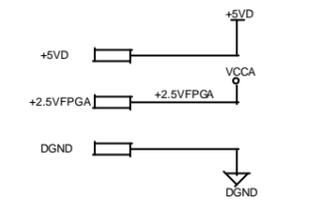


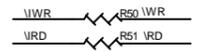
NOTES:
 KEEP THE PROBE CONNECTOR AS NEAR AS POSSIBLE TO THE CONTROL FPGA
 UT9Q512
 VDD: 9, 27
 VSS: 10, 28
 NC: 19, 36

EDAC40 (RT545X32S)
 VCCI (+5V): 12, 40, 60, 98, 115, 148, 164, 201
 VCCA: (+2.5VFPGA): 27, 41, 78, 114, 130, 145, 184
 GND: 1, 26, 28, 52, 77, 79, 105, 129, 131, 146, 157, 183, 185



If EDAC is present, do not mount

If EDAC is present, do not mount



REV	DATE	DRAWN	CHECK	ENG	FRASE	C.d.C.	CHANGE/AUTHORITY
CUSTOMER ID				EFFICIENCY		CARLO GAVAZZI SPACE	
DRAWING TITLE						SCALE	GEN. ITA. GEN. FA.
HSO/FIRST-DPU CPU BOARD Data Memory							
HIGH-ASSEMBLY				DRAWING NUMBER		SHEET OF	
DPU-EM-110.00.0				DPU-EM-110.020		4 8	