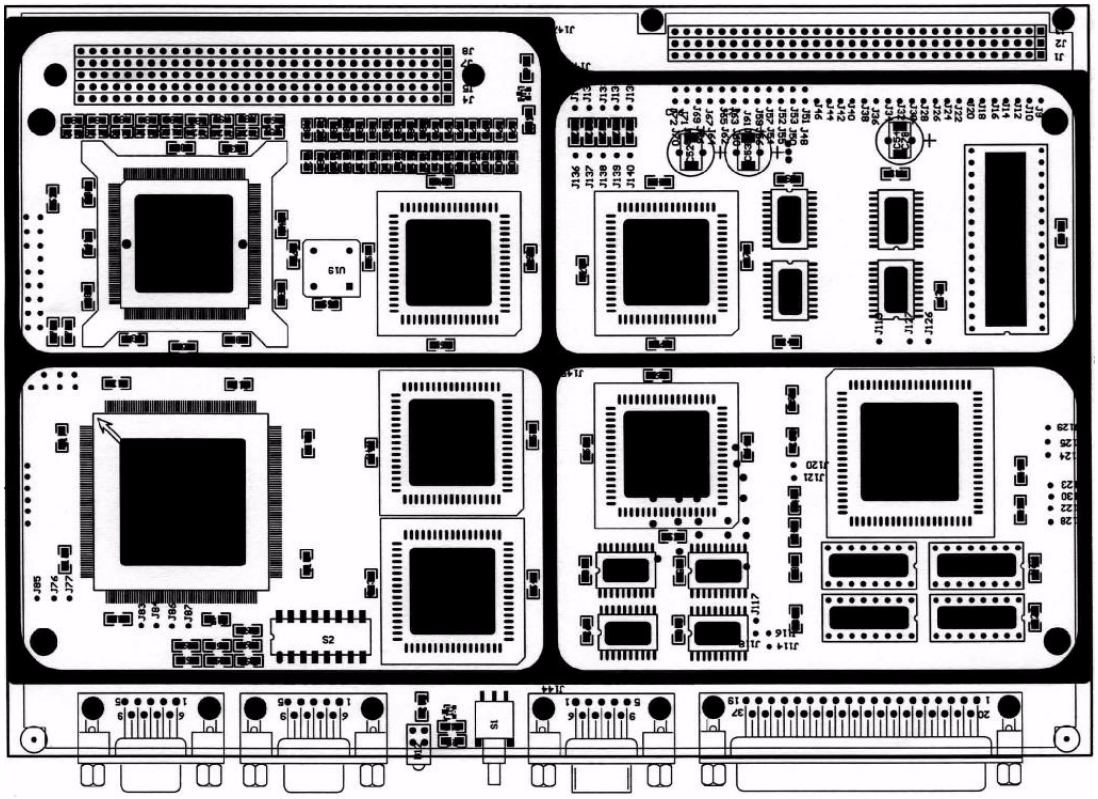
THARSYS

SPARC SC

SPACE EMBEDDED SINGLE BOARD COMPUTER FOR TEMIC ERC32 SINGLE CHIP



The THARSYS SPARC SC Single Board Computer is a 14 layers standard VME board built around the radiation tolerant ERC32 single chip by Temic Semiconductors.

THARSYS Single Board Computers, such as their SPARC RT SBC and Mil-1750 SBC, have been used for years by major aerospace firms and government organisations in the USA, Europe and Asia.

The THARSYS SPARC SC Single Board Computer reflects this experience and offers performances, flexibility and expansion capabilities, which makes the SPARC SC SBC an ideal basis for embedded space applications.

- ***Key features:***

- The processor ERC32 Single-Chip (TSC695E) includes on chip an Integer Unit, a Floating Point Unit, a Memory Controller and a DMA Arbiter.
- Operating frequency 25MHz with 1.10^{-4} frequency stability.
- 2-Mword of 15ns access time RAM (40-bit words).
- 8-Mbyte of FLASH memory.
- 512-kbyte of UV PROM or OTP PROM memory.
- Four 32-bit timers and one 16-bit timer.
- Watchdog.
- Eight RS422 and two RS232 serial interfaces.
- Interrupt controller with 41 external inputs.
- Wait states management.
- Error Detection and Correction mechanism.
- Up to 16-Mword RAM option.
- Temperature range: -40°C to 85°C.

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- ***Processing Unit:***

The TSC695E (ERC32 Single-Chip) is a high-performance 32-bit RISC embedded processor implementing the SPARC architecture V7 specification developed with the support of the European Space Agency.
Clocks: 25MHz or 12,5MHz can be dynamically selected by software.
Interrupt routing: 46 external interrupts.
Watchdog: one 1MHz counter is implemented in the Memory Controller.

- ***Wait states manager:***

The number of wait states is programmable for 8 device types. The user can select up to 3 wait states for RAM read and RAM write, up to 15 wait states for Extended RAM read/write, PROM read and 4 I/O peripheral read/write operations.

- ***Timers:***

The timers available are:
- General purpose timer (32-bit).
- Real time clock timer (32-bit).
- FPGA timer 1: 32-bit down counter (1µs accuracy).
- FPGA timer 2: 32-bit up counter providing a periodic external signal (100µs accuracy).
- FPGA timer 3: 16-bit down counter providing a periodic external signal with programmable duty cycle (10µs accuracy).

- ***I/O system:***

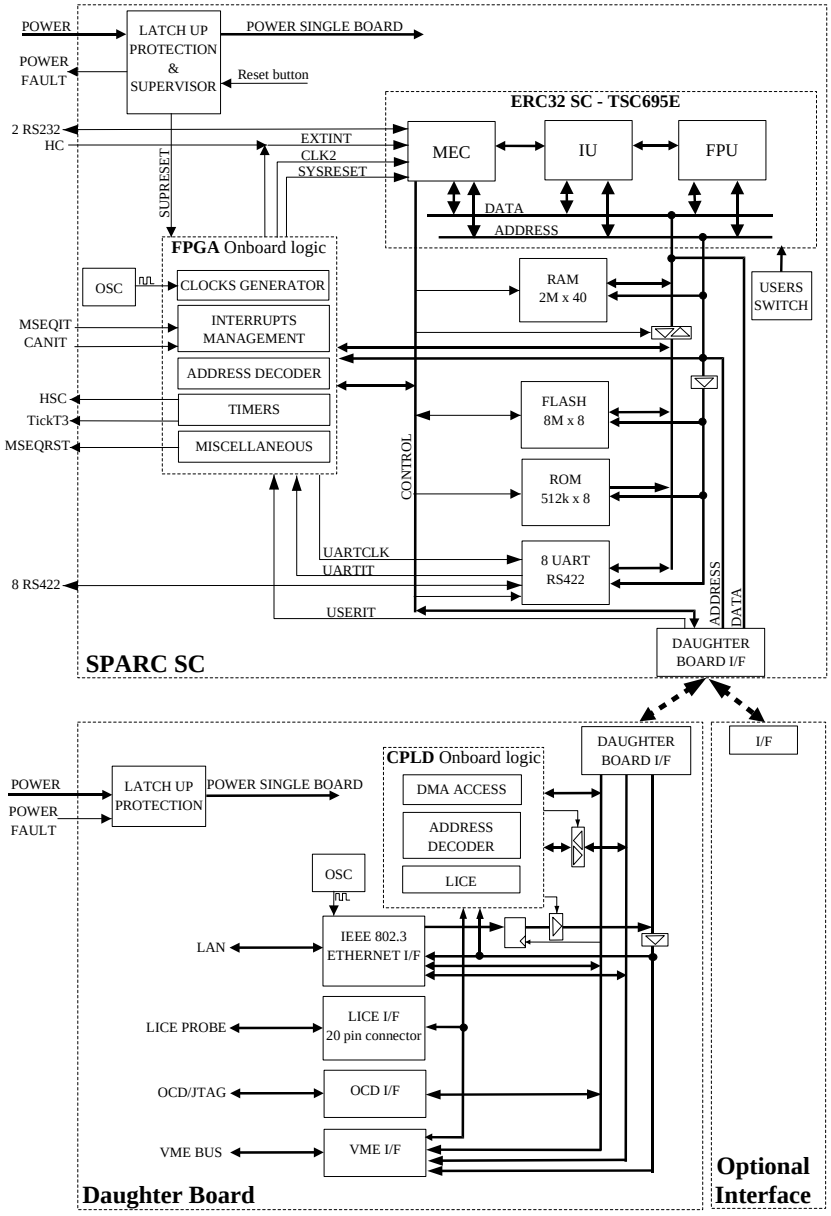
Serial interface: two RS232 and eight RS422 serial interfaces with programmable baud rates. Typical rates are 9600, 19200 or 38400 bauds.
Daughter board interface: address, data busses, main CPU and DMA signals provide extension capabilities.

- ***Memory system:***

RAM: 2-Mword of 15ns access time RAM. 40-bit word memory is provided for the parity and error detection and correction (EDAC) mechanisms. 16-Mword of RAM can be provided as an optional daughter board.
FLASH: 8-Mbyte of non-volatile memory.
PROM: 512-kbyte with GNU monitor (rdbmon) on DIL-32 socket.

- ***Dimensions:***

VME single slot (160mm x 233,35 mm).



Functional Diagram

- ***Private connector:***

Address, data busses, main CPU signals, DMA signals, external interrupts and periodic signals are available to the user on the 160 pins P1 VME connector.
Power is provided by the 96 pins P2 VME connector. CPU and FPGA JTAG signals are also available on this connector.

- ***Front panel:***

Power on and system available LEDs.
Reset push button.
Seven RS422 serial interfaces on one female DB37.
One RS422 serial interface on one male DB9.
Two RS232 serial interfaces on two female DB9.

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