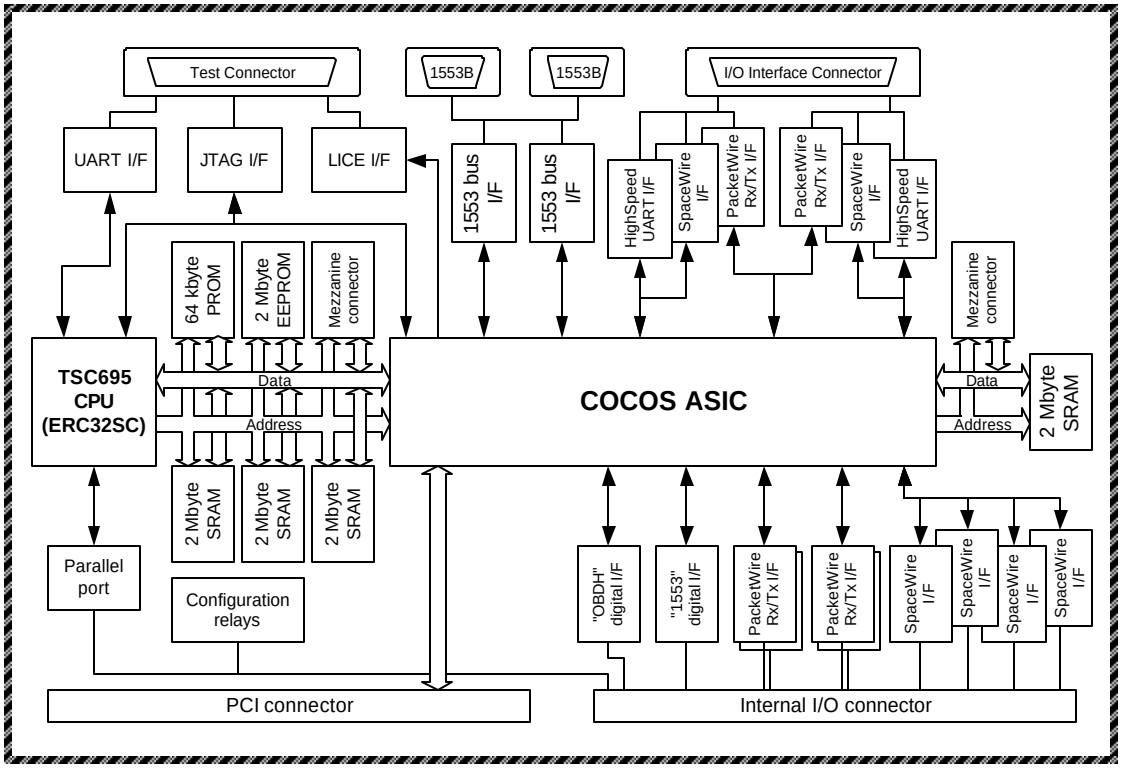
1. TIGER BOARD DESCRIPTION

1.1 Technical description

The processor is based on the TSC695 radiation hardened microprocessor from Atmel. The elements of the processor and memory functions is shown in the figure below.



The processor board has the following key characteristics:

The TSC695 processor

The processor used is a radiation hardened SPARC V7 processor specially designed for critical space applications. One of its main features is a very high degree of internal error detection. Up to 99% of internal errors are almost immediately detected and signalled to the outside world for proper handling. The CPU address, data and control buses are equipped with parity signals to allow for further immediate detection of CPU errors not covered by the internal mechanisms.

Processing capability

The CPU runs at 20 MHz where it delivers about 14 MIPS. It has a built-in IEEE-754 floating-point unit that, like the rest of the processor, includes support for concurrent error detection and testability.

Memory

The working memory for the processor consists of 6 Mbyte of EDAC-protected SRAM. Since the EDAC is included in the CPU it means that there are very few memory or wiring errors that will not be detected. Two data memory areas, defined by start and end addresses, can be write protected. Accesses to unimplemented memory areas are of course also detected and reported.
The boot software is implemented in 64 kbyte of PROM.

The application software may be stored in 2 Mbyte of E^2PROM with possibilities to patch. It is also possible to have the PROM removed and boot directly from the E^2PROM.
The memory may be extended using a mezzanine board extension connector. This mezzanine board may also contain a second COCOS chip with a lot of additional external interfaces.
There is also a working memory for the I/O ASIC (COCOS) that consists of 2 Mbyte of EDAC-protected SRAM which is also accessible by the processor. This is used as communication memory for the PCI and serial interfaces. It is possible to use the processor's working memory as communication memory as well. The COCOS ASIC then accesses the memory via DMA.

Interfaces

- Up to two high-rate UARTs with transfer rate from 150 baud up to 1.2 Mbaud are provided for typical control and data acquisition purposes.
- Dual MIL-STD-1553B buses with bus controller and bus monitor capabilities. One bus can also be remote terminal.
- Up to six SpaceWire (IEEE-1355.2) interfaces with LVDS. Two of these interfaces are available only if the high-rate UARTs are not used.
- Up to three PacketWire receiver links (synchronous serial links with clock, data, strobe and ready) with up to 20 Mbps data rate. Up to three PacketWire transmitter links with up to 20 Mbps data rate. If the high-rate UARTs or the external SpaceWire links are used, only the two internal PacketWire interfaces (2 Rx and 2 Tx) can be used.
- A 32-bit PCI 2.2 compliant back plane interface running at 20 MHz if used in CompactPCI Slot0 and running at up to 33 MHz when installed in other slots.
- In addition to the four PCI bus interrupts there are four additional interrupts. All four can be received through the backplane connector or two through the external connector and two trough the internal.

  All interfaces and interrupts are implemented in the COCOS ASIC developed by Saab Ericsson Space. The COCOS ASIC as also works as a support chip to the ERC32SC processor.

Test interface

Two RS-422 test UART interfaces for communication with a host computer during software development phases are implemented. It is also possible to connect a dedicated IEEE-1149.1 Test Access Port (JTAG) device for non-intrusive software debugging using CPU built-in debug function.

Power supplies

The processor board needs 5V and 3.3V from the backplane connector.

Mechanical interfaces

A mechanical frame is implemented to provide a sound mechanical and thermal environment.

Software

C and C++ with RTEMS operating system

Open Ravenscar Kernel with GNAT Ada compiler

1.2 Mechanical concept

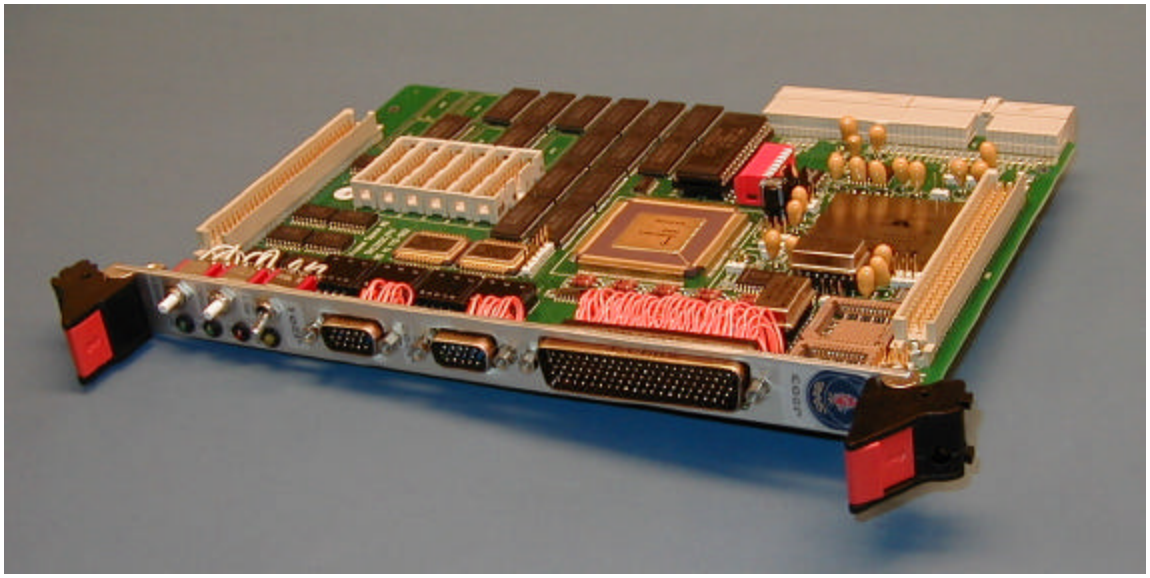
The design is implemented on a multi-layered printed circuit board (PCB). To allow efficient mounting of components on both sides of the PCB blind and buried vias are used. The PCB format is TBD mm and is equipped with a stiffener (also called frame) for mechanical support and thermal conduction. The frame is adapted to fit in the SE mechanical concept. The internal connectors to mate a back plane are two 174 pin CSD connectors, mounted to the opposite PCB side compared to the external connectors. The external connectors are one HDD-44 pin for I/O communication, two HDD-15 pin for 1553 communication and one HDD-44 socket as a test connector.

1.3 Budgets

Board size	256 x 186 mm
Module size	260 x 220 mm
Mass	≈ 900g incl mechanical frame and connectors

1.4 TSC695 CompactPCI Evaluation Board

The picture below shows an evaluation board developed by Saab Ericsson Space with the ERC32SC processor and an FPGA version of the COCOS ASIC with e.g. PCI, 1553B, SpaceWire, PacketWire and UART interfaces. It is fully compliant to be plugged into a 5 V CompactPCI system.



The evaluation board has reduced functionality but more RAM compared to the flight board. The board supports all the interfaces found on the flight board but due to constraints on the number of external connectors and the size of the FPGA, not all can be accommodated at the same time. A pair of Serial Link I/F can be configured to be PacketWire (Rx + Tx), two SpaceWire or two High Speed UARTs. The baseline is to have two PacketWire links, two SpaceWire links, two High Speed UARTs and one 1553B controller (BC/RT/BM) with dual buses (A & B). Other combinations are possible and are configurable during manufacturing.