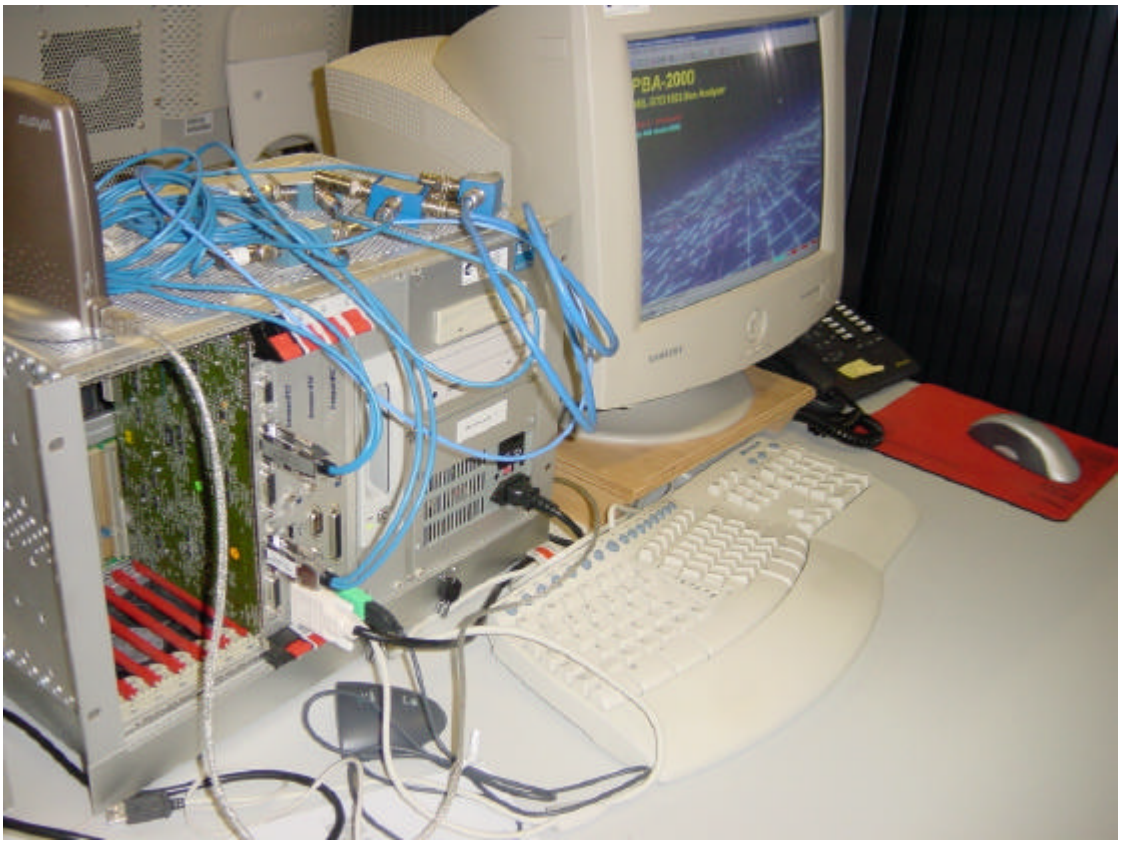
PBA-2000


DIRECT
DELL
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North Hills
Majestic

ABI - V6
1553 Interface

Features:

1 to 4 Dual Redundant 1553 Channels Featuring 100% Concurrent and Independent Operation:
- **Bus Controller**
- **31 Remote Terminals**
- **Dual Function Bus Monitor**

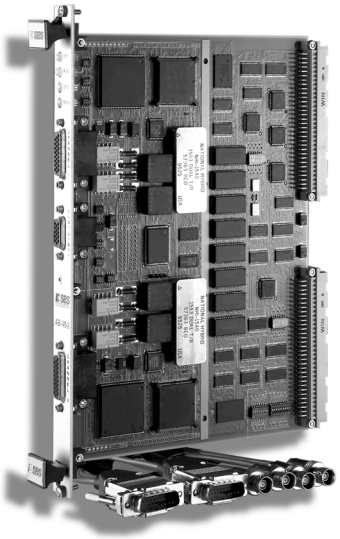
- **Bus Controller**
  Programmable Frame Lists
  BC - RT, RT - BC, RT - RT
  Mode Codes, Broadcasts, Time Delays

- **RT Functionality**
  RT Level Protocol Selection
  Definition Tables
  Programmable Response Time

- **Bus Monitor**
  Map Monitoring
  Sequential Monitoring
  Time Stamped, Double Buffered
  Error Tables & Definable Monitoring

- **Architecture**
  On-The-Fly Data Structures
  BC & RT Link Lists
  High Speed DSP
  Flexible Memory Structure
  Variable Voltage 1553 Transceivers

- **Software Support**
  No Cost Drivers & Libraries
  Including Source Code



The ABI-V6 interface provides a flexible, full function, one to four channel, dual redundant MIL-STD-1553 interface to the VMEbus system. This Advanced Bus Interface (ABI) architecture provides concurrent and independent operation of a Bus Controller (BC), 31 Remote Terminals (RT), and dual function Bus Monitoring (BM). The ABI-V6 interface equips the VMEbus system with a complete 1553 interface, including 1553A and/or 1553B selections, programmable BC frame lists, BC scheduling capabilities, RT response tables, pointer driven transmit and receive buffers, Map Monitoring, 100% Independent Sequential Bus Monitoring and extensive programmable event interrupts.

BC simulation structures consist of linked lists of 1553 command messages: BC-to-RT, RT-to-BC, RT-to-RT, mode code, broadcast and time delay block transmissions. RT simulation is defined by a simple series of pointers to RT definition tables which subsequently point to control data buffers. Bus activity to be monitored is definable in both the Map and Sequential monitoring modes, providing user defined linked lists of data buffers and sequential, time stamped and double buffered 1553 activity respectively. Both monitoring modes perform broad error monitoring, and provide a comprehensive error table that can be read at any time by the host processor.

Hardware Overview

The ABI interface is based upon an advanced high speed DSP, programmable logic and dual port RAM to deliver a highly reliable hardware platform that is feature rich and user friendly. Through the 128K bytes of dual port RAM per channel, the host processor has access to set up, monitor, and change the 1553 interface data structures at any time. Link-list memory architecture allows the user to structure interface memory usage for the maximum in flexibility and usefulness. The ABI-V6 provides storage for on-board firmware via Flash Memory.

Software Support Overview

SBS distributed software includes host processor device drivers to the dual port control and data structures, as well as, an application layer to these structures. Low level drivers and C libraries with source code are provided with the interface, at no cost.

Avionics and Telemetry Products, 2400 Louisiana Boulevard NE, #5-600, Albuquerque, NM 87110
1-800-SBS-1553 • 1-800-DATABUS
Tel (505) 875-0600 • Fax (505) 875-0400 • Email: sbssale@sbs.com • Internet: www.sbs-avionics.com

ABI - V6
Interface Specifications

ABI Functionality:

Bus Controller (BC)

- BC Retry
- Minor Frame Timing and Message Scheduling
- Programmable Intermessage Gap
- Programmable Delay Gaps and Null BC Blocks
- Multiple BC Data Buffers in a Link-List Structure
- Programmable RT No-Response Time-Out
- BC Dump Feature

Remote Terminals (RTs)

- 31 RTs and All Subaddresses Supported
- Transmit/Receive Buffers for Each Subaddress
- Multiple RT Data Buffers in a Link-List Structure
- Programmable RT Response Time and No-Response Selection

Map Monitoring

- Multiple Linked Buffers for Each Transmit/Receive Subaddress
- Mapped Buffers Read by Host Processor as Time Permits
- Number of Buffers per Transmit/Receive Subaddress is Programmable or User Definable to Account for Various Host Speeds

Sequential Monitoring

- Host Driver Selected Messages are Double Buffered
- Messages Timed Stamped
  1µSec 32 bit Clock or
  48 bit IRIG-B Clock *(optional)*
- Standard Firmware Performs Broad Error Monitoring
- Comprehensive Error Table Readable at Any Time by Host Processor

Self Test:

- Power-up Test with Status Register Report
- BIT - RAM and Encoder/Decoder Test
- Run-time Health Status Register
- "Unit Test" Program for 1553 Bus Functionality

Inputs/Outputs:

- Bi-directional External Trigger
- IRIG Clock Input *(optional)*
- Variable Voltage 1553 Outputs: 0-22V p-p
- External TTL/RS-422 System Clock Input

SBS guarantees a successful integration which includes no-cost phone, e-mail and ftp support, with on-site customer visits as necessary.

VME Functionality:

- VMEbus System
- D16/D32 Single Cycle Transfers
- D32/D64 BLT
- A24/A32 Addressing
- D08 Interrupts
- Memory Mapped
- Selectable Interrupt Requests
- Onboard Firmware Storage via Flash Memory

Interface Connections:

- $DB26_F$ to Coupling Harness -
  Cable Assembly: CA-2097
- Coupling Harness to Bus and I/O Connectors
- $DB15_F$ I/O Connector
- $BJ77_F$ Triax Connector to 1553 Bus

Interface Card Specifications:

- Maximum Power Consumption - Single Channel:
  5V @ 1.0 Amps
  12V @ 250 mAmps
- Maximum Power Consumption - Dual Channel:
  5V @ 1.5 Amps
  12V @ 500 mAmps
- Standard Commercial Operating Temperature:
  0° C to +60° C
  Designed to ≤ 95% rH non-condensing
- Optional Extended Operating Temperature:
  -40° C to +85° C
  Designed to ≤ 95% rH non-condensing
- Mechanical - Single Channel or Dual Channel:
  Standard 6u x 160mm Size

Software & Documentation Support:

- Low Level Drivers & C Library Sets with Source Code
- Borland and Microsoft C Compiler Compatible
- Hardware and Library Manual Set

Customer Support:

- Two Year Warranty
- Extended Warranties Available
- Driver and Library Upgrades
- Over 18 Operating Systems Supported on Various Platforms

Interface Model Numbers:

ABI-V6-1	Single Channel 1553 to VME Interface
ABI-V6-2	Dual Channel 1553 to VME Interface
ABI-V6-3	Triple Channel 1553 to VME Interface
ABI-V6-4	Quadruple Channel 1553 to VME Interface
ABI-V6XT-1	Single Channel 1553 to VME, Extended Temp.
ABI-V6XT-2	Dual Channel 1553 to VME, Extended Temp.
ABI-V6XT-3	Triple Channel 1553 to VME, Extended Temp.
ABI-V6XT-4	Quadruple Channel 1553 to VME, Extended Temp.
IRIG	IRIG B Time Receiver (Add "/IRIG" to Product Number)

- **Option Conformal Coat**

SBS Technologies, Inc.

SBS Technologies Inc., Avionics and Telemetry Products

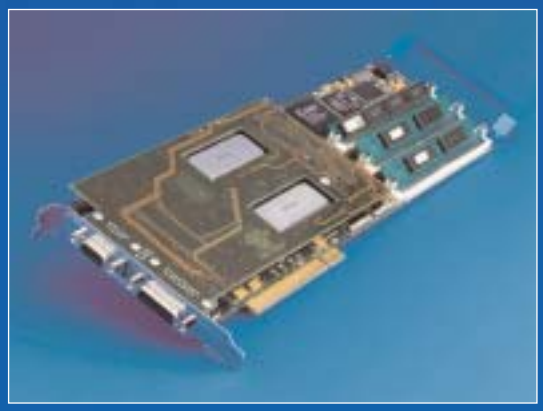
2400 Louisiana Boulevard NE, #5-600, Albuquerque, NM 87110 • 1-800-SBS-1553 • 1-800-DATABUS

Tel (505) 875-0600 • Fax (505) 875-0400 • Email: sbssale@sbs.com • Internet: www.sbs-avionics.com

Specifications subject to change without notice. Rev. 01/08/01

API1553-1/2

Single or Dual Stream MIL-STD-1553A/B
Test & Simulation Modules for PCI



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API1553-1/2

Single or Dual Stream MIL-STD-1553A/B Test & Simulation Modules for PCI

General Features

The API1553-1/2 is part of a new family of PCIbus cards offering full function Test, Simulation, Monitoring and databus analyser functions for MIL-STD-1553A/B applications. Two independent dual redundant MIL-STD-1553A/B streams are provided on the API1553-2 module (full length) and one single dual redundant MIL-STD-1553A/B stream on the API1553-1 module (short length).

The API1553-1/2 can be used for Protocol Testing and Simulation of MIL-STD-1553A/B Bus Controller, Multiple Remote Terminals and Chronological Monitoring at full bus load. All operations are performed concurrently with no degradation of performance in any operating mode. The API1553-1/2 module incorporates full protocol error injection and detection features with software programmable output amplitude and bus coupling modes of the electrical bus signals. The module fully supports the Protocol Testing requirements defined by the RT and BC Production Test Plans according to SAE-AS 4112 / 4114.

An on board IRIG-B time decoder / generator allows users to accurately synchronise single or multiple API1553-1/2 modules to a common time source.

The use of an Application Support Processor (ASP) executing the Driver Software allows application specific functions to be processed on-board significantly off-loading the host PC processor and PCIbus. This new concept allows users to implement system level functionality on a single interface card.

The API1553-1/2 uses a 'Common Core' hardware design utilising multiple RISC processors. A Physical Bus Interface (PBI) daughter board provides MIL-STD-1553A/B bus connections including a resistive terminated bus network.

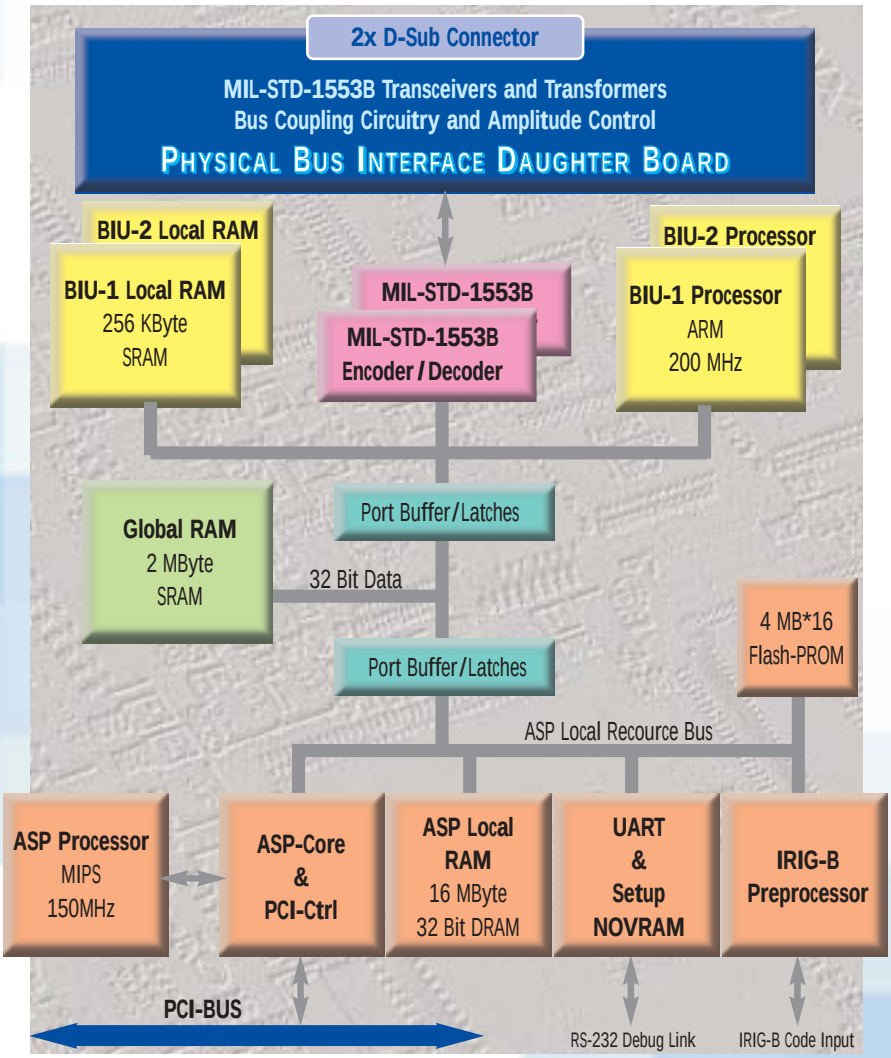
The API1553-1/2 module operates with the optionally provided PBA-2000 MIL-STD-1553B Databus Analyser Software for Windows.

Bus Controller

The API1553-1/2 provides real time Bus Controller functions on one or two dual redundant MIL-STD-1553A/B buses concurrently with Multiple RT and Chronological Monitor operation. A 200MHz RISC Processor provides true simulation of Bus Controller operations without host computer interaction.

Key features of the Bus Controller Mode include:

- Autonomous Operation including sequencing of Minor/ Major Frames
- Support for acyclic message insertion/deletion
- Programmable BC Retry without host interaction
- Full Error Injection down to word and bit level (AS4112 Compliant)
- Multi-Buffering for Data Consistency and Message Multiplexing
- Synchronisation of BC operation to external trigger inputs
- 4 µsec Intermessage Gaps



Multiple Remote Terminal

The API1553-1/2 simulates up to 32 Remote Terminals including all sub-addresses on one or two MIL-STD1553A/B bus systems concurrently with BC and Chronological Monitor operation. Alternately each of the 31 RT's can operate in a message oriented 'Mailbox Monitor Mode' to monitor non-simulated RT's.

Key features of the RT Mode include:

- Programmable RT Response Time down to 4 µsecs for each simulated RT
- Programmable & Intelligent Response to Mode Codes
- Full Error Injection down to word and bit level (AS4112 Compliant)
- Multi-Buffering with Real Time Data Buffer Updates

Chronological Bus Monitor

The API1553-1/2 offers single or dual stream bus monitoring and analysis with programmable trigger and capture features. The Bus Monitor provides accurate Time Tagging of all bus traffic to 1 µs resulution including response time and grap time measurements down to 0.25 µs resolution concurrently with BC and Multiple RT operation

Key features of the Chronological Monitor include:

- 100% Data Capture on two streams at full bus rates
- Autonomous message synchronisation and Full Error Detection
- Two Static/ Dynamic Complex Triggers with up to 8 sequences
- Message Filter and Selective Capture
- Bus Activity recording independent from trigger and capture mode
- External Trigger Inputs and Outputs
- Programmable Response Time Out

Bus Replay

The API1553-1/2 module is able to electrically reconstruct previously recorded MIL-STD-1553A/B databus traffic physically to the bus with excellent timing accuracy. Recorded data files can be selected for Physical Bus Replay with the ability to disable any or all RT responses from the record file to perform systems integration and test.

IRIG-B Time Code Decoder

An on board IRIG-B time decoder and generator allows synchronization of MIL-STD-1553A/B bus traffic using single or multiple API1553-1/2 modules. Multiple API1553-1/2 modules can be synchronised using one common IRIG-B time source or the on-board Time Code Generator of one API1553-1/2 module as the reference for accurate correlation of data across multiple MIL-STD-1553A/B data streams.

Application Support Processor

A 150 MHz Application Support Processor (ASP) provides unique on module processing functions typically provided by host PC processing systems.

Operational features include:

- Driver Software Execution on the board
- Control of RS232C debug Port for Firmware Updates
- Dynamic Data Generation
- Automatic Test Sequence Generation
- User Application processing on-board

MIL-STD-1553A/B Physical Bus Interface

A Physical Bus Interface Daughter board (PBI) provides MIL-STD-1553A/B transformer or direct bus coupling with variable output transceivers and a resistive bus termination to enable the direct connection of external BC or RT devices. The coupling mode to the external bus system is software programmable.

Driver Software Support

Since the Driver Software resides on the API1553-1/2 module, a High Level Application Interface is provided which is compatible with Windows 95/98 and Windows NT/2000. Host applications can be written in MSVC, Visual Basic, Delphi, Borland C++ etc. A LabVIEW application interface and LabWindows/CVI Function Panels are also provided.

RIGHT ON TARGET

Technical Data

Rev. 3. June 2001

Sub-System Interface
PCIbus Master & Slave (Revision 2.1)

Processors
Two 32-Bit, 200MHz ARM Processors
One 64-Bit, 150MHz MIPS Processor

Memory
API1553-1: 1 MByte Global RAM
16 MByte ASP RAM
API1553-2: 2 MByte Global RAM
16 MByte ASP RAM

Encoder/Decoder
One MIL-STD-1553A/B Encoder/Decoder per BIU with full error injection & detection capability

Time Tagging
46 Bit absolute IRIG-B Time with 1µsec resolution

Physical Bus Interface (PBI):
One or Two Dual Redundant MIL-STD-1553A/B Transceivers with Variable Output Amplitude, Programmable Bus coupling mode with on-board terminated Bus Network

Connectors
PCIbus Standard backplane connector
9 way D-Sub for MIL-STD-1553A/B connections
15 way D-Sub for Trigger and Timecode I/O

Dimensions
API1553-1: 175 mm x 107 mm “short length” PCI Format
API1553-2: 312 mm x 107 mm “full length” PCI Format

Power Consumption
API1553-1: 12.5 Watts typical @ 5V
API1553-2: 17.5 Watts typical @ 5V

Operating Temp. Range:
Standard: 0°C ... +45°C ambient
Extended: -15°C ... +60°C ambient

Storage Temperature Range:
-40°C ... + 85°C ambient

Humidity
0 to 95% non-condensing

Ordering Information

API1553-1
Single Stream, Dual Redundant PCIbus to MIL-STD-1553A/B Interface: BC, Multi-RT Simulator with Mailbox & Chronological Monitor including IRIG-B Time Decoder. 1 MB Global RAM, 16 MB ASP RAM

API1553-2
Dual Stream, Dual Redundant PCIbus to MIL-STD-1553A/B Interface: BC, Multi-RT Simulator with Mailbox & Chronological Monitor including IRIG-B Time Decoder. 2 MB Global RAM, 16 MB ASP RAM

API1553S-1, API1553S-2
Simulator only configuration available. Single Stream or Dual Stream.

API1553M-1, API1553M-2
Monitor only configuration available. Single Stream or Dual Stream.

ACB1553-PCI-1
Ready Made Adapter Cable. D-Sub to two TWINAX Connectors. 2m length. For all variants of API1553-1 cards.

ACB1553-PCI-2
Ready Made Adapter Cable. D-Sub to four TWINAX Connectors. 2m length. For all variants of API1553-2 cards.

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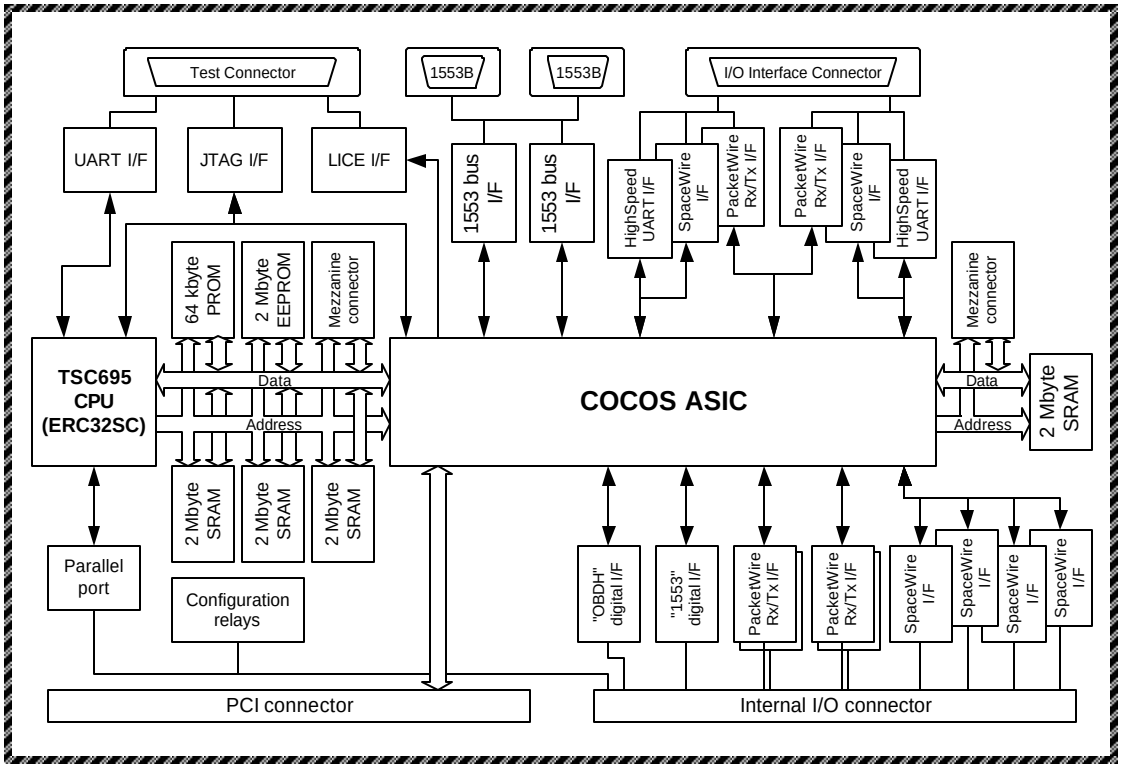
Right on Target

1. TIGER BOARD DESCRIPTION

1.1 Technical description

The processor is based on the TSC695 radiation hardened microprocessor from Atmel. The elements of the processor and memory functions is shown in the figure below.



The processor board has the following key characteristics:

The TSC695 processor

The processor used is a radiation hardened SPARC V7 processor specially designed for critical space applications. One of its main features is a very high degree of internal error detection. Up to 99% of internal errors are almost immediately detected and signalled to the outside world for proper handling. The CPU address, data and control buses are equipped with parity signals to allow for further immediate detection of CPU errors not covered by the internal mechanisms.

Processing capability

The CPU runs at 20 MHz where it delivers about 14 MIPS. It has a built-in IEEE-754 floating-point unit that, like the rest of the processor, includes support for concurrent error detection and testability.

Memory

The working memory for the processor consists of 6 Mbyte of EDAC-protected SRAM. Since the EDAC is included in the CPU it means that there are very few memory or wiring errors that will not be detected. Two data memory areas, defined by start and end addresses, can be write protected. Accesses to unimplemented memory areas are of course also detected and reported.
The boot software is implemented in 64 kbyte of PROM.

The application software may be stored in 2 Mbyte of E^2PROM with possibilities to patch. It is also possible to have the PROM removed and boot directly from the E^2PROM.
The memory may be extended using a mezzanine board extension connector. This mezzanine board may also contain a second COCOS chip with a lot of additional external interfaces.
There is also a working memory for the I/O ASIC (COCOS) that consists of 2 Mbyte of EDAC-protected SRAM which is also accessible by the processor. This is used as communication memory for the PCI and serial interfaces. It is possible to use the processor's working memory as communication memory as well. The COCOS ASIC then accesses the memory via DMA.

Interfaces

- Up to two high-rate UARTs with transfer rate from 150 baud up to 1.2 Mbaud are provided for typical control and data acquisition purposes.
- Dual MIL-STD-1553B buses with bus controller and bus monitor capabilities. One bus can also be remote terminal.
- Up to six SpaceWire (IEEE-1355.2) interfaces with LVDS. Two of these interfaces are available only if the high-rate UARTs are not used.
- Up to three PacketWire receiver links (synchronous serial links with clock, data, strobe and ready) with up to 20 Mbps data rate. Up to three PacketWire transmitter links with up to 20 Mbps data rate. If the high-rate UARTs or the external SpaceWire links are used, only the two internal PacketWire interfaces (2 Rx and 2 Tx) can be used.
- A 32-bit PCI 2.2 compliant back plane interface running at 20 MHz if used in CompactPCI Slot0 and running at up to 33 MHz when installed in other slots.
- In addition to the four PCI bus interrupts there are four additional interrupts. All four can be received through the backplane connector or two through the external connector and two trough the internal.

  All interfaces and interrupts are implemented in the COCOS ASIC developed by Saab Ericsson Space. The COCOS ASIC as also works as a support chip to the ERC32SC processor.

Test interface

Two RS-422 test UART interfaces for communication with a host computer during software development phases are implemented. It is also possible to connect a dedicated IEEE-1149.1 Test Access Port (JTAG) device for non-intrusive software debugging using CPU built-in debug function.

Power supplies

The processor board needs 5V and 3.3V from the backplane connector.

Mechanical interfaces

A mechanical frame is implemented to provide a sound mechanical and thermal environment.

Software

C and C++ with RTEMS operating system

Open Ravenscar Kernel with GNAT Ada compiler

1.2 Mechanical concept

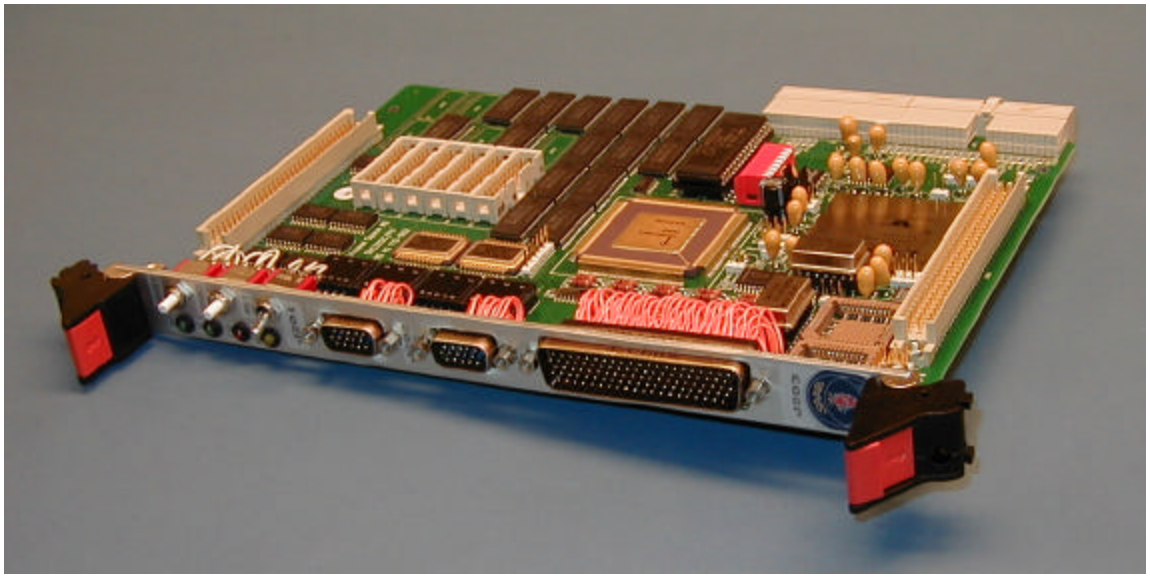
The design is implemented on a multi-layered printed circuit board (PCB). To allow efficient mounting of components on both sides of the PCB blind and buried vias are used. The PCB format is TBD mm and is equipped with a stiffener (also called frame) for mechanical support and thermal conduction. The frame is adapted to fit in the SE mechanical concept. The internal connectors to mate a back plane are two 174 pin CSD connectors, mounted to the opposite PCB side compared to the external connectors. The external connectors are one HDD-44 pin for I/O communication, two HDD-15 pin for 1553 communication and one HDD-44 socket as a test connector.

1.3 Budgets

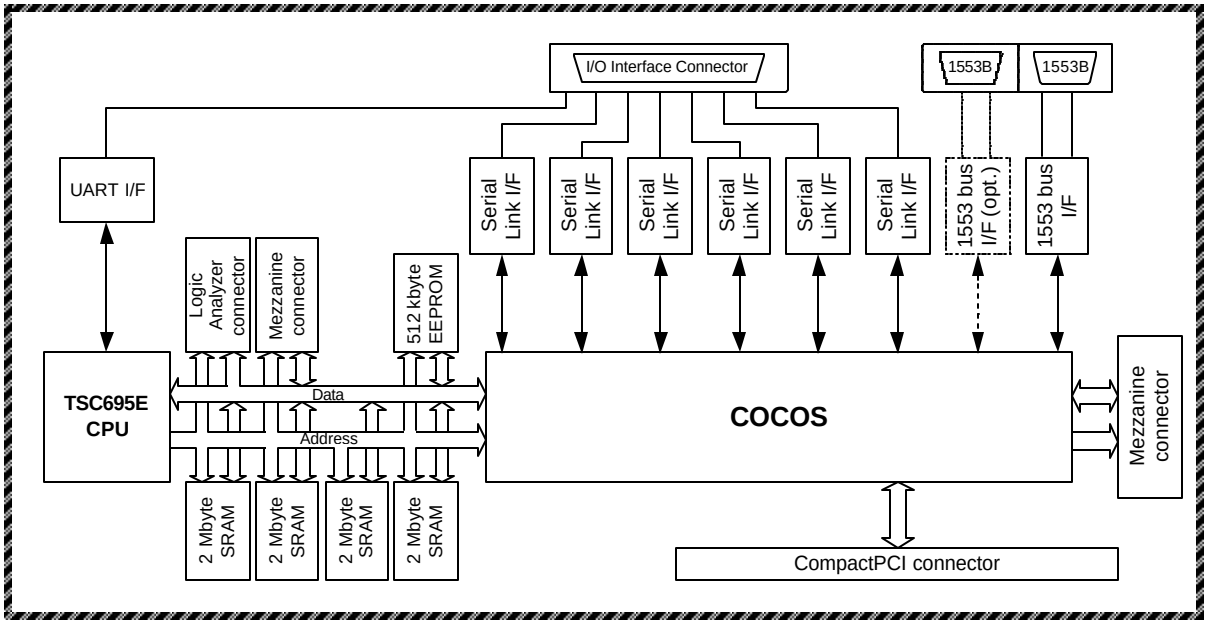
Board size	256 x 186 mm
Module size	260 x 220 mm
Mass	≈ 900g incl mechanical frame and connectors

1.4 TSC695 CompactPCI Evaluation Board

The picture below shows an evaluation board developed by Saab Ericsson Space with the ERC32SC processor and an FPGA version of the COCOS ASIC with e.g. PCI, 1553B, SpaceWire, PacketWire and UART interfaces. It is fully compliant to be plugged into a 5 V CompactPCI system.



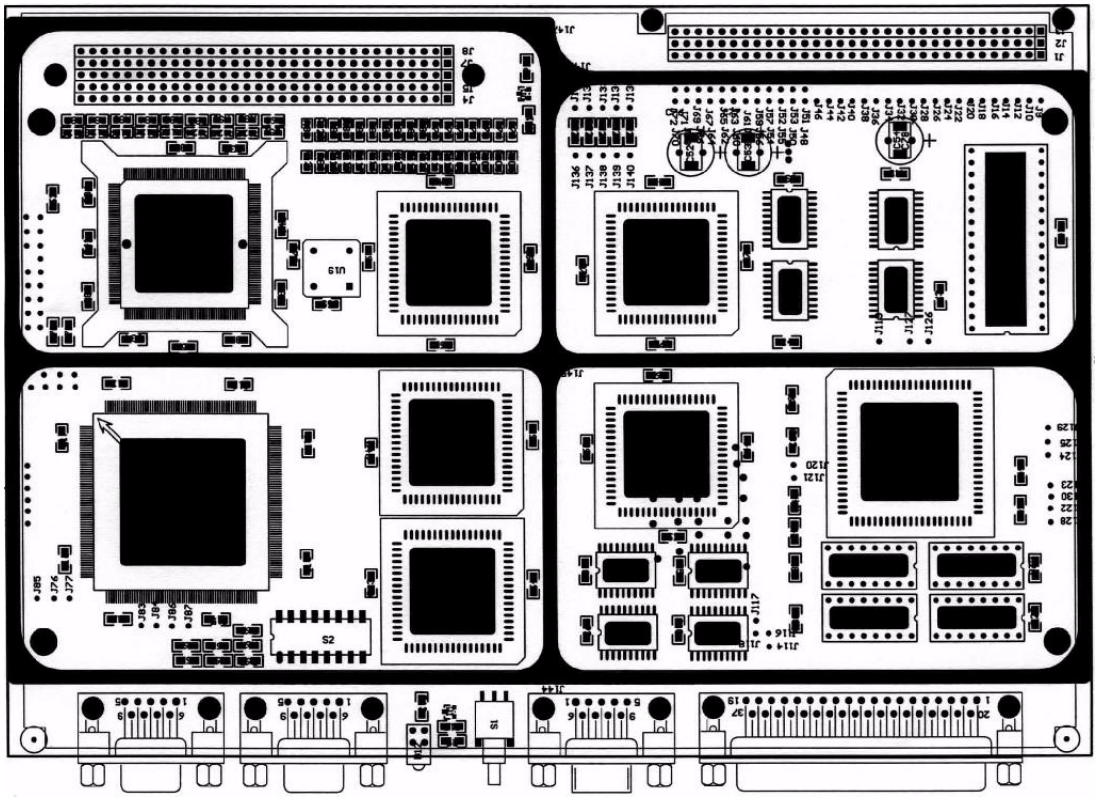
The evaluation board has reduced functionality but more RAM compared to the flight board. The board supports all the interfaces found on the flight board but due to constraints on the number of external connectors and the size of the FPGA, not all can be accommodated at the same time. A pair of Serial Link I/F can be configured to be PacketWire (Rx + Tx), two SpaceWire or two High Speed UARTs. The baseline is to have two PacketWire links, two SpaceWire links, two High Speed UARTs and one 1553B controller (BC/RT/BM) with dual buses (A & B). Other combinations are possible and are configurable during manufacturing.



THARSYS

SPARC SC

SPACE EMBEDDED SINGLE BOARD COMPUTER FOR TEMIC ERC32 SINGLE CHIP



The THARSYS SPARC SC Single Board Computer is a 14 layers standard VME board built around the radiation tolerant ERC32 single chip by Temic Semiconductors.

THARSYS Single Board Computers, such as their SPARC RT SBC and Mil-1750 SBC, have been used for years by major aerospace firms and government organisations in the USA, Europe and Asia.

The THARSYS SPARC SC Single Board Computer reflects this experience and offers performances, flexibility and expansion capabilities, which makes the SPARC SC SBC an ideal basis for embedded space applications.

- ***Key features:***

- The processor ERC32 Single-Chip (TSC695E) includes on chip an Integer Unit, a Floating Point Unit, a Memory Controller and a DMA Arbiter.
- Operating frequency 25MHz with 1.10^{-4} frequency stability.
- 2-Mword of 15ns access time RAM (40-bit words).
- 8-Mbyte of FLASH memory.
- 512-kbyte of UV PROM or OTP PROM memory.
- Four 32-bit timers and one 16-bit timer.
- Watchdog.
- Eight RS422 and two RS232 serial interfaces.
- Interrupt controller with 41 external inputs.
- Wait states management.
- Error Detection and Correction mechanism.
- Up to 16-Mword RAM option.
- Temperature range: -40°C to 85°C.

THARSYS - 7 bis, Rue de Partanaïs - 31650 Saint Orens de Gameville - FRANCE
Phone : +33 (0)5 61 000 888 - Fax : +33 (0)5 61 000 880 - Email : tharsys@csi.com

- ***Processing Unit:***

The TSC695E (ERC32 Single-Chip) is a high-performance 32-bit RISC embedded processor implementing the SPARC architecture V7 specification developed with the support of the European Space Agency.
Clocks: 25MHz or 12,5MHz can be dynamically selected by software.
Interrupt routing: 46 external interrupts.
Watchdog: one 1MHz counter is implemented in the Memory Controller.

- ***Wait states manager:***

The number of wait states is programmable for 8 device types. The user can select up to 3 wait states for RAM read and RAM write, up to 15 wait states for Extended RAM read/write, PROM read and 4 I/O peripheral read/write operations.

- ***Timers:***

The timers available are:
- General purpose timer (32-bit).
- Real time clock timer (32-bit).
- FPGA timer 1: 32-bit down counter (1µs accuracy).
- FPGA timer 2: 32-bit up counter providing a periodic external signal (100µs accuracy).
- FPGA timer 3: 16-bit down counter providing a periodic external signal with programmable duty cycle (10µs accuracy).

- ***I/O system:***

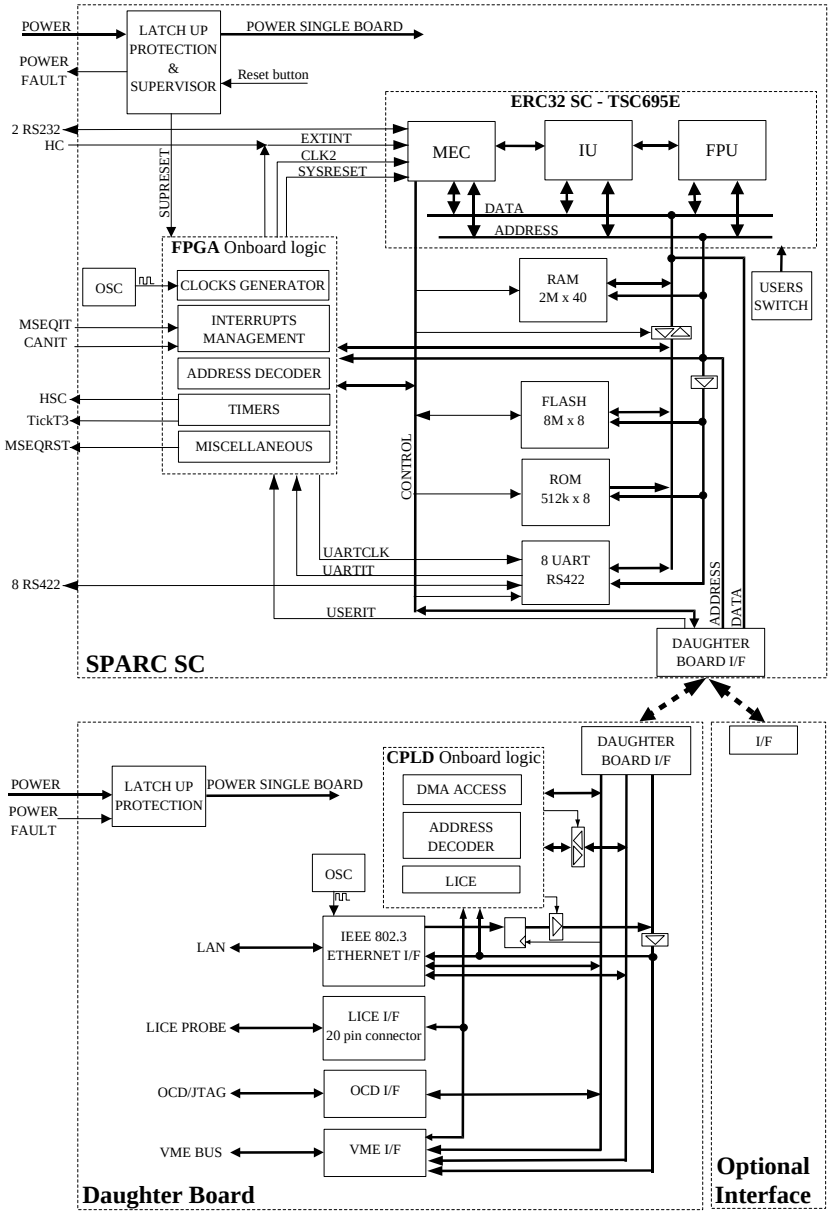
Serial interface: two RS232 and eight RS422 serial interfaces with programmable baud rates. Typical rates are 9600, 19200 or 38400 bauds.
Daughter board interface: address, data busses, main CPU and DMA signals provide extension capabilities.

- ***Memory system:***

RAM: 2-Mword of 15ns access time RAM. 40-bit word memory is provided for the parity and error detection and correction (EDAC) mechanisms. 16-Mword of RAM can be provided as an optional daughter board.
FLASH: 8-Mbyte of non-volatile memory.
PROM: 512-kbyte with GNU monitor (rdbmon) on DIL-32 socket.

- ***Dimensions:***

VME single slot (160mm x 233,35 mm).



Functional Diagram

- ***Private connector:***

Address, data busses, main CPU signals, DMA signals, external interrupts and periodic signals are available to the user on the 160 pins P1 VME connector.
Power is provided by the 96 pins P2 VME connector. CPU and FPGA JTAG signals are also available on this connector.

- ***Front panel:***

Power on and system available LEDs.
Reset push button.
Seven RS422 serial interfaces on one female DB37.
One RS422 serial interface on one male DB9.
Two RS232 serial interfaces on two female DB9.

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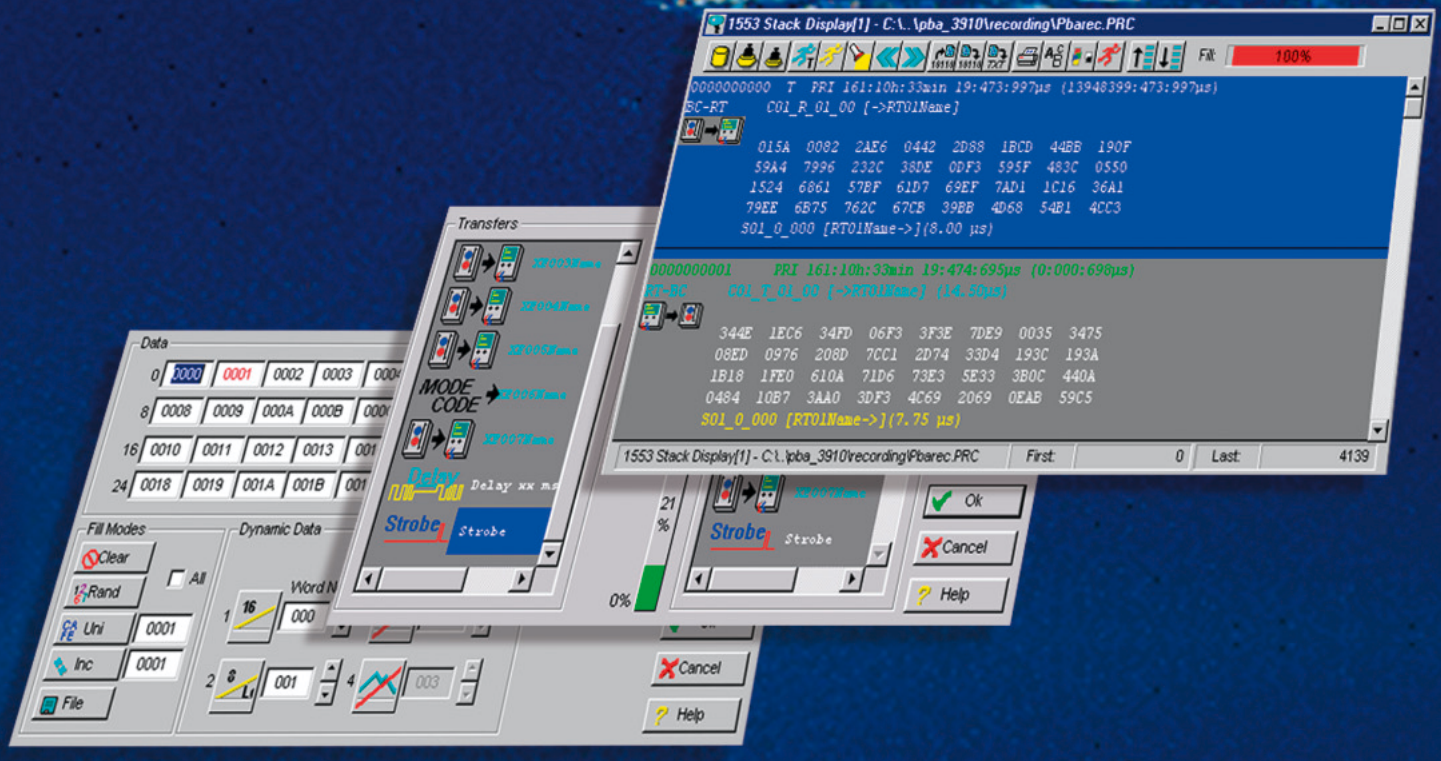
PBA-2000

PBA-2000-NET

MIL-STD-1553A/B Databus Analyser Software for Windows™



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PBA-2000 PBA-2000-NET

MIL-STD-1553A/B Databus Analyser Software for Windows™

The PBA-2000 is a powerful Windows based MIL-STD-1553A/B Databus Analyser and Systems Integration software package for use with AIM´s MIL-STD-1553A/B modules. An intuitive graphical user interface provides the ability to easily set-up complex Bus Controller, Multiple Remote Terminals, Bus Monitoring, Bus Recording and Physical Bus Replay functions. All operations can be performed concurrently using multiple Windows. External custom applications, including real time BC or RT simulations can be interfaced to the PBA-2000 Software using the 'Remote Control Interface'.

The PBA-2000 can support the test and integration of up to 16 dual redundant MIL-STD-1553A/B buses in single PC system. The PBA-2000-NET is optionally available to support the new Network Solutions family of Databus Analysers which allows multiple users connected via an network (Ethernet).

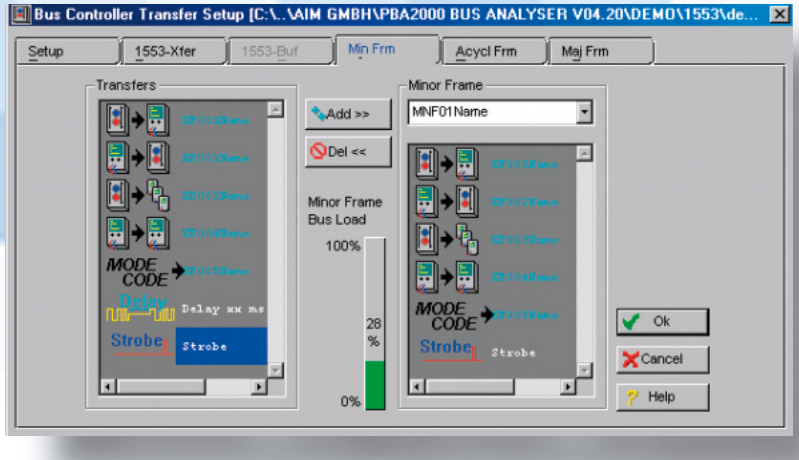
Extensive use of pop up menus, button bars, accelerator keys and on-line context sensitive help makes the PBA-2000 the most user friendly and easy to use Databus Analyser for MIL-STD-1553A/B testing.

General Features

- **Windows Multiple Document Interface**
- **System Status Display for Quick Look Analysis & Control**
- **Real Time Recording from Multiple Streams to PC hard disk**
- **Physical Bus Replay accurately Reconstructs your recordings**
- **Full Protocol Error Injection/ Detection in accordance with AS4112**
- **IRIG-B Time Correlation across Multiple Buses**
- **Save/Load Screen Layouts and Project Files**
- **Remote Set-Up using ASCII Files**
- **Optional Client/Server based PBA-2000-NET for remote control via a LAN**
- **Optional ParaView Software for Parameter Display, Control and Post Analysis**

Bus Controller Mode

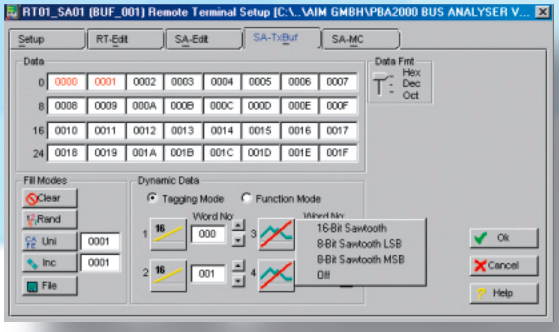
PBA-2000 BC mode supports all MIL-STD-1553A/B transfer types including Broadcast Commands, Mode Codes, Acyclic Transfers and Automatic Service Request handling. Users can easily add, edit or delete each BC transfer and build Major/ Minor Frames from the transaction lists. The use of multi buffering provides real time BC data simulations including static, dynamic and customer specific data functions.



- **Simulation of BC at full Bus Rates**
- **Programmable Minor/ Major Frames and Gap Times**
- **Enable/ Disable BC Transfer on the Fly**
- **Error Injection in accordance with AS4112 'RT Production Test Plan'**
- **Static/ Dynamic Data Functions: Random, Unique, Incremental and Customer Defined**
- **Real Time 'BC Activity Display' with Dynamic Data Editing**
- **Program External Strobe and Delays in Minor/ Major Frames**
- **Creation of BC set-up on-line or off-line**

Multiple Remote Terminal Simulation

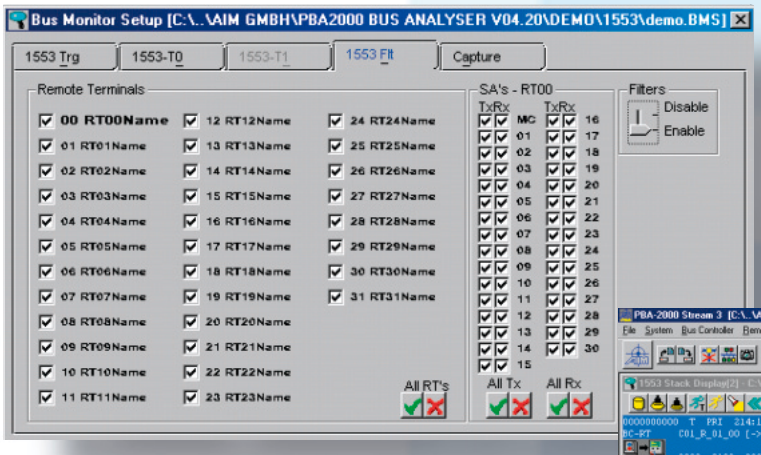
The PBA-2000 software simulates up to 31 Remote Terminals with all Sub-addresses. Each RT can be programmed for 'A' or 'B' Protocol for mixed bus applications. The use of multi buffering provides real time RT data simulations including static, dynamic and customer specific data functions. RT Mailbox Monitor Mode puts the RT into passive monitor mode to receive data to and from an external RT on the bus.



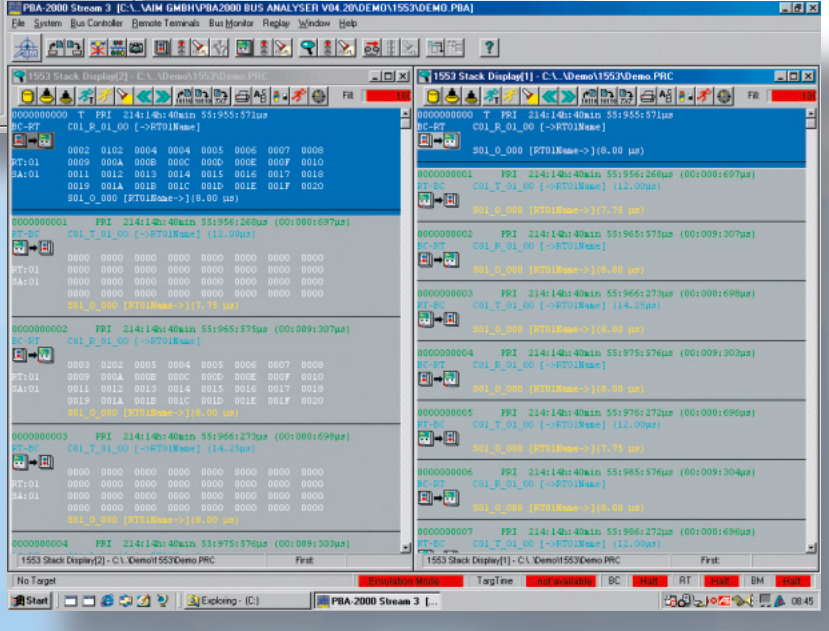
- Programmable Response Time for each simulated RT (4-32us)
- Error Injection in accordance with AS4112 'RT Production Test Plan'
- Static/ Dynamic Data Functions: Random, Unique, Incremental and Customer Defined
- Real Time 'RT Activity Display' with Dynamic Data Editing
- Fully Programmable Mode Codes
- Creation of RT set-up on-line or off-line

Databus Monitoring/Capture and Recording

The PBA-2000 provides powerful bus activity, bus monitoring and bus recording capabilities. Selective triggering, capture and filtering allows you to monitor all bus traffic or select only the MIL-STD-1553A/B words or messages of interest. Real time recording to the PC hard disk from multiple streams allows later retrieval and analysis of recorded data.



- Very accurately reconstructs Bus Traffic
- Turn ON/OFF selected or all RT's from Playback File
- RT's can be simulated or mailboxed during Replay
- Reconstruct MIL-STD-1553A/B bus recordings at remote sites
- Multiple buses can be played back simultaneously



- Quick Look 'RT Activity Display' counts Messages and Errors
- Multi Level Complex trigger
- Multiple Instances, Data Stack Displays: Chronological, Message and Compressed
- Absolute Time Measurement of MIL-STD-1553A/B Messages
- Time Tagging with internal or external IRIG-B
- Data Stack saved in ASCII Format for Post Analysis
- Real Time Recording to PC Hard Disk

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PBA-2000-NET

The PBA-2000-NET option is the Client/Server based solution allows multiple users to have access to multiple MIL-STD-1553A/B streams and control all PBA-2000 functions remotely via an Ethernet LAN.

- **Test multiple MIL-STD-1553A/B buses Remotely over the Ethernet**
- **Network Application Interface for Unique Customer Applications**
- **Run instances of PBA-2000 as Local or Remote Clients**

- **Bus Coupling Modes: Isolated, Transformer, Direct and Terminated Bus Network**
- **Dynamic Output Voltage control for Primary and Secondary Bus**
- **1MHz continuous Test Signal Output**

MIL-STD-1553 Bus Coupling

The PBA-2000 provides a fully programmable MIL-STD-1553A/B bus interface. Isolated mode is used to create BC or RT simulations without affecting the MIL-STD-1553A/B data bus.

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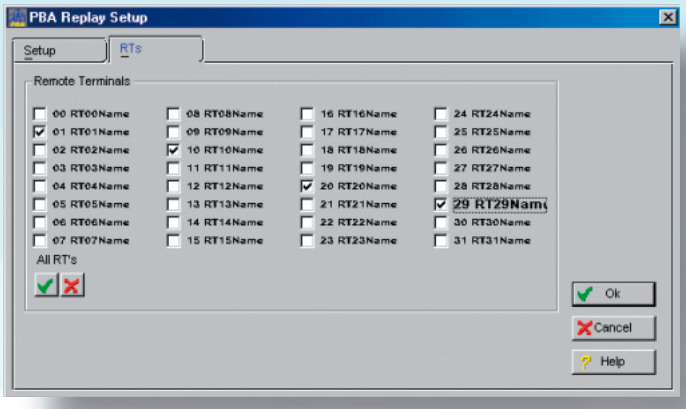

Physical Bus Replay

The PBA-2000 Physical Bus Replay Mode allows playback of the recording files to the dual redundant MIL-STD-1553A/B data bus. Bus Monitor functions can operate concurrently giving the ability to further monitor, filter and process the recording files. Any or all of the RT responses can be disabled from the recording file allowing real RT's to be connected and tested against real BC outputs.

Ordering Information

PBA-2000-PCI-SS
Single Stream MIL-STD-1553A/B Bus Analyser Software license
Executable Code for Windows 95/98/NT/2000

PBA-2000-PCI-DS
Dual Stream MIL-STD-1553A/B Bus Analyser Software license
Executable Code for Windows 95/98/NT/2000

PBA-2000-PCI-XS
Additional PBA licenses with access to one additional MIL-STD-1553A/B Stream

PBA-2000-NET-PCI-SS
Single Stream MIL-STD-1553A/B Bus Analyser Software via Network/Local, Executable Code for Windows 95/98/NT/2000

PBA-2000-NET-PCI-DS
Dual Stream MIL-STD-1553A/B Bus Analyser Software via Network/Local, Executable Code for Windows 95/98/NT/2000

PBA-2000-NET-PCI-XS
Additional PBA licenses via Network/Local with access to one additional MIL-STD-1553A/B Stream. Executable Code for Windows 95/98/NT/2000
Note: Third and additional stream each, up to a maximum of 16 MIL-STD-1553A/B streams

Minimum PC Computer Configuration
- 300 MHz Processor
- 64 Mbytes RAM
- 20 Mbytes free Disk Space
- Hard Disk determined by recording session requirements

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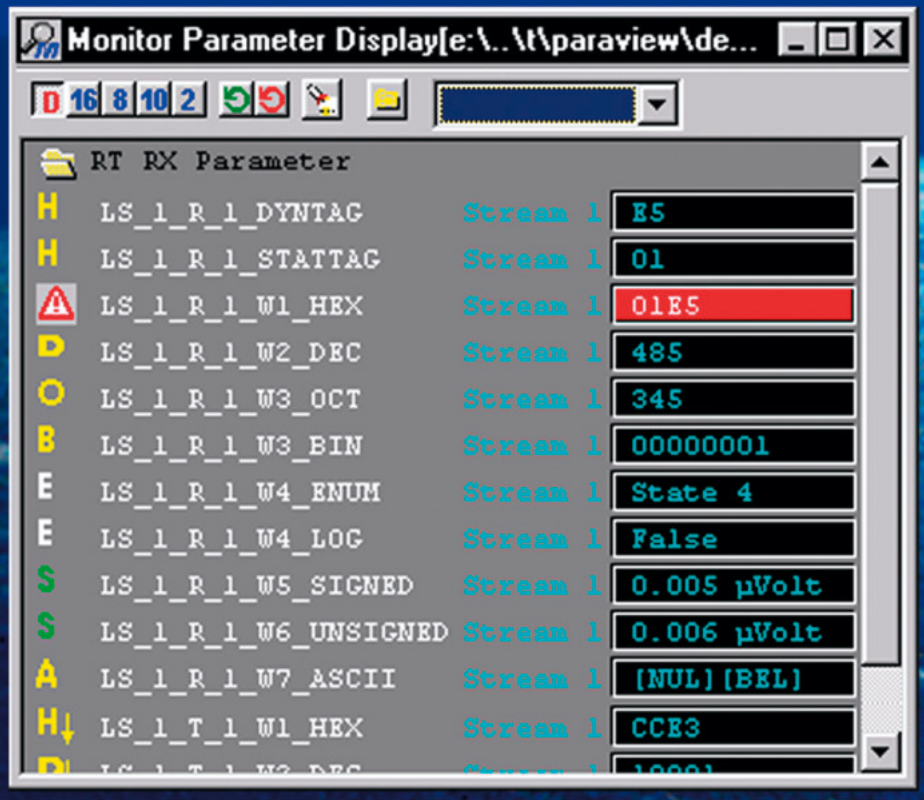
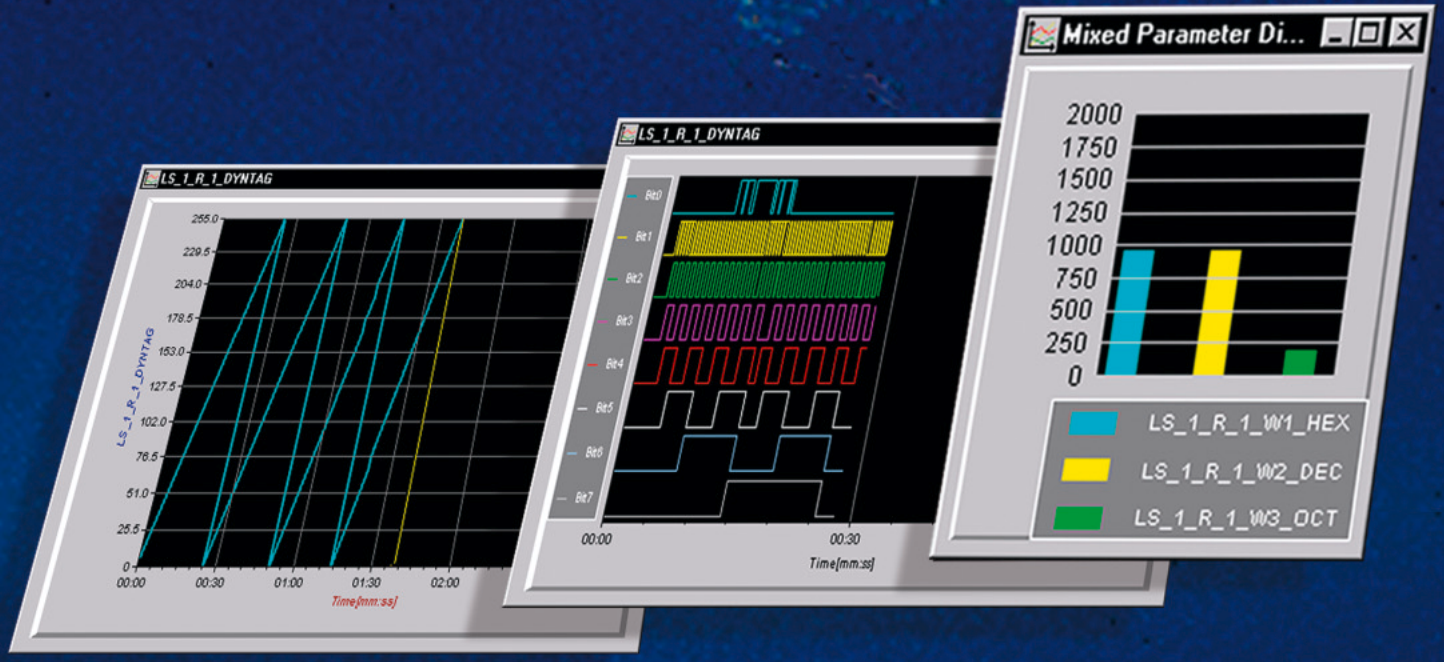
RIGHT ON TARGET

ParaView

ParaView-NET

PARAMETER VISUALISER SOFTWARE FOR WINDOWS™





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ParaView ParaView-NET

Parameter Visualiser Software for Windows™

ParaView is a software package to perform real time Parameter Visualisation and Control of databus parameters from multiple MIL-STD-1553A/B, STANAG3910, ARINC429 and AFDX buses. ParaView works in conjunction with AIM's Databus Anlaysers, PBA-2000/ PBA-3910/ PAA-429 and fdXplorer to provide real time Engineering Unit displays in alpha-numeric and graphical format.

ParaView-NET is optionally available to support the new Network Solutions family of Databus Analysers which allows multiple users connected via an network (Ethernet) to view and access pre-defined databus parameters.

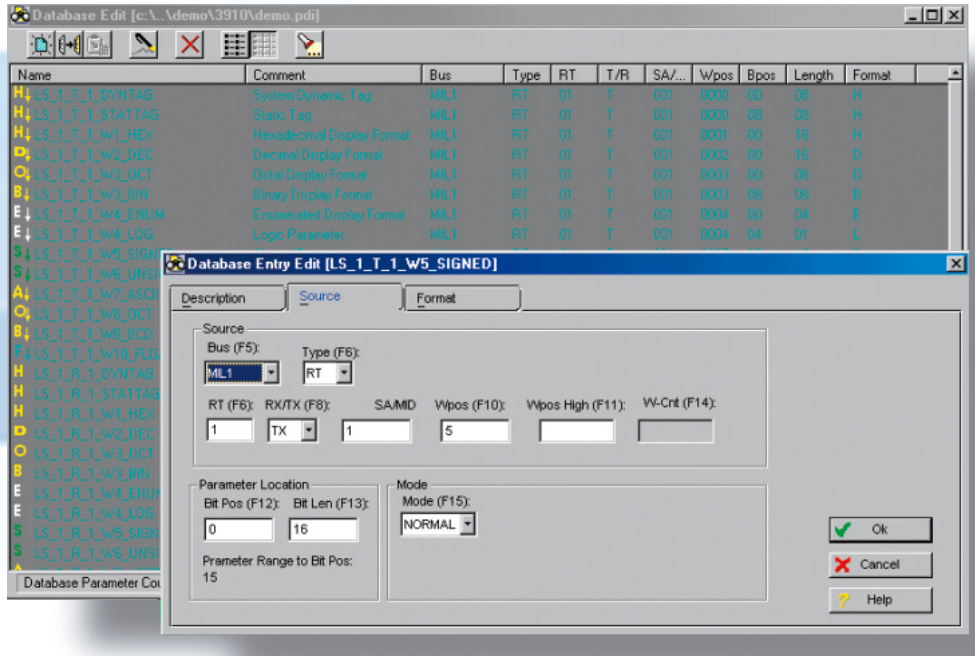
General Features

ParaView includes Parameter Extraction and Export functions, which can be used for Post Processing and Analysis of recorded data.

- **Define Parameters in a Common Database**
- **Supports multiple MIL-STD-1553A/B, STANAG3910, ARINC429 or AFDX streams**
- **Online Real Time Displays**
  - **Engineering Units**
  - **Graphical Displays/ Instruments**
  - **Strip Charts/ Scroll Graphs**
- **Alarm Limit Checking of Parameters**
- **Control Parameters**
- **System Parameters**
- **Run Time Logging of Parameters in EU format**
- **Perform Avionics Integration/ Test and Stimulation from one Package**

ParaView Database

The Parameter Database Interface (PDI) provides users the ability to define the name, source, format and location of the raw parameter for EU conversion from the incoming data stream.

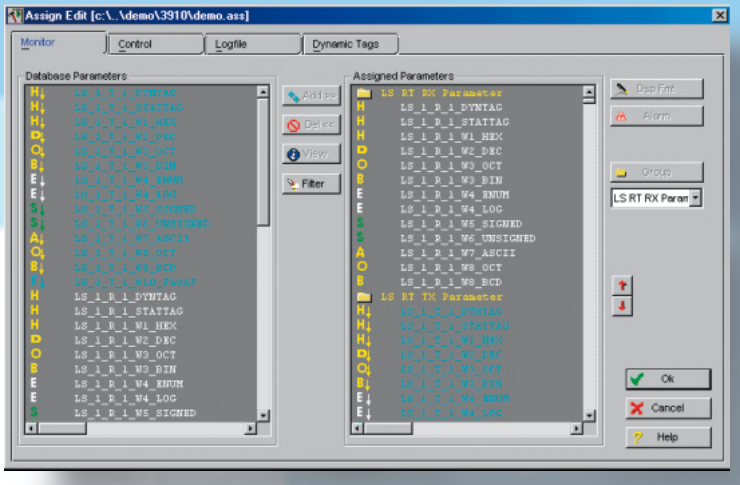


- **Define an unlimited number of Parameters in a Common Database**
- **Define Input Stream / Message location/ Word Position/ Bit Position**
- **Parameter width up to 32-bits**
- **Formats: ASCII/ BIN/ OCT/ DEC/ HEX BCD/ ENUMERATED/ IEEE754 (Single Precision) /LOGIC/ SCALED (Signed & Unsigned)**
- **PDI Supports Eurofighter TRACK/ MULTIPLEX DATA Formats**
- **Import/ Export and Edit via standard MS tools: e.g. MS-EXCEL or MS-ACCESS**
- **Generic ASCII format of PDI allows use of existing customer database (supporting ASCII data export capabilities)**
- **Expandable for customer specific or future requirements (Analog, Discretes etc..)**

ParaView Assign

The ParaView Assign function specifies which Parameters will be displayed in the Monitor, Control and System Parameter Displays. Log files store Monitor & Control parameters in Engineering Unit converted formats for later analysis and display.

- **Parameters for Display from any stream to one Display Window!**
- **Log files for recording of selected EU converted parameters**
- **Dynamic Tags for Control Parameters (MIL-STD-1553 and STANAG3910 only)**
- **Limit Checking of Parameters**
- **Parameter Groups on Demand**

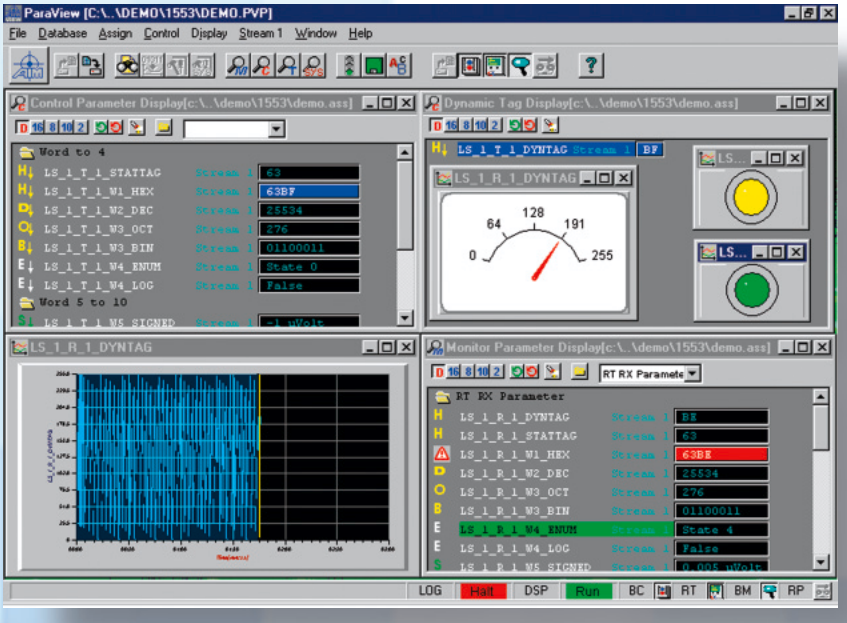


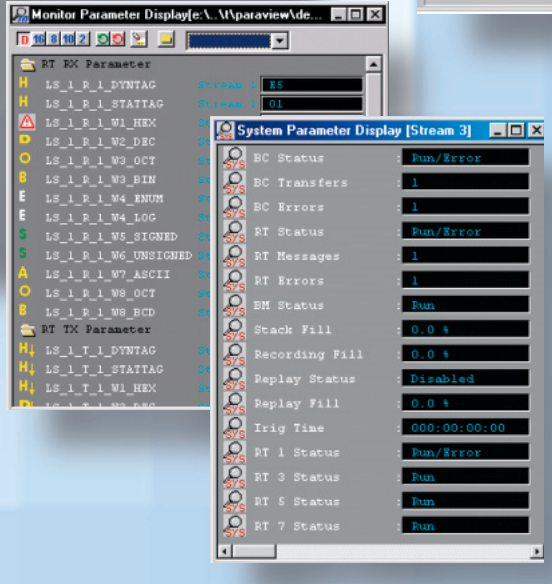
ParaView Monitor/Control

Monitor and Control parameters can be displayed in the default formats HEX, OCT, DEC or BINARY. Users can easily define Alpha-numeric and Graphical displays using various instrument displays including:

- **Meters**
- **Horizontal/ Vertical Scroll Graphs**
- **Horizontal / Vertical Sweep Graphs**
- **Horizontal/ Vertical Bar Graphs**
- **LED's**
- **Text Display (ASCII)**
- **Logic Graph**
- **Multiple Parameters displayed in one Mixed Instrument**

Customisation of each instrument is available to the user. Screen layouts can be saved and retrieved for specific applications.





ParaView System Parameters

The System Parameter display gives users the ability to monitor low level Databus Analyser information to the operator directly from the ParaView application such as BC Status, Message Events etc.

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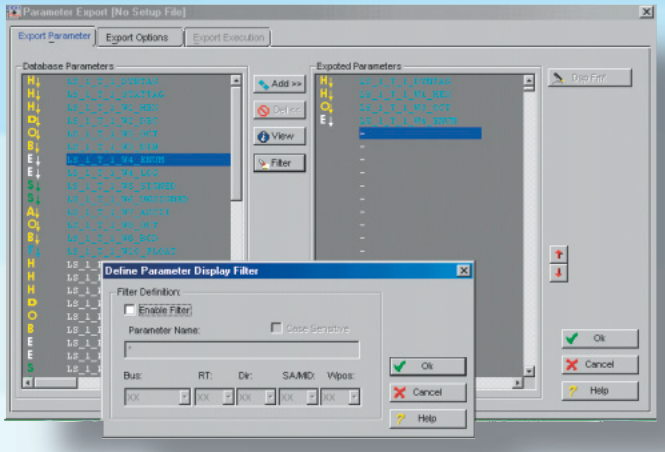
Enhanced PBA • PAA • fdXplorer low level Analyser Control

The ParaView software allows control of low level Databus Analyser functions directly from the application. This allows users to remain in the ParaView environment and control MIL-STD-1553B/ STANAG3910/ ARINC429 and AFDX project and set-up files from one Common user interface.

Parameter Extraction & Post Analysis

For post analysis and processing, ParaView offers the ability to extract selected parameters from PBA-2000, PBA-3910, PAA-429 and fdXplorer recording files and log files. An easy to use menu driven display prompts the user to select the required parameters for extraction and processing.



- **Process, Filter and Output Parameters for Post Processing**
- **Extract 'All' or Sample at 1ms to 1s**
- **ASCII Export Output files to customer generated post processing Software or Third Party Software**
- **Output File option compatible with DADisp**

Ordering Information

ParaView-1553
Option to PBA-2000-PCI/ PAA-429 Databus Analyser Software.
Bus Visualiser Software with Parameterisation & Graphical EU Displays and Multi-Stream Control to support up to 18 streams, Executable Code for Windows 95/98/NT/2000
Notes: One stream is defined as one dual redundant MIL-STD-1553A/B stream or one ARINC429 board with up to 32 channels.

Specify ParaView-1553-NET for the networked version: For one client seat.

ParaView-3910
Option to PBA-3910 Databus Analyser Software.
Bus Visualiser Software with Parameterisation & Graphical EU Displays and Multi-Stream Control to support up to 18 streams, Executable Code for Windows 95/98/NT/2000
Notes: One stream is defined as one dual redundant MIL-STD-1553A/B stream or one dual redundant STANAG3910 stream or one ARINC429 board with up to 32 channels.

Specify ParaView-3910-NET for the networked version: For one client seat.

ParaView-429
Option to PAA-429 Databus Analyser Software.
Bus Visualiser Software with Parameterisation & Graphical EU Displays and Multi-Stream Control to support up to 18 streams, Executable Code for Windows 95/98/NT/2000
Notes: One stream is defined as one ARINC429 board with up to 32 channels.

Specify ParaView-429-NET for the networked version: For one client seat.

Minimum PC Computer Configuration
- 300 MHz Processor
- 64 Mbytes RAM
- 20 Mbytes free Disk Space
- Hard Disk determined by recording session requirements

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