SPIRE-RAL-COM-0001489
From: Doug Griffin
To: Gary Parks
CC: John Delderfield, Bruce Swinyard, Eric Sawyer, Roy Blake (Tekdata)
Re: JPL 10209725-Prerelease 13, Received for comment Wed 8/1/03
Date: Tuesday, 14 January 2003 (Draft 0.1)
Issue: 0.1

Dear Gary,

I have looked closely at the Wiring Schematic you supplied to us last week and have a significant comment on it.

We need to have a flat layup on the harnesses between the 51-Way MDMs on the JFETs and the 51-Way Nanonics as these are implemented as flat woven harnesses.

I have drawn out in Figure 1 the pin assignments for the 51-Way Nanonics and the 51-Way MDMs as they are currently specified in JPL 10209725-Prerelease 13. The 12-ax cables have been drawn on this figure with heavy black dashed lines. Internal connections have been indicated with heavy dashed Cyan lines.The drawing reveals that it would be necessary to twist the 12-ax wires around each other[1].

This can be remedied by keeping the flat woven layup in the harness and performing the twisting of the 12-axes within the potting of the 51-Way MDM. This does not seem like a good solution.

The other solution, is to change the Schematic as shown in Figure 2. Attached is a marked up version of 10209725 that corresponds to Figure 2. John Delderfield has also produced a 3D representation of these changes.

Best regards,

Doug.

Note: Changes to
10209725 implies
changes to 10209722.
[DKG]

[1] There are two ways that the drawing can be represented depending on the orientation of the 51-Way MDM. In either case, a flat harness layup cannot be achieved.

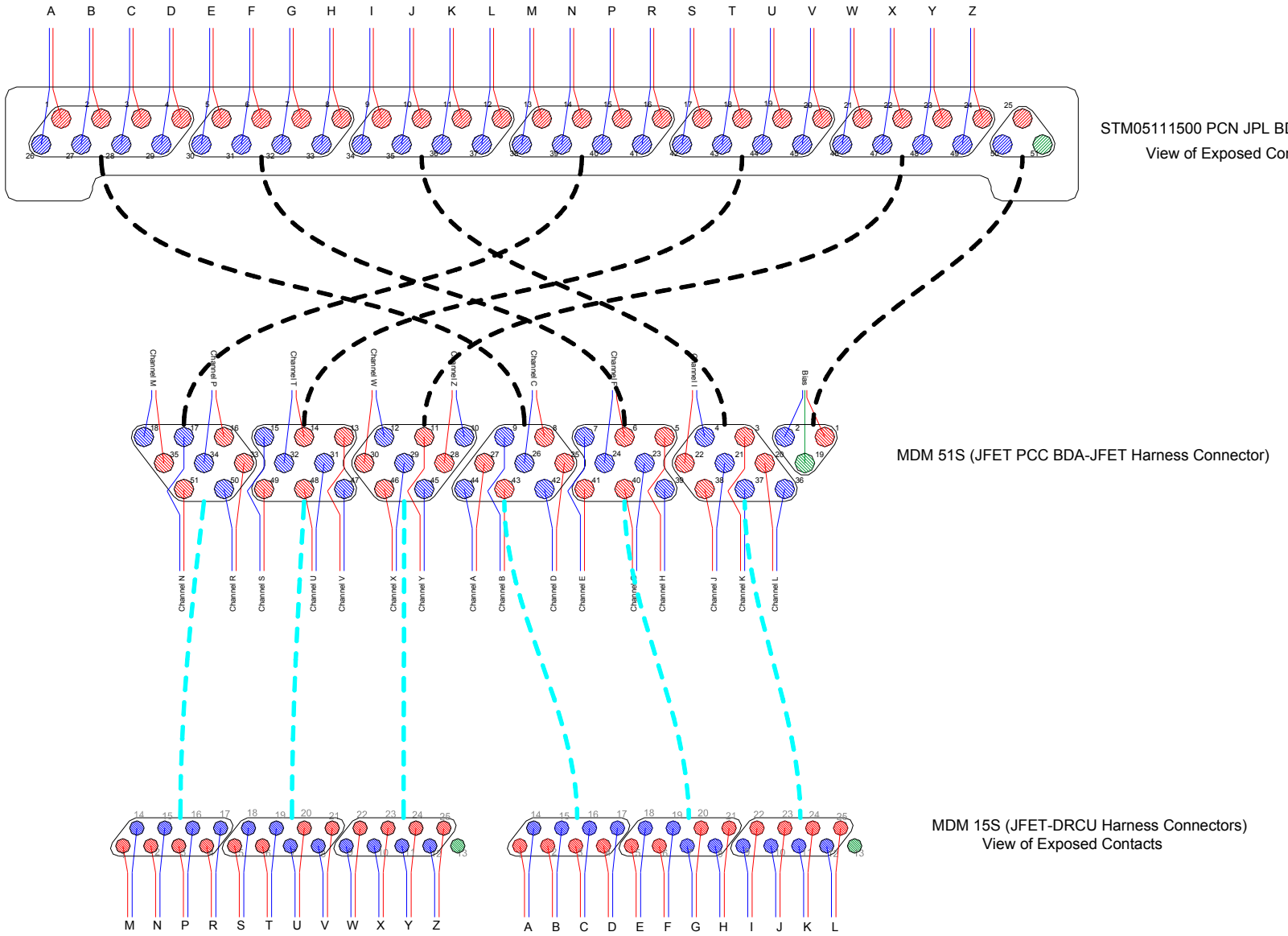


Figure 1 - Wiring as currently specified

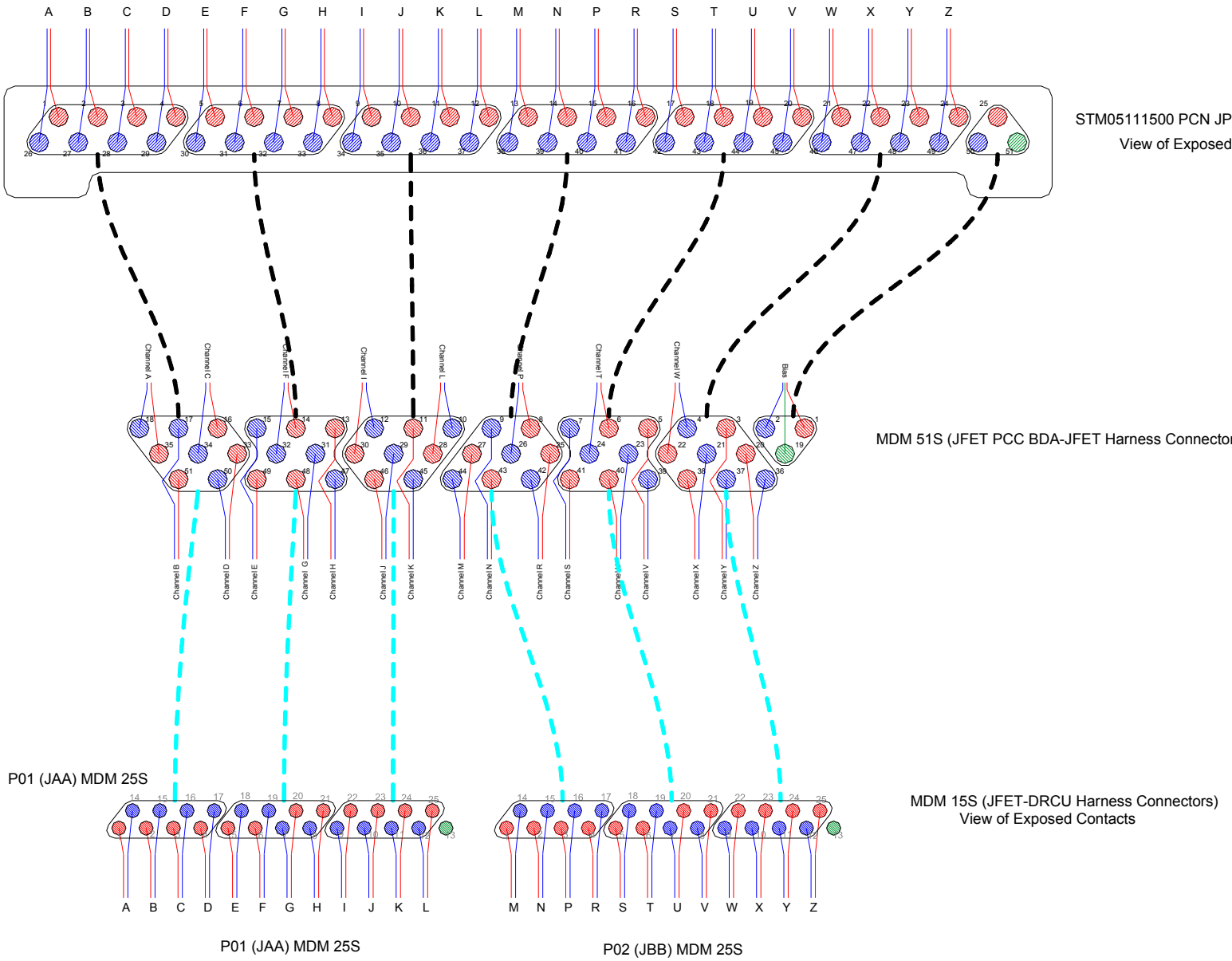
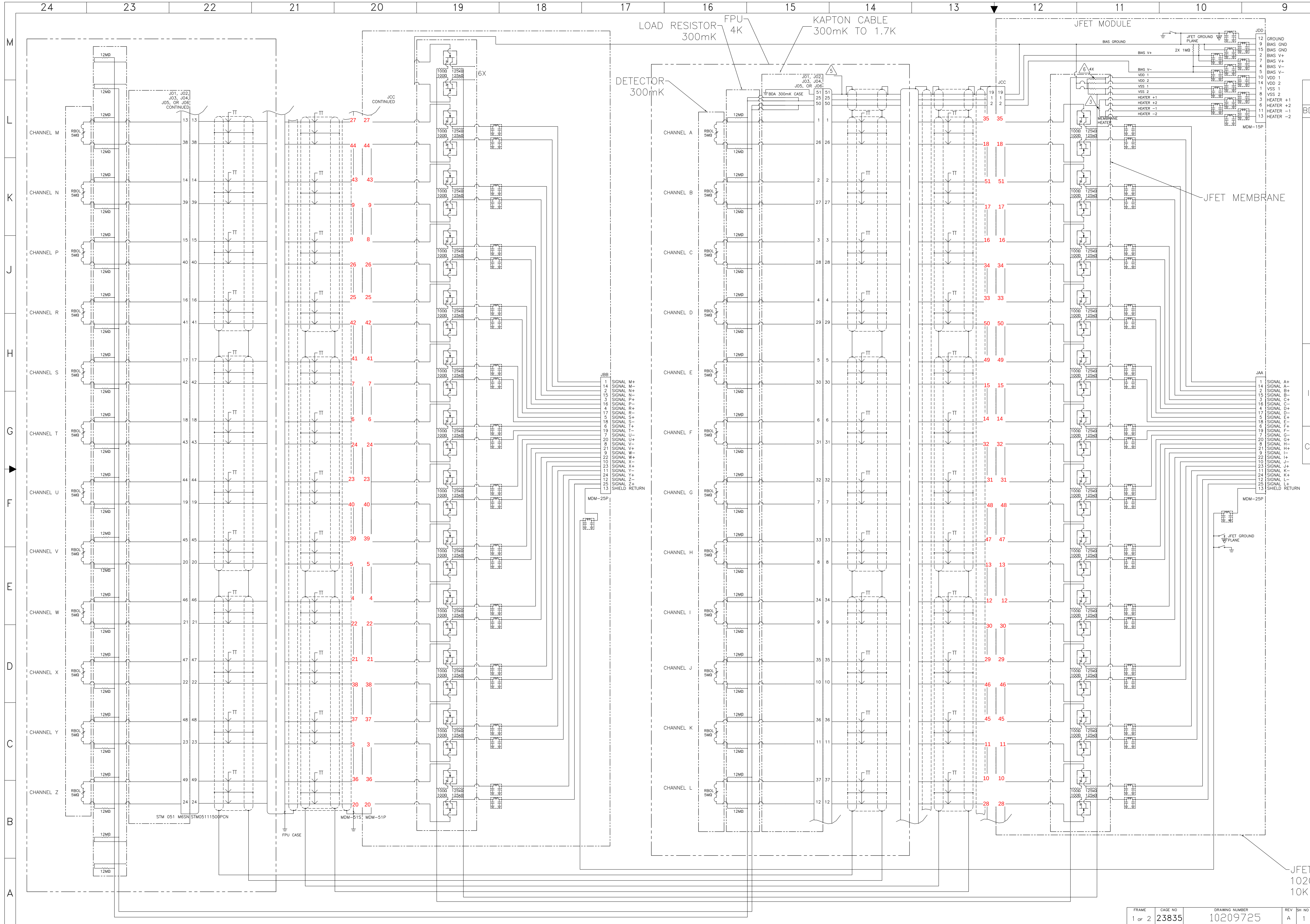


Figure 2 - Proposed modifications to JPL 10209725



ARRAY DEFINITION		10209800−1 P/LW		10209800−2 P/MW				10209800−3 P/SW						10209800−4 S/LW	10209800−5 S/SW	
BDA CONNECTOR		J05	J06	J01	J02	J03	J04	J01	J02	J03	J04	J05	J06	J05	J05	J06
PIXEL MAP	A	R1	E1	A13	R1	A7	E7	R1	E1	D6	F12	D11	G5	R1	R1	–
	B	A8	E2	T1	G1	A6	D7	D16	F1	B6	I11	A10	H6	T1	A4	–
	C	A7	E3	B12	T2	B6	F7	T1	T2	C5	E12	E10	I6	C1	A3	–
	D	A6	E4	C13	E1	C7	E8	B16	H1	A5	H12	C10	F6	DK1	A2	–
	E	A9	D1	A12	D1	A5	G8	C15	G1	E5	G12	B10	G6	B1	A1	–
	F	C9	D2	D12	F1	B5	F8	A15	I1	B5	F13	D10	H7	D1	DK1	–
	G	B8	D3	C12	E2	C6	E9	D15	H2	D5	E13	A9	F7	E1	B3	G3
	H	B7	D4	B11	G2	D6	G9	B15	F2	C4	I12	E9	I7	A1	B2	G4
	I	C7	C1	A11	F2	B4	D9	C14	I2	A4	H13	C9	G7	C2	B1	DK2
	J	B5	C3	E13	G3	C5	F9	D14	G2	D4	G13	B9	H8	D2	C3	F5
	K	B6	C5	D11	E3	D4	E10	A14	H3	B4	F14	D9	F8	B2	C2	F4
	L	A5	T2	C11	D3	A4	G10	A13	I3	C3	E14	A8	G8	E2	C1	E6
	M	T1	E5	B10	F3	C4	F10	B14	E2	B3	I13	C8	I8	A2	D3	E5
	N	B4	C6	A10	G4	B3	E11	C13	F3	A3	H14	E8	F9	C3	D2	E4
	P	C4	C8	D10	E4	C3	G11	B13	G3	A2	G14	D8	H9	D3	D1	D7
	R	B3	D5	B9	F4	B2	F11	D13	H4	D3	I14	B8	G9	B3	E3	D6
	S	C2	D6	C10	E5	D2	E12	A12	I4	C2	F15	C7	I9	E3	E2	D5
	T	B2	D7	C9	D5	A3	G12	C12	E3	B2	H15	E7	F10	C4	E1	D4
	U	B1	D8	A9	F5	A2	F12	D12	F4	D2	I15	A7	H10	DK2	F3	C6
	V	A3	E7	B8	G5	C2	G13	B12	G4	A1	G15	D7	G10	D4	F2	C5
	W	A4	E6	A8	E6	B1	DK2	E11	H5	C1	H16	B7	F11	C5	F1	C4
	X	A1	E8	DB	G6	A1	T/C	A11	E4	B1	DK2	C6	I10	B4	G1	B5
	Y	DK1	DK2	C8	F6	DK1	T/C	C11	I5	DK1	F16	E6	H11	A3	T1	B4
	Z	A2	E9	B7	G7	C1	T/C	B11	F5	D1	E15	A6	G11	T2	G2	T2
JFET INTERFACE	AA	HSJFP7 J13	HSJFP8 J15	HSJFP9 J17	HSJFP10 J19	HSJFP11 J21	HSJFP12 J23	HSJFP1 J01	HSJFP2 J03	HSJFP3 J05	HSJFP4 J07	HSJFP5 J09	HSJFP6 J11	HSJFS3 J05	HSJFS1 J01	HSJFS2 J03
	BB	HSJFP7 J14	HSJFP8 J16	HSJFP9 J18	HSJFP10 J20	HSJFP11 J22	HSJFP12 J24	HSJFP1 J02	HSJFP2 J04	HSJFP3 J06	HSJFP4 J08	HSJFP5 J10	HSJFP6 J12	HSJFS3 J06	HSJFS1 J02	HSJFS2 J04
	CC	HSJFP7 J35	HSJFP8 J36	HSJFP9 J37	HSJFP10 J38	HSJFP11 J39	HSJFP12 J40	HSJFP1 J29	HSJFP2 J30	HSJFP3 J31	HSJFP4 J32	HSJFP5 J33	HSJFP6 J34	HSJFS3 J13	HSJFS1 J11	HSJFS2 J12
	DD	HSJFP7 J47	HSJFP8 J48	HSJFP9 J49	HSJFP10 J50	HSJFP11 J51	HSJFP12 J52	HSJFP1 J41	HSJFP2 J42	HSJFP3 J43	HSJFP4 J44	HSJFP5 J45	HSJFP6 J46	HSJFS3 J17	HSJFS1 J15	HSJFS2 J16
FPU HARNESS		7	8	9	10	11	12	1	2	3	4	5	6	15	13	14
CRYO HARNESS		6	6	5	5	4	4	9	9	8	8	7	7	1	2	2

7. INFORMATION IN THIS DOCUMENT IS ALSO CONTAINED IN THE HARNESS DEFINITION DOCUMENT, RAL DOCUMENT SPIRE–RAL–PRJ–000608. IN AREAS WHERE THERE ARE CONFLICTS, THE HARNESS DEFINITION DOCUMENT TAKES PRECEDENCE.

6. ESD PROTECTION RESISTORS ARE 7 TIMES THE SOURCE RESISTOR.

5. GROUND WIRE TO BE TERMINATED AT INSTRUMENT INTEGRATION. WIRE WILL HAVE A MINIMUM LENGTH OF 150MM.

4. UNLESS OTHERWISE NOTED, ⏚ IS JFET CHASSIS GROUND.

3. JFET MEMBRANE HEATER IS 0.0204 TIMES THE SOURCE RESISTOR.

2. ALL RESISTORS HAVE A TOLERANCE OF ±40%.

1. THIS TECHNICAL DATA IS EXPORT CONTROLLED UNDER U.S. LAW AND IS BEING TRANSFERRED BY JPL TO PPARC PURSUANT TO THE NASA / PPARC LETTER OF AGREEMENT WHICH ENTERED INTO FORCE ON DECEMBER 2, 1999. THIS TECHNICAL DATA IS TRANSFERRED TO PPARC FOR USE EXCLUSIVELY ON THE NASA/PPARC SPIRE ON FIRST COOPERATIVE PROJECT, MAY NOT BE USED FOR ANY OTHER PURPOSE, AND SHALL NOT BE RE–TRANSFERRED OR DISCLOSED TO ANY OTHER PARTY WITHOUT THE PRIOR WRITTEN APPROVAL OF NASA.

NOTES: UNLESS OTHERWISE SPECIFIED

QTY REQD	ITEM NO	REF DES	CAGE NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	MATERIAL OR NOTE	ZONE

PARTS LIST

MATERIAL

METRIC

THIRD ANGLE PROJECTION

NEXT ASSEMBLY: SPIRE — USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS

LINEAR TOLERANCES:

0–6	± 0.1
OVER 6–30	± 0.2
OVER 30–120	± 0.3
OVER 120–315	± 0.5
OVER 315–1000	± 0.8
OVER 1000	± 1.2

ANGULAR TOLERANCES: ± 0.5°

MACHINE FINISH (MICROMETERS) 3.2

DO NOT SCALE DRAWING

INTERPRET DWG PER ANSI Y14.100M

CONTRACT NO 960939

APPD ____ DATE ____

DWN D CRUMB 5/13/01

CHK

STRUCT

MATL

THRM CONT

ENGR

DSGN SUPV

JET PROPULSION LABORATORY

CALIFORNIA INSTITUTE OF TECHNOLOGY
PASADENA, CA 91109

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WIRING SCHEMATIC, SPIRE

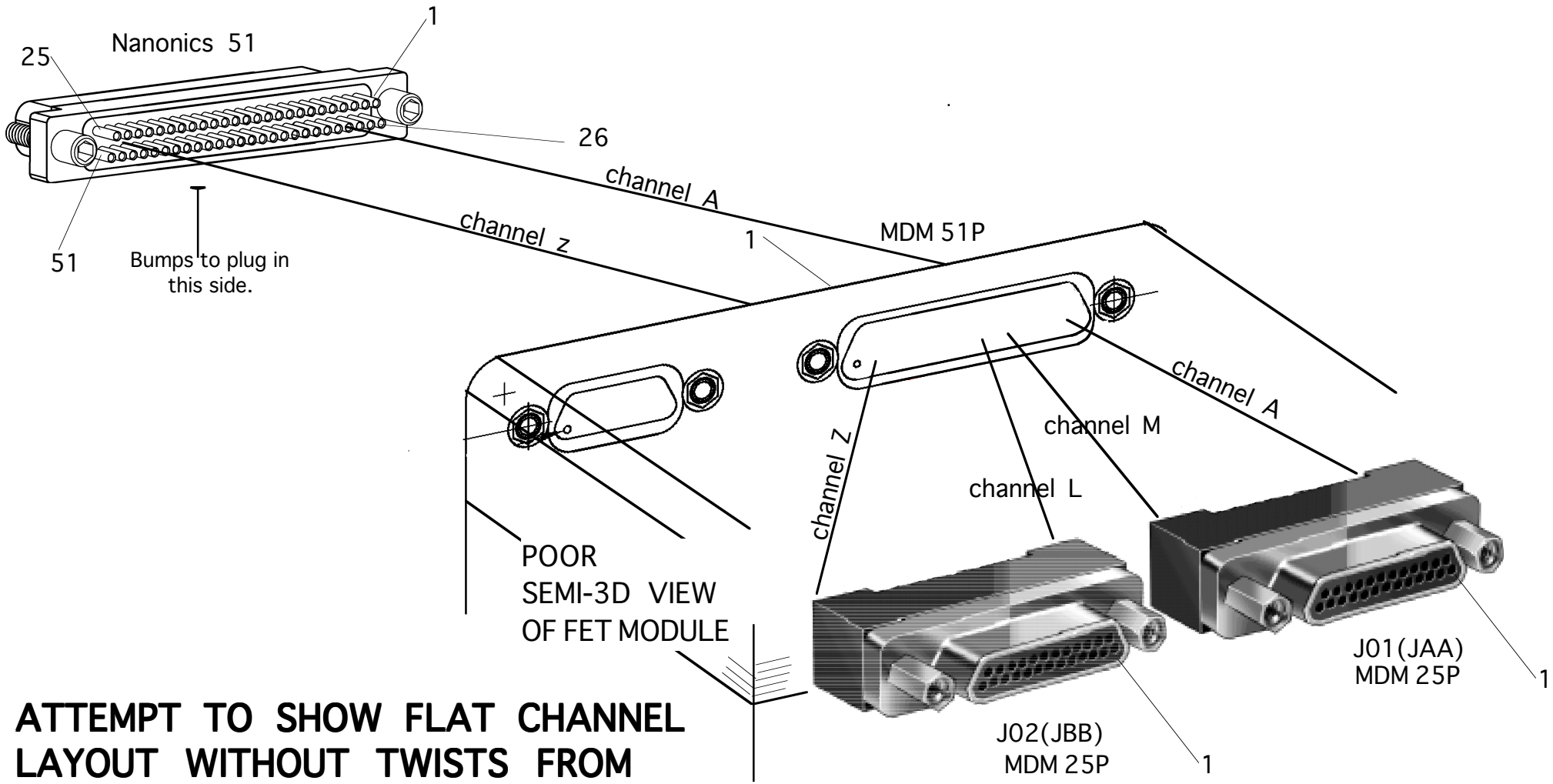
SIZE A0 — CAGE NO 23835 — 10209725 — REV A

SCALE NONE — UNCLASSIFIED — SHEET 1 OF 1

REV 2/00

AutoCAD GENERATED

FRAME 1 of 2 — CASE NO 23835 — DRAWING NUMBER 10209725 — REV A — SH NO 1



ATTEMPT TO SHOW FLAT CHANNEL LAYOUT WITHOUT TWISTS FROM NANONICS TO JFET O/PS