SPIRE-RAL-COM-0001480
From: Doug Griffin
To: Gary Parks
CC: John Delderfield, Bruce Swinyard, Eric Sawyer
Date: Tuesday, 07 January 2003
Issue: 0.1

Dear Gary,

As promised last week, please find below a detailed list of the issues with the JPL documentation that we have found. Some of these issues were detected after the Dec. 2002 Saclay meeting.

John and I have extensively discussed these comments. None of them imply changes to the hardware, but they do impact on the Astrium S/C I/F and on the order of the pixels on the DCU connectors.

What we have proposed does not necessarily represent the only documentation corrections compatible with existing hardware.

We await the update to the Wiring Schematic that details the changes to the hardware that you informed me of during the phone conversation yesterday.

Would you please respond to the comments referring to the number in the left hand column? I will fill out the Closure column in due course and re-issue.

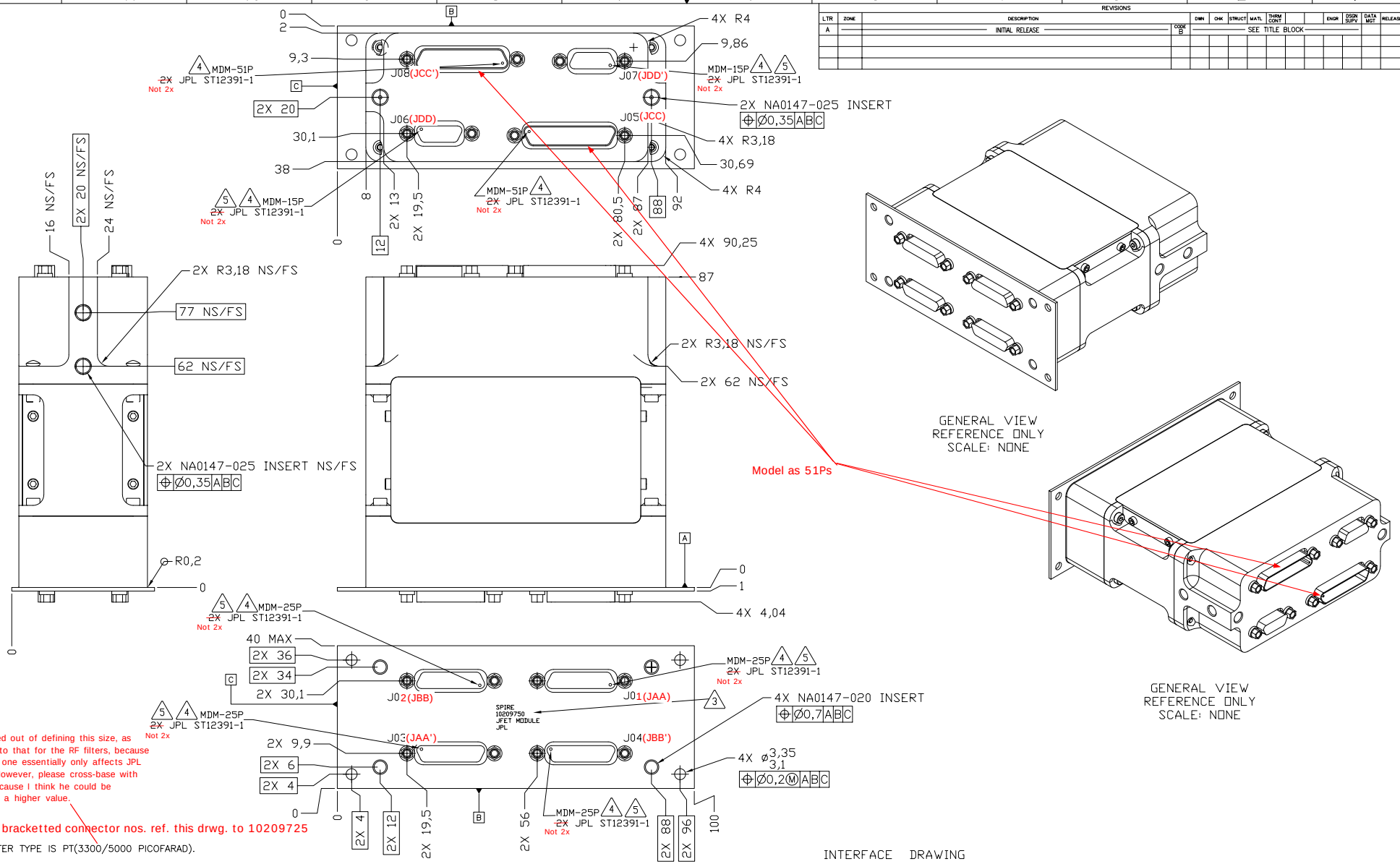
Cheers,

Doug.

p.s. Sorry that I did not get it to you yesterday. The task was more complex than I had anticipated

Comment Number	Drawing number and issue	Sheet # / Grid reference	RAL Comment	Closure
1	10209725-X231	Sheet 1 Grid L2	• There is disagreement between the BDA connectors indicated as being populated on the SPIRE Wiring Diagram and the BDA ICDwg. • The correct allocation is: • 10209725-X231 ○ PLW J05, J06 ○ PMW J01, J02, J03, J04 ○ PSW J01, J02, J03, J04, J05, J06 ○ SLW **J05** ○ SSW J05, J06	
2	10209721-A	Sheet 4, Grid G11	• Reference: Comment 1 • PLW Should be: J05, J06 (John Coker has signed this issue, I understand that it is OK from a mechanical point of view to move it from J01, J02 but MSSL need to sign off on this)	
3	10209721-A	Sheet 7, Grid G11	• Reference: Comment 1 • SLW Should be: J05 (John Coker has signed this issue, I understand that it is OK from a mechanical point of view to move it from J01 but MSSL need to sign off on this)	
4	10209722-A Prerelease 6	Sheet 1, Grid D2, H8, G7	• View of 51-Way MDM connectors (J05 and J08) shown at D2 as Sockets; should be Pins • View of 51-Way MDM Connectors (J05, J08) are drawn as sockets (double line around the "D" profile instead of a single line); should be Pins • See "JD Annotated 10209722.pdf"	
5	10209722-A Prerelease 6	Sheet 1, Various Grid	• To have agreement in nomenclature between 10209722 and 10209725, the connector labels should be changed on 10209722 as follows:	

Comment Number	Drawing number and issue	Sheet # / Grid reference	RAL Comment	Closure
			o J01 -> J02 (JBB) (Grid C9) o J02 -> J01 (JAA) (Grid C7) o J03 -> J03 (JAA') (Grid C9) o J04-> J04 (JBB') (Grid C7) o J05 -> J05 (JCC) (Grid G7) o J06 -> J06 (JDD) (Grid G9) o J07 -> J07 (JDD') (Grid H7) o J08 – J08 (JCC') (Grid H9) • See "JD Annotated 10209722.pdf" • Note: Both John and I agree that it would in fact be better if the labels J01 through J08 were removed from the drawing and replaced simply with JAA, JBB, JAA', JBB' etc. as it has been agreed that the units will be supplied without J numbers inscribed next to the connectors. The Jxx labels will be added by RAL after JPL delivery.	
6	10209722-A Prerelease 6	Sheet 1, Various Grid	All connectors labelled as being x2 (i.e. Two off). This is incorrect. They are all one off.	
7	10209722-A Prerelease 6	Sheet 2, Various Grid	• J01 should be signals A-L • J02 should be signals M-Z • J03, J04 and J08 should be suffixed with an apostrophe • See "JD Annotated 10209722.pdf"	



GENERAL VIEW
REFERENCE ONLY
SCALE: NONE

GENERAL VIEW
REFERENCE ONLY
SCALE: NONE

I've stayed out of defining this size, as opposed to that for the RF filters, because this BDA one essentially only affects JPL items. However, please cross-base with Viktor because I think he could be modelling a higher value.

6. The bracketted connector nos. ref. this drwg. to 10209725

5 FILTER TYPE IS PT(3300/5000 PICOFARAD).

4 CONNECTOR CUT OUTS SIZED TO ALLOW PROPER MATING OF SOCKET CONNECTORS.

3 ASSEMBLY NUMBER, NAME, TITLE, DASH NUMBER, AND REV LETTER TO APPEAR AS SHOWN IN THIS AREA.

2. THIS IS THE INTERFACE CONTROL DRAWING FOR THE JFET MODULE ASSEMBLY, JPL PART NUMBER 10209750, REFERENCE DESIGNATION TBD. JPL DRAWING NUMBER 10209750 SHALL CONTAIN THE FOLLOWING NOTE: THIS ASSEMBLY MEETS THE INTERFACE REQUIREMENTS OF JPL INTERFACE CONTROL DRAWING 10209722.

1. THIS TECHNICAL DATA IS EXPORT CONTROLLED UNDER U.S. LAW AND IS BEING TRANSFERRED BY JPL TO PPARC PURSUANT TO THE NASA / PPARC LETTER OF AGREEMENT WHICH ENTERED INTO FORCE ON DECEMBER 2, 1999. THIS TECHNICAL DATA IS TRANSFERRED TO PPARC FOR USE EXCLUSIVELY ON THE NASA/PPARC SPIRE ON FIRST COOPERATIVE PROJECT, MAY NOT BE USED FOR ANY OTHER PURPOSE, AND SHALL NOT BE RE-TRANSFERRED OR DISCLOSED TO ANY OTHER PARTY WITHOUT THE PRIOR WRITTEN APPROVAL OF NASA.

NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS

LTR	ZONE	DESCRIPTION	DWN	CHK	STRUCT	MATL	THRM CONT	ENGR	DSGN SUPV	DATA MGT	RELEASE DATE
A		INITIAL RELEASE CODE B					SEE TITLE BLOCK				

INTERFACE DRAWING

PARTS LIST

QTY REQD	ITEM NO	REF DES	CAGE NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	MATERIAL OR NOTE	ZONE

MATERIAL

METRIC

THIRD ANGLE PROJECTION

NEXT ASSEMBLY: SPIRE

USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS

LINEAR TOLERANCES:

0–6	± 0.1
OVER 6–30	± 0.2
OVER 30–120	± 0.3
OVER 120–315	± 0.5
OVER 315–1000	± 0.8
OVER 1000	± 1.2

ANGULAR TOLERANCES: ± 0.5°

MACHINE FINISH (MICROMETERS) 3.6

DO NOT SCALE DRAWING

INTERPRET DWG PER ANSI Y14.100M

CONTRACT NO 960939

APPD DATE

DWN D CRUMB 01/09/02

CHK

STRUCT

MATL

THRM CONT

ENGR

DSGN SUPV

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
PASADENA, CA 91109

RELEASED THROUGH EDMG

JFET MODULE, INTERFACE DRAWING

SIZE	CAGE NO		REV
A1	23835	10209722	A

SCALE 2:1 | UNCLASSIFIED | SHEET 1 OF 2

REV 2/00

AutoCAD GENERATED

A1 10209722

J01 JFET OUTPUT 1, ~~SIGNALS 1-12~~	
PIN #	PIN PURPOSE
1	SIGNAL A+
2	SIGNAL B+
3	SIGNAL C+
4	SIGNAL D+
5	SIGNAL E+
6	SIGNAL F+
7	SIGNAL G-
8	SIGNAL H-
9	SIGNAL I-
10	SIGNAL J-
11	SIGNAL K-
12	SIGNAL L-
13	FPU GND
14	SIGNAL A-
15	SIGNAL B-
16	SIGNAL C-
17	SIGNAL D-
18	SIGNAL E-
19	SIGNAL F-
20	SIGNAL G+
21	SIGNAL H+
22	SIGNAL I+
23	SIGNAL J+
24	SIGNAL K+
25	SIGNAL L+

J02 JFET OUTPUT 1, ~~SIGNALS 13-24~~	
PIN #	PIN PURPOSE
1	SIGNAL M+
2	SIGNAL N+
3	SIGNAL P+
4	SIGNAL R+
5	SIGNAL S+
6	SIGNAL T+
7	SIGNAL U-
8	SIGNAL V-
9	SIGNAL W-
10	SIGNAL X-
11	SIGNAL Y-
12	SIGNAL Z-
13	FPU GND
14	SIGNAL M-
15	SIGNAL N-
16	SIGNAL P-
17	SIGNAL R-
18	SIGNAL S-
19	SIGNAL T-
20	SIGNAL U+
21	SIGNAL V+
22	SIGNAL W+
23	SIGNAL X+
24	SIGNAL Y+
25	SIGNAL Z+

J03 JFET OUTPUT 2, ~~SIGNALS 13-24~~	
PIN #	PIN PURPOSE
1	SIGNAL A'+
2	SIGNAL B'+
3	SIGNAL C'+
4	SIGNAL D'+
5	SIGNAL E'+
6	SIGNAL F'+
7	SIGNAL G'-
8	SIGNAL H'-
9	SIGNAL I'-
10	SIGNAL J'-
11	SIGNAL K'-
12	SIGNAL L'-
13	FPU GND'
14	SIGNAL A'-
15	SIGNAL B'-
16	SIGNAL C'-
17	SIGNAL D'-
18	SIGNAL E'-
19	SIGNAL F'-
20	SIGNAL G'+
21	SIGNAL H'+
22	SIGNAL I'+
23	SIGNAL J'+
24	SIGNAL K'+
25	SIGNAL L'+

J04 JFET OUTPUT 2, ~~SIGNALS 1-12~~	
PIN #	PIN PURPOSE
1	SIGNAL M'+
2	SIGNAL N'+
3	SIGNAL P'+
4	SIGNAL R'+
5	SIGNAL S'+
6	SIGNAL T'+
7	SIGNAL U'-
8	SIGNAL V'-
9	SIGNAL W'-
10	SIGNAL X'-
11	SIGNAL Y'-
12	SIGNAL Z'-
13	FPU GND'
14	SIGNAL M'-
15	SIGNAL N'-
16	SIGNAL P'-
17	SIGNAL R'-
18	SIGNAL S'-
19	SIGNAL T'-
20	SIGNAL U'+
21	SIGNAL V'+
22	SIGNAL W'+
23	SIGNAL X'+
24	SIGNAL Y'+
25	SIGNAL Z'+

J05 JFET INPUT 1	
PIN #	PIN PURPOSE
1	VOLTAGE +
2	VOLTAGE -
3	SIGNAL Z-
4	SIGNAL Z+
5	SIGNAL W-
6	SIGNAL W+
7	SIGNAL T+
8	SIGNAL T-
9	SIGNAL P+
10	SIGNAL P-
11	SIGNAL L-
12	SIGNAL L+
13	SIGNAL F+
14	SIGNAL F-
15	SIGNAL C+
16	SIGNAL C-
17	SIGNAL B+
18	SIGNAL B-
19	BIAS GND
20	SIGNAL Y-
21	SIGNAL X-
22	SIGNAL V-
23	SIGNAL U-
24	SIGNAL S+
25	SIGNAL R+
26	SIGNAL N+
27	SIGNAL M+
28	SIGNAL K-
29	SIGNAL J-
30	SIGNAL I-
31	SIGNAL H-
32	SIGNAL G-
33	SIGNAL E+
34	SIGNAL D+
35	SIGNAL A+
36	SIGNAL Y+
37	SIGNAL X+
38	SIGNAL V+
39	SIGNAL U+
40	SIGNAL S-
41	SIGNAL R-
42	SIGNAL N-
43	SIGNAL M-
44	SIGNAL K+
45	SIGNAL J+
46	SIGNAL I+
47	SIGNAL H+
48	SIGNAL G+
49	SIGNAL E-
50	SIGNAL D-
51	SIGNAL A-

J06 JFET SERVICE 1	
PIN #	PIN PURPOSE
1	Vss
2	V+
3	H+
4	V-
5	V-
6	H+
7	V+
8	Vss
9	BIAS GND
10	Vdd
11	H-
12	CHASSIS GND
13	H-
14	Vdd
15	BIAS GND

J07 JFET SERVICE 2	
PIN #	PIN PURPOSE
1	Vss'
2	V+'
3	H+'
4	V-'
5	V-'
6	H+'
7	V+'
8	Vss'
9	BIAS GND'
10	Vdd'
11	H-'
12	CHASSIS GND'
13	H-'
14	Vdd'
15	BIAS GND'

J08 JFET INPUT 2	
PIN #	PIN PURPOSE
1	VOLTAGE '+
2	VOLTAGE '-
3	SIGNAL Z'-
4	SIGNAL Z'+
5	SIGNAL W'-
6	SIGNAL W'+
7	SIGNAL T'+
8	SIGNAL T'-
9	SIGNAL P'+
10	SIGNAL P'-
11	SIGNAL L'-
12	SIGNAL L'+
13	SIGNAL F'+
14	SIGNAL F'-
15	SIGNAL C'+
16	SIGNAL C'-
17	SIGNAL B'+
18	SIGNAL B'-
19	BIAS GND'
20	SIGNAL Y'-
21	SIGNAL X'-
22	SIGNAL V'-
23	SIGNAL U'-
24	SIGNAL S'+
25	SIGNAL R'+
26	SIGNAL N'+
27	SIGNAL M'+
28	SIGNAL K'-
29	SIGNAL J'-
30	SIGNAL I'-
31	SIGNAL H'-
32	SIGNAL G'-
33	SIGNAL E'+
34	SIGNAL D'+
35	SIGNAL A'+
36	SIGNAL Y'+
37	SIGNAL X'+
38	SIGNAL V'+
39	SIGNAL U'+
40	SIGNAL S'-
41	SIGNAL R'-
42	SIGNAL N'-
43	SIGNAL M'-
44	SIGNAL K'+
45	SIGNAL J'+
46	SIGNAL I'+
47	SIGNAL H'+
48	SIGNAL G'+
49	SIGNAL E'-
50	SIGNAL D'-
51	SIGNAL A'-

SIZE	CAGE NO		REV
A1	23835	10209722	A
SCALE NONE	UNCLASSIFIED	SHEET 2 OF 2	

10209722 A1

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REV 2/00