SPIRE Detector Summit Meeting
Saclay, December 12/13 2002
Draft Minutes

Present:	Project Team	Matt Griffin	Bruce Swinyard	John Delderfield
	JPL	Gary Parks	Viktor Hristov	
	CEA	Jean-Louis Augueres Dominique Schmitt	Christophe Cara Henri Triou	Frederic Pinsard

Contents

1. Review of actions from weekly telecons (last telecon Dec. 3rd)

Blue = updates
Green = actions closed at this meeting

No.	Action	Responsible	Due date	Status
Actions from July 9 telecon				
47	Update Major Milestones List	Ken	Next telecon (July 23)	The MMA is to be updated in accordance with the dates for JPL deliveries agreed at this meeting for the updated business agreement.
Actions from August 20 telecon				
65	Draw up vibration test procedure for the instrument STM, including policy for accelerometry.	Berend	Feb. 1	Open. To be addressed after the FEA analysis is complete.
Actions from summit meeting of 28 August 2002				
70	Send out the STM ICDs	Dustin	Sept. 20	Closed. ICDs issued in preparation for this meeting.
73	Sort out value to be attached to JPL H/W deliveries to UK	Jerry	Before first delivery	Closed. JPL will assign a value corresponding to the marginal cost of replacement of a unit. This will correspond to a few $100k per BDA unit.
Actions from Oct. 22 telecon				
77	Clarify with JPL and MSSL what will be the policy for accelerometry for warm and cold STM vibration tests.	Eric	Report on progress at next telecon	Closed by subsuming under Action 65.
Actions from Nov. 12 telecon				
83	Assess implications of Viktor's proposed specs. on the DRCU and compatibility with the existing QM1 design.	CEA	Detector Meeting on Dec. 12/13	Closed. See minutes of splinter meeting on this subject (Section 7.1.1)
85	Assess feasibility of Boulder or CEA for EM electronics tests	Jerry/Jean-Louis	Next telecon (Nov. 19)	Closed. See section 7.2 below.
86	E-mail Eric on proposed STM delivery dates	Jerry	Nov. 15	Closed in discussion of Business Agreement revision. See Section 6 below
Actions from November 19 telecon				
88	Review JPL schedule with objective of maintaining required delivery dates.	JPL/RAL	Continues	Continuing. New baseline defined in revised Business Agreement.
89	Respond to Jamie's ECR list	Bruce	Nov. 26	Closed. See these minutes, Section 2.
Actions from November 26 telecon				
90	Determine whether BDA accelerometers can be used at 20 K.	Jerry	Next telecon if possible	Closed.
91	Write note on Kevlar tension tests for the UK Project and Lionel.	Jerry to arrange	For Dec. 12 meeting at the latest	Closed. See Section 4.5 and Annex 2 to these minutes
Actions from December 3 telecon				
92	Send Jamie plots revealing cooler cold and warm Q-factors if available	Eric	6 Dec.	Open
93	Liase with Lionel on setting up cooler/Kevlar MRB	Bruce	11 Dec	Closed. Lionel agrees it's a good idea. MRB will require JPL, RAL, MSSL, Cardiff, CEA, ESA. New action on BMS to propose date and venue

No.	Action	Responsible	Due date	Status
94	Liase on planning a "dummy shipment" to test the process before "non-return" flight hardware is shipped to RAL.	Jerry and Eric	6 Dec.	Open. Bruce to raise at PT meeting Monday. If JPL qualify the CQMs, then the process will need to be sorted out soon as they will then not go back to the US.
95	Update Pete on when CQM SLW and SSW filter stacks needed (by tomorrow)	Jerry	6 Dec.	Closed. Need dates are defined in update to Business Agreement.
96	Issue draft agenda for Detector Meeting	Matt and Bruce to	6 Dec.	Closed
97	Check if Lionel can attend the Detector Meeting	Bruce	11 Dec.	Closed - Lionel can't attend

2. Review of JPL documents

- The JPL document set was reviewed - See Annex 1 for a summary of the discussion and list of points raised.
- Actions from this are not included here - it is assumed they will be covered through normal work.

3. JPL EIDP contents

- Standard RAL template was sent out by Eric on September 16
- JPL will review this and comment
- RAL template should be regarded as an initial guide
- If there is a standard JPL template, it is likely to cover most areas
- A guideline is that most of the EIDP should be compiled from existing documents produced within institutes as part of normal engineering and PA work rather than material specially for the EIDP.
- For the bolometers, the Project (and ESA) would like to see clear and comprehensive information on the detector characteristics and performance.
- Action: Gary to arrange for JPL comments on the EIDP template to be sent to Eric
- Action: Bruce to propose set of data on bolometer performance and characteristics to be included in the EIDP.

4. JPL programme overview

4.1 Performance testing plans

- Gary handed over latest SPIRE BDA Cold Vibration Test Plan (D-24013) to Bruce.
- Meeting a May 2003 delivery date would necessitate eliminating optical testing. This has been given lower priority than other tests.
- BODAC is being commissioned now and the plan is to have BODAC up and running by the middle of January. The DAQ and the analogue chain are all OK. In-band noise tests with resistor packs are starting now, and the Pathfinder BDA will then be used for dry run
- Two months testing per BDA is assumed.
- PFM testing has to start in June to stick to the PFM schedule.
- The test schedule assumes that JPL can "fill the pipeline" with BDAs to be tested - so the Kevlar problem has to be solved quickly.
- Bruce: the possibility of another visitation from the UK could be considered provided ITAR restrictions don't make that impractical.

4.2 Feedhorn testing status

- Action: Gary to send the now available feedhorn test report to Bruce and Matt..
- Optical efficiency values have been updated through the SSSD ECR.

4.3 JFETs

- QM JFET assembly is being finished now.
- A wiring error on the boards has been fixed by remanufacturing - new board arrival is imminent.
- QM tests will start next week.
- Cold measurement of the offsets; vibration and thermal cycling; noise tests to be done by end Feb.
- CQM build will be in parallel and CQM tests will start immediately after the QM tests.
- The six JFET mass dummies are on schedule.

4.4 RF filters

- JPL have had a bad time with Cristek.
- After strong representations to Cristek top management a recovery plan has been defined. The programme is to be tracked by weekly telecons.
- The QM RF filter unit should be at JPL on December 24.
- Action: JPL to make sure that the chimney is clear.
- The 12 STM units are due by the end of February.
- The extent of validation tests at JPL is TBD, so a few weeks is to be allowed for that. Temperature cycle tests will be very important
- Action: Gary to check whether thermal cycling will be done by Cristek or whether it will need to be done at JPL.
- Bruce: In case there are problems with delivery of the RF filter modules in time for the STM, we may need to plan for dummy units built to the ICD but with straight wire connections internally.
- Action: Gary to investigate feasibility of providing dummy RF filter modules as a backup if needed.

4.5 Kevlar performance and stability

- Terry and Henry have run tests to simulate all the steps involved in BDA assembly procedure
- Analysis of these and other data points to the following interpretation:
- The stiffness is very high, so a small change in extension corresponds to a large change in tension
- The CTE is much higher (factor of 3) than implied by data in the literature.
- The Kevlar is expanding on bake-out and cooling resulting in a big drop in tension.
- See Annex 2 for details
- Action: Bruce to arrange dedicated Kevlar telecon in early January and circulate relevant parties proposing date and venue for Kevlar MRB.

4.6 JFET offsets

- CEA propose 13 mV instead of 15 mV
- It was agreed that 13 mV should be adopted for the specification. If it is found that this cannot be met when JFETs are being selected, then JPL will submit a waiver.

4.7 Mechanical qualification

- Issues to be sorted out are Kevlar behaviour and vibration requirements.
- JPL want to finish the flight qualification for the CQMs (which will become Flight Spares), which requires qualification before measurement of the real levels in the instrument STM (which is planned for April 2003).
- JPL need to clarify the requirements with Berend
- Test data to date indicate that the BDA can survive at levels of 0.2 g^2 Hz^{-1}

- But slipping is the open issue - it occurs even at low-levels (0.02 g^2 Hz^{-1}). The baseline solution is to increase pretension. If that works then the programme is OK. If not then more work will be needed and then there will be delay and a big risk for qualification. In that case would ship CQMs would be unqualified and JPL would have to qualify them in later years.
- JPL have new CTE measurement programme (Gary to get report tomorrow)

4.8 Harness definition

- JPL are holding issue of Tekdata harness contract until HDD Issue 1.1 is issued. The due date for this is December 20.
- Action: Doug to issue HDD by December 20 as a matter of high priority.

4.8.1 Telecon on vibration levels with Berend

- Berend: The email of 12 November stands and is the specification against which JPL are allowed to notch in their subsystem tests. This is a spec four times lower than last year with the allowance to notch.
- Gary: Force limiting should provide an additional roll-off above the instrument first mode (according to Terry) - should provide additional reduction above 200 Hz which is where BDA is most sensitive.
- Berend: Analysis of the impact of force-limiting at instrument-level showed very little difference.
- These levels are still higher than what we said at the ESTEC meeting we needed at the BDA.
- Berend: It's hoped that in STM tests levels (in March/April) the actual levels will turn out to be lower
- Gary: Misalignment is the major worry.
- Bruce: If it keeps moving serially in the same direction it's a serious problem with a possible thermal short - for qualification this must be demonstrated not to be a problem.
- Note: Berend away until 7 Jan.

5. Instrument-level schedule overview (Bruce)

- Two versions of the CQM AIV schedule have been produced:
  (i) Full version including all desired STM tests, with delivery in February 2004
  (ii) Curtailed version with STM thermal tests eliminated to allow delivery in November 2003.
- SPIRE has told ESA and Industry that we will work towards delivering on time if required. For that, the BDAs and the QM1 electronics would need to turn up in time.
- A clear response from Industry on which versions of the schedule we should follow is needed by the end of February
- Jean-Louis: Staffing problems at LAM mean that QM1 integration is not going to be possible until June, maybe later. The DCU should be OK - maybe March. For the FCU, there are no technical difficulties but some management problems. CEA deliveries are generally OK for the longer schedule.
- So to meet the compressed schedule would require integration of the MCU at RAL
- August is a bad period due to the French holiday season
- Action: Matt to consult with Bruce and Eric and write formally to Passvogel emphasising the need for a clear and well-thought-out decision on whether SPIRE should pursue a full or curtailed STM/CQM schedule.

6. JPL Business Agreement Revision

- Annex A to the Business Agreement was updated.
- Action: Matt to circulate the final version of the ECR and the updated Business Agreement for signature.
- Points noted during the discussion:
  - Since JPL will have all the parts, it could make sense for them to assemble the JFET rack
  - Need to keep JPL technical team alive for post-delivery support.

- JPL's favoured option is to deliver qualified CQMs which will not need to be refurbished for the FS.

7. Warm Electronics

7.1 Unit-level delivery acceptance testing of the DCU

After discussion in the main meeting and with Jamie by telephone, the following baseline was agreed:

- *Test philosophy*
  - *It is noted that the IID-A specifications are for unit-unit configurations, and so are not fully applicable in this case (noise exported by the DCU to the BDAs) because the current levels are very low.*
  - *Acceptable noise levels shall be specified in terms of voltage.*
  - *The test set-up shall be specified. It will involve measurement at the DCU interfaces to the BDA without connection to a flight representative external harness.*
  - *Nominal impedance values shall be given to allow current levels to be verified by calculation.*
  - *This test applies to the integrated DRCU (i.e., including the DCU and its flight power supply).*

- *Definition of test specifications*
  - *JPL have provided noise voltage specifications at the DCU bias and JFET power outputs*
  - *JPL will provide in addition the nominal impedances that are applicable at frequencies from DC up to 10 MHz*
  - *The maximum acceptable noise level at higher frequencies is 150 uV rms from 10 MHz up to the 100 MHz (corresponding to at least 30 dB of attenuation by the RF filters)*

- A splinter meeting (Viktor, Dominique, John, Christophe) was held with the objective of defining the above more quantitatively and with considering whether an alternative test scheme suggested by CEA, involving current measurements on bundles of DCU lines, could be better.
- It is noted that EMI picked up by the harness could inject more noise than the DCU, and that this must be assessed, but the purpose of the current exercise is to place specifications on the conducted noise produced by the DCU itself, and to define how the DCU can be verified with respect to those specifications by unit-level testing

7.1.1 Report from DCU specifications splinter (John)

- Revision of test philosophy and test specifications
- The test philosophy and definition of test specifications given in Section 7.1 above were recast as follows (with some minor wording changes by Matt in addition):

Test philosophy

- *Acceptable noise levels shall be specified in terms of Voltage (TBC) at the DCU connector interface under defined test set-ups.*
- *The test set-ups shall be specified. Parameters will be measured at the DCU interfaces towards the BDA, but without connection to a flight representative external harness*
- *The test philosophy shall distinguish between the operation of the DCU in flight and how it operates in the test configurations. The latter should give at least spot measurement confidence of successful operation in the former.*
- *Nominal impedance values for flight and test shall be considered (with a defined accuracy spread if this is relevant to the parameter being assessed). Modelling shall tie together the current/voltage/power as needed to relate specifications with measured variables.*
- *These tests apply to the integrated DRCU (i.e., at least the DCU and its flight power supply) and shall form part of SAp-SPIRE-HT-0088-02.*

- *It is noted that the IID-A specifications are for standard equipment unit-unit configurations, and so do not correspond to the full requirement or necessarily the best test configurations in this case.*

Definition of test specifications

- *JPL have provided noise voltage specifications at the a.c. bias and JFET Vss/Vdd DCU outputs. They have also specified a total LIA differential input noise contribution.*
- *The maximum acceptable DCU equivalent input noise contribution at higher frequencies could be 150 nV $Hz^{-1/2}$ from 10 MHz up to 1 GHz (TBC by JPL as this is higher than the integrated 150 mV rms previously suggested).*
- *JPL will provide in addition the nominal cold-end impedances that are applicable at frequencies from DC up to 10 MHz*
- *Actions below formulated on 13th December should be major steps towards establishing both test configurations and test specification values.*

- Further discussion
  - Dominique suggested a configuration that could measure CM voltage
  - Viktor proposed linking tests closely to what the modelling did.
  - Dominique showed an input averaging adaptor plugged over a bundle into the DCU to measure CM voltage. This involved inductors.
  - There was discussion of the need for capacitors, the size of resistors that would not compromise the noise, the use of 50-Ω termination to suit low noise WB EMC equipment (and would it attenuate noise itself?).
  - A filter connector could be an easy way to provide a lot of capacitors.
  - Conclusion: any test needs very careful design and analysis before it is carried out.
  - An equivalent circuit presented by Viktor (see Annex 3) was discussed.
  - It might be necessary to build a special low-noise amplifier in order to carry out the tests and maybe not just feed signals straight into standard test apparatus.
  - Discussion on how not to include differential noise in the common-mode measurement.

- Actions:
  - Viktor to produce a note before Christmas working through some of the discussion, considering the use of bundled wires.
  - Dominique to draft out possible test configurations before Christmas.
  - JPL and CEA to respond to the other's suggestions within a further two weeks, in detail, in writing, not concentrating on matters not previously raised by the other.
  - John to obtain and circulate better values for the cryoharness impedances, particularly the proposed shields.

- Note: Dominique will not be not available until mid-February - Christophe will be only communication point until then.

7.2 EM test location: Boulder or Paris

- Gary:
  - JPL discussed this internally after the last telecon. Jamie regards the first tests as very important and to be done optimally.
  - The system is working in Colorado and JPL can support meaningful tests there in January. If system is moved, tests will likely be later - not desirable.
  - So JPL prefer to test in Colorado first then ship
- Jean-Louis:
  - The schedule is a worry, with the possibility that the electronics may not be ready in January.
  - The dewar needs to be moved to CEA anyway
  - There is an advantage in shipping the dewar in a period when tests are not being done.

  - CEA are willing to send staff to Colorado to learn all about the system.
- Gary:
  - If the tests in Boulder slip to February then JPL can probably accommodate that
  - Viktor and Jamie will not be able to spend long periods at CEA.
  - Can CEA could take responsibility for learning how to set it up in Colorado and then setting up at CEA?
- Matt:
  - CEA staff would have to be able to run, assemble, disassemble and check out the dewar - be able to set it up at CEA just as it was at Boulder.
  - A standard test needs to be defined that can be repeated at CEA having been done initially at Boulder
- Jean-Louis:
  - If the system was well-understood by CEA staff, then CEA would need some level of assistance but not for long periods. The main area where Jamie and Viktor would be needed is in ensuring the tests are properly set up and to validate the measurements

- Conclusion:
  - If the in-depth training of CEA staff can be assured (and agreed in writing) by JPL/CEA then the CEA option looks acceptable
  - JPL would be responsible for demonstrating that the system at Boulder, and CEA responsible for receiving and recommissioning at CEA.
  - Action: Gary and Jean-Louis to produce a proposal based on CEA taking responsibility for setting up the system in CEA having received relevant in-depth training beforehand at Boulder.

7.3 Splinter meeting on the DCU/telemetry interface (Bruce and Christophe)

- Bruce has produced a separate write-up of this splinter and distributed it to CEA

7.4 RF filtering within the DCU

- The present DRCU design does not have any RF filters between the analogue and digital parts, nor are there connectors between them.
- CEA's philosophy is that they are responsible for producing a design to meet explicit specifications at the interface.

7.5 DRCU Document review status

- Most of the comments can be implemented in the next versions in a routine way.
- Today's splinter meeting on the DPU interface has further clarified some issues.
- The DCU is in good shape; the FCU and SCU need some more attention
- Matt: Can we have deadline date for revised document?
- Internal CEA review is needed before final versions of the documents can be released. The plan is to issue them one-by one as they are produced.
- John: Specification and interface docs are the highest priorities
- Conclusion: CEA will update the documents with a target date of the beginning of February..

7.6 DCU EM/QM1 Preliminary Test Plan

- Henri has written a first draft test plan (see Annex 4) working from the specifications in the BDA SSSD (copies were distributed at the meeting)
- Action: John and Viktor to provide e-mailed comments (by 20 December) on the test plan, especially on
  - the appropriateness of the tests to verify the requirements;
  - whether any other tests are needed;

- the test principles initially (details can be defined later)
- the QM1 configuration (as opposed to the final configuration.

7.7 Plan for March DRCU Programme Review

- CEA are concerned that the review should not create too much extra work
- The situation at LAM is a major concern at the moment
- The broad objectives of the review are as in Matt's e-mail to Jean-Louis and Laurent. The approach is to make sure the review gives us a clear picture of current status and future options.
- The review format and preparation should be based on a more-or-less completed DDR plus a review viewgraphs package without the need to write many new documents specially for the review.
- The review should therefore take note of rather than scrutinise in detail the technical design
- Important issues would be the AIV plans, the model philosophy, the level of resources available to implement the plan
- Action: Matt to clarify the review format and objectives by drafting a proposed agenda and review preparation plan.

7.8 JPL-CEA warm electronics test results/future programme

7.9 PSU procurement status

- Sign-off foreseen in June
- 14 month lead time from contract kick-off
- One STM, one EM, and one FM will be built.
- The EM will be tested with QM2
- The PSU procurement is on the CEA critical path

7.10 PSU Specification

- RAL will consolidate comments raised into an E-mail.
- CEA will check board level turn on current transient, and to compare with latch-off area of post regulators.

7.11 Mass and power breakdown

- The mass budgets submitted by CEA in mid-2002 were based on a computer mechanical model.
- Tests on STM will consolidate the mechanical design
- The PSU contractor has not yet been chosen, and hence has not confirmed that the unit can be realised within the mass allocation.
- Power taken by initial boards indicate that the power budget is OK to stay as it is at present.
- The PACS supply efficiency is estimated to be 65-75% which would be OK for SPIRE.

7.12 FMECA

- It is thought that CEA's DRCU FMECA may have been carried out before the inclusion of the LIA power supply post-regulators.
- These is a cross-link between halves of the LIA boards.
- Certain functions are also cross-linked in PCB tracking between halves of the LIA boards before travelling via pins to the DCU motherboard.
- Unless risks of failure appear high and not just statistical, the present routing of the BDA pixels through the LIAs will be maintained.
- Action: Christophe to check FMECA and update if necessary.

8. Thermal modelling/JFET tradeoffs

- Not covered due to lack of time. To be addressed in weekly telecons

9. Planning of JPL AIT support for 2003 and 2004

- Not covered at the meeting due to lack of time
- Action: Matt to include support of AIT at RAL on the agenda for the next telecon.

10. Summary of all open actions

Actions from July 9 telecon				
No.	**Action**	**Responsible**	**Due date**	**Status**
47	Update Major Milestones List	Ken	Next telecon (July 23)	The MMA is to be updated in accordance with the dates for JPL deliveries agreed at this meeting for the updated business agreement.
Actions from August 20 telecon				
No.	**Action**	**Responsible**	**Due date**	**Status**
65	Draw up vibration test procedure for the instrument STM, including policy for accelerometry.	Berend	Feb. 1	To be addressed after the FEA analysis is complete. Open
Actions from November 19 telecon				
No.	**Action**	**Responsible**	**Due date**	**Status**
88	Review JPL schedule with objective of maintaining required delivery dates.	JPL/RAL	Continues	Will be addressed at weekly telecons and by e-mail as appropriate. Continuing. New baseline defined in revised Business Agreement.
Actions from December 3 telecon				
No.	**Action**	**Responsible**	**Due date**	**Status**
92	Send Jamie plots revealing cooler cold and warm Q-factors if available	Eric	6 Dec.	Open
94	Liase on planning a "dummy shipment" to test the process before "non-return" flight hardware is shipped to RAL.	Jerry and Eric	6 Dec.	Open. Bruce to raise this at PT meeting Monday. If JPL qualify the CQMs, then the process will need to be sorted out early as they will then not go back to the US.
95	Update Pete on when CQM SLW and SSW filter stacks needed (by tomorrow)	Jerry	6 Dec.	Closed. Need dates are defined in update to Business Agreement.
Actions from this meeting				
No.	**Action**	**Responsible**	**Due date**	**Status**
96	Arrange telecon on Kevlar in January in preparation for MRB	Bruce	15 Jan.	
97	Issue HDD (high priority)	Doug	20 Dec.	To be sent out by Doug Monday Dec. 23
98	Arrange for JPL comments on the EIDP template to be sent to Eric	Gary	15 Jan.	
99	Propose set of data on bolometer performance and characteristics to be included in the EIDP	Bruce	15 Jan.	
100	Arrange for feedhorn test report to Bruce and Matt.	Gary	6 Jan.	
101	Check whether thermal cycling will be done by Cristek or whether it will need to be done at JPL.	Gary	15 Jan.	

102	Investigate feasibility of providing dummy RF filter modules as a backup for the STM if needed	Gary	15 Jan.	
103	Write formally to Passvogel emphasising the need for a clear decision on whether SPIRE should pursue a full or curtailed STM/CQM schedule.	Matt	15 Jan.	
104	Circulate the final version of the ECR and the updated Business Agreement for signature.	Matt	20 Jan.	Closed 19 Dec.
105	Produce a note before Christmas working through some of the discussion, considering the use of bundled wires.	Viktor	20 Dec.	
106	Draft out possible test configurations before Christmas	Dominique	20 Dec.	
107	Respond to above notes	JPL, CEA	15 Jan.	
108	Obtain and circulate better values for the cryoharness impedances, particularly the proposed shields.	John	15 Jan.	
109	Produce a proposal for EM testing at Saclay based on CEA taking responsibility for setting up the system at CEA having received relevant in-depth training beforehand at Boulder.	Gary and Jean-Louis	15 Jan.	
110	Provide e-mailed comments on the draft QM electronics test plan	John and Viktor	20 Dec.	
111	Draft proposed agenda and preparation plan for DRCU review	Matt	20 Dec.	Closed 20 Dec.
112	Include JPL support of AIT at RAL on the agenda for the next telecon.	Matt	6 Jan.	
113	Check DRCU FMECA and update if necessary.	Christophe	1 Feb.	

11. List of Annexes

1 Review of JPL Document Set

2 Summary of JPL measurements of Kevlar properties

3 Cold-end-harness-warm-end equivalent circuit

4 DCU EM/QM1 Preliminary Test Plan

Annex 1

Review of JPL Document Set

Delivered documents

721-A:
- Is signed - RAL need signed version back from JPL.
- Change notice for sheet 7/7 position G11 needs J01 changed to J05 – JPL need to raise this.
- Sheet 2/7 show pin 1 position on connectors JD CR.
- The viewing holes for alignment need to be shown – need to call up filter mount ICD for the fiducial marks?

722-A51:
- RAL will sign and this goes under change control – need 3-D model that goes with this drawing

723-A:
- Is signed – RAL need this back from JPL with JPL signatures on

725-A121:
- Changes to sort out wiring inconsistency (+/- sense of pixels) have been implemented.
- J04 shows channels x,y,z as temp control – should add note that these are channels allocated for t/c but they are conditioned by a separate JFET module – this will be done by CR.
- Correction of position of S/LW connector has been implemented – now comes on J05.
- Are the unused channels really still connected or are they disconnected?

727-X21:
- Resistor packs? – make this "A" version for signature.

- 728-X11:
  Resistor packs? – include accelerometer and cabling on drawing.

Backharness ICD will not exist – RAL are providing JFET racks to JPL – these will be shipped in new year. Gary will advise on the procedure for this.

Interface Control Document

- Section 4 Ref1 should be Doug's document for Tekdata contract – Bruce to find
- Ref 2 is Cardiff declared material list – Bruce to find
- Ref 3 design description doc. – Bruce to find
- Figure 1 – Update diagram to make like it should be.
- Section 6.3.1 – washer type – should these be Bellville types to take up thermal mismatch? Dustin to check with MSSL.
- Refs 6,7,8 are not provided – where did Ref 4 and 5 go?

- 6.3.3 – should be headed “Cristek Filter Module”
- New words should be added into section 6.3.3.
- “The RF Filter Modules (ICD3) shall be secured in place by RAL supplied studlocks see A3-KE-0104-375-A torques to 2 lb-in and A3-KE-0104-374-A locked with locking screws A3-KE-0104-376-A.”
- Reference the RAL drawings in the RD list.
- Section 6.4.1 - drawing needs to be improved
- 6.4.2. Textual change – “wiring for JFETS and BDAs is shown in diagram in ICD4”
- 6.4.2 – John will check connectors offline – add text “these are termed backharnesses” in middle of sentence.
- 7.1 The Kevlar pre-load value was 33 it is currently 50 but is subject to change.
- References should be uniform throughout document.
- 7.2 Reference definition of MOS or give formula.
- 8 Incorrect reference? Should be ICD1. Wording doesn’t make sense as written
- 9 References are wrong – should be ICD4 and ICD5.
- 9.1 Add a general statement under 9.0 “Numerical values are to be found in AD4” – that is call up the SSSD to define the word “accurate” etc…
- 9.5 should be split into description of the backharnesses and the F-harnesses which link the JFETs to the BDAs.
- Where have the DML and DPL gone – note these in “Section 10” as references.

SSSD-ECR

- PFM JFET optimisation
  - Tentative agreement is that they should be optimized for operation at ~120K and a waiver will be applied for if the power dissipation of the PFM units is higher than specified.

Annex 2

Summary of JPL measurements of Kevlar properties

CH 14

Section 513 Fax Cover

JPL
Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena, CA 91101

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TO: GARY PARKS
FAX: 0033 1 43 222180
PHONE: 00331 43 20 02 37

FROM: HENRY ABAKIANS
FAX: (818) 393-4699
PHONE:

REMARKS: ☐ Urgent ☐ For your review ☐ Reply ASAP ☐ Please Comment

Gary,

I am sending the slides as well as the handouts

Call me if you need additional info

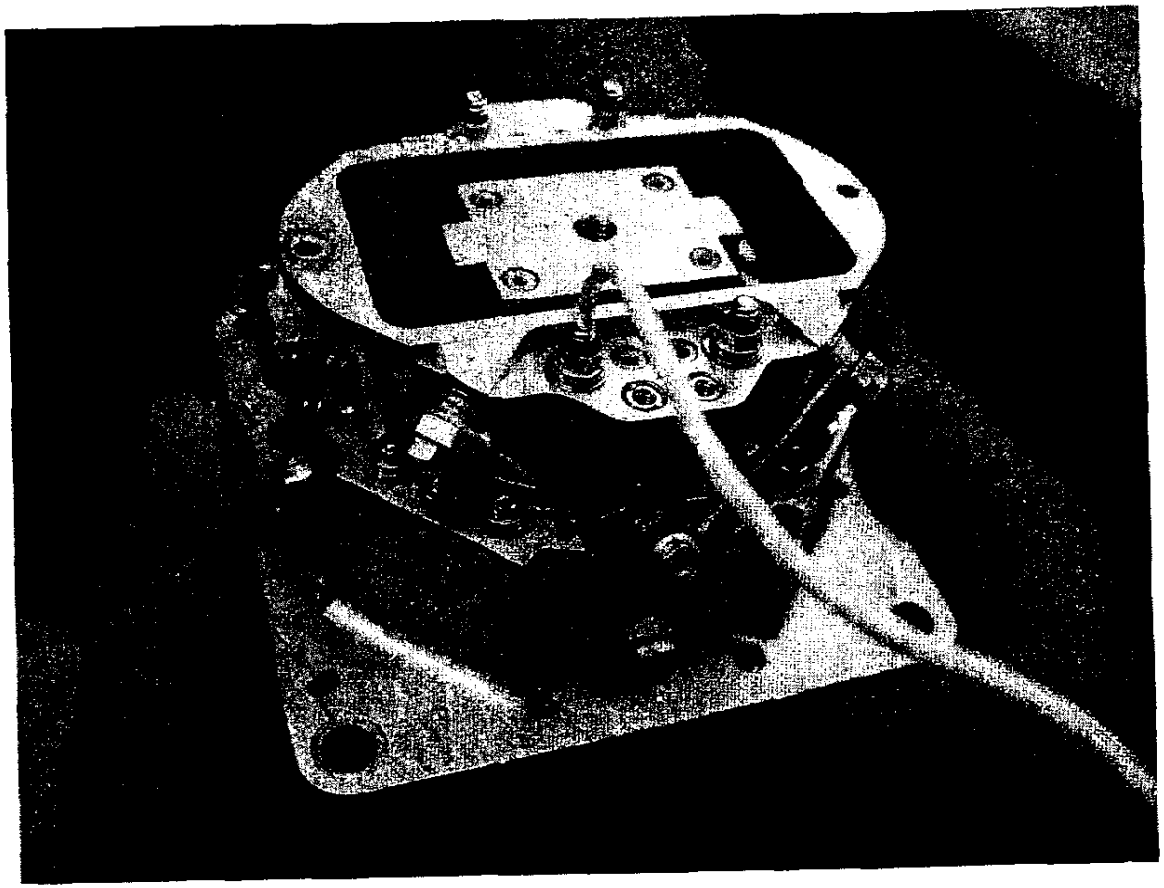
(818) 281-9756

Henry

Herschel/Planck - SPIRE
December 12, 2002

Summary of Vibration testing and material properties measurements

BDA Metrology



Metrology measures centers E and F of the two circles

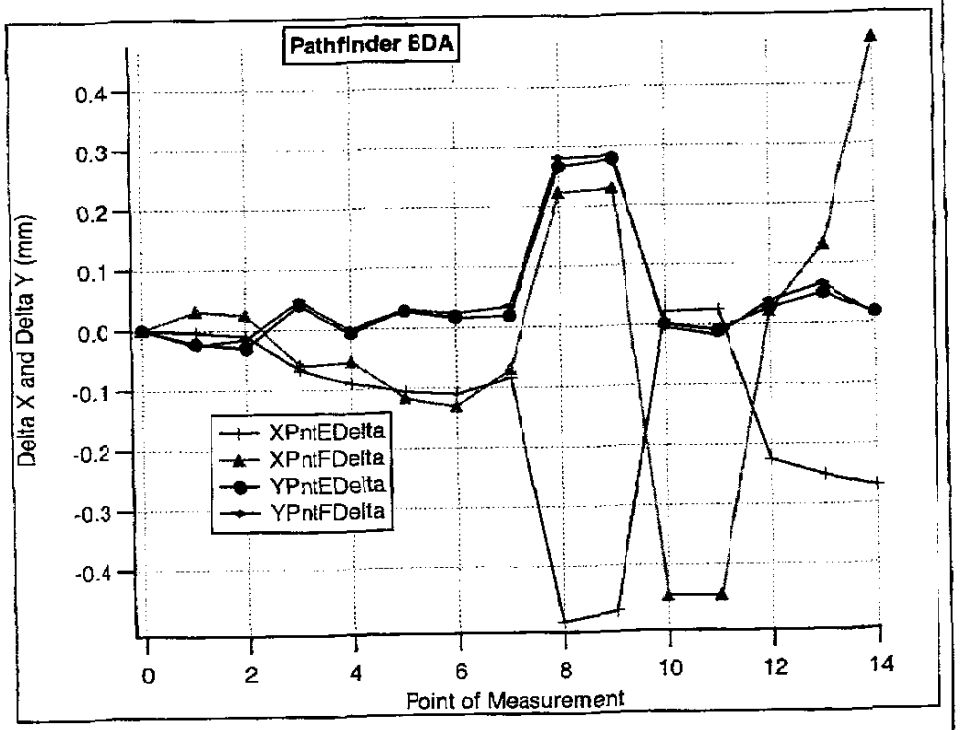
Random Vibration testing for Pathfinder, STM and MQM BDAs

- Only modes at 293 K and 100 K are presented
- The metrology data lists the maximum cumulative movement after test
- No appreciable movement has been noticed in the warm tests (293 K)

Random Vibration testing for Pathfinder, STM and MQM BDAs

BDA unit	Frequency of the first mode at 293K	Frequency of the first mode at 100K	Test level	Metrology (maximum movement)	comments
Pathfinder (33 lbf tension)	242 Hz	256 Hz	0.8 g2/Hz (notched)	500 µm (cold)	2-axis vibe test (z,x)
Pathfinder (15 lbf tension)	210 Hz	-------	0.05 g2/Hz	-------	1 axis vibe test
MQM with shims (33 lbf tension)	248 Hz	284 Hz	0.05 g2/Hz	250 µm (cold) (120+80+50)	3-axis vibe test
STM (33 lbf tension)	276 Hz	238 Hz	0.02 g2/Hz	150 µm (cold)	1 axis vibe test

Metrology Data: Pathfinder BDA unit

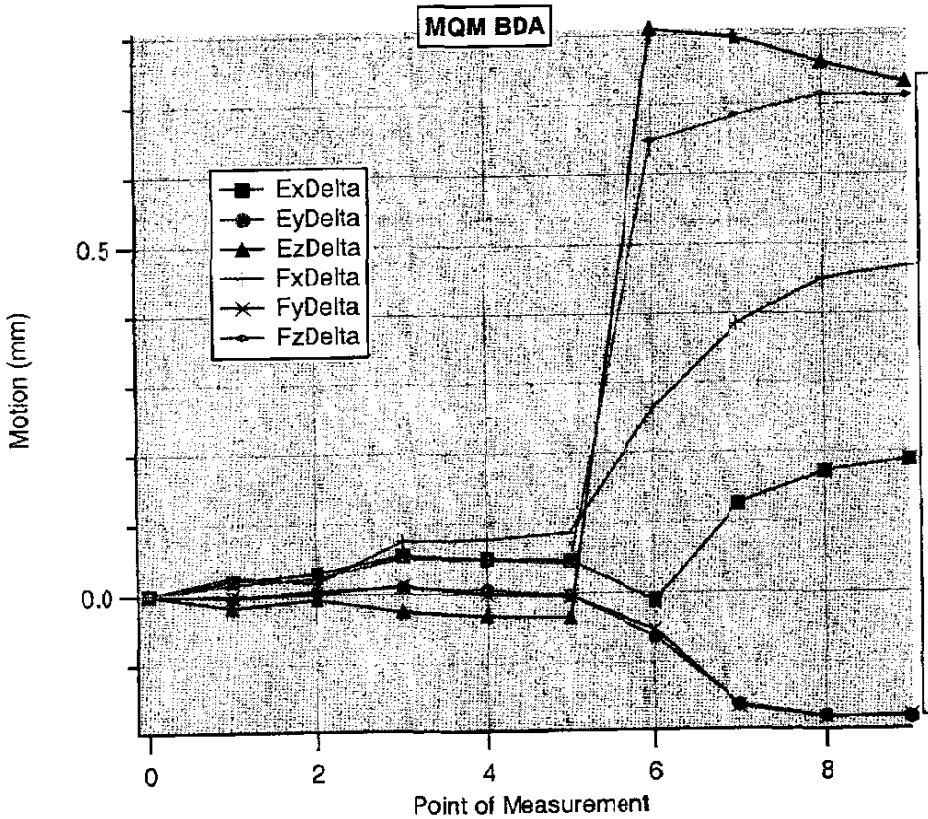


Point 0 : Before initial bakeout
Point 2 : Before warm vibe w/ 1 ¼ wraps. Kevlar broke during warm vibe.

BDA restrung. Point 3, is the re-baseline.

Point 3 : Before warm vibe
Point 4 : After warm vibe
Point 5 : After 1st thermal cycle
Point 6 : After 2nd thermal cycle
Point 7 : After aborted cold vibe.
Point 8 : After Cold vibe to full level ($0.8\ g^2/Hz$ notched) in z-axis and x-axis
Point 9 : With flexure angle measurement
Point 10 : BDA restrung w/ 15 lbs kevlar
Point 11 : 15 lbs in Kevlar, Post signature vibe
Point 12 : Restrung with 33 lbs, Before 0.1 g^2/Hz
Point 13 : After 0.1 g^2/Hz. 1 axis cold,
Point 14 : After 0.2 g^2/Hz. 1 axis cold,

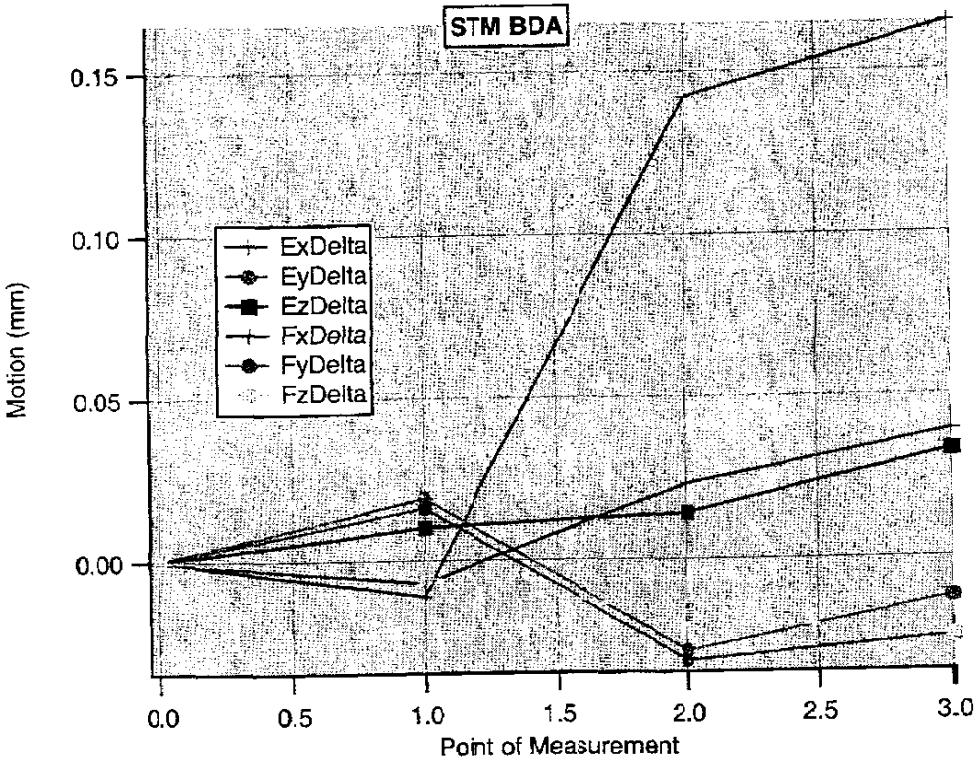
Metrology Data: MQM BDA unit



Point 0:	Baseline (with snubbers, no metal shims)
Point 1:	Post Warm Vibe, 3 axes
Point 2:	Post thermal cycle to 90 K
Point 3:	Post low level random vibe, cold, y-axis
Point 4:	Snubbers removed
Point 5:	Post low level random vibe, cold, y-axis
Point 6:	After Metal shims were added
Point 7:	Post cold vibe test, x-axis
Point 8:	Post cold vibe test, y-axis
Point 9:	Post cold vibe test, z-axis

Test level: 0.05 g^2/Hz
(100 to 300 Hz)

Metrology Data: STM BDA unit



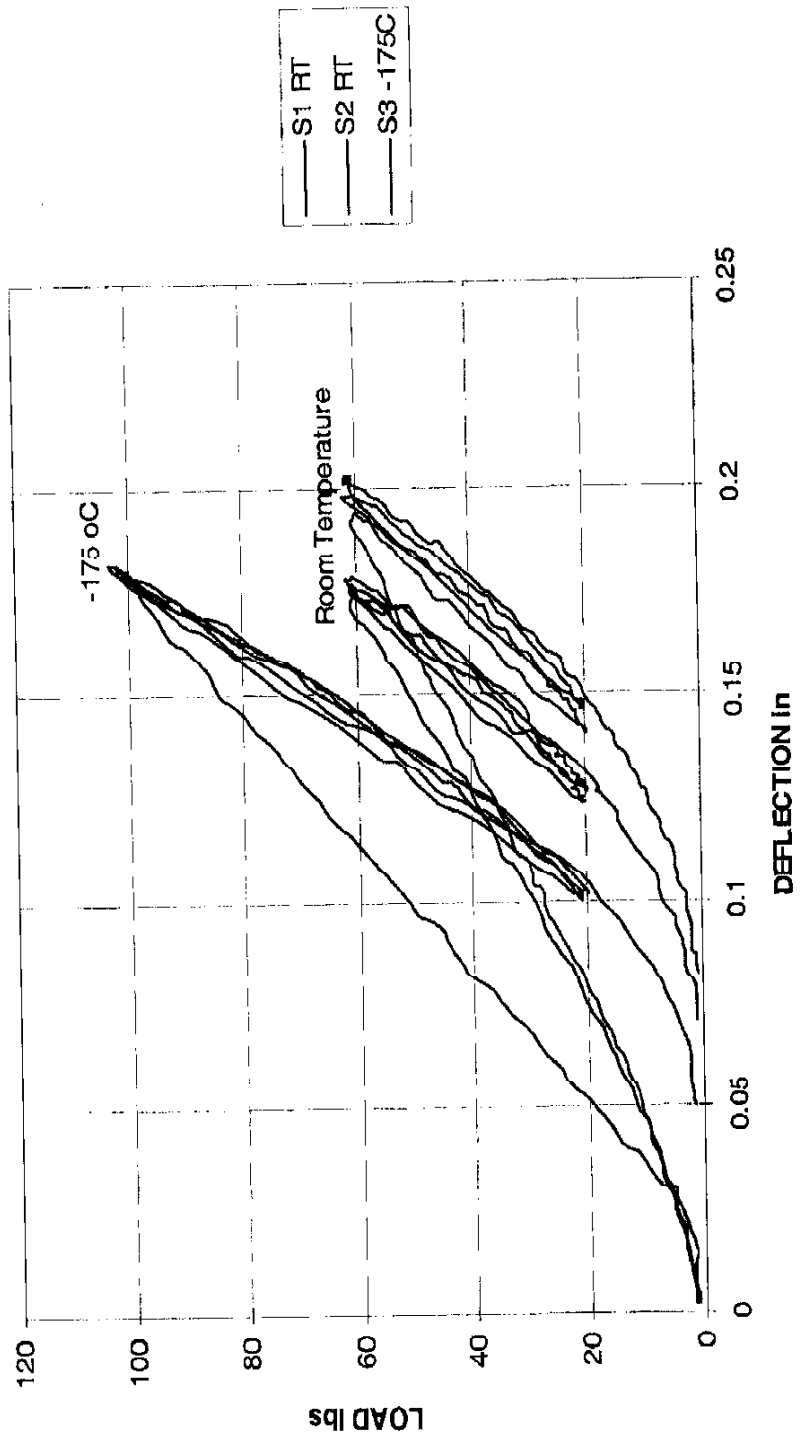
Point 0:	Baseline Measurement
Point 1:	After bakeout, pre-vibe
Point 2:	After Cold workmanship vibe, y-axis
Point 3:	After thermal cycle to 10 K

Test level: 0.02 g^2/Hz
(100 to 300 Hz)

Kevlar and Vespel material properties measurements

	Kevlar	Vespel	temperature	notes
Coefficient of thermal expansion	−14.0 μm/m°C to −11.9 μm/m°C	41.2 μm/m°C to 50.4 μm/m°C	100 °C to −150 °C	
Spring constant	775 lbf/in	N/A	Room temperature	Kevlar samples were 9.0 inches long
Spring constant	1000 lbf/in	N/A	−175 °C	Kevlar samples were 9.0 inches long

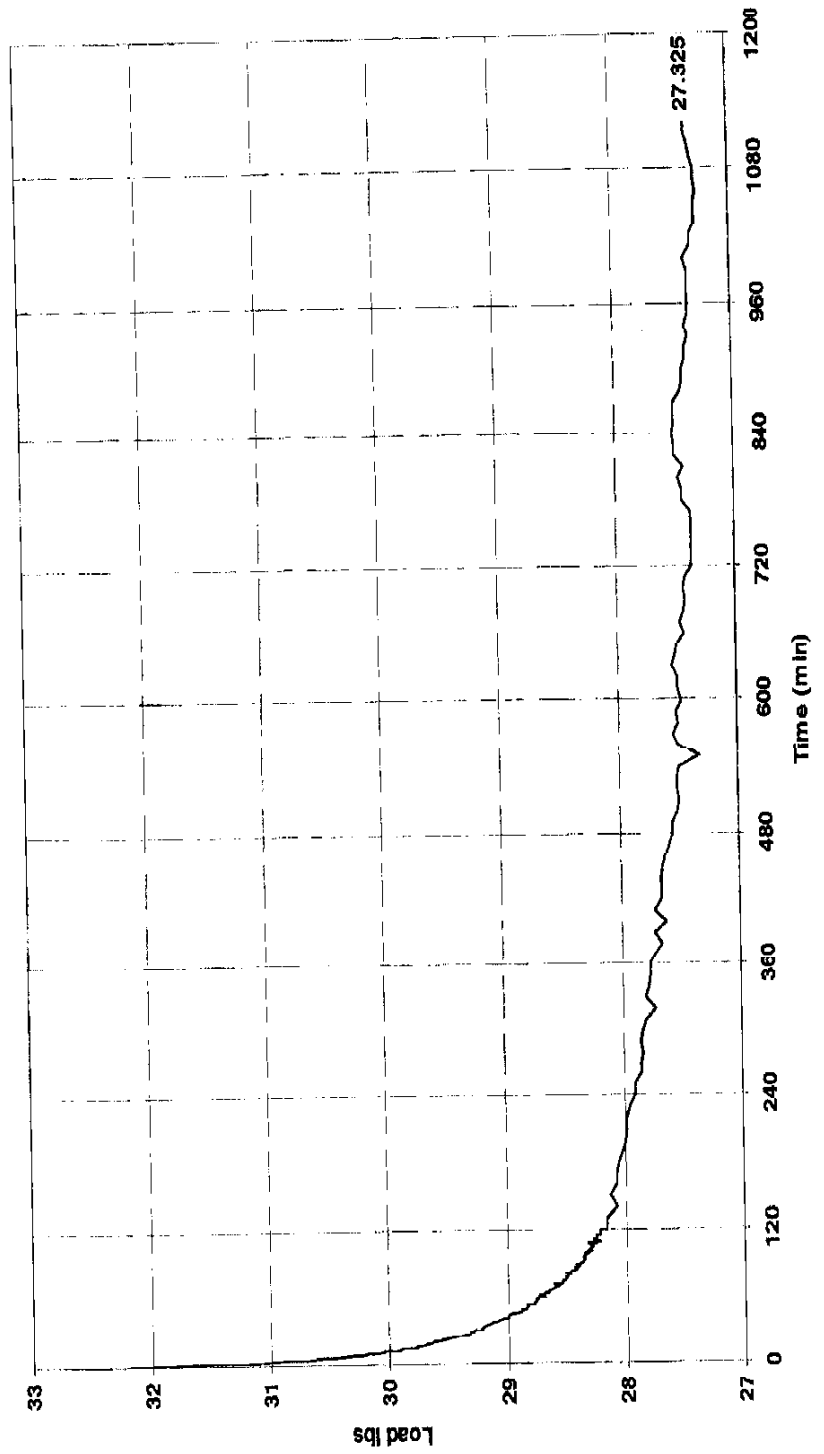
Kevlar spring constant



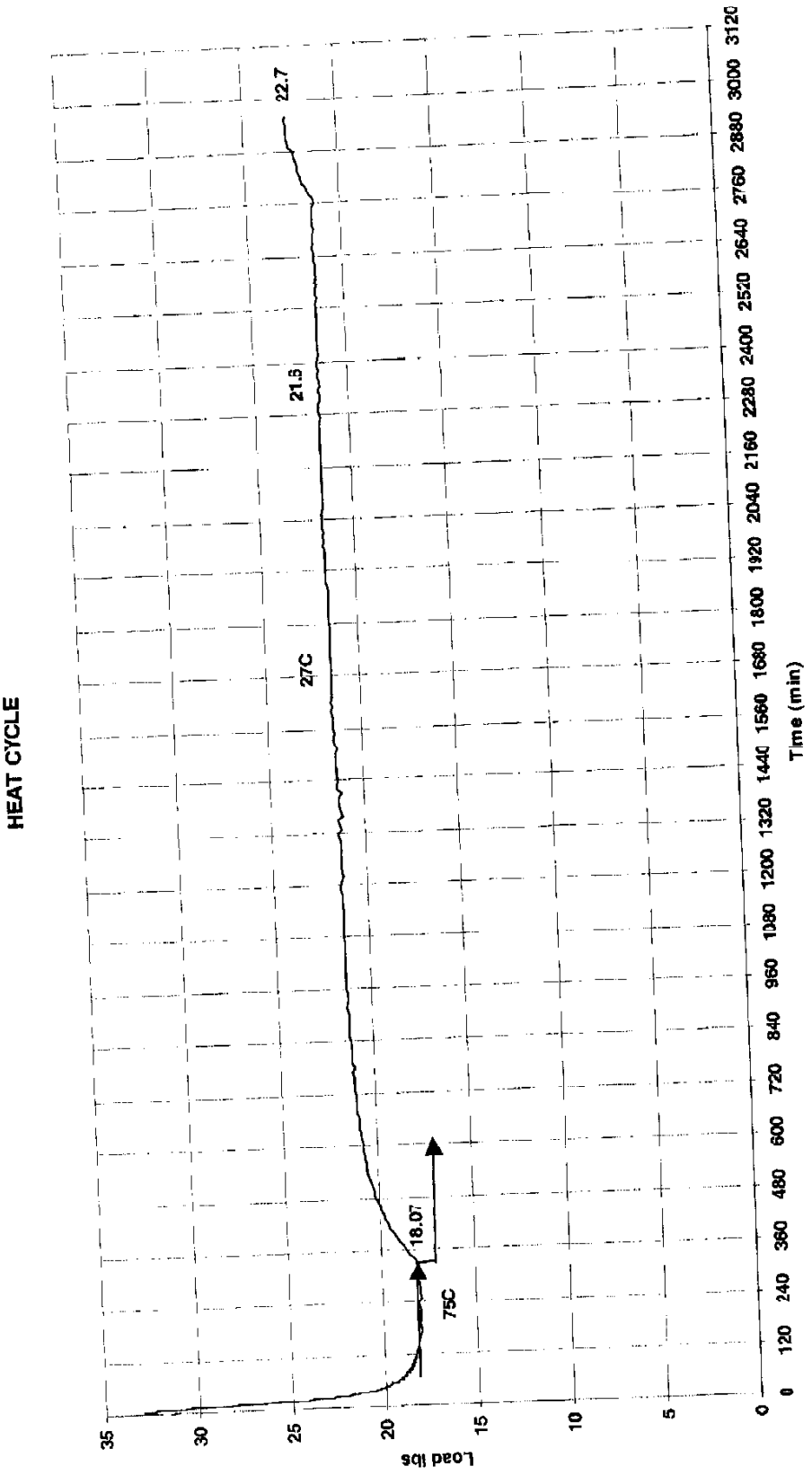
Kevlar tension variations as a function of temperature and time

- A number of tests were performed to ascertain the impact of creep at room, as well as elevated temperatures
- In these tests Kevlar sample length was kept constant (12 inches):
  - Test C1 measured the variation in tension as kevlar was creeping (initial tension 33 lbf).
  - Test C2 re-tensioned the sample from test C1 to 33 lbf, increased the temperature to 75 °C, and back to room temperature

Test C1: Variation of tension as a function of time at 22 °C (kevlar sample length is constant)



Test C2:Tension vs. time as kevlar is heated and cooled (the sample in this test is from test C1 re-tensioned to 33 lbf)



Kevlar temperature test results and Summary

- The kevlar string lost approximately 6 lbf in tension due to creep (this test was performed in 40% relative humidity environment) – Test C1
- The bake out at 75°C caused the kevlar to lose approximately 15 lbf of tension – Test C2
- As the kevlar cooled back to room temperature only 4 lbf of tension was recovered – Test C2
- The above test results are due to creep, as well as the impact of humidity (tension in kevlar drop as relative humidity drops). Preliminary results from repeating test C1 in vacuum indicates tension losses of 11 lbf (vs. 6 lbf in 40% relative humidity)

Herschel/Planck - SPIRE
December 12, 2002

Summary of Vibration testing and material properties measurements

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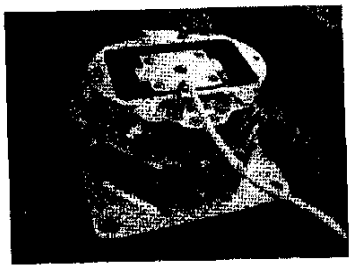

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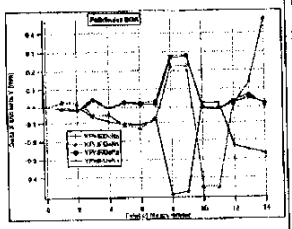
Metrology Data: Pathfinder BDA unit



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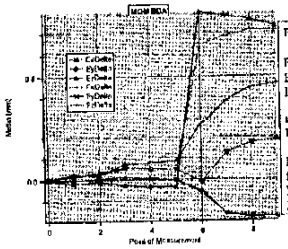

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Point 6: After Metal shims were added
Point 7: Post cold vibe test, x-axis
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Test level: 0.05 g²/Hz (100 to 300 Hz)

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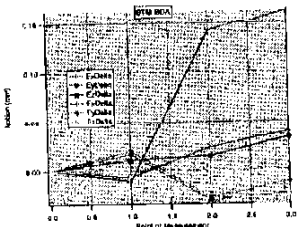

Point 0:	Baseline Measurement
Point 1.	After bakeout, pre-vibe
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Point 3	After thermal cycle to 10 K

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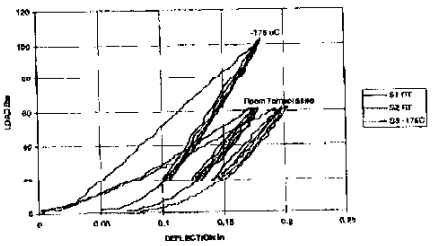

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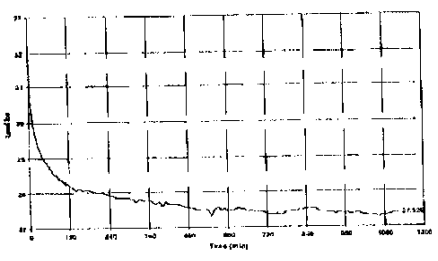

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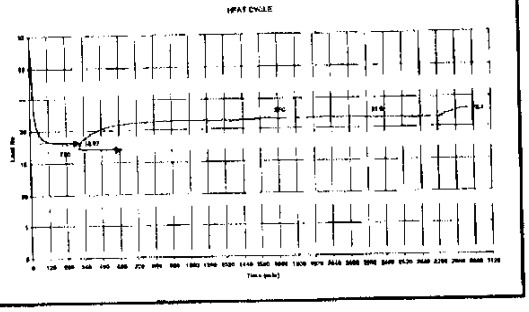

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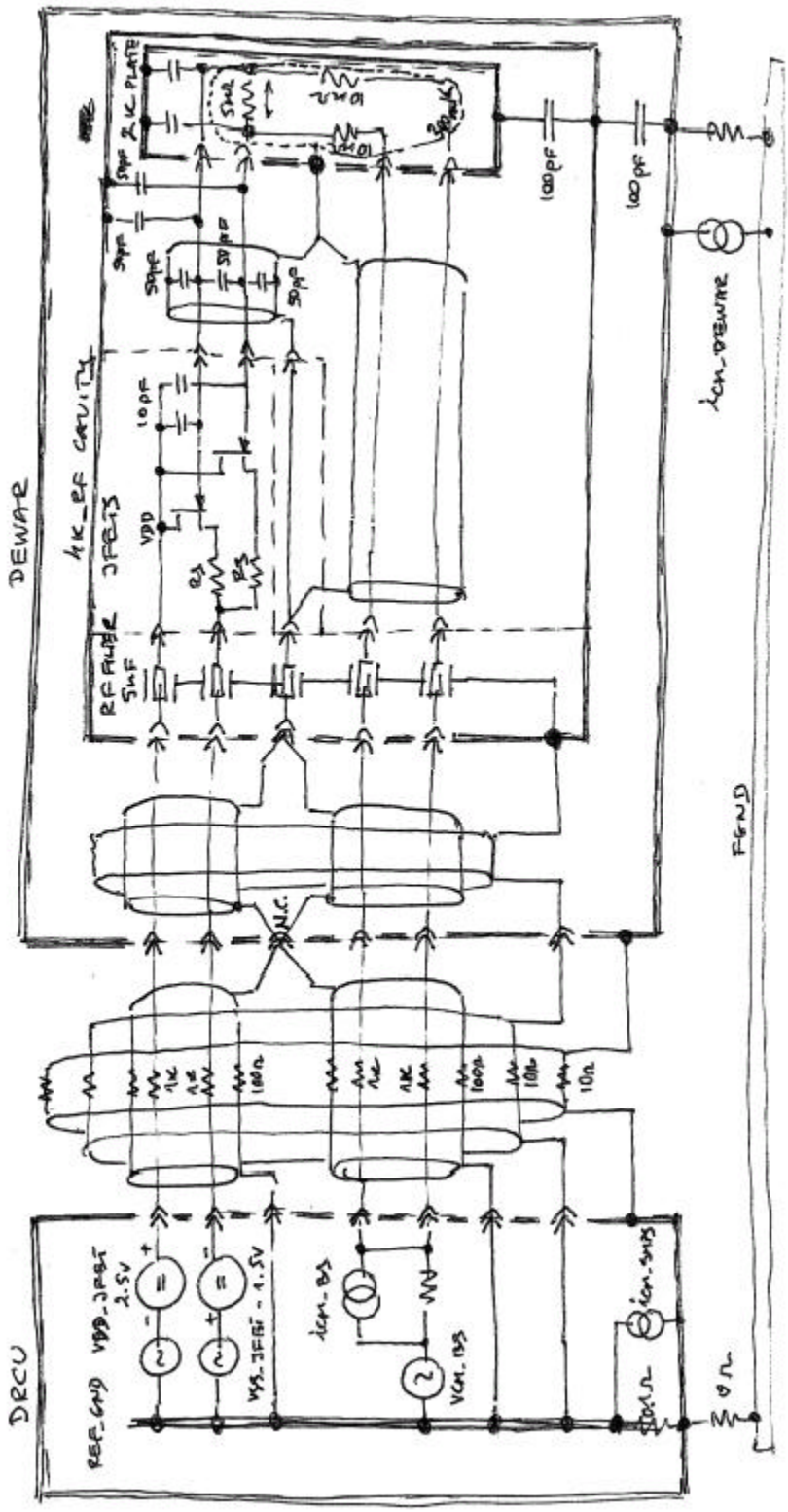
Annex 3

Cold-end-harness-warm-end equivalent circuit

Annex 3: Equivalent circuit model presented by Viktor



Annex 4

DCU EM/QM1 Preliminary Test Plan

HERSCHEL/SPIRE

DETECTOR CONTROL UNIT
EM/QM1
PRELIMINARY TEST PLAN

	Function	Name	Date	Visa
Prepared by	SPIRE AIV	H. TRIOU	26/11/2002	
Verified by	SPIRE SYSTEM	C. CARA		
Approved by				

DOCUMENT STATUS and CHANGE RECORD

Date	Issue	Affected pages
26/11/2002	0.-	Creation

1 INTRODUCTION

1.1 PURPOSE

Following the tests performed on LIA_P, LIA_S, BIAS and DAQ-IF boards, the purpose of this document is to detail the tests that will be performed on assembled DCU unit. This document follows a specific order:

- first the test configuration that will be used,
- followed by the functional tests on assembled DCU EM,
- then the performance tests on DCU EM associated with Bolometers,
- finally the cross matrix showing in which test the requirements are tested.

As a matter of fact, this document describes the functions and performances that will be tested in the frame of the engineering model. Therefore, this document will be used a guideline for a detailed test plan.

1.2 APPLICABLE DOCUMENTS

Herschel SPIRE Detector Subsystem Specification Document	SPIRE –JPL-PRJ-000456
DRCU Subsystem Specification	Sap-SPIRE-Cca-25-00

1.3 REFERENCE DOCUMENTS

DCU LIA_PTEST PLAN	SAp-SPIRE- FP-0064-02

2 Test configuration on assembled DCU

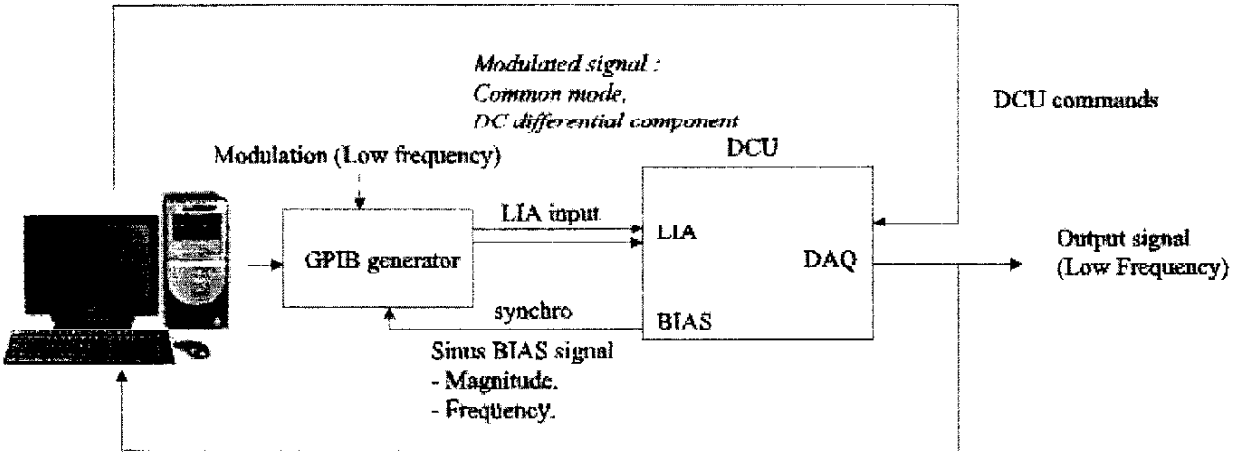
2.1 Boards configuration

For the preliminary tests, we shall work on an assembled DCU EM that contains one LIA_P board, 1 LIA_S board, 1 DAQ IF, 1 BIAS.

The final DCU QM1 will, in addition include one more LIA_P board and two more LIA_S boards.

2.2 Test configuration

The test configuration for DCU EM functional tests will be as follows:



DCU EM functional tests configuration

We shall command the DCU by sending commands to DCU DAQ interface (FPGA). Simultaneously, we generate a modulated signal at LIA input using a phase locked GPIG generator. The signal at LIA input is then synchronized with the BIAS output signal.

2.3 LIA Input signal (all channels)

The signal that will be generated for tests purpose as LIA inputs will be sinus signals over [50 Hz – 300 Hz] modulated by a signal over [0,03 Hz – 5 Hz] for photometer and [0,03 Hz – 25 Hz] for the spectrometer (The spectrum analysis at DAQ-IF output will be performed over [0,03 – 5 Hz] for photometer and [0,03 – 25 Hz] for spectrometer).

The generated signal have the following characteristics :

Modulated differential voltage :

$\mathbf{V_D} = \mathbf{m_{BIAS}} \sin(2.\pi.f_{BIAS} . t) . (1\text{-}n/\mathbf{m_{BIAS}}) . \sin(2.\pi.f_{SOURCE\ low\ frequency} . t) + \mathbf{U_{DV}}$

$\mathbf{U_{DV}}$ = 5 mV maxi : continuous differential voltage,

$\mathbf{m_{BIAS}}$: magnitude of the sinus BIAS = 10 mV rms.

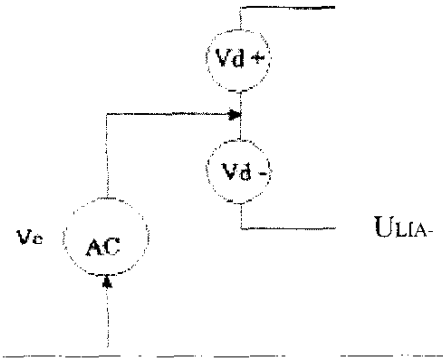
$\mathbf{V_{d+}} = V_D/2$

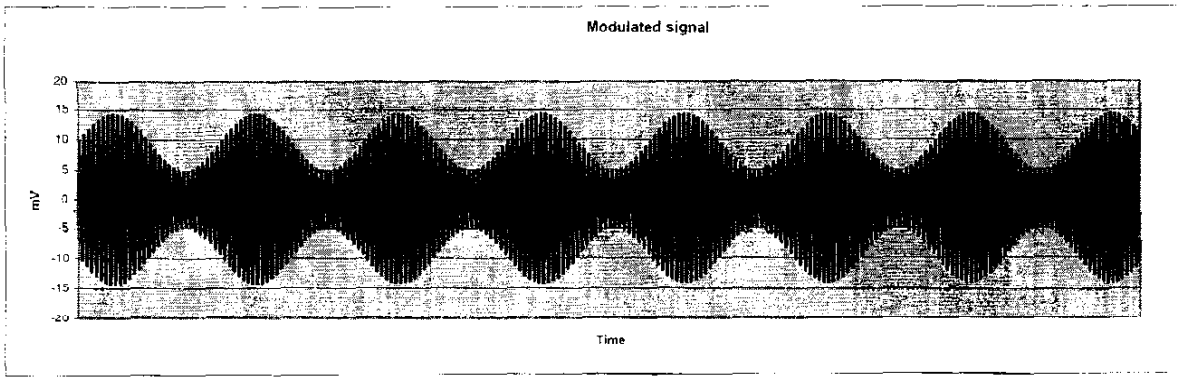
$\mathbf{V_{d}} = -V_D/2$

$\mathbf{U_{LIA+}} = \mathbf{V_{d+}} + \mathbf{Vc}$

$\mathbf{U_{LIA-}} = \mathbf{V_{d-}} + \mathbf{Vc}$

Vc = 1 V DC maxi : common mode





Representation of the modulated signal

Note . with reference to BDA-DRCU-22 , the maximum level at LIA input is

- *11 mV (photo)*
- *17 mV(spectro)*

We shall test the characteristics considering a modulation level belonging to [0, max level].

The test conditions will be as described above :

- Common mode : 1 V DC maxi,
- Continuous differential voltage : 5 mV DC (TBC),
- Magnitude of sinus BIAS : 10 mV rms.

3 Functional tests on DCU EM

3.1 Test of transfer function

For the test to be performed, we shall :

⇨ **Define the sinus BIAS frequencies tested**, for example 50, 100, 150, 200, 250 and 300 Hz.

⇨ **Define the sinus BIAS magnitude for the test** (for simulation of the bolos bias signals):

- o Is it necessary to test with different levels ? => define these levels
- o Is there a minimum level for the test ?

⇨ **Define the common mode levels** : set at 1 V DC maxi

⇨ **Define the continuous differential voltage** : set at 5 mV maxi

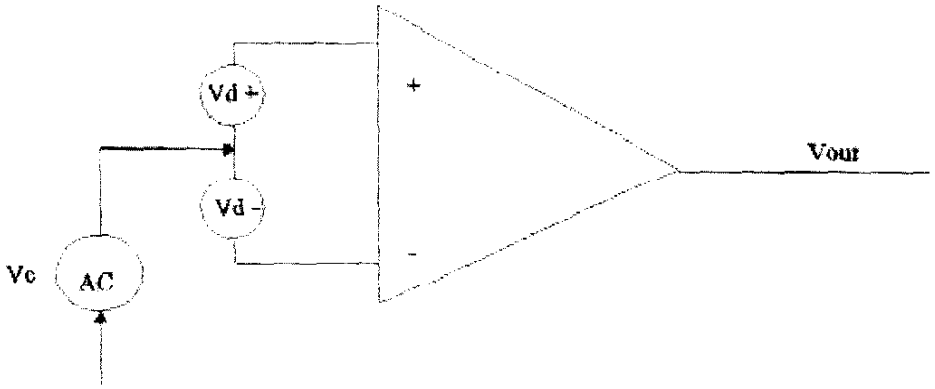
Note : all measurements will be performed with the signal al DAQ output analyzed by the PC.

- We test the cut off frequency over the specified frequency range. We check ***BDA-DRCU 13*** and ***BDA-DRCU 14***.
- We will check that the gain specification is fulfilled for spectrometer and photometer channels:
  - o output signal / input signal, see ***DRCU REQ-32 : AC gain = 375 +/- 0.5 % (photo) and 265 +/- 0.5 % (spectro)***.
  - o Measurements will be made on all channels with reference to the input modulation signal.

- We will also test the « offset » function (the offset being the same on all channels) to check the capacity of decoding increased output signals levels.
  - o How to set the offset depending on the bias magnitude ?

3.2 Common mode rejection measurement

With reference to ***BDA-DRCU-11 (resp. DRCU REQ-32)***, we shall check that the less performing channel with respect to common mode rejection (as identified during boards tests) is compliant with the specification of – 60 dB over [50 – 300 Hz].



The test configuration is as follows : we choose Vd = 0 and we test the common mode filtering (Vout measurement) at numeric DAQ IF output.

We measure Vout/Vc and we divide by the gain to refer it to the input.

The test configuration is the one described above, with input signal being the common mode applied on both +/- inputs.

We shall define further the common mode level and frequencies applicable for the tests.

3.3 Cross Talk measurement

Global cross talk tests will be performed for DCU QM1 complete tests, however, for DCU EM tests, we may (**TBC**) perform some of these tests on the DCU signal processing chain (TBC). We may then test whether cross talk effects appear by checking the DAQ-IF output levels (pixel by pixel) when only some LIA channels have signal applied to their input.

The cross talk requirements are given in ***BDA-DRCU-25***.

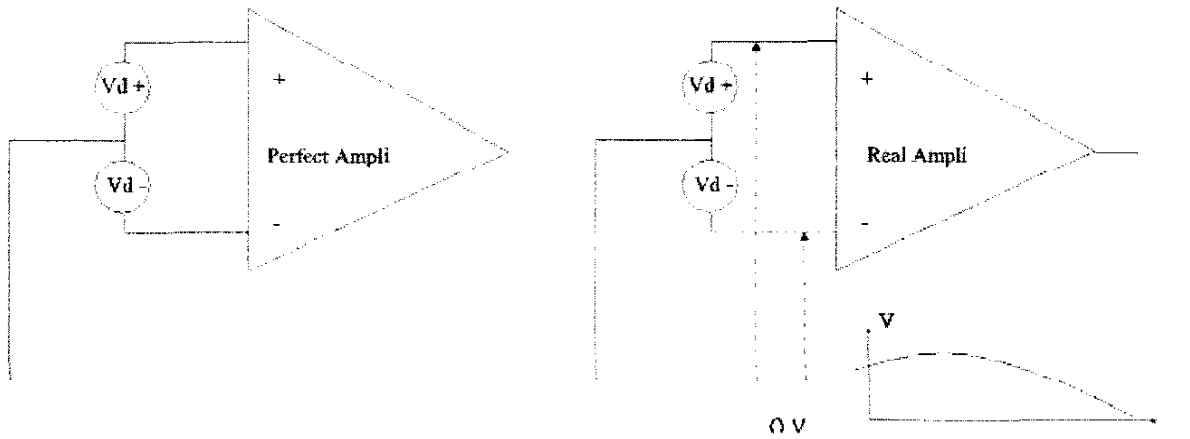
To be more representative of the real effects, the cross talks tests shall be performed on the full DCU QM1 (TBC).

3.4 Noise measurements

We shall check the specification of 7nV/sqrt (Hz) expressed in ***BDA-DRCU-01***.

For this, we can either create a short circuit at LIA input or send a non modulated sinus BIAS signal (with appropriate magnitude) at LIA input :

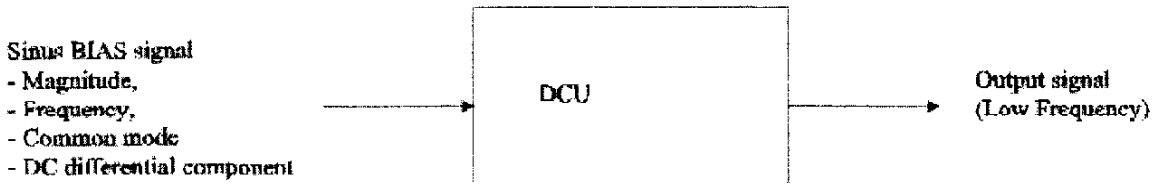
- Short circuit :



Equivalent Input : 7 nV rms / sqrt (Hz) : value for equivalent mpax output signal

Output signal PSD

- Sinus BIAS signal applied to LIA input (with appropriate magnitude level)



The output noise level divided by the gain gives us the equivalent input noise that has to be compared to the specification.

- The measurement shall be made over [0,03 – 5 Hz] for photometer and [0,03 – 25 Hz] for spectrometer considering sinus BIAS frequency range of [50 – 300 Hz]
- We shall define these frequencies
- Noise measurements shall be performed on all LIA channels.

The test configuration is the one described in § 2.2 with the PC commanding the appropriate signal to the GPIB generator.

Note : in both cases, it is possible that the signal level at DAQ-IF output be less than the first level (16 bits ADC converter).

3.5 DCU input impedance / capacitance

Checked by design and analysis.

3.6 Tests of saturation

With reference to ***BDA-DRCU-22***, we shall test the saturations on LIA-P ou LIA-S channels according to the maximum specified levels of 11 mV rms et 17 mV rms respectively (we increase the magnitude beyond the maximum level and we check saturation level at digital output). For this, we will modify in an appropriate way the magnitude of the modulation signal. It is also interesting to perform these tests with maximum DC and common mode levels according to ***BDA-DRCU-01***.

Applying directly Vbias at LIA input (0,5 V magnitude sinus), we shall check that the nearby amplification channel remain functional.

3.7 Tests of linearity

Test of the linearity can be performed by changing the following values (TBC):

- Sinus BIAS magnitude (maximum 100 mV rms),
- Magnitude of the modulation signal (maxi 10 mV rms).

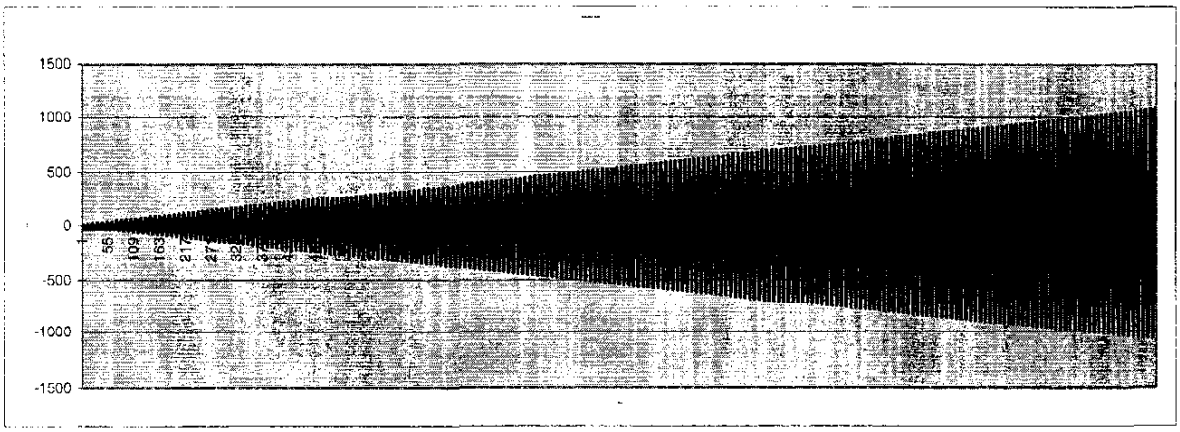
Two test configurations are proposed :

- In the first configuration, we will modify in an appropriate way the magnitude of the sinus BIAS signal and check that the 16 bits ADC converter generates signals in accordance with these variations.

In such a configuration, no modulation is applied to the sinus BIAS.

The following second tests configurations with modulated signals can be selected to test the linearity :

- to modulate the sinus BIAS with triangular signal and check that the output signal corresponds statistically to the modulation signal (in that case, we can choose the frequency of the modulation),



modulated signal

- to modulate the sinus BIAS with white noise and check (statistically) the white noise at DAQ-IF output (L. Vigroux proposal).

These tests shall be performed over the sinus BIAS frequency range.

We here notice that this allow to test the way the encoder works.

The test configuration is the one described in § 2.2 with the PC commanding the appropriate signal to the GPIB generator.

3.8 Tests of the sinus bias signals for bolos and temp (BIAS output)

There exists three kind of BIAS outputs (photometer, spectrometer and temperature). The test principle is identical for all channels. We shall check the output signal (frequency, magnitude, noise) :

⇨ The noise specification of 20 nV / sqrt (Hz) (ref. ***BDA-DRCU-05***). Under nominal load conditions, we shall analyse the spectrum of the output signal and check that the specification is fulfilled,

⇨ These tests shall be performed over the sinus BIAS frequency range **TBD**,

⇨ This test has to be performed over a temperature range **TBD**.

We shall precise the montage for these tests.

3.9 Tests on JFETS commands (BIAS output)

Requirements on JFETS are listed in ***DRCU REQ-35, 36 and 37.***

DRCU REQ-35

For DCU EM tests we will check the noise allocation on both Vdd and Vss :
- ⇨ Over the allocated frequency range,
- ⇨ Over a temperature range to be defined,
- ⇨ The tests shall be performed in a sizing configuration, id est Vss = - 5 V.

DRCU REQ-36

We shall test the overshoot with an oscilloscope : the results must appear in the test report (action F. Pinsard).

DRCU REQ-37

With reference to ***BDA-DRCU-10***, we shall test that the listed parameters can be commanded as specified.

More generally, we shall check all JFETS commands (and all output levels over 8 bits) using the dedicated command interface.

We shall also test the noise on JFETs.

3.10DAQ-IF tests

The measurements (reference ***DRCU REQ-38***) will be performed at variable sampling frequencies to check the susceptibility of the acquisition over the frequency (nominal frequencies are 16 Hz for photometer and 80 Hz for bolometer).

Note : DAQ-IF tests have up to now been performed at 100 Hz.

3.11 Alimentation tests

We will test the susceptibility of the DCU performances with respect to the alimentation (+/- 9 V analogic and 5 V numeric). We consider that the 5V alimentation stability will be sizing with respect to the performances. Therefore, we will only test the susceptibility to the 5V alimentation.

We here recall that post regulators on back planes make the DCU not sensible to the +/- 9 V analogic supply variations.

We shall only test relevant characteristics under non nominal alimentation conditions so as to evaluate the susceptibility :

- LIA :
  - Transfer Function,
  - Noise
- BIAS
  - Signal magnitude

To set the downgraded alimentation (5 V) values, we can refer to the specifications concerning the end of life alimentation performances (2,5 % max level).

As an example, we could perform the tests with 4,8 V, 5V and 5,2 V.

Problem : up to now, the voltage is generated by fixed regulators and therefore is not adjustable.

⇨ To provide an adjustable alimentation
⇨ To gather information concerning regulators (noise spectrum)

3.12Miscalineous Tests on DCU :

Consumption

With reference to the preliminary test plan, we need to add consumption tests, which induces :

i. To test the DCU consumption (at different temperature levels),
ii. To get an ammeter connected in line to check consumption.

A Precise criterion for the DCU consumption does not exist (DRCU consumption only).

Generators :

We need two generators with triple outputs (+5 V, +9 V, -9 V) with adjustable values on all outputs (following end of life specification of 2,5 %).

We shall precise the alimentation specification.

Temperature tests

We need a device to simulate temperature variations (it needs to dispose of a sufficient volume to get the DCU with its connected inserted inside).

We will test the noise performances Tests with reference to BDA-DRCU 19.

⇨ ***We shall precise the montage***

⇨ ***We shall precise the temperature range***

In addition we may test gain performances depending on temperature variations.

4 DCU EM with JPL bolometers performance tests

Before the DCU EM performance tests to be performed with JPL bolometers, it is necessary that:

⇨ The bolometers be tested with JPL dedicated electronic devices. This means that the noise level at bolometers/JFETS output be compliant with the requirements.

⇨ The assembled DCU has undergone successfully the tests listed in chapter 3.

⇨ Before to go further, we shall,

- get informed about the availability of the tested JPL FPU (cryostat + bolometers).
- get informed about the number of available (tested) bolometers.

In case such a DCU and FPU tested configuration is available, the DCU can be connected to it so as to perform the performance tests listed below.

We note that the FPU configuration will allow limited performance tests : the bolometers with not be irradiated and no chopper device will be available.

As a consequence, we will simulate the variation of the resistance by generating a Sinus BIAS signal with a step in amplitude : this will induce a variation of the bolometer's resistances correlated with the power dissipated inside.

This kind of measurement will be performed :

- At different BIAS frequencies [50, 300 Hz],
- With different amplitude step values.

The other kind of test will consist in checking, for each pixel available, the sync optimal phase value. This optimal phase should be the same for each bolometer. To check this, we will identify the optimal phase for each tested pixel.

5 TRACEABILITY MATRIX

The hereafter matrix identifies, for each requirement, the test that allows to verify it :

Requirement ID	Description	Element	test
BDA-DRCU-01	The DRCU signal processing electronics shall have less than 7 nV/rtHz as seen post demodulation, after digitzation. Noise is referred to the input over the frequency range 0.05 to 25 Hz. This performance must be accomplished with a bias input signal to the DRCU of 10 mVrms AC, 5 mV DC, 1 V DC common-mode offset, with an input load of 7 kOhms.	LIA	Noise measurements
BDA-DRCU-03	Input capacitance to be less than 100 pF, measured from the DRCU DxMA connector pins without the harness.	DCU	DESIGN
BDA-DRCU-04	Input impedance to be larger than 1 M□ from 50 – 300 Hz.	DCU	DESIGN
BDA-DRCU-05	The DRCU shall provide 5 BDA bias signals, adjustable from 0 to 200 mV rms, and 1 bias signal for temperature readout adjustable from 0 to 500 mV rms. - The temperature readout biases are to be divided from a common oscillator, - Each bias shall be adjustable with 8 bit precision - The frequency of each bias shall be adjustable between 50 and 300 Hz, with a precision of 5 Hz Voltage noise on the bias lines, within the modulated band (50 – 300 Hz), measured at the DRCU DxMA connector, shall be < 20 nV/rt Hz	BIAS	Tests sinus bias for commands for bolos and temp (BIAS output)
BDA-DRCU-06	The DRCU shall provide 15 commandable JFET source voltages with 256 levels. The range of Vss is from 0 V to – 5 V.	BIAS / JFET	
BDA-DRCU-07	Vdd shall be adjustable from 1.5 to 4 V	BIAS / JFET	
BDA-DRCU-08	Vdd and Vss lines individually must source 1 mA to 5mA. Noise on Vss < 1 □V/rt Hz, and noise on Vdd < 0.3 □V/rt Hz within modulated band (50,	BIAS / JFET	

	300 Hz) measured at the DRCU DxMA connector.		
BDA-DRCU-09	Each Vdd and Vss supplies must be commandable ON/OFF for spectrometer and photometer independently without overshoot. Each Vdd and Vss are turned on and off together..	BIAS / JFET	
BDA-DRCU-10	The DRCU shall provide 2 double wired JFET heater lines with adjustable amplitude and duration. The supplies must be able to provide 5 V and 25 mA (photometer), 3 V and 10 mA (spectrometer). Each heater line is commandable ON / OFF, with a minimum duration of 10 s.	BIAS / JFET	
BDA-DRCU-11	The common-mode rejection is –60 dB (50 – 300 Hz).	LIA	Common mode rejection measurement
BDA-DRCU-12	The DRCU shall provide a dynamic range at the ADC sufficient to maintain the noise performance of the detectors under maximal signal conditions. This is estimated to be 16 ADC telemetry bits.	LIA	
BDA-DRCU-13	The signal bandwidth of the photometer channels shall be 0.03 Hz to 5 Hz. The 5 Hz cutoff should have a precision of 1 %.	LIA	Test of transfer function
BDA-DRCU-14	The signal bandwidth of the spectrometer channels shall be 0.03 Hz to 25 Hz. The 25 Hz cutoff should have a precision of 1 %.	LIA	Test of transfer function
BDA-DRCU-15	The sampling of the photometer channels shall be synchronized with the bias, at a rate selectable between □bias/2 to □bias/256.	DCU	
BDA-DRCU-16	The sampling of the spectrometer channels shall be synchronized with the bias, at a rate selectable between □bias/2 to □bias/256.	DCU	
BDA-DRCU-17	The DRCU shall provide two adjustable power supplies for temperature control using a heater located at the 300 mK stage. This supply must provide at least 300 mV and 50 □A.	DCU	

BDA-DRCU-18	Noise performance BDA-DRCU-01 shall be maintained under bias range 50 – 300 Hz.	DCU	
BDA-DRCU-19	DRCU noise performance (BDA-DRCU-01) to be maintained under a warm electronics thermal drift of 1 K / hour (TBC).	LIA	Temperature tests
BDA-DRCU-21	Thermal requirement on JFET power is dV/V < 500 ppm / K for Vdd and Vss		
BDA-DRCU-22	The DRCU shall not saturate at an input voltage as large as 11 (TBC) mV_{rms} at input (photometer), 17 (TBC) mV_{rms} at input (spectrometer). DRCU channels shall remain functional if one input signal goes to Vbias.	LIA	Tests of saturation Tests of linearity
BDA-DRCU-23	The conducted RF on all lines connecting to the bolometers or JFETS, originating in th DRCU, shall be less than 0.1 nA ms as measured over a frequency range of 0 –10 GHz. (This assumes an attenuation of 40 dB by the RF filters).		
BDA-DRCU-23	BIAS, JFET power, and readout electronics for the spectrometer arrays are to run from separate dedicated power supplies, with independent, isolated grounds.		
BDA-DRCU-25	The electrical cross-talk between channels in the DRCU shall be less than 0.05 % (TBC). The electrical cross-talk shall be verified by varying the input signal on one channel and measuring the response in other channels. The input signal level to each channel must be representative.	LIA	Cross Talk measurement
BDA-DRCU-26	Each signal input to the LIA module must be connected to ground by a diode. This provides both protection and allows the JFETs to turn on without the JFET heater.	LIA	