Minutes of SPIRE Grounding Review
RAL, 23, 24 Sept. 2002
SPIRE-UCF-MOM-001405

Matt Griffin, Oct. 10 2002

Present	
SPIRE Project Team	John Delderfield Doug Griffin Matt Griffin Eric Sawyer Bruce Swinyard
CEA	Jean-Louis Augueres Christophe Cara Dominique Schmitt Laurent Vigroux
JPL/Caltech	Jamie Bock Viktor Hristov Gary Parks
Advisers	Astrid Heske (ESA) Bernard Jackson (ESA) Filippo Marliani (ESA) Laurent Trougnou (Alcatel) Ray Carvell (PPARC; Day 1 only) Colin Cunningham (SPIRE)

Day 1 (Sept. 23rd)

1. Introduction Matt

- See presentation
- Key points:
- Need keep to the schedule but avoid excessive risk.
- Need to adopt a disciplined and focussed approach to the review.
- Choice of optimum grounding scheme must take schedule into consideration, not just technical aspects
- Jamie, Matt and Laurent have to arrive at a consensus
- Late decision on finalising the grounding scheme can be traced to and understood in the context of lack of effort at JPL, CEA and Project Team. The challenge is to devise a workable solution and implement it while still living with such constraints
- Proposed agenda were agreed with possible need to revise Day-2 agenda depending on Day-1 outcome.

2. Summary of Documents (John)

- See presentation

3. SPIRE System Grounding Philosophy (John)

- See presentation
- Important considerations to be kept in mind during the review would be
    - Requirements on noise levels
    - Noise sources
    - How grounds are configured
    - Screening of noisy from quiet sections
    - PSU filtering configuration details

- Distinguish between keeping lines quiet wrt local grounds and keeping the local grounds themselves quiet.

4. AIV Schedule Overview (Eric)

- See presentation
- Key points
  - SAp deliveries are currently consistent with the master schedule
  - QM1 and QM2 will not have representative power supply
  - PFM electronics arrive only just before calibration
- Discussion
  - Laurent: Need to issue PSU call for tender. Still lacking final specification - this is most urgent thing to define.
    - Jamie: Could we get a more representative PSU for the CQM?
    - Laurent:
      - CEA will try to make the power supply bench as representative as possible.
      - CEA will have to decouple as much as possible the schedule of the PSU from everything else.

5. JPL View in Grounding Scheme (Jamie and Viktor)

- See presentation
- Discussion
  - Difficulty of translating system level requirements as in the BDA SSSD into specific requirements on the warm electronics - detailed specifications have been left up to the Project Team
  - Colin: The key point is "Keep the electrical potential of the cavity as close as possible to the ground level of the bolometer bias generator" - this should be the main design principle for the grounding scheme.
  - Jamie: It's the power from the SMPS that's critical, not just the noise, because the bolometer will respond to the power.
  - Viktor: Cold end grounding means "the Faraday cage is at the at the same potential as the detectors".

6. CEA View on Grounding (Christophe and Dominique)

- See presentation
- Key points
  - Christophe's part:
    - Outline of DRCU architecture.
  - Dominique's part:
    - 0.1 nA over 0.1 - 10 GHz (now 0 - 10 GHz) is the only quantitative specification in the BDA SSSD (7 Nov. 2001 version - this is the version that was reviewed at RAL in November - the latest signed version has been updated but not in relevant areas)
    - CEA have chosen to try and meet this requirement by implementing a direct metallic connection at the DCU end - conductive filler contacting ground plane to chassis - to be as passive as possible for the bolometers. The reference ground is then at DRCU level.
- Discussion:
  - Inconclusive discussion on how to arrive at specifications for the DRCU - issue deferred until tomorrow.

Day 2 (Sept. 24th)

7. Introduction and revise agenda (Matt)

- Revised agenda agreed with two technical meetings to define scheme and DRCU specifications
- Main objectives:
- Meeting 1:
    - Clarify what's proposed
    - Assess technical feasibility, pros and cons
    - Decide whether it can be the basis of an agreed implementation
    - Draw up a sufficiently detailed grounding diagram to define unambiguously the chosen option
- Meeting 2:
    - Define the list of requirements needed to implement the scheme at the warm end (CEA) and the cold end (MSSL/Cardiff)
    - Fill out this list as much as possible
    - Identify and plan additional work needed to complete the requirements list
    - Time permitting:
    - Consider verification and integration plan
    - Consider future EMC modelling

8. Summary of proposed options (John)

- See viewgraphs
- Discussion:
    - Note that all the harness between SVM and CVV is optimised for thermal performance, not to provide low-impedance connection between them to keep the voltages down
    - Overall shields inside the CVV. SPIRE has not accepted removal of these (ECR still under consideration).
    - Internal design of the DRCU to reduce noise needs to be considered (outside the scope of this review)

9. Technical Meeting 1: Identifying an Agreed Grounding Scheme

- After lengthy discussion, the following was unanimously agreed, and now defines the SPIRE system grounding scheme.

1. The 4-K box will be a Faraday shield closed by RF filters.
2. The 4-K box will be connected to the DCU chassis via the harness over-shield (inside the cryostat) as defined in the Harness Definition Document.
3. This overshield will have to go via multiple contacts, not backshell, at the CVV connectors (which is acceptable as the shileding does not have to be perfect)
4. The 2-K detector boxes shall be isolated from 4-K box
5. The 2-K boxes shall be connected to 0 V in the DCU via analogue connections in the bias line
6. The 300-mK stages shall be connected to the 2-K stages inside their BDAs
7. The 300-mK thermal straps shall have electrical breaks.
8. The spectrometer and photometer 2-K boxes shall be isolated from each other.
9. The inner shields around signal lines shall be connected to 0 V at the JFETs but not at the DCU side (TBC).
10. The inner shields (only on the bias lines) are connected to 0 V at the DCU and to 2-K box (TBC)

Notes: "0 V" refers to the bias board ground plane which is connected to the chassis.

- Some issues are TBC as indicated, but do not have an immediate bearing on the design of the DCU.
- Further discussion, conjecture or philosophising that may take place will have no relevance to the implementation.
- ESA/Industry state that overall shield inside the CVV (required in this scheme) is not agreed. The overall shield from 4-K box to JFETs is uncontentious as it is a SPIRE item.

10. Technical meeting 2: Drawing up DRCU Requirements

- CEA want requirements on the following for each interface category:
    - Conducted emission.
    - Extended noise allocation over wider bandwidth
    - Dynamic impedance for the LIAs

- Discussion:
    - Frequency range for requirements:
      Jamie: It's DC - daylight at the bolometer end . . . and what matters is the total integrated power.
      Matt: We need to define the range. - this will \need further discussion between CEA, JPL, and the Project Team
    - DCU internal design:
        - Viktor: Why not use an RF connectors?
          Dominique: Because we don't want to have capacitors at both ends of the line causing two-way reflections
        - Jamie: Why not specify a filter design and then put specifications on the power supply - this could be faster?
        - John: That would mix responsibilities.
        - Jamie: JPL wish to consult with CEA on the relevant aspects of the DCU design, and strongly believe that this is the best approach
        - Laurent V: CEA need these interface specifications in any case for verification. CEA will be happy to work with JPL in discussing and agreeing the internal DCU architecture and design - as already done in the case of the bias and LIAs.
    - EMC modelling
        - Dominique: For PACS, the requirements are defined by extensive EMC modelling
        - Filippo: A similar model of the SPIRE system would allow to provide CEA with requirements
        - Matt: EMC modelling at that level has not been carried out due to lack of effort within the Project Team and lack of support from JPL and CEA. Lack of effort and lack of time will preclude doing this on the necessary timescale - we have to find a workable solution that does not rely on this. But the model would need to be built up - based.
        - Laurent V: It's clear that there's no time to do a detailed modelling. So we need to make the best guess that we can based on existing knowledge and use this as a starting point for DCU design.

- **DRCU schedule and programmatics**
- The grounding scheme as agreed at this meeting is largely compatible with the existing DRCU design - no major changes will be needed
- CEA now have enough information to go ahead with the PSU procurement: it is agreed that this should now proceed.
- It is important now to define the DCU design to allow that procurement to start.

- CEA need a first rough estimation of the interface specifications within 1 month to allow them to fix the overall DCU architecture

How to define the interface specifications

- Matt: A pessimistic approach should be to assume that the harness does not attenuate the injected noise, so that whatever the requirements are at the detector end, the same requirements could be applied at the warm end
- Jamie: The RF impedance of the JFET/bolometer looking from the cryoharness side is very difficult if not impossible to know, making it difficult to define specs on the interface in any reliable way

- 6 or 7 November for next get-together . . . . .

11. Advisers' comments

Colin Cunningham:

1. Significant progress has been made and communication and understanding greatly improved.
2. The agreed grounding scheme needs to be converted to a drawing.
3. Now it is time to regard that as fixed and move on.

Laurent Trougnou (by e-mail after the review) :

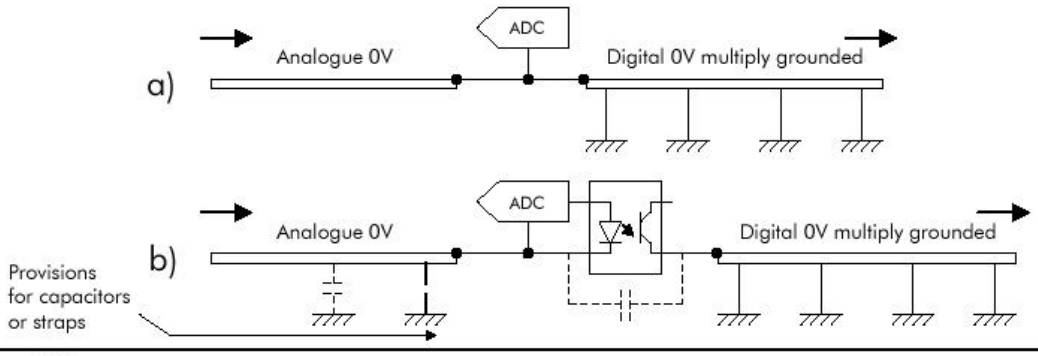
1. Comments include those as an independent EMC expert or "adviser", and comments as ASPI representative for what concerns the interfaces with the spacecraft and the Instrument EMC qualification before delivery
2. It is very positive that RAL, JPL and CEA have come to an agreement concerning the basic grounding concept.
3. Consider each detection chain as a whole, the susceptibility/immunity of which can involve multiple criteria, i.e. not only the spurious power likely to be transmitted to the bolometers (JPL criterion), but also the analogue signal integrity in general, such phenomena as RF detection and ground loop coupling to be taken into account. The grounding of the mixed analogue/digital circuits (internal to the DRCU) is also to be considered as critical, and is likely to drive to some extent the Instrument grounding. Please find enclosed the advice given in the frame of the EMC WG meeting #14 (see diagram below from H-P-ASPI-MN-1360_AD_grounding.pdf).
4. In your detail grounding design, avoid mixing techniques used to ensure the detection chains immunity to (very) low frequency interference with techniques used to avoid HF interference.
5. SPIRE's cryoharness overshielding strategy is still controversial, ESA and ASPI not being in favour of the use of overshields inside the cryostat. The overshield strategy that you wish to adopt is not yet defined in detail, even within the RAL team.
6. Note that, as a minimum, the spacecraft design is to have the external cryoharness overshielded from the CVV connector up to the SVM bracket connector. The overshield will be in continuity at both ends with the backshells over 360°.
7. I have noted that the CQM Instrument will not integrate the DC/DC converters that will be part of the flight design, but linear power supplies. Of course this is regrettable, but this being said it also means that the detection chains immunity to noise on the secondary power inputs to the DCU should be characterised as early as possible and in any case before delivery, so that you can anticipate with very good confidence the CS/CE margins at this interface (as soon as the converters CE on the secondaries is characterised).

ALCATEL SPACE

Herschel-Planck

EMC/Power WG meeting #14 : EMC

- Internal grounding of mixed analogue/digital units
  - Connection of analogue and digital 0V at the <ADC]
  - The rest of the unit digital electronics should be referenced to chassis
  - If insulation of analogue 0V from chassis absolutely necessary in the unit where A to D conversion is made, consider insulating the <ADC] 0V from the next digital stages by opto-couplers, while keeping provisions at PCB level for capacitors or straps to chassis



L. Trougnou, EMC
Alcatel Space Industries

EMC_meeting_230402.ppt - 29/04/2002 - 4
M054-1

Consolidated comments of the ESA representatives (by e-mail from Astrid)

1. CEA/JPL/RAL are to be congratulated that a significant outcome of the review was to agree a valid grounding concept.
2. Clearly, the wide geographical distribution of the SPIRE instrument contributors makes communication difficult and is an obstacle to progress. We encourage the SPIRE consortium to maintain close communication seen at the review within the instrument team

General:

3. The Grounding Scheme is now clear and should be transferred to a drawing and circulated to all the parties involved.

4. The SPIRE cryoharness overshielding protection is still an open issue. ESA and ASPI have not baselined the use of overall shields inside the cryostat, and SPIRE must bear in mind the possibility that internal cryostat overshielding cannot be included. With the actual design RF protection is not provided by inner shields which are used only as an extension of the 0 V bias board ground plane.

5. Since the CQM Instrument will be supplied with linear power supplies that do not reproduce the flight configuration, the test at CQM level for conducted noise will not demonstrate the detection chains immunity to noise on the secondary power from the DCU. SPIRE should find appropriate means to demonstrate the CS/CE margin at this interface. Characterisation of the CE on the secondary power lines is needed.

6. We agree with the points raised by Laurent Trougnou (ASPI), in particular his points 3 and 4.

Future work:

7. The very scrupulous approach followed during the review should be maintained in order to guarantee the best exploitation of the human resources available in the project.

8. The good level of communication at the review should be continued and proposal to hold weekly telecons will help with this in addition we would encourage CEA/JPL/RAL to hold face to face meetings/reviews whenever appropriate.

9. On-time CQM delivery is a firm requirement, hence meeting the schedule, and any kind of trade-offs that implies - are essential parts in arriving at an imp

12. Summary and conclusions

- This summary has been drawn up by Matt after the meeting

1. The SPIRE grounding scheme is now defined and is as described in Section 9 above. It will be drawn up and issued as a formal Project document.
2. The scheme is compatible with the current basic design of the DRCU, so a major re-design will not be needed.
3. CEA now have enough information to proceed with the PSU procurement, which should be done as a high priority.
4. JPL strongly favour an approach to the DCU design in which they collaborate with CEA on optimising the DCU design.
5. CEA are happy with that approach and welcome JPL's support, but also require explicit specifications on the interfaces.
6. JPL will look at whether such interface specifications can be derived from analysis and/or tests on existing systems (e.g., Bolocam or BOOMERanG).
7. It will be important to follow up this meeting by maintaining and monitoring a good level of activity across the project. It is proposed that this be coordinated through the weekly (normally Tuesday 16:00 UK time) telecons between the SPIRE Project Team and JPL, with CEA participating in future to cover this issue. The next telecon is scheduled for Tuesday Oct. 8 (TBC - Matt will be in touch about the arrangements and agenda).
8. Immediate priorities will be:
   (i) initial definition of interface specifications for the DRCU (without additional EMC modelling);
   (ii) issue of a grounding scheme drawing to reflect the review's conclusions; *
   (iii) refining DRCU interface specifications without additional circuit modelling;
   (iv) consultation between JPL and CEA on aspects of the DCU design relating to the bolometer and JFET lines;
   (v) completion of the DRCU DDR (currently in progress);
   (vi) reviving and extending EMC modelling of the whole system.

   * See *SPIRE Grounding and Screening Philosophy* (SPIRE-RAL-PRJ-00624, Issue 1.0, 1 Oct. 2002)

Annexes

1. **Presentation by John Delderfield**
2. **Presentation by Jamie Bock and Viktor Hristov**
3. **Presentation by Christophe Cara**

SPIRE-RAL-MHO-001367

GROUNDING REVIEW

Introduction

Dr. John **Delderfield**
SPIRE SYSTEMS ENGINEER

DOCUMENTS submitted for this REVIEW, all on LiveLink

Review Plan and Agenda SPIRE-UCF-NOT-001366(Upd. 16/9)

Presentations

GROUNDING SCHEME-JPL SPIRE-RAL-MHO-001375
GROUNDING OVERVIEW_JD SPIRE-RAL-MHO-001367

Background information

GROUNDING and SCREENING PHILOSOPHY
SPIRE-RAL-PRJ-00624 amended 13/8/2002
New Overall Spire Grounding SPIRE-RAL-MHO-001368

Background information (contd.)

Detector SubSystem Specification SPIRE-JPL-PRJ-000456v3

DETECTOR READOUT & CONTROL UNIT SUBSYSTEM SPECIFICATION SPIRE-SAP-PRJ-000461 26/06/02v 0.92

DETECTOR READOUT & CONTROL UNIT INTERFACE CONTROL DOCUMENT SPIRE-SAP-PRJ-000451 26/06/02v0.7

DETECTOR CONTROL UNIT DESIGN DOCUMENT SPIRE-SAP-PRJ-001243 05/07/02v0.2

Impact of the Grounding in the cold end for the DRCU design SPIRE-SBT-MHO-001383

Introduction to EMC TECHNICS for HERSCHEL INSTRUMENTATION SPIRE-SBT-NOT-001382

DCU Internal Grounding Scheme SPIRE-SBT-MHO-001378

DETECTOR READOUT & CONTROL UNIT GROUNDING SCHEME SPIRE-SBTL-NOT-001379

DRCU-PSU Implementation & Ground-PSU Policy SPIRE-SBT-MHO-001380 and 81

ERIC TO SET THE SCENE w.r.t. SCHEDULE

- Grounding and EMC have always been recognised as critical areas for the correct operation of SPIRE.
- A top level controlled instrument document, SPIRE Grounding Philosophy, **SPIRE-RAL-PRJ-00624** includes discussion and reasons, rather than just being a list of tabulated requirements.
- This document contains the SPIRE System grounding diagram, which is repeated in the IID-B.
- The process of optimising the grounding/screening has involved discussions between JPL, CEA & RAL, plus inputs from the Herschel Plank Working Group (linked by Doug Griffin).
- The requirements and to some extent the implementation have been confirmed, reviewed and agreed at SPIRE's major milestone ESA reviews.

- Overview of Project Progress
- Summary of SPIRE grounding

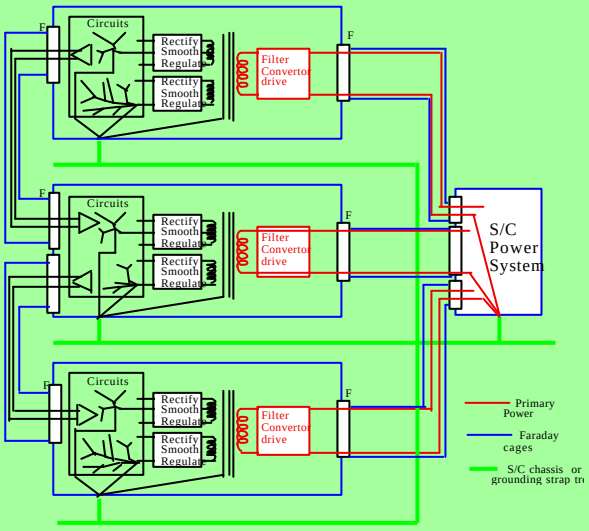
SPIRE Project Progress

Position at Instrument Intermediate Design Review, April 2001

Electrical Design and Grounding Scheme

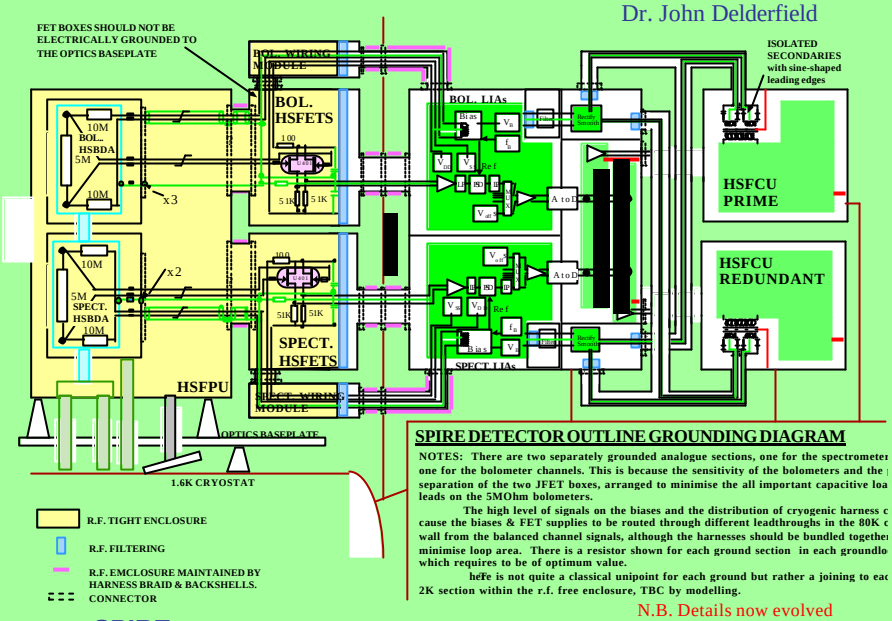
Dr. John Delderfield

SIMPLISTIC GROUNDING



Electrical Design and Grounding Scheme

Dr. John Delderfield



SPIRE DETECTOR OUTLINE GROUNDING DIAGRAM

NOTES: There are two separately grounded analogue sections, one for the spectrometer one for the bolometer channels. This is because the sensitivity of the bolometers and the separation of the two JFET boxes, arranged to minimise the all important capacitive loa leads on the 5MOhm bolometers.

The high level of signals on the biases and the distribution of cryogenic harness c cause the biases & FET supplies to be routed through different leadthroughs in the 80K c wall from the balanced channel signals, although the harnesses should be bundled together minimise loop area. There is a resistor shown for each ground section in each groundlo which requires to be of optimum value.

here is not quite a classical unipoint for each ground but rather a joining to eac 2K section within the r.f. free enclosure, TBC by modelling.

N.B. Details now evolved

Electrical Design and Grounding Scheme

Dr. John Delderfield

- **Grounding and EMC are design drivers for Spire.**
- **Bolometers must not receive wire or field-coupled stray energy**
- **FPU and JFETs form closed isolated Faraday cage**
- **DCU analogue sections very carefully coupled to this with attention to cryoharness detail: differential, screened, separate chassis and signal grounds, non-standard power-supply config., control of imbalances injected into signal ground/digital noise.**
- **Decided by discussion last November, but recently written up in SPIRE-RAL-PRJ-00624 to avoid ambiguities, etc.**
- **Details of system still to be tied down. DCU seals and screens,**

Assumed EMI and Spurious Signal Culprits

Radiated EM power reaching inside the CVV

- Radio frequency E-fields
- Low frequency B-fields
- Sub-mm photons (straylight)

Conducted spurious currents and voltages

- Direct signal corruption on to signal wires
- RF capacitive couplings, e.g. between inner and outer braids
- Indirect signal corruption via ohmic heating of the 5

Blue text added to slide for this grounding review, but not new info.

"Three Pronged" Analysis Approach

Modelling

– ***orcad*** model of the bolometer biasing and detection circuit

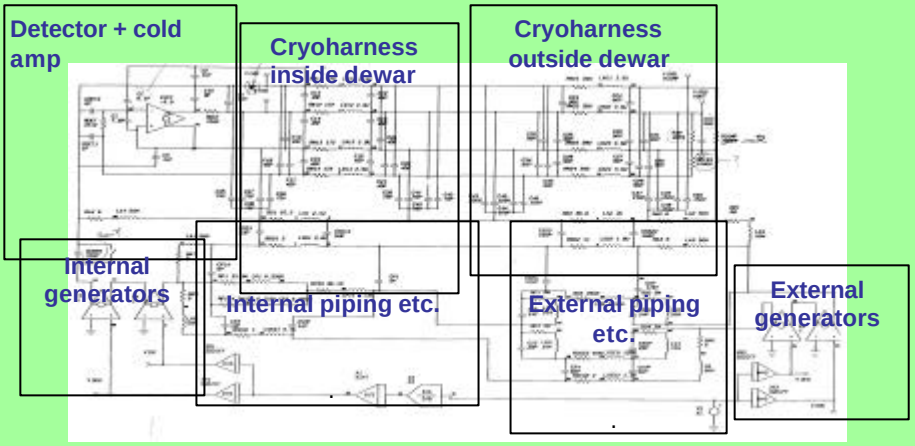
Testing within RAL EMC facility

– Detector harness shielding tightness

– Detector harness microphonic susceptibility

– Attenuation of FPU structure

orcad modelling (3)
CVV Modelling



Testing within RAL EMC facility

Facility

- Constructed to MIL STD 461/462
- 10 KHz to 1 GHz (10-30 V/m)
- E-Fields and B-Fields
- 1m x 1m x 1m space envelope

A simple mock-up of the SPIRE Optical Bench and Photometer cover to be fabricated

- Welded photometer cover
- Cover screwed to optical bench
- Internal light baffles to be included

Future of SPIRE EMC

Complete ***orcad*** simulations

Complete EMC testing at RAL

Complete ESTEC EMC

- To summarise, for SPIRE's IBDR in April 2001 there was a Baseline Grounding / EMC design in place, reviewed and agreed, together with a approach to verifying it.
- This was fed down into sub-system requirements, for instance putting into JPL's SubSystem Specification Document that the link between the chassis and the analogue grounds of the bolometer system would be at the cold end.

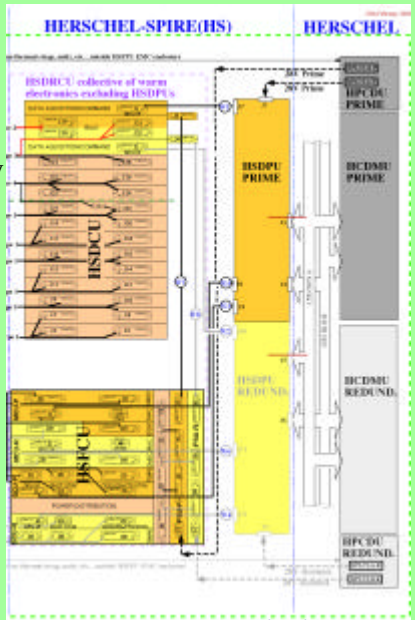
- What progress had been made at the Instrument Baseline Design Review, March 2002?
- The SPIRE Harness Definition document (which includes the Cryoharness) and Instrument Block Diagram had been detailed almost to the state that they are in today.
- The Spire Grounding Philosophy document was further evolved after meetings with CEA to work through how the DRCU was being implemented, and discussed with JPL. Its issues were dated 24th August, 10th September and 24th September, & the last issue expanded the Grounding Diagram to include the CVV system and the HSFCU.

Warm Electronics

HSDRCU=:

- HSFCU with power supply is Prime and Redundant, only to be powered by Herschel to match the active HSDPU.
- HSDCU has P/R bias generators and interfaces to HSDPU, but the remainder of the bolometer system is non-redundant.

Supplied [with "W" harnesses] by CEA Saclay; SVM routings needed.

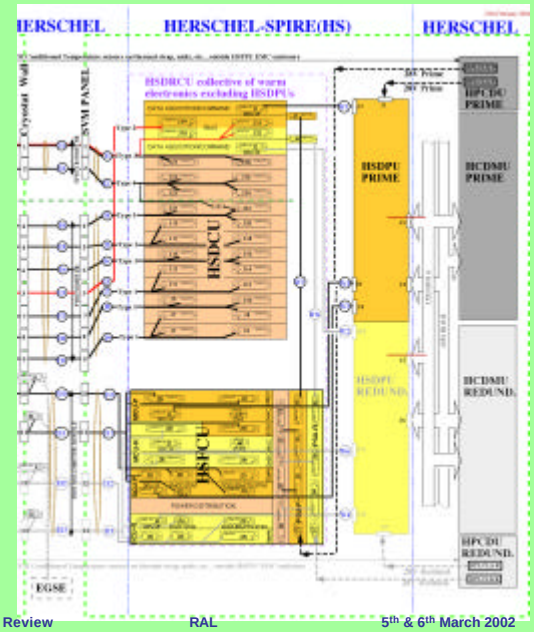


HSDCU =

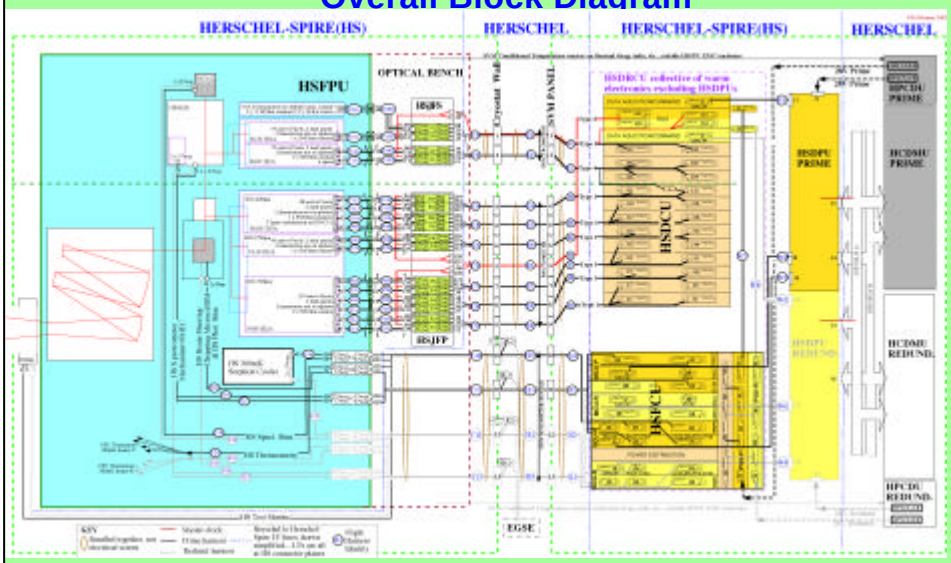
Harness Outside CVV

Warm electronics+ SPIRE Herschel instrument harness from HSDRCU to connectors on CVV.

- pin-out details now all sorted.
- “I” harness definition



Overall Block Diagram



Electrical I/F Comments

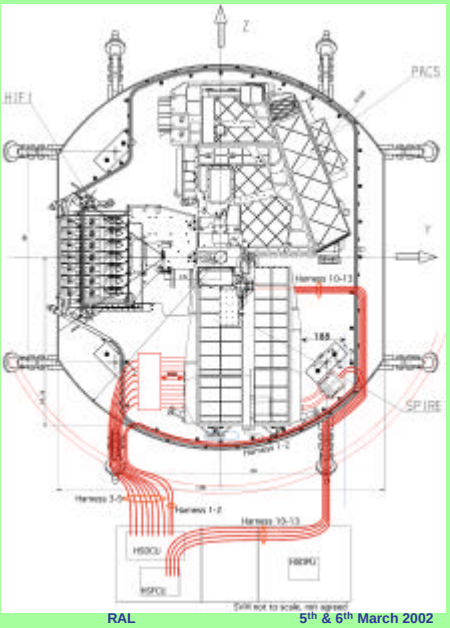
Herschel/Spire interfaces now simplified by removal of multiple sync. signals and RTU launch-lock readout.

HSFCU/HSFPU interfaces simple in that [excepting

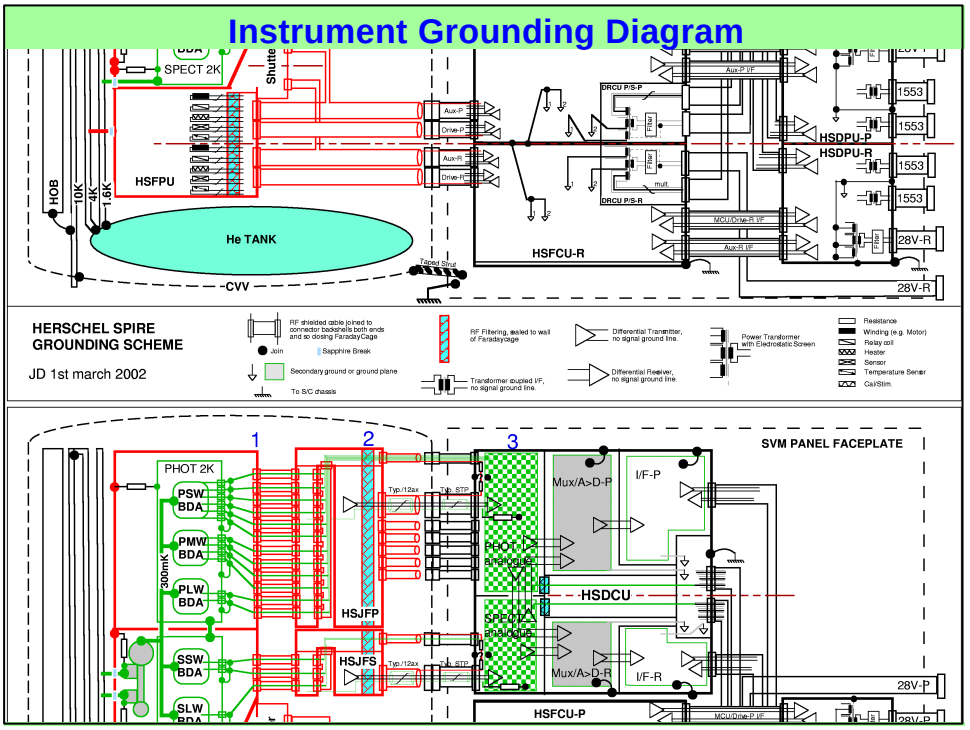
Harness Routings

The HSFPU J19=J30 now linearly disposed in a single filter unit some 75 mm above

RAL suggestion 25/10/01



Instrument Grounding Diagram



Grounding Comments

All HSFPU electrical items isolated from chassis.

Conventional grounding of HSFCU, HSDPU, and other than the analogue front-ends of HSDCU. All non-bolometer loads in HSFPU

Together with the IFETs, the HSFPU forms a Faraday cage aimed at preventing the bolometers receiving wire or

So at the Instrument Baseline Design review in March 2002, from which the consortium went forward to implement detailed designs, we had sorted a many things out, including the harness, but:

i. the link between bolometer bias ground and chassis was to be at a choice of 3 positions, but the hardware did not implement low temperature hardware ground breaks
ii. I had just removed question marks on the DRCU power supply grounds for the review!

Consider an overview of SPIRE grounding.

Let us extract some points from **SPIRE-RAL-PRJ-00624**:

• In general terms SPIRE shall conform to an ESA classical unit-by-unit secondary power configuration.
•It has a chassis/box that is closed to form a conductive Faraday cage, with all apertures including vents and joints having controlled geometry with adequately small maximum dimensions.
•Primary power is "isolated" from chassis
•Each unit is powered with secondary (or conditioned) power which is isolated from the primary power buses and unipoint grounded via a link to unit chassis.
•All signal inputs and outputs are differential and ideally pass through filter connectors. Signal ground lines do not pass between units. Inputs are normally high impedance and are required to maintain a defined high impedance w.r.t. chassis. Outputs are required to have controlled slew rates, with minimum skew to limit common mode spikes and little ringing.

•The secondary grounds within each unit are carefully configured in a documented way and if multiple supplies are used the grounds for each supply are separately controlled with a minimum of joins between the supplies, classically just one at the unit unipoint.
•Theoretically there should be no current flow in any ground wire, which should only be used for signal voltage reference. This is just one example of the general requirement that any device taking a.c. current shall have adequate local decoupling/filtering, obviously to ensure its own correct operation, but also adequately to inhibit noise propagation to other elements in the unit; logic or digital functions can be the most troublesome with their a.c. components taking the form of switching noise.
•Depending on the susceptibility of circuits, logic signals that travel a distance across a unit may need to be slowed down with series resistors and squared up again on receipt by Schottky buffers such that excessive dV/dT noise is not broadcast.

•The whole arrangement so far described is prefixed by "in general terms".
•The configuration is best suited to systems in which each unit operates over a restricted range of signal level. In Spire this would apply to the HSDPU.
•Otherwise isolation of noise from high level circuits such as power convertors to sensitive analogue elements get more and more impossible to achieve. Considering the front-end signal source in Spire, we have an noise spec. of 7nV/√Hz at about 2.5MΩ and 300mK.
•There comes a point when the need to control noise requires separate preamplifier unit(s), preferably with an electrostatic screen separating it (them) from any digital functions such as multiplexors or A-D convertors, with the signals then transferring to a conventional unit via balanced digital I/Fs.

•The power needs to be fed to this system's analogue sections extremely quietly, prefiltered and actively regulated with external sensing in an external unit. It must then be filtered in a separate compartment within the analogue unit that has bulkhead connectors feeding to the analogue system.
•Grounding has to be very carefully configured as secondary grounds are implicitly distributed outside of one unit. If one considers the whole volume of the various units in this supply system as if it were joined into one by the harness screens that join them, the grounding it should look like a unipoint tree as if it were still within one unit.
•Multichannel operation requires adequate interchannel screening and a configuration that keeps any designed-in signal cross-talk to below specified levels.

The essential features of SPIRE's implementation are:

•signal power gain from external JFET amplifiers

•separate analogue ground paths, without loops, between spectrometer and photometer systems

•maintenance of single point ground joins to S/C chassis

•analogue power, quiet and regulated, supplied from a unit external to the one that houses the sensitive analogue systems, without ground switching.

•ground-plane option invoked to keep a large area of analogue signal ground quiet in each of the spectrometer and photometer parts

•the detectors to be in a Faraday cage with full filtering on all wires entering it (non-bolometer ones not shown) extended with full shielding into the JFET boxes.

•a separate compartment division is introduced in the JFET boxes with ceramic feed-through filtering to close the Faraday cage..*now connectors are filtered.*

The essential specifications are (contd.):

•unipoint analogue ground for the 300mK BDA system with minimised voltages between the bolometers and their local chassis.

•information transfer out of the digital part of the HSDCU via normal balanced ESA-type digital interfaces, both fast and slow, to the HSDPU (not shown but having its own separate conventional grounding scheme).

•The need to bundle together groups of long harnesses between HSJFETs and HSDCU (not shown here but see instrument block diagram) to minimise loop area between bias routed analogue ground lines and differential signal lines.

•An optimised multiplexing/transfer of data from the analogue sections of the DCU to the back-end digital ones to minimise current injection back into the analogue ground and hence potentially back to the detectors.

There's a great deal more detailed discussion in SPIRE-RAL-PRJ-00624 with which anyone critiquing the situation in detail should acquaint themselves.

The extracts I have just presented are all very long-standing, i.e pre-dating IBDR.

The document has recently been extended to include some coverage of the Tiger Team activities.

So why does SPIRE need a Grounding Review at all?

Comparing the IBDR grounding diagram with the earlier IIBR version shows evolution of the grounding. An option of joining the bolometer analogue ground to a chassis unipoint at the warm end is shown. This was included as a request from CEA as a link that could be tried/considered as SPIRE designed/tested out its system; we stated it would not be a design driver forcing changes on the cold SPIRE units.

CEA and JPL worked together to try out some QM HSDCU boards using the IBDR grounding approach.

But in moving towards a DRCU Power Supply specification, pressed by SPIRE System to complete a baseline design with power supply grounds, secondaries, filtering, prime/redundant drawn out as whole scheme, CEA observed that any warm-end sourced Common Mode noise (best thought of as charge or current injection) had to be returned via warm end loops and not loops that went to the cold-end and back.

Given that there are at least three factors in this budget {how much noise is generated, how it is filtered + the loops this uses, and the analogue circuits' susceptibility}, keeping any noise local to its source was an approach that could not be disagreed with and this was written up within an Addendum to SPIRE-RAL-PRJ-00624 issued 5th June 2002.

So, again, why are we needing a Grounding Review at all?

CEA further suggested that the warm-end grounding of the bolometer analogue grounds was mandatory, a position that I initially rebuffed by requesting we keep to the IBDR baseline. However it then became clear that the next generation of HSDCU PCBs had already been designed non-compliantly, i.e. without selectable chassis links.

A detector summit minuted that any analogue ground PCB links to chassis should be removable **not** solid groundplane. However there was some delay before I realised that this had not been actioned….possibly because CEA were not informed officially!

So the first way of sorting this out was to set up a directed activity specifically to work the grounding through, a decision minuted as forming a Tiger Team. We held numerous three party telephone conferences and exchanged notes/analyses etc..

It's worth just noting two topics that the Tiger Team explored to try and help the situation:

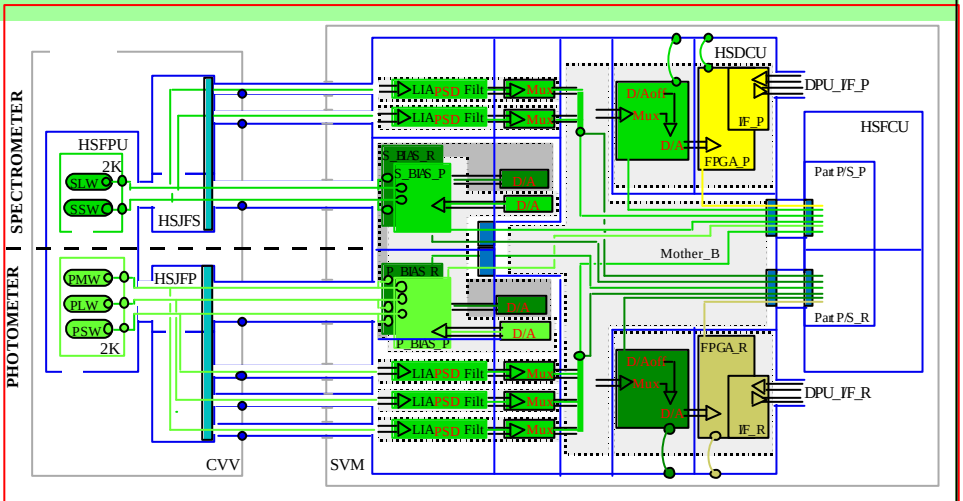
- The SPIRE DPU does not condition power for other units but PACS' does. To help keep the HSFCU power supply simpler, and to the more easily return DPU I/F common mode currents to the DPU, we suggested these sections of the HSDRCU be DCU powered. CEA decided it best not to proceed along this route.
- There is always advantage to defining a system's I/Fs, notwithstanding that some are more subtle than others and that the definitive requirement is that the final integrated system works well. The DRCU has straightforward I/Fs defined to the HSDPU and the HPCDUs (power). Working from JPL's SSSD with its classical columns of item definition and matching requirement, CEA were asked what extra item definitions they wanted to have requirements for at the DRCU bolometer harness connector I/Fs.

Recognising schedule urgency the Tiger Team concluded in my issuing a document called "SPIRE Grounding" on 16th July which proposed a way forward (now added into the top level document). It may still be the outcome of this review, but not all parties felt able to sign up to it with a good level of confidence, so this review was called on 19th July.

So here we are, after a delay to get our presentation material together.

Just a quick lead-in to the next presentations:

Consider detector grounding, built up from HSDCU DDR documents.



HSDCU NOTE: Omits heaters, temperature sensors and other non-signal items.
All the RED lettered items have to have digital links to BOTH prime and redundant FPGAs

As we listen to other presentations, pick up on :
•Requirements on noise levels
•Noise sources, internal to SPIRE and external
•How grounds are configured, and noise kept off them
•How noisy sections are “Faraday” screened away from quiet ones
•Power supply/filtering configuration details,

Take care to distinguish keeping power rails quiet w.r.t. local ground and keeping local ground itself quiet, i.e. NOT using it for supply current return path.

The agenda now calls for JPL, CEA and the Review Team each to present their perspectives on the situation.

What we have heard:

•Requirements on noise levels

-Detectors and leads to be in VERY quiet environment

•Noise sources, internal to SPIRE and external

-Switched mode power supply

-Digital switching

-Currents returned along grounds

-External fields CVV to SVM to DRCU

•How grounds are configured, and noise kept off them

-Separated into categories with special care for analogue

•How noisy sections are "Faraday" screened away from quiet ones…….

•Power supply/filtering configuration details…….

Suggested adaptation arising from Tiger Team.

•Removed all grounding option numbers as we are going a route at this stage of defining one baseline grounding configuration.

•No longer tie all relevant chassis and analogue grounds together tightly in the FPU.

•Put in cold-end ground breaks in 300mK straps, and around 2K boxes.

•Complete instrument Faraday cage by re-connecting shields at CVV wall.

•Inside the FPU join all sensitive parts together tightly with the existing multi-wire and braid harnesses that form the extended analogue ground wiring.

•Ensure this forms an internal Faraday shield around the detectors+ their bias and signal wiring back to the JFET modules.

•Carry both Spectrometer and Photometer analogue grounds back at low impedance to the separate analogue bias grounds in the HSDCU.

•Link these separate analogue bias grounds in the HSDCU to DCU chassis at their connectors, **the main grounding point.**

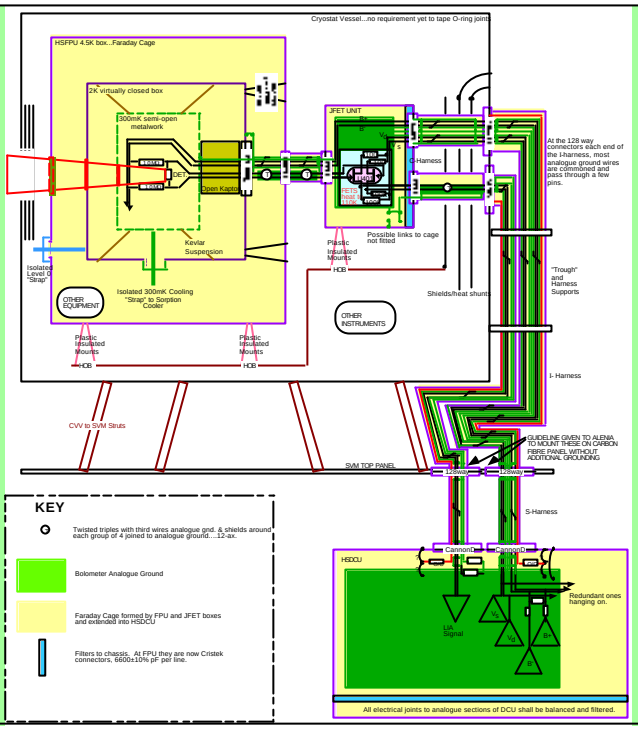
•Connect the inner screens around the bolometer signals between the JFETs and the HSDCU to this ground in the JFET modules, providing good signal screening, but leave them nominally open at the HSDCU LIA inputs…saves loops, more es pecially if keep BDA grounds separately routed.

•Take every precaution to stop power supply noise and any digital noise entering the shielded volumes in the analogue bias generators are housed, with absolutely no returning of IC power currents into analogue ground (except by capacitive strays).

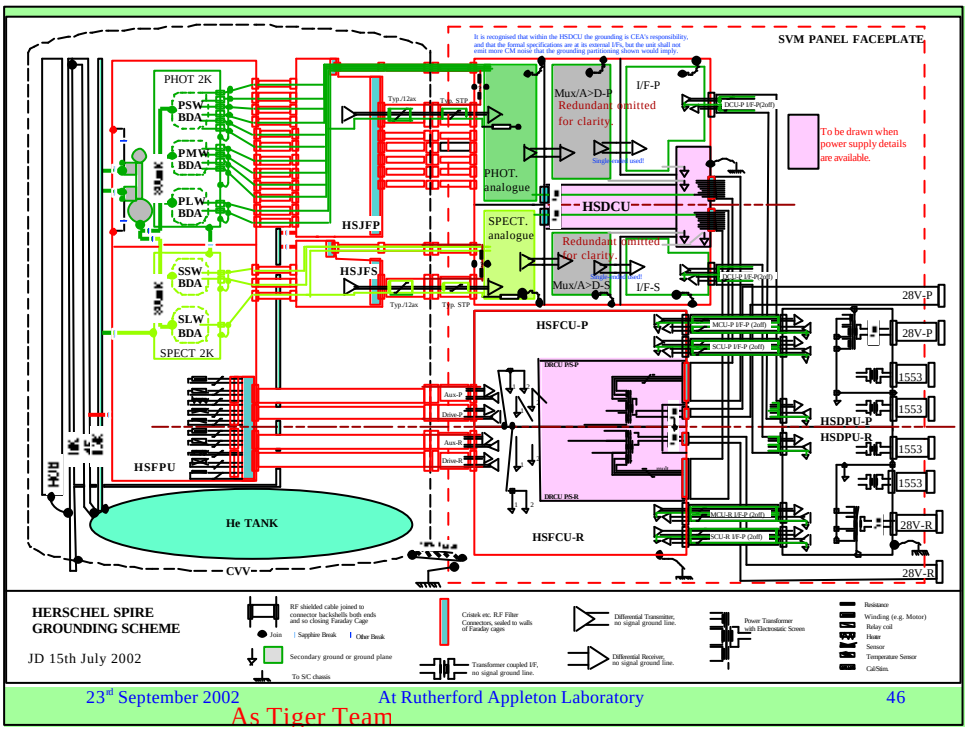
•Separately trade off the grounding of LIAs with similar detailed design to stop power supply noise and any digital noise entering their shielded volumes. I show them grounded via Motherboard link, but power levels may be high enough that each BDA's LIAs merit their own winding in which case they too can common at the DCU input I/F.

Configuration as described applied to one detector.

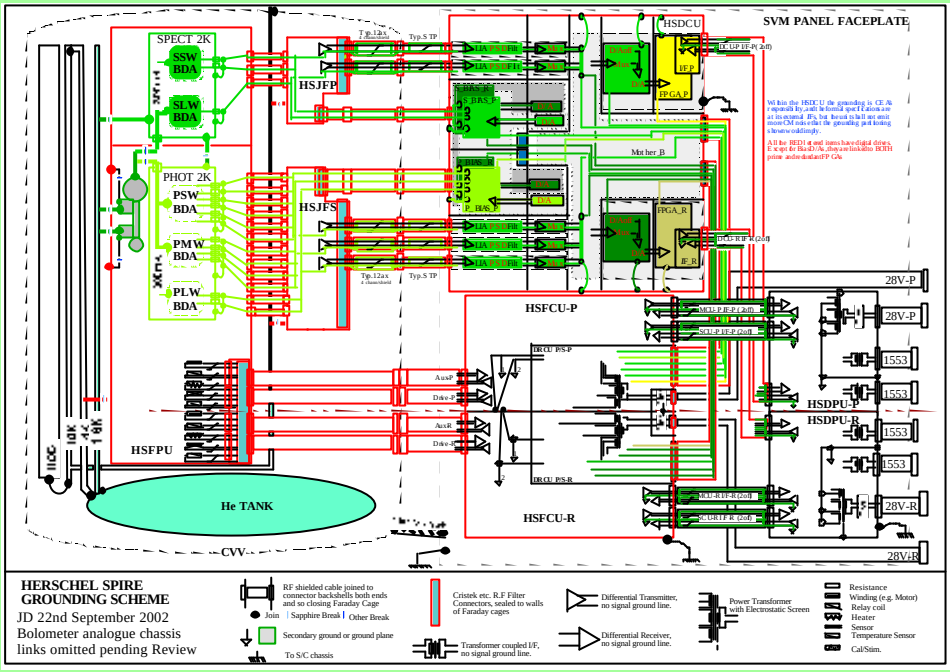
See version on wall



23rd September 2002



As Tiger Team



Better DRCU

TRADE_OFF TABLE

Route Forward	Tech	Herit	Progr	Isol.	Risk
Cold end only grounding	Poor PS CM	**JPL**	Delay	No	?
Warm end only grounding	Poor Bol.	CEA	OK	Yes	?
Warm end link and closed analogue shields	OK	?	OK	Yes	?

GROUNDING SCHEME-JPL

Jamie Bock - JPL
Viktor Hristov - CalTech

JPL's Role in Warm Electronics Development

- **Instrument gives performance requirements on detectors**
- **JPL gives performance requirements to the DRCU**
- **JPL gives environment requirements on the instrument**
  All these requirements are summarized in BDA-SSSD
- **Instrument imposes environmental requirements to sub-systems**
  e.g. Harness Definition Document, Grounding Network Document
- ~~***Some* sub-system requirements given in BDA-SSSD***~~

- **JPL and CEA share in EM design and development**
- **JPL and CEA coordinate in testing of all models of electronics**
- ~~**CEA responsible for fabrication and performance of flight electronics**~~

BDA-SSSD Performance Requirements (for reference)

3.3.2.6 DRCU Requirements

Requirement ID	Description	Reference	Compliant
BDA-DRCU-01	The DRCU signal processing electronics shall have less than 7 nV/√Hz as seen post demodulation, after digitization. Noise is referred to the input over the frequency range 0.05 to 25 Hz. This performance must be accomplished with a bias input signal to the DRCU of 10 mVrms AC, 5 mV DC, 1 V DC common-mode offset, with an input load of 7 kΩ. Thermal requirements on bias stability are implicit in this requirement.	JPL	Yes
BDA-DRCU-02	Requirement deleted	JPL	
BDA-DRCU-03	Input capacitance to be less than 100 pF, measured from the DRCU DsMA connector pins without the harness.	JPL	Yes (may be verified by design)
BDA-DRCU-04	Input impedance to be ≥ 1 MΩ from 50 – 300 Hz.	JPL	Yes (may be verified by design)
BDA-DRCU-05	The DRCU shall provide 5 BDA bias signals, adjustable from 0 to 200 mV_{rms} and 1 bias signal for temperature readout, adjustable from 0 to 500 mV_{rms}. The temperature readout biases are to be divided from a common oscillator. Each bias shall be adjustable with 8-bit precision. The frequency of each bias shall be adjustable between 50 and 300 Hz, with a precision of 5 Hz. Voltage noise on the bias lines, within the modulated band (50 – 300 Hz), measured at the DRCU DsMA connector, shall be < 20 nV/√Hz	JPL	Yes TBC by SAp
BDA-DRCU-06	The DRCU shall provide 15 commandable JFET source voltages with 256 levels. The range of Vss is from 0 V to –5 V.	JPL	Yes
BDA-DRCU-07	Vdd shall be adjustable from 1.5 to 4 V.	JPL	Yes

BDA-SSSD Performance Requirements (for reference)

BDA-DRCU-08	Vdd and Vss lines individually must source 1 mA to 5 mA. Noise on Vss < 1 μV/√Hz, and noise on Vdd < 0.3 μV/√Hz within modulated band (50 – 300 Hz), measured at the DRCU DsMA connector.	JPL	Yes
BDA-DRCU-09	Each of the 15 Vdd and Vss supplies must be commandable ON/OFF for spectrometer and photometer independently, without overshoot. Each Vdd and Vss pair are turned on and off together.	JPL	Yes
BDA-DRCU-10	The DRCU will provide 2 double-wired JFET heater lines with adjustable amplitude and duration. The supplies must be able to provide 5 V and 25 mA (photometer), 3 V and 18 mA (spectrometer). Each heater line is commandable ON/OFF, with a minimum duration of 10 s.	JPL	Yes
BDA-DRCU-11	The common-mode rejection ratio shall be better than –60 dB (50 – 300 Hz).	JPL	Yes
BDA-DRCU-12	The DRCU shall provide a dynamic range at the ADC sufficient to maintain the noise performance of the detectors under maximal signal conditions as defined below in BDA-DRCU-22.	JPL	Yes
BDA-DRCU-13	The signal bandwidth of the photometer channels shall be 0.03 Hz to 5 Hz. The 5 Hz cutoff should have a precision of 1 %.	JPL	Yes
BDA-DRCU-14	The signal bandwidth of the spectrometer channels shall be DC to 25 Hz. The 25 Hz cutoff shall have a precision of 1 % or better.	JPL	Yes
BDA-DRCU-15	The sampling of the photometer channels shall be synchronised with the bias, at a rate selectable between $v_{bias}/2$ to $v_{bias}/256$.	JPL	Yes
BDA-DRCU-16	The sampling of the spectrometer channels shall be synchronised with the bias, at a rate selectable between $v_{bias}/2$ to $v_{bias}/256$.	JPL	Yes
BDA-DRCU-17	The DRCU shall provide 2 adjustable power supplies for temperature control using a heater located at the 300 mK stage. This supply must provide a maximum of 340 mV and	JPL	TBD by SAp

BDA-SSSD Performance Requirements (for reference)

	50 µA, to be adjustable with (TBD by JPL) precision, and have a stability of (TBD by JPL)		
BDA-DRCU-18	Noise performance BDA-DRCU-01 shall be maintained under bias range 100 – 500 Hz	JPL	Yes
BDA-DRCU-19	DRCU noise performance (BDA-DRCU-01) to be maintained under a warm electronics thermal drift of 1 K/hour (TBC).	JPL	Yes
BDA-DRCU-20	*This requirement has been deleted and replaced by an appropriate note in BDA-DRCU-01*	N/A	N/A
BDA-DRCU-21	The requirement on JFET power supply voltage stability is $dV/V < 500$ ppm hr^{-1} for Vdd and Vss under a warm electronics thermal drift of 1 K hr^{-1} at the feet of the DCU box.	JPL BDA-DRCU-01	TBD by SAp
BDA-DRCU-22	The DRCU shall not saturate at an input voltage as large as 11 nV_{rms} at input (photometer), 17 nV_{rms} at input (spectrometer). DRCU channels shall remain functional if one input signal goes to Vbias	JPL	Yes
BDA-DRCU-23	The conducted RF current on all lines connecting to the bolometers or JFETS, originating in the DRCU, shall be less than 0.1 nA rms (TBC by JPL/RAL/SAp) over a frequency range of 0 - 10 GHz. (This assumes an attenuation of 40 dB by the RF filters).	JPL BDA-ISY-01	To be verified by instrument test
BDA-DRCU-24	Bias, JFET power, and readout electronics for the spectrometer and photometer arrays are to run from separate dedicated power supplies, with independent, isolated grounds.	JPL	TBD by SAp/RAL
BDA-DRCU-25	The electrical cross-talk, over the detector signal frequency band, between channels in the DRCU shall be less than 0.05 %. The electrical cross-talk shall be verified by varying the input signal on one channel and measuring the response in other channels. The input signal level to each channel must be representative.	JPL	Yes
BDA-DRCU-26	Each signal input to the I/A module must be connected to ground by a diode. This provides both protection and allows the JFETs to turn on without the JFET heater.	JPL	Yes

BDA-SSSD Environmental Requirements

3.3.5 SPIRE Instrument System Specifications

Requirement ID	Description	Reference	Compliant
BDA-ISY-01	The dissipated RF power at the detectors, arising from external sources on the spacecraft that propagate to the bolometers by radiation (EMI) or conduction, shall contribute < 1E-17 W/√Hz noise to the bolometers (< 5 nV/√Hz equivalent detector noise post-demodulation). EMI-induced current at the bolometers shall be < 1 pA rms.	JPL	TBC by instrument -level testing
BDA-ISY-02	The signal from microphonics (including both voltage and thermal response), arising from external sources on the spacecraft, shall contribute < 1E-17 W/√Hz noise to the bolometers (< 5 nV/√Hz over a > 25-Hz band around a chosen bias frequency within the allowed range of 50 and 300 Hz). For the third and fifth harmonics of the bias frequency, the noise specification is higher by factors of 3 and 5, respectively). Note: a system study is to be carried out to verify the need for this requirement on the harmonics.	JPL	TBC by instrument -level testing

BDA-SSSD Environmental Requirements

Table 3-3-3 Nominal Noise* Budget (in nV/√Hz)

	P/LW	P/MW	P/SW	S/LW	S/SW
Photon	21	26	30	24	30
Phonon	9	9	9	9	9
Johnson	7	7	7	7	7
Load resistor	2	2	2	2	2
JFET	7	7	7	7	7
LIA	6	6	6	6	6
A/D	4	4	4	3	3
Quad. Subtotal	26	30	33	28	34
Thermal*	< 6	< 6	< 7	< 11	< 11
EMI/EMC	< 5	< 5	< 5	< 5	< 5
Microphonic	< 5	< 5	< 5	< 5	< 5
Bias lines	< 4	< 4	< 4	< 4	< 4
Quad. Total	< 28	< 32	< 35	< 31	< 37

*Referred to the detector at DC.
†T_n < 300 nK/√Hz at the detector.

BDA-SSSD takes these and imposes requirements on:
- **^{3}He Cooler stability**
- **Noise on bias and JFET power**
- **Faraday cage**
- **Grounding**

Most systems-level requirements must be left to the instrument

BDA-SSSD Environmental Requirements on Sub-Systems

BDA-STR-03	The BDAs and JFETs shall be housed in an RF-tight shield. The JFET modules form part of this RF shield. All electrical, and thermal penetrations into the shield will be RF blocked or attenuated. The instrument optical aperture shall be designed to be compatible with the inclusion of a wire mesh RF filter should it prove necessary to minimise RF disturbance at the detectors. It shall be possible to electrically isolate the RF shield from the Herschel optical bench. The defining point for electrical ground of the RF shield shall be at the BDAs either at the 2.5 or 300 nK level. TBD.	BDA-ISY-01	Compliance to be verified by CQM instrument-level testing.
BDA-STR-04	The wiring harness shall have a mechanical resonant frequency greater than 1 kHz when secured in the FPU.	JPL	Design: TBC by JPL and MSSL.
BDA-WIR-02	The signal-wire-to-signal-wire capacitance of the cables running from the BDA to the JFET modules (including connector contribution) will be < 50 pF, after mounting.	IRD-FPHR-R01	Yes
BDA-HCO-02	Design values of detector performance require temperature stability at the point of thermal control (near the evaporator) of 10 μK/√Hz from 0.1 – 10 Hz. This assumes that the BDA acts as a 100-s thermal low-pass filter.	IRD-COOL-R05 BDA-PER-10	Compliance to be verified by instrument-level testing of the CQM.

Unsolicited Recommendation from JPL SPIRE Review 17 September

It would be a grave mistake to make a decision based only on analysis, or on experience with instruments based on other detector technologies, to ground the system warm. The SPIRE grounding architecture poses unique, and arguably unprecedented, challenges:

A) Bolometric detectors are known to be much more sensitive to most forms of EMI/RFI. This is because bolometers are indiscriminant detectors of power. A bolometer with NEP = 10-16 W/Hz^0.5 can be much more sensitive to EMI/RFI than a photoconductor with NEP orders of magnitude smaller.

B) The SPIRE FPU is separated from the warm electronics by ~ 7 m of cabling.

... What little experience there is provides painful lessons in how severe EMI/RFI problems can be, and how costly to remedy late in the program ...

D) The SPIRE observing strategy requires that the detector noise spectrum is free of excess noise over a broad band extending down to 0.1 Hz.

The board notes that it is difficult to guarantee that new effects that are very difficult to analyze - or even to anticipate - will not turn up when SPIRE is integrated into Herschel, and that *it may be prohibitively expensive in time, money, and risk to fix such problems after the instruments are integrated.*

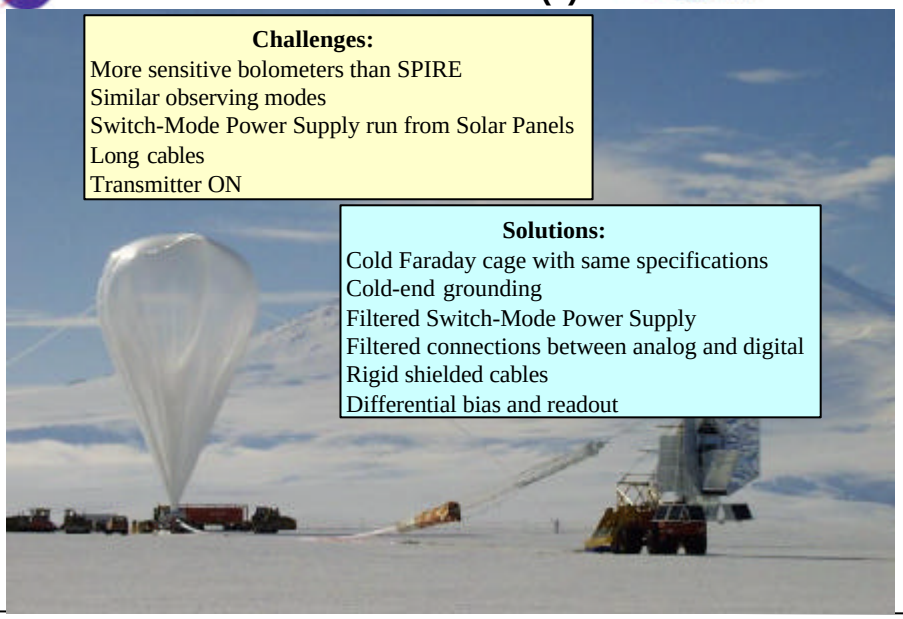
IRTS: The Infrared Telescope in Space
(An Example of the Worst-Case Scenario)

- **Bolometer sensitivities and readout similar to SPIRE**
- **SMPS developed in Japan without regard to bolometer requirements**
  Fixed early on and unchangeable thereafter
- **Electronics and bolometers tested independently to specification**
- **But bolometers completely inoperable during first integration!**
  Heated to >> 1 K by SMPS spikes at 10-20 MHz at 0.5 V_{p-p}
- **Cold filtering and electrical isolation implemented post-facto**
  Expensive, time-consuming, and instrument blinded during integration
- **System noise in flight still degraded**

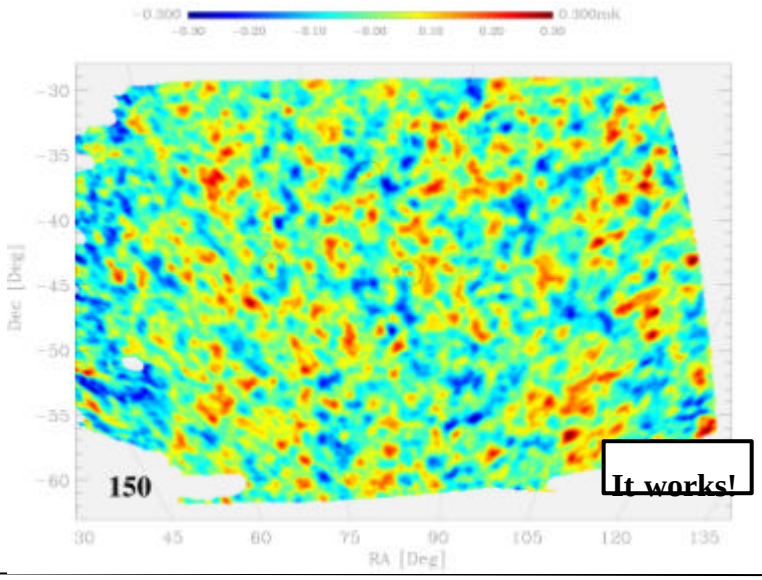
BOOMERAnG (1)

Challenges:
More sensitive bolometers than SPIRE
Similar observing modes
Switch-Mode Power Supply run from Solar Panels
Long cables
Transmitter ON

Solutions:
Cold Faraday cage with same specifications
Cold-end grounding
Filtered Switch-Mode Power Supply
Filtered connections between analog and digital
Rigid shielded cables
Differential bias and readout

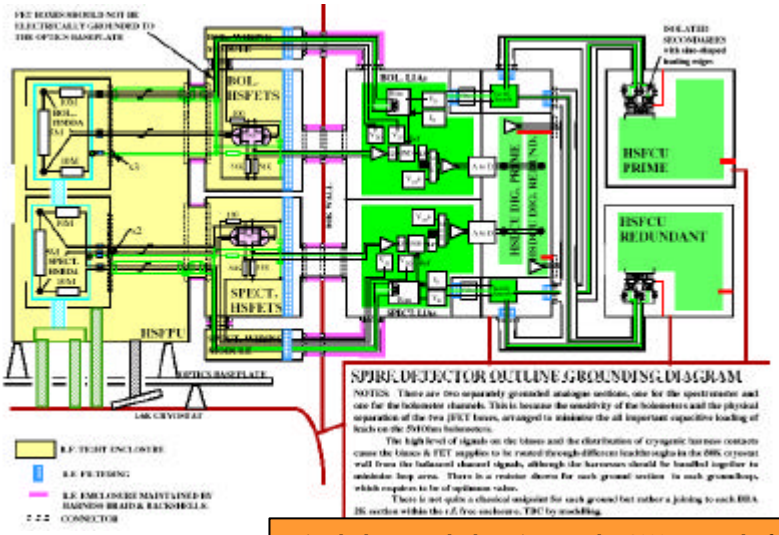


BOOMERAnG (2)



It works!

Grounding Network Documentation



Project had an agreed scheme in November 2000 as a result of many meetings and telecons. Some "details" to be worked out.

Additional Costs - to JPL – due to Grounding and Noise Issues

- **JPL supplying cryogenic RF filters for all sub-systems**
- **Differential readouts: twice the JFETs and wires**
- **JPL procuring expensive shielded cable with twisted triples**
- **JPL recently changed BDA and JFET grounding to be flexible**
- **Significant complexity added to BDA, JFET, and LR design to include cross-talk ground wires**

JPL thinks these issues are important to the success of SPIRE, And JPL is sharing the burden of the sub-systems requirements.

Recommended Approach

Lowest risk approach is to adopt configuration of a proven system

Departure from demonstrated configuration requires complete justification

- Analysis is complicated (and too late at this point)
- Best guide is experience and working, tested example

We can't prove CEA grounding scheme won't work, but

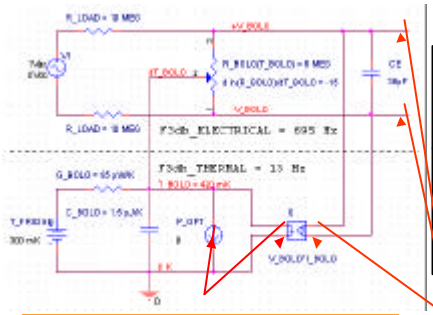
- It seems the burden of proof is to show that is *does* work
- Standard of proof must be high because the consequences are large

SPIRE should implement demonstrated architecture with

- Differential bias and readout
- Cold Faraday cage
- Cold-end grounding
- Filtered power supply to at least BOOMERANG specs

***Now* is the time to build in systems flexibility**

EMI susceptibility of an NTD-Ge bolometer



The ways to mitigate with the EMI susceptibility practiced in the bolometric receivers I have been familiar with are:

➢Keep the bolometer and the front-end electronics in an RF-tight cavity. Keep the EMI sources out of the cavity. Each electrical lead entering the cavity must be RF filtered.

➢Keep the electrical potential of the cavity as close as possible to the "ground" level of the bolometer bias generator to reduce the effects of the stray capacitance coupling. **Hence the concept of "cold-end grounding".**

The high frequency EMI may be absorbed by the bolometer the way the optical radiation does, or it may be antena coupled to the bolometer thermistor via it's electrical leads. In the both cases the EMI will act like additional heat source in the bolometer heat balance. The bolometer performance will suffer both because of the reduced resonsivity due to the elevated base temperature and because of the additional noise due to the EMI statistical nature. This will ultimately lead to reduced NEP of the system and will reflect upon the time needed for a given science task to be accomplished.

At lower frequency ranges, the EMI couples to the high-impedance bolometer leads via the stray capacitances of the wiring and the input impedance of the front end electronics. The in-band component of the EMI, combined with the microphonic response of the wiring variable stray capacitances will both drive unwanted bias currents through the bolometer and will interfere with the odd harmonics of the Lock-In Amplifier carrier. Again the system performance will suffer due to elevated noise level and poor stability of the readout.

Major EMI Sources

➢The high frequency EMI have radiative and conductive components. The two major sources of the radiative EMI are the onboard transmitters and the Switch Mode Power Supplies (SMPS). The conductive component is generated by the SMPS and the state transients of the digital electronics. The combination of the former two appears as a common mode currents acting between the system frame ground and any power and signal line entering their domain, and as voltages on the power lines and the signal outputs. In the specific case of the SMPS, part of the energy accumulated in the inductors and the parasitic inter-winding capacitors tend to escape during the transition times of the switching components. They manifest as short spikes at each SMPS transition and have very wide frequency spectrum. Due to the high commutating power this EMI carries significant energy and is very difficult to suppress. To mitigate the SMPS EMI the next basic steps are usually taken:

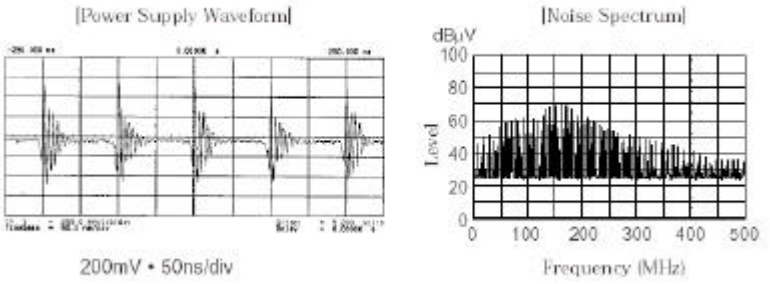
•To reduce the parasitic inter-winding coupling, the SMPS inductors are properly sectioned and shielded. Snubber networks are applied to reduce the dV/dT during the transitions.

•The DC/DC converter and the necessary filters are sectioned into a RF- tight compartment tied to the primary power supply ground. Every single lead between the RF compartments propagates via feed-through capacitors.

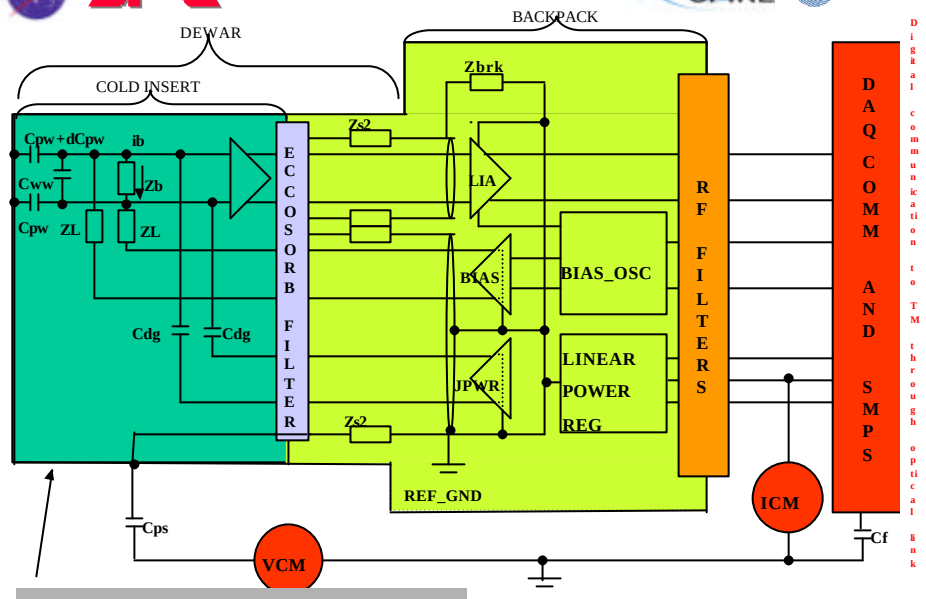
Failure to properly address the SMPS EMI issues can result in serious systems -level problems with bolometers as demonstrated by the bolometric receiver FIRP onboard the IRTS.

➢The low frequency EMI are generated by various power consumers inside the cryostat and between the cryostat and the frame ground. Such sources can be the various heaters, motors, ac signals in close proximity to the high-impedance bolometer wiring, the various ground loops.

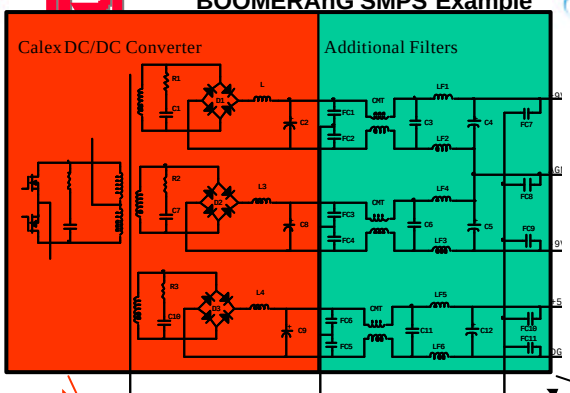
Example of a SMPS-generated EMI in the time and in the frequency domains.



BOOMERAnG COLD-END Grounding

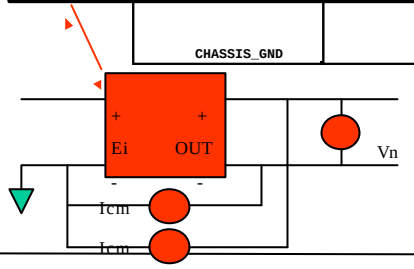


BOOMERAnG SMPS Example



➢The Calex DC/DC converter and the Additional filters located in a Faraday cage tied to the frame ground

➢The Additional Filters are located into a separate compartment of the Faraday cage. Each of the DC/DC converter leads passes through a feed through capacitor to shunt the Icm to the frame gnd and use of a CM transformer to further reduce the Icm. The Vn is reduced by a p filter after the CM transformer.



SMPS Faraday Cage

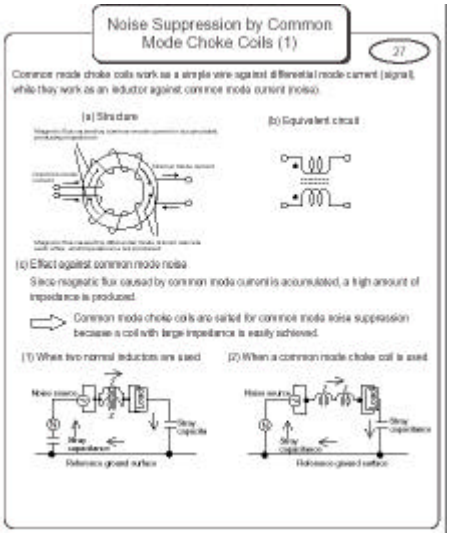
Calex DC/DC converter noise

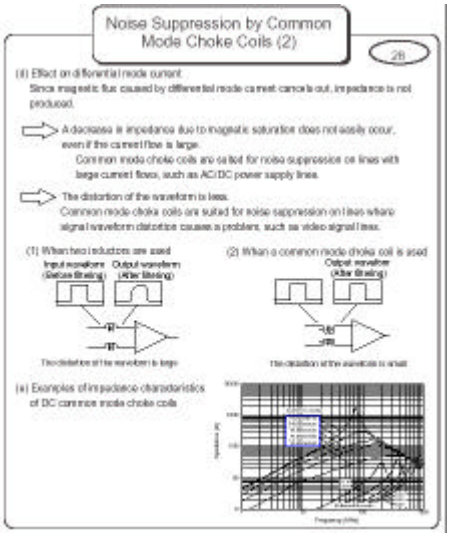
Icm [0-20 MHz] < 2 mA pp

Vn [0-20 MHz] < 40 mV p-p

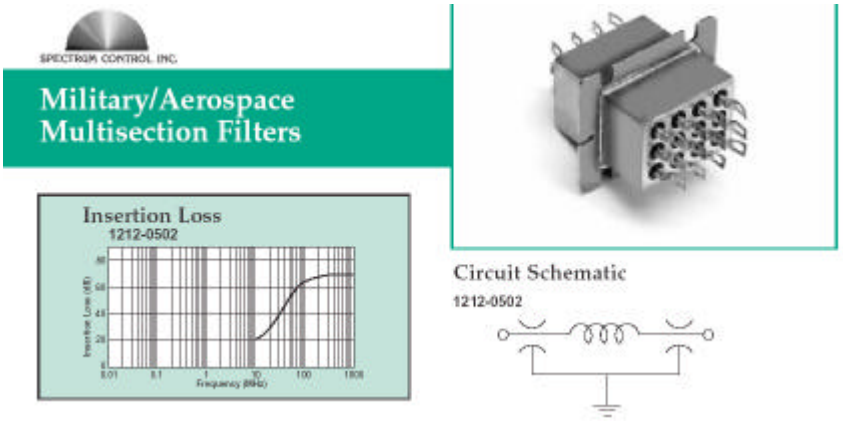
Low cost power supply, simple RF filters and power regulators

The first filtering stage of the BOOMERAnG' SMPS is a Common Mode Transformer (CMT)





The second stage of the BOOMERAnG's filter is a comersially available RF filter by SPECTRUM CONTROL INC. Each power line passes through it.



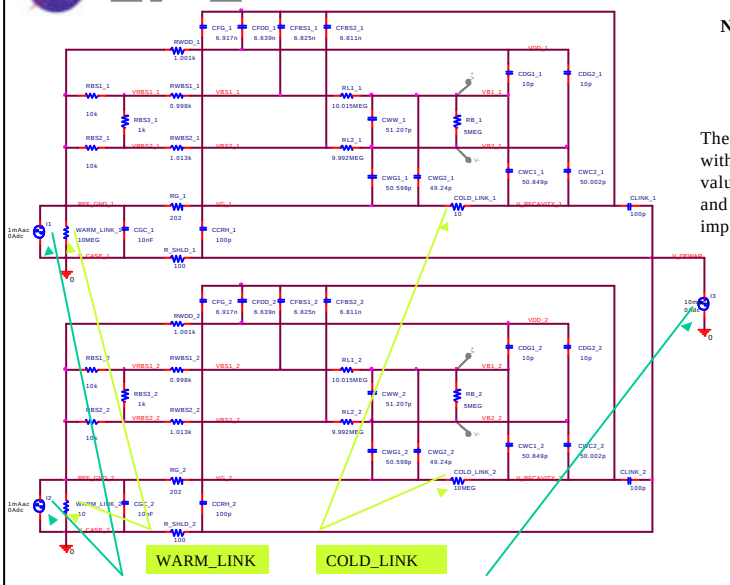
Naïve SPICE model for comparative study of the bolometer's EMI susceptibility for a COLD-END and the WARM-END grounding schemes.

To further illustrate the merits of the two grounding schemes, I produced (and distributed) a naïve SPICE model of possible EMI pickups by a bolometer from a "SMPS" ICM source acting between the warm electronics bias reference and the frame grounds, and from an ICM source acting between the warm electronics frame ground and the dewar located some 5 meters away and linked by some 50 Ohm to the warm electronics frame. The value of the "SMPS" ICM has been chosen by the value of typical DC/DC converter of 1 mA amplitude. The value of the dewar_to_frame ICM has been chosen such, that it generates power equivalent to the bolometer NEP of 1E-17 watt/RtHz.and it happen to be only some 10 mA amplitude. Not included in the model are the EMI voltages referenced to the bias ground and the signal lines, because they will have the same contribution in the both cases.

This naïve model contains two identical blocks that represent the possible capacitive and conductive coupling of a bolometer to it's environment. It is intended to be used in the low to med frequency range to avoid the inclusion of the ESR/ESL for the resistors and the capacitors and distributed parameters of the transmission lines. The capacitors and the resistors in a block are randomized within 3% for the resistors and 5% for the capacitors to simulate a realistic balanced bias/readout case.

The only difference between the two blocks is in the value of the impedances linking the bolometer reference ground to the bolometer Faraday cage and to the warm electronics frame ground. In the COLD_END case represented by the top block, the COLD_LINK = 10 Ohm, the WARM_LINK = 10 MOhm. For the WARM-END case the COLD_LINK = 10 MOhm, the COLD-LINK = 10 Ohm respectively.

The schematic diagram of the model and the simulation results of the EMI power absorbed by a bolometer for the both cases are shown in the next two slides.



Naïve SPICE model of a bolometer EMI susceptibility.

There are two identical blocks with only difference of the values of the WARM_LINK and the COLD_LINK impedances.

The upper block with WARM_LINK = 10 MOhm and COLD_LINK = 10 Ohm represents the COLD-END GROUNDING.

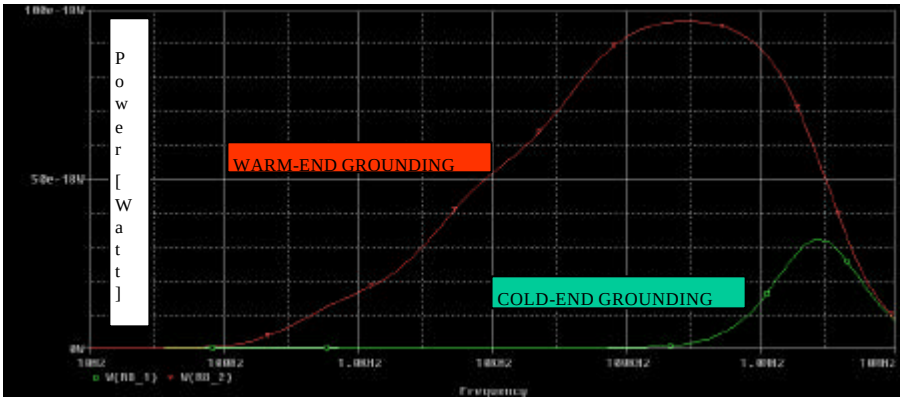
The lower block with WARM_LINK = 10 Ohm and COLD_LINK = 10 MOhm represents the WARM-END GROUNDING.

1 mA "SMPS" Current EMI sources between the signal and frame ground

10 mA Current source acting between the dewar and the warm electronics frame ground

SIMULATION RESULTS:

EMI Power Dissipated On The Bolometer in the cold-end grounding case (green) and in the warm-end grounding case (red)



The WARM-END grounding scheme is more susceptible to a EMI acting between the warm electronics frame ground and the dewar (the 10 mA source).

COMPROMISE SOLUTION (1)

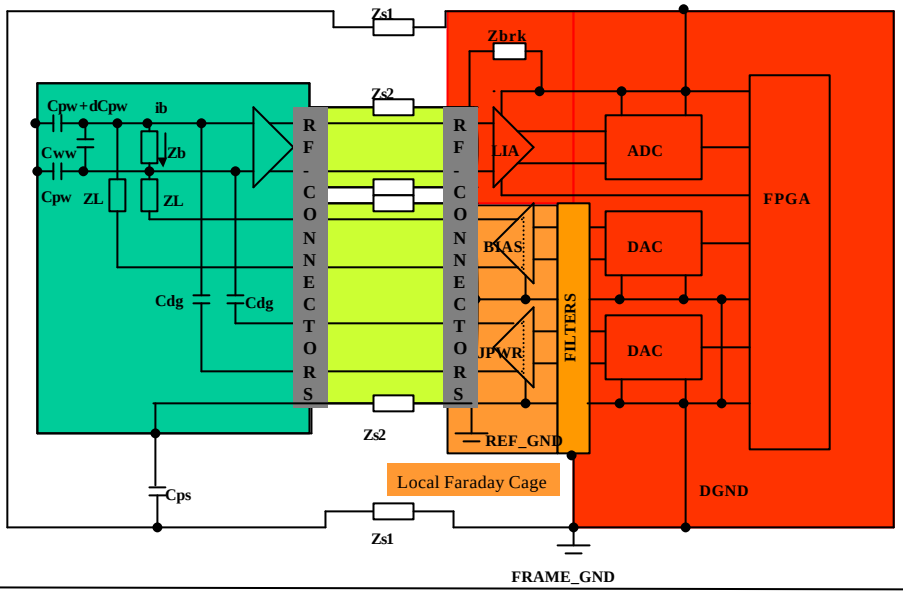
As it come to pass, the current design of the DRCU imposes a WARM-END grounding scheme. Although we cannot exclude the possibility that warm-end grounding can work, we think it is a reasonable requirement that the system must be able to run in BOTH ground configurations, for maximum flexibility.

Currently the boards are designed with a common ground plane for both the digital "dirty" ground and the "clean" analog ground. Furthermore there was a pressure to connect each board ground plane to the warm electronics frame permanently, via the board sliders. This has not been accepted nor implemented in the current QM board design, so it is still possible to connect the various boards to various grounds.

Taking in account the ICM EMI sources due to the digital electronics and the SMPS, what happen to reside in the same compartment as the "mixed analog" boards like the LIAs and the bias generators, it may be feasible to tie the signal grounds of modules not directly connected to a bolometer (like all the grounds except the BIAS/JFET_POWER ground) to the frame to satisfy the SAp concerns related to maximally short return path for the ICM.

For the BIAS/JFET_PWR ground however it is highly desirable to be connected to the cold Faraday cage. This can be done by providing separate insulated power for this board specifically. The catch here is that both the bias generator and the JFET_PWR contain DACs connected to the FPGA by multiple digital lines, hence they have to share the dirty DAQ/IF ground. Furthermore the first DAC of the bias generator is driven by a fast clock. This problem can be mitigated by proper partitioning of the BIAS/JFET_PWR boards to an analog part (only the BIAS and JFET_PWR drivers) with it's clean ground and to mixed analog-digital (the DACs and the accompanied electronics) that may be tied to the frame ground like the rest boards. The clean analog ground can be connected to the cold faraday cage on one end and to the mixed ground via high-impedance filters to avoid possible ground loops on the other. All the WE connectors to the DEWAR have to be RF-Filtered. A possible implementation is demonstrated on the next slide.

COMPROMISE SOLUTION (1) DIAGRAM



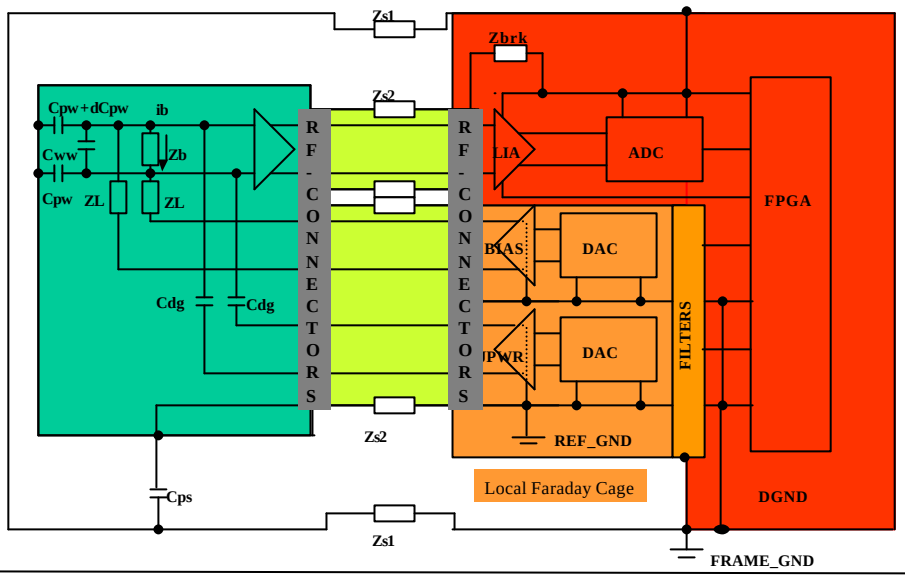
COMPROMISE SOLUTION (2)

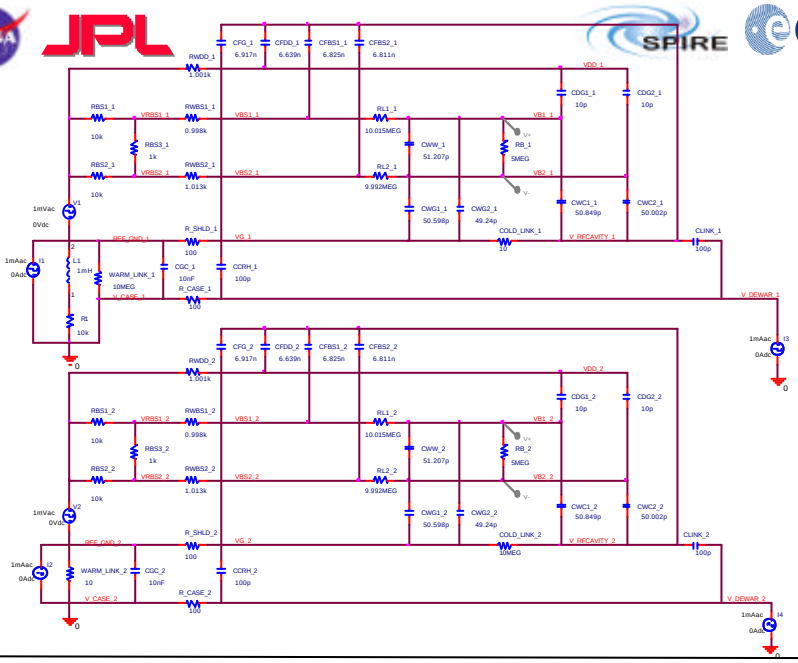
For further reconciliation of the two grounding schemes with no BIAS/JFET_PWR board redesign, we may install the above mentioned board in Faraday cage of it's own, and filter any line entering the RF-tight cavity, as shown on the next slide.

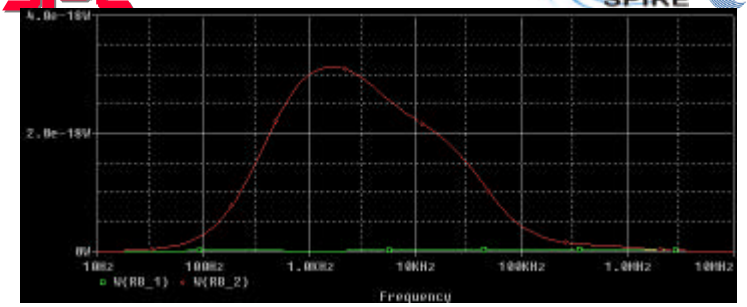
The BIAS/JFET_PWR board communicates with the FPGA on the DAQ/IF board via multiple digital lines. The maximum clock frequency applied to the first bias DAC is equal to 2*256*Fbias. For Fbias of 200 Hz, the fastest digital signal that enters the BIAS board is about 100 KHz, so the filtering will be a lot more difficult compared to the COMPROMISE SOLUTION (1), where the fastest signal is the analog bias @ 200 Hz.

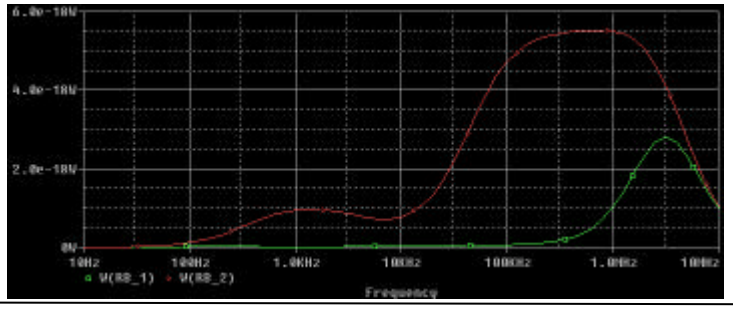
Because we will need to introduce high impedance decoupling between the DAQ GND and the BIAS GND, each digital signal must be transmitted differentially, with a Common Mode Choke and a RF-Filter inline.

COMPROMISE SOLUTION (2) DIAGRAM






4.0e-18V
2.0e-18V
0V
10Hz
100Hz
1.0KHz
10KHz
100KHz
1.0MHz
10MHz
V(RB_1)
V(RB_2)
Frequency

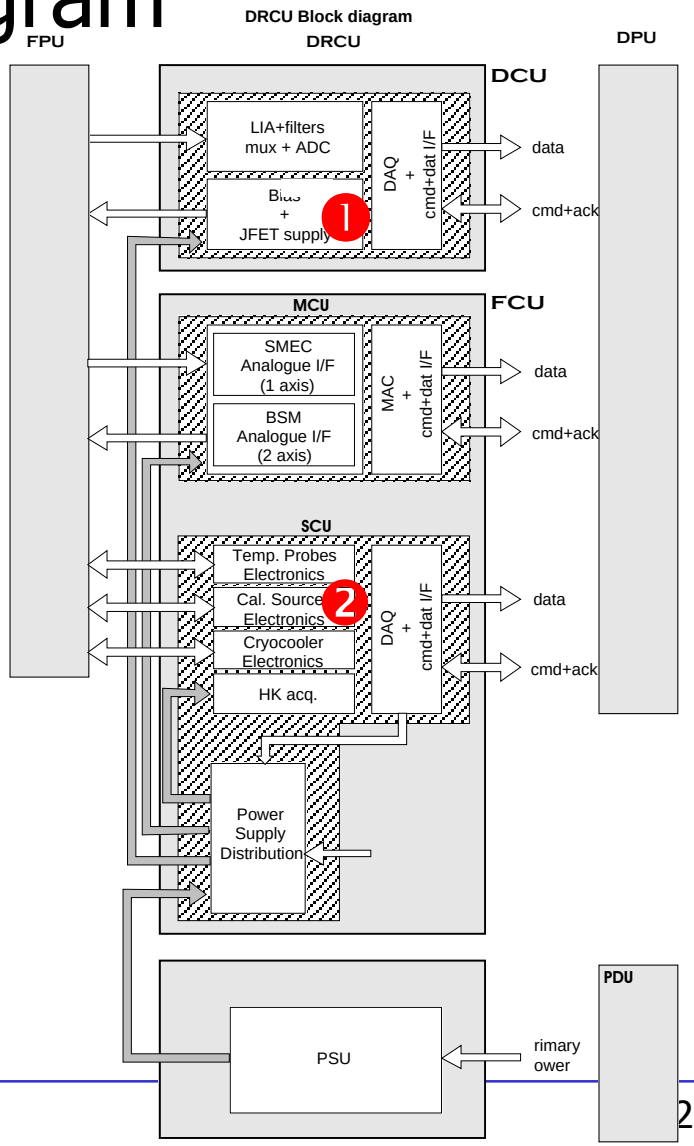

6.0e-18V
4.0e-18V
2.0e-18V
0V
10Hz
100Hz
1.0KHz
10KHz
100KHz
1.0MHz
10MHz
V(RB_1)
V(RB_2)
Frequency

Design Overview

- The ***DRCU*** is a two-box units:
  - The FPU Control Unit comprises
    - The FTS and BSM associated electronics which constitutes the Mechanisms Control Unit (MCU)
    - The Calibrators, cooler and thermometer associated electronics along with the power control functions which constitutes the Subsystems Control Unit (SCU)
    - The Power Supply (PSU)
  - The Detector Control Unit comprises analog and digital electronics exclusively devoted to bolometers operation (DCU)

Block Diagram

- ❶ The Detector Control Unit
- ❷ The FPU Control Unit
- ◆ The Mechanisms Control Unit
- ◆ The Subsystem Control Unit
- ◆ The Power Supply Unit



DCU

Specifications Overview (1)

- ***Analog Processing channels***
  - Functions : receive, amplify, demodulate & filter bolometer signals
  - 336 total number : 288 for photometer & thermometer + 66 for spectrometer
  - Specifications:
    - gains:
      - **Photometer : 375**
      - **Spectrometer : 265**
    - Input signal bandwidth:
      - **Photometer : 0.1 to 5 Hz**
      - **Spectrometer : 0.1 to 25 Hz**
    - Input noise ≤ 7 nV rms/rt(Hz)

DCU

Specifications Overview (2)

- ***Analog Processing channels …***
  - Signal dynamic
    - **Photometer : 270 000**
    - **Spectrometer : 170 000**

DCU
Specifications overview (3)

- ***Bias generators***

  - Functions : generate AC and DC biases for bolometers and JFETs
  - 2 types are defined:
    - Adjustable AC biases:
      - Photometer: 1 sine generator / 4 channels with independent amplitudes
      - Spectrometer: 1 sine generator / 2 channels with independent amplitudes
    - Adjustable DC biases (with on/off command):
      - Photometer: 12 generators for JFET + 1 for heater
      - Spectrometer: 3 generators for JFET + 1 for heater

DCU
Specifications Overview (4)

- ***Bias generators …***

  – Specifications:

AC bias

- Voltage range is 0 to 200 mV rms for bolometers and 0 to 500 mV for thermometers
- Accuracy: 1 mV (equivalent to 8-bit DACs)
- Frequency range: 50 to 300 Hz

DC bias

- Voltage range (Vss): 0 to -5 V
- Output current: 5 mA max

DCU

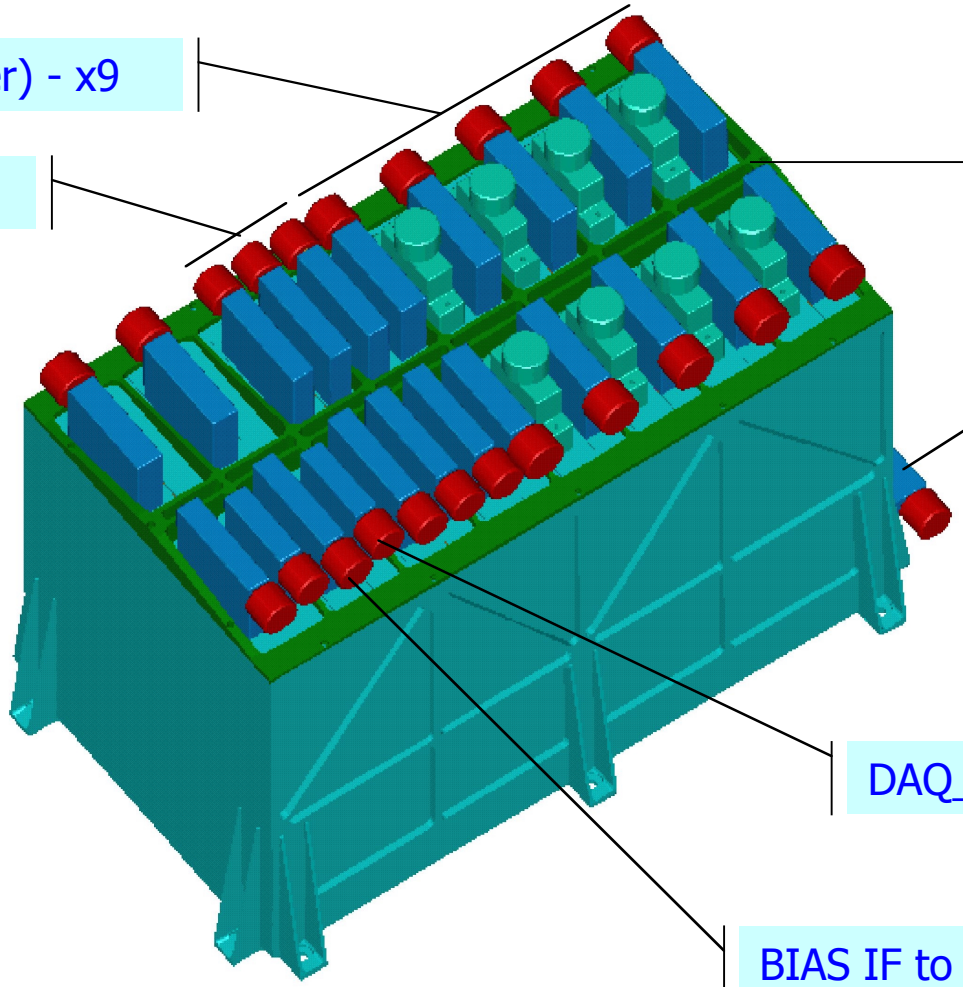
Specifications overview (5)

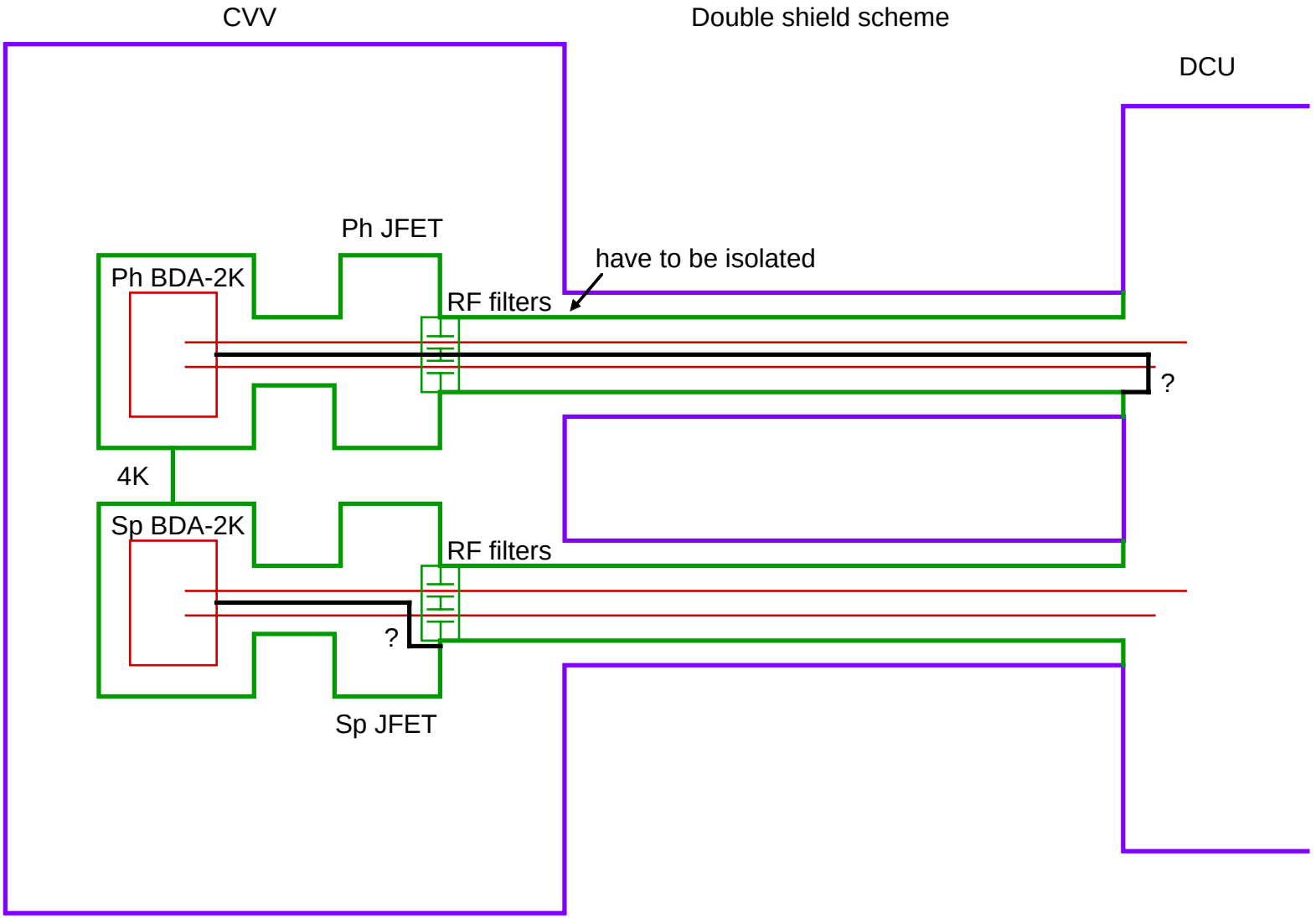
- ***Data acquisition & DPU interface***
  - Functions: digitize signals (from bolometers & H/K parameters), built / transmit data formats, receive / decode low-level commands.
  - Specifications:
    - Digitizing resolution: 19 bits (16-bit ADC + 4-bit offset)
    - Frame rate : 1 to 1/256 of AC bias frequency (max. 300 Hz)
    - Frame acquisition time ≤ 3 ms
    - Data formats and Command are defined in DRCU ICD
    - Electrical interface : RS422

DCU
Internal Architecture (1)

- Electrical
  - 5 board types:
    - ***LIA_P (Photometer Lock-In Amplifier) - 9 x 32 analog channels***
    - ***LIA_S (Spectrometer Lock-In Amplifier) - 3 x 24 analog channels***
    - ***BIAS (Bolometer/JFET Bias) - 1 M + 1 R***
    - ***DAQ_IF (Data Acquisition & DPU IF) - 1 M + 1R***
    - ***DCU_BP (backplane & LIA supplies linear regulators) - 1 M/R***
- Mechanical
  - Single board geometry & stiffeners
  - Total of 16 modules

DCU
Internal Architecture




CVV
Double shield scheme
DCU
Ph JFET
Ph BDA-2K
have to be isolated
RF filters
?
4K
Sp BDA-2K
RF filters
?
Sp JFET

Triple shield scheme