Consolidated Comments on DCRU Documents
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ID	Document	Section	Raised by	Comment	Response
GEN 1	All		EAC (PA)	There is no CIDL Configured Item Document/Drawing List. (ESA and SPIRE requirement).	Configuration Item Data List is under construction.
2	All		EAC (PA)	There are several TBW's or will insert XYZ here when ready throughout the set of documents.	Will be corrected in next release of document set.
3	All		EAC (PA)	DCU Design document, purpose and scope of this document be TBW, should not still be undefined at this stage	Document will be corrected : **OK,** I will add this information on next release.
4	All		EAC (PA)	PA Plan is missing from this document list.	CEA has already provided it's standard PA plan (sent to Kelsh DM, KING KJ , November 2000)

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DRCU1	DRCU Spec. Doc. SAP-PRJ-000461 (Sap-SPIRE-CCA-25-00)	2.1	BMS	Figure 2.1a is scrambled Figure 2.1a has "OEP" outside the FPU – it should be inside	Figure is now corrected and is no more scrambled even in pdf format
2	*ditto*	DRCU-REQ-45	BMS	…and here's the rub! When does the filtering get specified?	The DCU is powered by the FCU's PSU; the DCU's power filtering has no impact at instrument / system level, except for radiated emission matters where IID applies.
3	*ditto*	Fig 4.2-b	BMS	This figure does not accord with the power supplies specified elsewhere in the document (DRCU-REQ-43 and DRCU-REQ-99) and is therefore confusing – remove or replace.	YES - This figure does not reflect any more the design and especially for power supplies. Shall be corrected
4	*Ditto* Also applies to DRCU/DPU I/F Doc	DRCU-REQ-79 (and maybe elsewhere)	BMS	Parameter names used here are not consistent with the interface specification. In the interface doc (…) it uses FPUTEMP# -here the temperatures have more meaningful names – use these please!	ICD shall be modified according to actual SCU design in order to define unambiguously temperature measurement channels. Action on SCU designers List available (see attached file): ICD to be updated
5	*ditto* Also applies to DRCU/DPU I/F Doc	DRCU-REQ-83	BMS	Please define the SCUSTATUS word as soon as possible – it does not appear at all in the I/F parameter list although it can be requested by dedicated command! (cf. ICD section 2.2.14.3 and 2.2.15)	Action on SCU designers Description available (see attached file): ICD to be updated
6	*ditto*	DRCU-REQ-85 DRCU-REQ-86	BMS	Wrong document called up – should be AD24?	DRCU-REQ-85 and 86 have been modified to: The thermometry sub-system (main part) shall have the following channels according to AD24 except for cryo-cooler related temperature probes (text in blue) where AD21 is considered
7	*ditto*	DRCU-REQ-88	BMS	Number of steps for full range operation is over specified – PCAL requirement is for 256 steps – if it is convenient to have a single type of DAC then o.k. else it is unnecessary.	HSO-CDF-ICD-013-2-0 specifies a 12-bit resolution HSO-CDF-ICD-011-2-0 specifies a 12-bit resolution
8	*ditto*	4.6.1	BMS/JD	Post regulation is shown for LIA supplies but not for DAQ/Bias supplies. Where does this happen?	Post regulators are only required for LIA electronics since input stage of the design has a poor PSRR

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9	*ditto*	4.7.3	BMS	Can we have an extra requirement that the outputs of all FPGA controlled supplies (heaters; mechanism drives etc) are kept low during initialisation and are kept low until commanded otherwise.	YES - This requirement has already been considered for MCU and SCU designs. OK for the DCU
10	*ditto*	DRCU-REQ-120	BMS	What does S/W crash refer to? The DPU or any software local to the DRCU?	This refers to MCU S/W exclusively
11	*ditto*	4.7.5	BMS	Please check this against the Operating Modes document version 3 issued Jan 2002 as the naming of modes has been changed and we have defined two standby modes one for PHOT and one for SPEC.	Chapter 4.7.5 has been updated: please check
12	*ditto*	DRCU-REQ-122	BMS	Reword and add new requirement: *122: The DRCU shall provide capabilities for the DPU to detect internal failures* *122 bis: The MCU shall provide capabilities to detect and handle failures in the sub-system that might cause immediate danger to the mechanism.*	OK - Has been modified & added
13	*ditto*	4.9.3	BMS	The diagram is unreadable – please make it bigger.	OK size is doubled
14	*ditto*	5.1.3	BMS	Are these requirements still relavant given that the interface drawing exists?	Will stay in the document even if no more formally useful
15	*ditto*	8	BMS	The reliability figure for the DCU has been discussed in a technical note. The FMECA has covered the rest of the reliability discussion?	
16	*ditto*	11 and section 1.3	BMS	AD13 through 17 aren't mentioned/used – did they go missing?	AD14 to AD17 have been removed from previous document issue when refreshing AD list.
17	*ditto*	12	BMS	Table is incorrect? QM1 and QM2 do not have Flight Equivalent power supplies with or without redundancy.	Table is a copy and paste of DRCU Development Plan -> document to be updated (Action : JLA)
18	*ditto*	4.4.3	PH	REQ-85, the range for the SCAL 4% and 2% source (T-SCAL2, TSCAL4 is listed as 10K to 80K. This should read 4K to 150K	OK range update was missing (demonstrate the interest for generating ECR to keep track of requirement modification

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ICD 1	DRCU ICD SPIRE-SAP-PRJ-000451 (Sap-SPIRE-CCA-075-02)	5.4.3.2.1	DKG	Include jumper connections from pins 1 to 21; 2 to 22, 20 to 30; 4 to 24; 5 to 25; 3 to 6 of J29 and also J30 to allow for robustness in the SMEC Launch Latch drives.	OK - Update missing in the released ICD - Has been done

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DCU1	DCU Design Description SAp-SPIRE-FP-0063-02	3.2	BMS	What does this table mean? It is not complete.	I will remove this table from the document, all the information about the power supplies are in the PSU document
2	*ditto*	Whole doc.	BMS	Circuit diagrams are unreadable (e.g. Picture 4-8)	Ok they will be removed
3	*ditto*	4.1.3.1 4.1.6.1	BMS	I believe the offset in the first part of the picture comes from the JFETs? Please identify the source of the offset is the text or on the picture.	Yes, the offset comes from the JFET, that Will be added on next release.
4	*ditto*	4.1.3.2 4.1.3.3 4.1.6.2 4.1.6.3	BMS	Can we have the transfer functions of the filters in tabular or polynomial form please. Then we can use them in the instrument models.	OK, I Will add the transfer functions on next release.
5	*ditto*	4.1.8.1	BMS	The description is a bit hard to follow! What is the final relationship between DATA and the amplitude of the bias that is actually output from the circuit? Is the statement about the resistors associated with the absence of the redundant cards from QM1 or does it represent a design option?	5sin(wt)xDATA/256*R1/(2R2+R1) Yes, the statement about the resistors is associated with the absence of the redundant cards from QM1 and it doesn't represent a design option.
6	*ditto*	4.1.8.1 4.1.11	BMS	There is no description of how the phase of the demodulation signal is altered for each BDA module? I hope this is implemented!	OK and yes it is implemented!
7	*ditto*	4.1.12.1	BMS	Is FRAME=0 equivalent to continuous output of frames as specified in the ICD? Do both FRAME and START have to be high for data to be output?	Yes
8	*ditto*	4.1.12.3 (Page 61)	BMS	Is an average of two values at all useful? Why isn't it 4 values as in the photometer?	The timing is to short to do more than 2 sampling average.
9	*ditto*	4.1.12.5	BMS	I think I understand how it works but it isn't completely obvious from this section! Just a leetle more explanation?	Ok I will add some information on next release.
10	*ditto*	4.1.12.7	BMS	Do 1 and 2 represent design options to be decided upon?	YES, we are going to use the first one

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SCU1	SCU Design Description SEDI/SCU/MM /2002-1	1.1.3	BMS	We don't seem to have a copy of AD5? SEDI-SPIRE-OG-0001-02	The AD5 document is a technical description of the DPU interface, primarily intended to provide common understanding for the 3 DRCU implementations: DCU, MCU and SCU. This document is available.
2	*ditto*	2.1	BMS	Block diagram shows "AC Modulation(x4)" – why is this when there is only one AC temperature channel?	The block diagram is ambiguous. The AC channel requires 4 signals to support the On/Off and modulation controls, whereas the DC channels require only one signal for On/Off control. Will be clarified in next release.
3	*ditto*	2.2 3.1 3.2	BMS	We would like some clarification of the operation of the acquisition sequencer and the data frame transfer: i) Which takes priority – the Acquisition Sequencer or the Get Parameter request? We wish to have the data in the frames at even sampling rates – therefore we would wish the Acquisition Sequencer to have priority. A timing diagram would be useful ii) Does the FPGA assemble a complete data then transfer it, or does it transfer the payload piecewise?	i) There is no actual priority between the "Acquisition Sequencer" and "Get Parameter" actions, which are served on a first-come first-served basis. Analysis has shown that the sampling interval specification (all data sampled within 6ms) is guaranteed, even under worst case "Get Parameter" activity. ii) The FPGA transfers the payload piecewise (word per word).
4	*ditto*	3.2.1.1	BMS	Similar comment – Data Frame and Packet used interchangeably – please use Data Frame as packet means something else to the DPU.	Will be modified on next release.
5	*ditto*	4.1.1 4.2.1 4.3.1	BMS	Maximum lead resistances are specified in the DRCU Specification document and the Harness Definition Document. These should be used to specify the design?	The harness resistance is a concern for the Sorption Pump Heater, which is marginal at maximum harness resistance [With a 100 Ohm harness resistance, the +-9V circuit saturates at 35.5 mA (500 mW dissipation in the 402 Ohm load occurs at 35.3 mA)]. Requires further investigation, or relaxation (reduction) of the harness resistance spec.
6	*ditto*	4.1.4.5 4.2.4.4	BMS	Does this test mean that the effect of the lead resistance can be ignored? The lead resistance does not seem to be included in the simulation – what is the dissipation going to be in the cryoharness?	Knowing the heater currents and harness resistance, the cryoharness dissipation should obviously be considered. This is not specifically a SCU issue.

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7	*ditto*	4.2.4.1	BMS	Check with Lionel Duband whether 4pW is significant in terms of the operation of the heat switch sorption pump.	To my knowledge, still to be checked by the system team.
8	*ditto*	4.3.1	BMS	The Spec Doc (AD1) specifies 6 kΩ for the heater resistance	Yes. Taken into account in the design. Will be modified on next release.
9	*ditto*	4.4.1.2 4.4.1.3	BMS	This is an incorrect description of the SCAL sources – the Spec. Doc (AD1 v0.92) has the correct specification (2% and 4% sources) with both types of source having the specification as for "SCALP". The "SCALF" drive is not required, we need 2x the "SCALP" design.	Yes. Taken into account in the design. Will be modified on next release.
10	*ditto*	4.8	BMS	Is this power supply monitoring associated with the SCU staus word?	No. The power supplies are measured on request and are made available in parameters ScuCHTp05, -n09 and –p09. These values are not checked by the SCU.
11	*ditto*	5.2.1	BMS	How does this work? Analogue or digital?	As stated, analogue.
12	*ditto*	6.1	BMS	The notes on the next page make explicit that all output voltages and currents are held low in the reset state. Maybe make this clear in this section? Also is it really true that the SCU is "stateless" when it leaves reset? I hope that the outputs are definitively held low until commanded otherwise?	At time of writing, the need to have outputs low at start-up was not a requirement, but this feature had been included however. This is now a requirement. Will be described more clearly in next version. The text says " the DPU is stateless once out of reset". This means that after reset, it does not keep track of command history, and always act identically under identical commands.
13	*ditto*	6.2	BMS	Its not clear how the sampling frequency is set – FRAMECONF? It is reasonably urgent that the SCUSTATUS word is defined as this will be used for error detection in flight and we need to get on with the FDIR.	FrameConf has two fields: The 1-bit "Type" field selects between "normal" and "test pattern" frames, and the "Rate" field R gives the frame rate division factor. The resulting frame repetition rate is 80/(R+1) Hz. Will be updated in next version.
14	*ditto*	7.1	BMS	Read DRCU-REQ-89 in the latest version of AD1 v0.92 Both SCAL devices are four wire to allow remote sensing of voltage and therefore current stabilisation?	The cross reference table is based on DRCU spec. v0.90. The numbering has changed in spec. v0.92. Will be updated in next release.

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15	*ditto*	4.4	PH	Description of SCAL out of date, flood and point sources no longer used	Yes. Will be updated in next release.
DPU-ICD 1	*DRCU to DPU ICD Sap-SPIRE-CCA-076-02*	General comment	RCI at IFSI	One very important comment is that, as far as we know, the DRCU-DPU ICD is the one we wrote (SPIRE-IFS-PRJ-000650 of 2/4/2001). We always said that we will discuss and include in that document the DRCU people comments, but the need of a single document is to avoid ambiguities and unnecessary efforts (i.e. we are the custodian of the ICD).	
2	*ditto*	2.1.1	RCI	DRCU subsystems, if addressed individually reply with a response word with the following ..... Should read: DRCU subsystems, if addressed individually with SYN0=0 reply with a response word with the following ...	OK text modifed

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3	*Ditto*	2.4.1.2	RCI	when a "Set_parameter" command is received the subsystem responds to the DPU by transferring a command acknowledge word (positive or negative) on the response line. Should read: When a "Set_parameter" command with SYN0=0 is received the subsystem responds to the DPU by transferring a command acknowledge word (positive or negative) on the response line.	§2.1.4.2 ??? Text modified The next sentence has to be modified in the same way. A "Get_paramater" command with a SYN0=1 don't generate any response. This is due to the interpretation of the SYN bit at the interface circuitry level and then independently from the command id itself
4	*Ditto*	2.1.5.1	RCI	The RES signal shall by modified on the rising edge of the CLK signal and being sampled by the DPU on the next falling edge of the CLK signal. Should read: The RES signal shall be modified on the falling edge of the CLK signal and being sampled by the DPU on the next rising edge of the CLK signal.	Not only text to modify : H/W is designed according to the first sentence as given by this document a long time ago. Why a so late comment, while the H/W is now existing. Must be checked with designers…
5	*Ditto*	2.1.5.3	RCI	Delta T1 is missing in the max command rate formula. In any case the formula is very optimistic as the actual max rate (if SYN0=0) is around 500 commands per second.	This value is given for information only. I agree as not very realistic

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6	*Ditto*	2.2.5.2	KJK	Add / to SetGetPhotoJfetPwr and SetGetPhotoOffset In SetGetPhotoOffset the channel number can only be 0 to 31 (not 0 to 32), which presumably correspond to channel numbers 1 to 32 in table 2.2.6.4. Similarly for SetGetSpectroOffset.	Text & value corrected for both Photometer and Spectrometer. 0 to 31 (physical address) effectively corresponds to 1 to 32 (LIA_P channel number) 0 to 23 (physical address) effectively corresponds to 1 to 24 (LIA_P channel number)
7	*Ditto*	2.2.5.3	KJK	SetGetSpectroHeaterPwr should be SetGetSpectroHeaterBias (to be consistant with Photo table)	Oops - Corrected
8	*Ditto*	2.2.6.1.4	KJK	Description for SetDemodPh should be 'Set the bolometer group demodulation phase shift'	Corrected. Command acronyms also corrected to respectively SetPhotoDemaPh and GetPhotoDemoPh (Photo was missing)
9	*Ditto*	2.2.6.1.6	KJK	Heading should be PhotoHeaterBias to be consistant with table 2.2.5.2.	Oops - Corrected
10	*Ditto*	2.2.6.5.8	KJK	Description for GetSpLWJfetVSS should be 'Get S-LW JFET source voltage' Description for SetSpLWJfetVSS should be 'Set S-LW JFET source voltage'	Letters inverted - Corrected
11	*Ditto*	2.2.6.7.1	KJK	I imply from the desciption of the science frames in section 2.3.5 that if bit 3 is set to 1 (test) then bits 2 to 0 may only be set to 0 or 4. What happens for other combinations?	I already address this point with F.PINSARD but with not conclusion. I have the feeling the definition of this command has to be modified or even splitted into 2 or 3 commands; the present definition is to confusing even for us! Action open to enhance this point

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12	*Ditto*	2.2.7.1	KJK	If PhotoDivBias (why not BiasDiv - see 2.2.6.1.1?) is set to 0 the sampling frequency will be infinite! What actually happens? Presumably setting Channel_P1 to 0 selects Channel 1 of LIA_P1 etc?	$F_{sampl}=\frac{F_{bias}}{2.(1+Div\_photo\_sampl)}$ yes
13	*Ditto*	2.2.7.2	KJK	If SpectroBiasDiv (why is it BiasDiv rather than DivBias?) is set to 0 the sampling frequency will be infinite! What actually happens? Presumably setting Channel_S1 to 0 selects Channel 0 of LIA_S1 etc?	ditto
14	*Ditto*	2.2.7.3	KJK	Data modes 05 and 06 are reversed with respect to section 2.2.6.7.1	Ok 05= acquisition S-LW ; 06= acquisition S-SW
15	*ditto*	2.2.8.1	KJK	Step 1: to set the Photo Bias Frequency the parameter is PhotoMClkDiv Step 2: to set the Photo Sampling Frequency the parameter id PhotoBiasDiv (or PhotoDivBias) Step 3: There are 448 cases for each BDA Step 25: Why has value EF been chosen? Step 30: There are 448 cases for each BDA Step 38: Why has value EF been chosen?	OK OK OK Put the bias output to 0V OK Put the bias output to 0V
16	*Ditto*	2.2.8.4.1	KJK	Step 1: Ther is no such command Step 1: Ther is no such command	Yes they is StartFrame

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17	*Ditto*	2.2.15	KJK	There are parameters that are missing compared to previous version of the ICD, such as DAQ and LIA voltage supplies. Is this deliberate or are they to be found somewhere else?	DAQ and LIA supply voltages are no more routed through the SCU (using the now removed DISTRIB module). Those parameters are transmitted as binary flag by the DCU (see §2.2.5.6: PWR_STATUS)
18	*Ditto*	2.3.5.3.1.	KJK	The table shows a Data Structure length of 294 for frames of Photometer Full Array. There are 288 detector channels to be sampled (see table 2.3.5.3.2). There is one word at the end of the Data Structure containing the ADC Status. What are the other 5 words? Similarly the other Frame lengths are 5 words longer than necessary - or does the table give the total length of the frame rather than the length of the Data Structure?	The last column corresponds to the total length of the frame. Table column heading has been corrected

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19	*Ditto*	2.3.5.3.2	KJK	It is not clear in which order the pixels are stored in the data frame. Can I assume that the pixels are stored in the order reading across each row (CH1/LIA_P1, CH16/LIA_P2 .....) for each row in turn, starting at the top? Is it true that the first 144 data in this table correspond to the Photometer SW array, the next 96 data correspond to the MW Array and the final 48 data correspond to the LW array? And this is the order in which they will appear in Frame IDs 2, 3, and 4? Is the arrangement similar for the spectrometer table?	The tables (for photometer and spectrometer modes) give the order the analog channels are temporally multiplexed for each ADC. The order the pixels are stored in the data frame is obtained be assuming ADC 1 to ADC 6 interleaved by the FPGA. Then the table is to be read line by line. According to the SPIRE block diagram (from John) the BDA channel to DRCU board cross reference is: - PSW 1 to 144 : J5/J6 = LIA_P1 J7/J8 = LIA_P2 J9/J10 = LIA_P3 J11/J12 = LIA_P4 J13 = LIA_P5 - PLW 1 to 48 : J14 = LIA_P5 J15/J16 = LIA_P6 - PMW 1 to 96 : J17/J18 = LIA_P7 J19/J20 = LIA_P8 J21/J22 = LIA_P9 - SSW 1 to 48 : J23/J24 = LIA_S1 J25/J26 = LIA_S2 - SLW 1 to 24 J27/J28 = LIA_S3 - T/C : J22 = LIA_P9 To get an answer to the second part of your question please refer to the extract of the ICD. Tables are now in colours each one corresponding to a wavelength.

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20	*Ditto*	2.3.5.3.4	KJK	I believe frame type T4 contains the 32 bit time reference of the crossing, rather than the delta time. Can you confirm this? I would have expected Frame Type T7 to contain similar data to type T6 (i.e. jiggle position and error signal) Again the table seesm to give the Total Frame Length rather than the Data Structure length. Please clarify.	See proposal for chapter update according to D.FERRAND document MCU/DCU Command Telemetry (20/09/2002) Yes. Column heading modified to Frame length
21	*Ditto*	2.3.5.3.5	KJK	Why is the Frame T10 of length 30. This implies only 25 hsk parameters, but my reading of section 2.2.14 indicates more parameters are available. Please put a table of which parameters go where in the Frame.	DRCU spec. (DRCU req 79) specifies a list of 24 parameters. Then the length of the frame is given by: 1 wd for length + 1 wd for frame ID + 24wds for data + wd 1 for Data Status + 2wds for frame time + 1 wd for check word = 30 wds **Action to SCU designers to give such list**

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22	*Ditto*	2.3.6	KJK	I have tried to understand the reference document but I think there is more information needed to allow someone to calculate the pseudo random sequence expected. We need to know which bits are being fed back into the register and whether they are being modified before being fed back. A table of the first few values for each LFSR would be useful to allow us to check our code. Please clarify whether all the data in a single frame has the same value or is a new value calculated for each data in the frame?	Yes such a table has to be given in the ICD. **Action on myself to prepare tables for DCU/MCU and SCU** No - a new value is calculated