



SPIRE Technical Note

Ref: SPIRE-RAL-NOT-001399

Issue: 1.0

Date: 07/10/02

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Consolidated Comments on DCRU Documents

Edited: B. Swinyard/E Sawyer

ID	Document	Section	Raised by	Comment	Response
GEN 1	All		EAC (PA)	There is no CIDL Configured Item Document/Drawing List. (ESA and SPIRE requirement).	
2	All		EAC (PA)	There are several TBW's or will insert XYZ here when ready throughout the set of documents.	
3	All		EAC (PA)	DCU Design document, purpose and scope of this document be TBW, should not still be undefined at this stage	
4	All		EAC (PA)	PA Plan is missing from this document list.	



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DRCU1	DRCU Spec. Doc. SAP-PRJ-000461 (Sap-SPIRE- CCA-25-00)	2.1	BMS	Figure 2.1a is scrambled Figure 2.1a has "OEP" outside the FPU – it should be inside	
2	<i>ditto</i>	DRCU-REQ-45	BMS	...and here's the rub! When does the filtering get specified?	
3	<i>ditto</i>	Fig 4.2-b	BMS	This figure does not accord with the power supplies specified elsewhere in the document (DRCU-REQ-43 and DRCU-REQ-99) and is therefore confusing – remove or replace.	
4	<i>Ditto</i> Also applies to DRCU/DPU I/F Doc	DRCU-REQ-79 (and maybe elsewhere)	BMS	Parameter names used here are not consistent with the interface specification. In the interface doc (...) it uses FPUTEMP# -here the temperatures have more meaningful names – use these please!	
5	<i>ditto</i> Also applies to DRCU/DPU I/F Doc	DRCU-REQ-83	BMS	Please define the SCUSTATUS word as soon as possible – it does not appear at all in the I/F parameter list although it can be requested by dedicated command! (cf. ICD section 2.2.14.3 and 2.2.15)	
6	<i>ditto</i>	DRCU-REQ-85 DRCU-REQ-86	BMS	Wrong document called up – should be AD24?	
7	<i>ditto</i>	DRCU-REQ-88	BMS	Number of steps for full range operation is over specified – PCAL requirement is for 256 steps – if it is convenient to have a single type of DAC then o.k. else it is unnecessary.	
8	<i>ditto</i>	4.6.1	BMS/JD	Post regulation is shown for LIA supplies but not for DAQ/Bias supplies. Where does this happen?	
9	<i>ditto</i>	4.7.3	BMS	Can we have an extra requirement that the outputs of all FPGA controlled supplies (heaters; mechanism drives etc) are kept low during initialisation and are kept low until commanded otherwise.	



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ICD 1	DRCU ICD SPIRE-SAP-PRJ - 000451 (Sap-SPIRE- CCA-075-02)	5.4.3.2.1	DKG	Include jumper connections from pins 1 to 21; 2 to 22, 20 to 30; 4 to 24; 5 to 25; 3 to 6 of J29 and also J30 to allow for robustness in the SMEC Launch Latch drives.	



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DCU1	DCU Design Description SAp-SPIRE-FP-0063-02	3.2	BMS	What does this table mean? It is not complete.	
2	<i>ditto</i>	Whole doc.	BMS	Circuit diagrams are unreadable (e.g. Picture 4-8)	
3	<i>ditto</i>	4.1.3.1 4.1.6.1	BMS	I believe the offset in the first part of the picture comes from the JFETs? Please identify the source of the offset is the text or on the picture.	
4	<i>ditto</i>	4.1.3.2 4.1.3.3 4.1.6.2 4.1.6.3	BMS	Can we have the transfer functions of the filters in tabular or polynomial form please. Then we can use them in the instrument models.	
5	<i>ditto</i>	4.1.8.1	BMS	The description is a bit hard to follow! What is the final relationship between DATA and the amplitude of the bias that is actually output from the circuit? Is the statement about the resistors associated with the absence of the redundant cards from QM1 or does it represent a design option?	
6	<i>ditto</i>	4.1.8.1 4.1.11	BMS	There is no description of how the phase of the demodulation signal is altered for each BDA module? I hope this is implemented!	
7	<i>ditto</i>	4.1.12.1	BMS	Is FRAME=0 equivalent to continuous output of frames as specified in the ICD? Do both FRAME and START have to be high for data to be output?	
8	<i>ditto</i>	4.1.12.3 (Page 61)	BMS	Is an average of two values at all useful? Why isn't it 4 values as in the photometer?	
9	<i>ditto</i>	4.1.12.5	BMS	I think I understand how it works but it isn't completely obvious from this section! Just a leettle more explanation?	
10	<i>ditto</i>	4.1.12.7	BMS	Do 1 and 2 represent design options to be decided upon?	



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SCU1	SCU Design Description SEDI/SCU/MM /2002-1	1.1.3	BMS	We don't seem to have a copy of AD5? SEDI-SPIRE-OG-0001-02	
2	<i>ditto</i>	2.1	BMS	Block diagram shows "AC Modulation(x4)" – why is this when there is only one AC temperature channel?	
3	<i>ditto</i>	2.2 3.1 3.2	BMS	We would like some clarification of the operation of the acquisition sequencer and the data frame transfer: i) Which takes priority – the Acquisition Sequencer or the Get Parameter request? We wish to have the data in the frames at even sampling rates – therefore we would wish the Acquisition Sequencer to have priority. A timing diagram would be useful ii) Does the FPGA assemble a complete data then transfer it, or does it transfer the payload piecewise?	
4	<i>ditto</i>	3.2.1.1	BMS	Similar comment – Data Frame and Packet used interchangeably – please use Data Frame as packet means something else to the DPU.	
5	<i>ditto</i>	4.1.1 4.2.1 4.3.1	BMS	Maximum lead resistances are specified in the DRCU Specification document and the Harness Definition Document. These should be used to specify the design?	
6	<i>ditto</i>	4.1.4.5 4.2.4.4	BMS	Does this test mean that the effect of the lead resistance can be ignored? The lead resistance does not seem to be included in the simulation – what is the dissipation going to be in the cryoharness?	
7	<i>ditto</i>	4.2.4.1	BMS	Check with Lionel Duband whether 4pW is significant in terms of the operation of the heat switch sorption pump.	
8	<i>ditto</i>	4.3.1	BMS	The Spec Doc (AD1) specifies 6 kΩ for the heater resistance	



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9	<i>ditto</i>	4.4.1.2 4.4.1.3	BMS	This is an incorrect description of the SCAL sources – the Spec. Doc (AD1 v0.92) has the correct specification (2% and 4% sources) with both types of source having the specification as for “SCALP”. The “SCALF” drive is not required, we need 2x the “SCALP” design.	
10	<i>ditto</i>	4.8	BMS	Is this power supply monitoring associated with the SCU staus word?	
11	<i>ditto</i>	5.2.1	BMS	How does this work? Analogue or digital?	
12	<i>ditto</i>	6.1	BMS	The notes on the next page make explicit that all output voltages and currents are held low in the reset state. Maybe make this clear in this section? Also is it really true that the SCU is “stateless” when it leaves reset? I hope that the outputs are definitively held low until commanded otherwise?	
13	<i>ditto</i>	6.2	BMS	Its not clear how the sampling frequency is set – FRAMECONF? It is reasonably urgent that the SCUSTATUS word is defined as this will be used for error detection in flight and we need to get on with the FDIR.	
14	<i>ditto</i>	7.1	BMS	Read DRCU-REQ-89 in the latest version of AD1 v0.92 Both SCAL devices are four wire to allow remote sensing of voltage and therefore current stabilisation?	
15	<i>ditto</i>	4.4	PH	Description of SCAL out of date, flood and point sources no longer used	



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DPU-ICD 1	<i>DRCU to DPU ICD Sap-SPIRE-CCA-076-02</i>	General comment	RCI at IFSI	One very important comment is that, as far as we know, the DRCU-DPU ICD is the one we wrote (SPIRE-IFS-PRJ-000650 of 2/4/2001). We always said that we will discuss and include in that document the DRCU people comments, but the need of a single document is to avoid ambiguities and unnecessary efforts (i.e. we are the custodian of the ICD).	
2	<i>ditto</i>	2.1.1	RCI	DRCU subsystems, if addressed individually reply with a response word with the following Should read: DRCU subsystems, if addressed individually with SYN0=0 reply with a response word with the following ...	
3	<i>Ditto</i>	2.4.1.2	RCI	when a "Set_parameter" command is received the subsystem responds to the DPU by transferring a command acknowledge word (positive or negative) on the response line. Should read: When a "Set_parameter" command with SYN0=0 is received the subsystem responds to the DPU by transferring a command acknowledge word (positive or negative) on the response line.	



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4	<i>Ditto</i>	2.1.5.1	RCI	The RES signal shall be modified on the rising edge of the CLK signal and being sampled by the DPU on the next falling edge of the CLK signal. Should read: The RES signal shall be modified on the falling edge of the CLK signal and being sampled by the DPU on the next rising edge of the CLK signal.	
5	<i>Ditto</i>	2.1.5.3	RCI	Delta T1 is missing in the max command rate formula. In any case the formula is very optimistic as the actual max rate (if SYN0=0) is around 500 commands per second.	
6	<i>Ditto</i>	2.2.5.2	KJK	Add / to SetGetPhotoJfetPwr and SetGetPhotoOffset In SetGetPhotoOffset the channel number can only be 0 to 31 (not 0 to 32), which presumably correspond to channel numbers 1 to 32 in table 2.2.6.4. Similarly for SetGetSpectroOffset.	
7	<i>Ditto</i>	2.2.5.3	KJK	SetGetSpectroHeaterPwr should be SetGetSpectroHeaterBias (to be consistent with Photo table)	
8	<i>Ditto</i>	2.2.6.1.4	KJK	Description for SetDemodPh should be 'Set the bolometer group demodulation phase shift'	
9	<i>Ditto</i>	2.2.6.1.6	KJK	Heading should be PhotoHeaterBias to be consistent with table 2.2.5.2.	



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10	<i>Ditto</i>	2.2.6.5.8	KJK	Description for GetSpLWJfetVSS should be 'Get S-LW JFET source voltage' Description for SetSpLWJfetVSS should be 'Set S-LW JFET source voltage'	
11	<i>Ditto</i>	2.2.6.7.1	KJK	I imply from the description of the science frames in section 2.3.5 that if bit 3 is set to 1 (test) then bits 2 to 0 may only be set to 0 or 4. What happens for other combinations?	
12	<i>Ditto</i>	2.2.7.1	KJK	If PhotoDivBias (why not BiasDiv - see 2.2.6.1.1?) is set to 0 the sampling frequency will be infinite! What actually happens? Presumably setting Channel_P1 to 0 selects Channel 1 of LIA_P1 etc?	
13	<i>Ditto</i>	2.2.7.2	KJK	If SpectroBiasDiv (why is it BiasDiv rather than DivBias?) is set to 0 the sampling frequency will be infinite! What actually happens? Presumably setting Channel_S1 to 0 selects Channel 0 of LIA_S1 etc?	
14	<i>Ditto</i>	2.2.7.3	KJK	Data modes 05 and 06 are reversed with respect to section 2.2.6.7.1	



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15	<i>ditto</i>	2.2.8.1	KJK	<p>Step 1: to set the Photo Bias Frequency the parameter is PhotoMClkDiv</p> <p>Step 2: to set the Photo Sampling Frequency the parameter id PhotoBiasDiv (or PhotoDivBias)</p> <p>Step 3: There are 448 cases for each BDA</p> <p>Step 25: Why has value EF been chosen?</p> <p>Step 30: There are 448 cases for each BDA</p> <p>Step 38: Why has value EF been chosen?</p>	
16	<i>Ditto</i>	2.2.8.4.1	KJK	<p>Step 1: Ther is no such command</p> <p>Step 1: Ther is no such command</p>	
17	<i>Ditto</i>	2.2.15	KJK	There are parameters that are missing compared to previous version of the ICD, such as DAQ and LIA voltage supplies. Is this deliberate or are they to be found somewhere else?	
18	<i>Ditto</i>	2.3.5.3.1.	KJK	The table shows a Data Structure length of 294 for frames of Photometer Full Array. There are 288 detector channels to be sampled (see table 2.3.5.3.2). There is one word at the end of the Data Structure containing the ADC Status. What are the other 5 words? Similarly the other Frame lengths are 5 words longer than necessary - or does the table give the total length of the frame rather than the length of the Data Structure?	



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19	<i>Ditto</i>	2.3.5.3.2	KJK	<p>It is not clear in which order the pixels are stored in the data frame. Can I assume that the pixels are stored in the order reading across each row (CH1/LIA_P1, CH16/LIA_P2) for each row in turn, starting at the top?</p> <p>Is it true that the first 144 data in this table correspond to the Photometer SW array, the next 96 data correspond to the MW Array and the final 48 data correspond to the LW array? And this is the order in which they will appear in Frame IDs 2, 3, and 4?</p> <p>Is the arrangement similar for the spectrometer table?</p>	
20	<i>Ditto</i>	2.3.5.3.4	KJK	<p>I believe frame type T4 contains the 32 bit time reference of the crossing, rather than the delta time. Can you confirm this?</p> <p>I would have expected Frame Type T7 to contain similar data to type T6 (i.e. jiggle position and error signal)</p> <p>Again the table seems to give the Total Frame Length rather than the Data Structure length. Please clarify.</p>	



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21	<i>Ditto</i>	2.3.5.3.5	KJK	<p>Why is the Frame T10 of length 30. This implies only 25 hsk parameters, but my reading of section 2.2.14 indicates more parameters are available. Please put a table of which parameters go where in the Frame.</p>	
22	<i>Ditto</i>	2.3.6	KJK	<p>I have tried to understand the reference document but I think there is more information needed to allow someone to calculate the pseudo random sequence expected. We need to know which bits are being fed back into the register and whether they are being modified before being fed back.</p> <p>A table of the first few values for each LFSR would be useful to allow us to check our code.</p> <p>Please clarify whether all the data in a single frame has the same value or is a new value calculated for each data in the frame?</p>	