Herschel SPIRE	**CEA/SAp August 2002 Status and Progress Report**	DSM-DAPNIA SAp-FIRST-DR-0192-02 H0523 30/08/2002 Page 1/7

Management & System

Meetings	
28/08	SPIRE AIV internal meeting
30/08	SPIRE AIV internal meeting
Management act.	
Project control	➢ SPIRE master schedule updated. ➢ DCU EM QM1 detailed schedule. ➢ SPIRE FPU simulator detailed schedule update. ➢ Action list update. ➢ SPIRE reporting.
SAp / JPL	➢ F. Pinsard stay at Caltech : • 11/04 to 10/06: DAQ IF + board test • 24/06 to 12/07: BIAS board test • 29/07 to 15/08: LIA-P • 02/09 to 30/09: LIA-S test board + functional system test • 22/10 to 09/12: integration, functional test, performances test (tbc)
Cooler harness procurement	➢ STM & CQM cooler harness will be procured via Tekdata. Order will be placed as soon as Specification will be available from RAL.

Problem Areas	**Remedial Actions**
➢ Lack of agreement on the Grounding scheme approach could impact both DRCU design and delay.	➢ A dedicated review is going to be held in September.
➢ Potential risk on DRCU FM delivery: Grounding scheme issue prevents (among else) to send out the PSU call for tender.	➢ See DRCU workpackage section.
➢ 1 month delay on QM1 delivery mainly due to DCU development schedule slippage.	➢ None. Minor issue compared to the grounding scheme one.

Actions

Still Opened

Ref.	*Meeting*	*Actionnee*	*Due date*	*Action*
/	/	/	/	/

Closed

Ref.	*Meeting*	*Actionnee*	*Due date*	*Action*
/	/	/	/	/

Project Milestones

Main Delivery Milestones	*Resp.*	*Baseline*	*Current*
DRCU QM1 delivery to RAL	SAp	03/03/2003	04/04/03
FPU Simulator (version 1) delivery to RAL	SAp	03/03/2003	04/04/03
DRCU QM2 delivery to RAL	SAp	05/01/2004	05/01/2004
DRCU FM delivery to RAL	SAp	30/07/2004	30/07/2004

DRCU

DCU/QM1

Status

- **DAQ IF**
  - 2 test boards available at JPL
  - Test completed.
- **BIAS**
  - Board assembly achieved 29/05
  - Board test performed
- **LIA-P**
  - PCB fabrication achieved
  - Board test performed
- **LIA-S**
  - Board assembly achieved
- **Back-Planes**
  - Functional test backplane built.
  - Performance test backplane study started
- **Test plan**
  - Test plans: LIA-P, LIA-S, BIAS, DAQ-IF available in draft form.
  - Functional test plan: writing in progress.

Progress during the month

LIA-P test completed
LIA-S board assembly
Performance test backplane study

SCU/QM1

Status

- Heaters: prototype test achieved.
- Temperature sensors: test successful
- DPU I/F command and data I/F achieved.
- Analog port study achievement, software preliminary study in progress.
- Test board analog port study in progress.

- **SCU Documentation**
  - Draft Specification and preliminary (H/W & VHDL) design available.
  - Draft DPU/SCU ICD issued.
  - Test plan writing in progress

- **Functions**
  - Heater & temperature: implementation achieved
  - Calibrator: implementation achieved.
  - HSK: prototype board in fabrication, 2 people were added for a few month's to study it, the test software and a FPGA to convert different communication protocols.
  - SCU logic (pinout): study achieved
  - SCU logic (logic): study in finalisation

- **Boards**
  - Temperature: design PCB achieved. PCB layout in finalisation.
  - Cchkif: design PCB achieved. Board scheme finalisation.
  - Back plane: design PCB in finalisation.

Progress during the month

None due to vacation period

MCU I/F	**Status**
	➢ Design available at LAM & SAp ➢ MCU QM1 delivery to SAp confirmed 12/12/2002.
	Progress during the month
	/
PSU	**Status**
	➢ Separated power bench will be used for QM1 and QM2. ➢ Draft Specification available. ➢ Call for tender process stuck ➢ Contractual specification writing stuck ➢ Wait for S/C I/F to continue…See problem area.
	Progress during the month
	Little because of lack of I/F specification (grounding scheme).
DRCU Boxes	**Status**
	➢ Modeling completed. ➢ DCU board front panel design achieved ➢ **DCU Box.** • STM: detailed design achieved, fabrication in progress. • QM1: available at SAp. • QM2 & FM: I/F available. ➢ **FCU Box.** • STM: detailed design achieved, ready for fabrication. • QM1: Available at SAp. Thermal & dynamic studies in progress • QM2 & FM: I/F available
	Progress during the month
	DCU STM fabrication. DCU QM1 & FCU QM1 box fabrication achieved and delivered to SAp FCU box thermal & dynamic studies.

Test Equipments & others

LTU #1

Status

- Specifications: available (see documentation).
- Hardware & software architecture definition: near to completion.
- Software development: in progress.
- Software procurement: in progress
- Hardware procurement: in progress.
- Power bench: specification writing in progress.

Progress during the month

Soft development.

FPU Simulator #1

Status

- Specification available
- Electronics prototyping ongoing
- S/W evaluation on going
- Rack study in progress 80%.

- **PXI TRIG IO**
  - Hardware test achieved. Second fabrication achieved. VHDL update achieved. Functional test of the 2nd PXI achieved.

- **PXI BOLO SPIRE**
  - Electronic & design Achieved. VHDL soft studies. Test software specification writing achieved. Test board configuration study & realisation achieved. Functional test achieved.

- **PXI heater/Supply**
  - Design achieved. Manufacturing file □ritten. Test software specifications achieved. Test board configuration study & realization achieved. Onboard VHDL software study achieved.
  - PXI part fabrication started week 21 (sub-contractor SPCI & ERTE).

- **PXI Cernox DC & AC**
  - Analogue studies & design achieved. Complementary tests achieved. Manufacturing file writing achieved, Test software specifications achieved. Test board configuration study & realisation achieved.
  - Onboard VHDL software study over at 50%. PXI part fabrication started week 21 (sub-contractor SPCI & ERTE).
  - Functional test achieved

- **Software**
  - Supervision software specification writing. Output & input file configuration specification writing. PXI BOLO SPIRE, PXI HEATER / SUPPLY, PXI CERNOX, PXI TRIGGER IO test software development achieved. Supervision software on going

Progress during the month

PXI TRIG IO : functional test of the 2nd PXI TRIG IO achievement
PXI Heaters/supply test achievement
PXI CERNOX: functional test achievement
Supervision Software on going
Rack study

Part procurement	**Status**	
	➢ Declared components list update: edition 13 ➢ OP400 qualification review 12/02/02. Fabrication started. ➢ Harnesses connector estimation carried out. ➢ ATP update with Technologica	
	Progress during the month	
	None due to vacation period	
Harness	**Status**	
	➢ DCU test Harness at JPL configuration scheme available ➢ Connectors procurement on going	
	Progress during the month	
	Configuration of DCU test harness to be used at JPL Request for quotation.	
Containers	**Status**	
	➢ Specification available.	
	Progress during the month	
	None	
AIV	**Status**	
	➢ DRCU development tree available (last version 30/11/2001) ➢ DCU Board Test plan writing in progress. ➢ DRCU AIV plan in progress.	
	Progress during the month	
	DRCU AIV plan writing.	
PA/QA	**Status**	
	➢ DML and DPL draft available. ➢ Reference documentation list update on going	
	Progress during the month	
	Updating of the reference document list. Building of Requirement Cross verification table. Non conformity management	

Problem Areas	Remedial Actions
/	➢ /

Milestones		Status
DCU EM QM1 delivery to SAp from JPL	06/11/2002	Delayed by 1 month
DRCU QM1 harnesses need date	09/12/2002	On schedule
LTU DRCU available	09/12/2002	On schedule
SPIRE FPU simulator #1 need date delivery to SAp	06/11/2002	Delayed by 1 month
Detector test cryostat delivery to SAp by JPL	25/11/2002	On schedule
MCU QM1 + simulator need date delivery to SAp	10/12/2002	On schedule
SCU QM1 delivery by SEDI need date	24/01/2003	On schedule
DRCU QM1 delivery to RAL	**03/03/2003**	**Delayed by 1 month**
SPIRE FPU simulator #2 need date	28/07/2003	On schedule
SCU QM2 need date	27/08/2003	On schedule
MCU QM2 delivery to SAp need date	27/08/2003	On schedule
DRCU QM2 delivery to RAL	**05/01/2004**	**On schedule**
MCU FM delivery to SAp need date	26/04/2004	On schedule
SCU FM need date	05/05/2004	On schedule
DRCU FM ready for delivery to RAL	**30/07/2004**	**On schedule**

Documentation progress this month		
Title	**Reference**	**Progress**
Evaluation report for test plan of DCU boards	SAp-SPIRE-JF-0079-02	Achieved
DRCU AIV Plan	SAp-SPIRE-HT-0082-02	Draft

Documentation List		
Title	**Reference**	**Version, date**
Reference documentation		
➢ SPIRE Instrument Development Plan IIDR	/	Issue 1.1 12/4/2001 IIDR
➢ SPIRE Major Milestone List issue 1.3 IIDR	SPIRE-RAL-PRJ-000455	Issue 1.3
➢ SPIRE Instrument Requirements	34	Issue 1.0 23/11/00
➢ Cryo-cooler Control Specification	/	/
➢ Calibrator SSSD: SCAL ➢ Calibrator SSSD : PCAL	HSO-CDF-SP-001 HSO-CDF-SP-003	Issue 1.0 10/9/2001 Issue 1.0 11/9/2001
➢ Detector SSSD	/	Issue 3.1 – draft
➢ Shutter SSSD	Not yet	/
➢ Instrument Interface Document part A	SCI-PT-IIDA-04624	3.0 01/07/2002
➢ Instrument Interface Document part B SPIRE	SCI-PT-IIDB/SPIRE-02124	2.0, 31/07/2001
➢ SPIRE configurable document tree	SPIRE-RAL-PRJ-00033	3.1 03/05/2001
➢ SPIRE product tree	SPIRE-RAL-PRJ-00455	1.0 09/11/1999
➢ SPIRE instrument development plan	SPIRE-RAL-PRJ-0035	1.0 20/05/2000
➢ SPIRE management plan	SPIRE-RAL-PRJ-00029	01/01/2001
➢ SPIRE Data ICD	SPIRE-RAL-DOC-001078	1.0 draft1 15/01/2002
➢ SPIRE instrument AIV plan	SPIRE-RAL-PRJ-000410	2.1 29/03/2001
➢ SPIRE harness definition	SPIRE-RAL-PRJ-000608	1.0 08/07/2002
Management		
➢ Management plan for the Herschel project.	SAp-FIRST-JLA-0038-01	3.0 23/11/2001
➢ Actions list	SAp-FIRST-DR-0050-01	
➢ DRCU & WIH Development Plan	SAp-SPIRE-JLA-0047-01	3.0 27/11/2001
➢ SPIRE product tree	SAp-FIRST-DR-0071-02	1.2
➢ WBS Herschel	SAP-FIRST-DR-0043-01	2.1
➢ WBS SPIRE	SAP-FIRST-DR-0045-01	2.1
➢ SPIRE master schedule	SAp-SPIRE-DR-0053-02	3.2 30/08/2002
➢ DCU EM QM1 at JPL detailed schedule	SAP-FIRST-DR-0050-01	4.7 30/08/2002
➢ SPIRE FPU simulator detailed schedule	SIG-FIRST-PdA-0052-01	12.0 30/08/2002
➢ SCU QM1 detailed schedule	SEI-SPIRE-MM-0049-01	11 30/08/2002
➢ LTU & power bench detailed schedule	SAp-FIRST-DR-0069-02	2.9 30/08/2002
DRCU		
➢ DRCU Specifications document	SAp-SPIRE-Cca-0025-00	Issue 0.92 26/06/2002
➢ DRCU Development Tree	H0030	30/11/2001
➢ DRCU ICD	SAp-SPIRE-Cca-0075-02	0.7 26/06/2002
➢ DRCU DPU ICD	SAp-SPIRE-Cca-0076-02	0.7 26/06/2002
➢ DCU design document	SAp-SPIRE-FP-0063-02	0.2 05/07/2002
➢ Test plan DAQ IF	SAp-SPIRE-FP-0067-02	0.1 draft
➢ Test plan BIAS	SAp-SPIRE-FP-0066-02	0.1 draft
➢ Test plan LIA P	SAp-SPIRE-FP-0064-02	0.1 draft
➢ Test plan LIA S	SAp-SPIRE-FP-0065-02	0.1 draft
➢ SPIRE test configuration,	SAp-SPIRE-LD-0015-01	3.0 08/2001
➢ FPU simulator specifications for DCU / SCU test	SIG-SPIRE-PdA-0030-01	19/03/2001
➢ SPIRE LTU specifications	SAp-SPIRE-FD-0071-02	1.0 22/04/2002
➢ DRCU AIV Plan	SAp-SPIRE-HT-0082-02	draft
QA		
➢ Standard product assurance plan	SAp-GERES-Flo-436-00	1.0 09/11/2000
➢ SPIRE liste des documents à produire	SAp-SPIRE-Flo-0028-00	0.2 15/12/2000
➢ Organisation de la gestion documentaire sur Herschel au SAp	SAp-FIRST-DR-0053-01	1.1 06/12/2001
➢ Gestion des documents sur la base Herschel	SAp-FIRST-DR-0072-02	1.3 15/04/2002
➢ Procédures de contrôle projet sur Herschel	SAp-FIRST-DR-0125-02	1.2 13/05/2002
➢ DRCU FMECA Report		Issue 1.0 25/10/2001
➢ Analyse de fiabilité du DRCU	SAp-SPIRE-Flo-0039-01	21/08/2001
➢ DRCU processor board PA specification	SAp-SPIRE-Flo-0020-00	10/01/2001
➢ Plan d'action de AP du projet Herschel	SAp-FIRST-Abx-0137-02	Issue 1.1 18/06/2002
➢ Evaluation report for test plan of DCU boards	SAp-SPIRE-JF-0079-02	Issue 1.0