Herschel SPIRE

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Control Unit (SCU)

This document describes the SCU, one of the 3 sub-units of the Herschel/SPIRE/DRCU electronic subsystem.

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1 Introduction

This section gives an overview of the Herschel/SPIRE/DRCU Subsystem Control Unit.

1.1 Applicable documents

1.1.1 Specification documents

- AD 1 : « DRCU Subsystem Specification », Sap-SPIRE-Cca-0025-00, V0.91 ;

1.1.2 Interface documents

- AD 2 : « DRCU Interface Control Document », Sap-SPIRE-Cca-0075-02, V0.6 ;
- AD 3 : « DPU Interface Control Document », SPIRE-IFS-PRJ-650, V1.0.

1.1.3 Technical documents

- AD 5 : « A Generic DPU Interface for SPIRE DRCU subsystems », SEDI-SPIRE-OG-0001-02, V0.4.
- AD 6 : « Note on temperature measurement using CERNOX probe for the SPIRE and PACS instruments », C. CARA - 28/06/01 ;

1.2 Overview

The Subsystem Control Unit (SCU) is an ancillary unit of the DRCU, in charge of various acquisition, control, support and monitoring functions, as specified in AD 1.

1.2.1 Acquisition and control functions

The SCU is in charge of the following low-level acquisition and control functions :

- Control and monitoring of the cryo-cooler heaters (recycling heater [SCU-FUNC-01], gas switch heater [SCU-FUNC-02] and FPU thermal strap [SCU-FUNC-03]) ;
- Control and monitoring of the photometer and spectrometer IR calibrators (PCAL, SCAL Point and SCAL Flood) [SCU-FUNC-04] ;
- Acquisition of the FPU thermal sensors (thermometry subsystem) [SCU-FUNC-05, -06].

1.2.2 Support and monitoring functions

The SCU is in charge of the following low-level support and monitoring functions :

- Logical On/Off control of some PSU secondary power supplies (DCU-LIA P/S, DCU-BIA P/S) [SCU-FUNC-13] ;
- SCU power supply monitoring [SCU-FUNC-07, -11] ;
- SCU and PSU electronics temperature monitoring [SCU-FUNC-07, -11] .

1.2.3 DPU interface functions

To support the above functions, the SCU decodes [SCU-FUNC-08] and responds [SCU-FUNC-11] to DPU commands, according to the DPU Cmd protocol. When in operation, it creates and produces a sequence of measurement Data Frames [SCU-FUNC-12], according to the DPU Data protocol. Each Data Frame carries the value of a relative Time Stamp, which is locally maintained in the SCU [SCU-FUNC-10].

2 Architecture

This section gives a general view of the SCU functions and behaviour.

2.1 Block diagram

The SCU block diagram is given in Figure 1 .

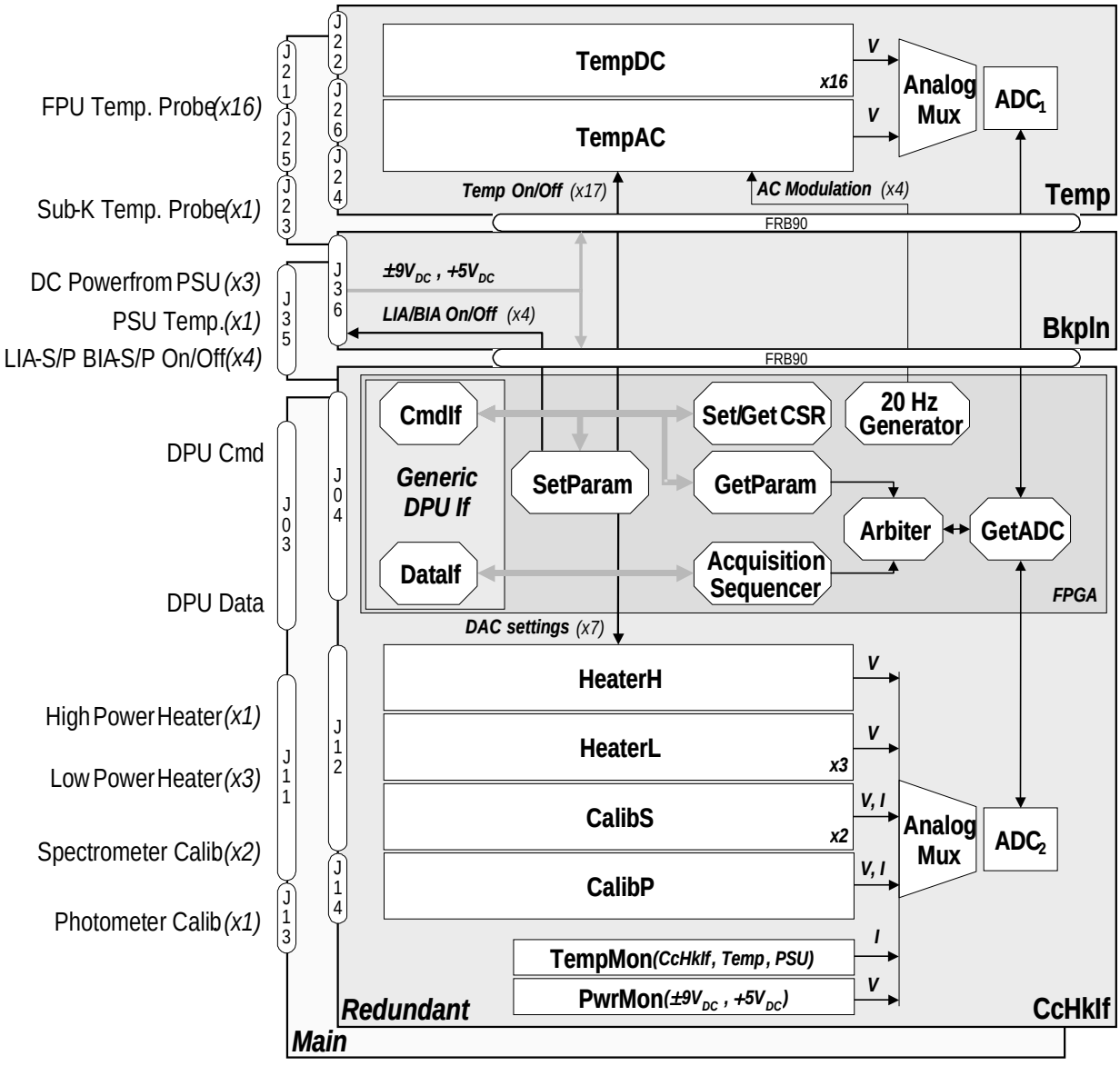


Figure 1 SCU block diagram

The independent single-channel analogue signal conditioning circuits –TempDC, TempAC, HeaterH, HeaterL, CalibS, CalibP, TempMon and PwrMon– are supervised by the SCU Subsystem Logic. This logic is installed in a Field Programmable Gate Array (FPGA) logic cicuit.

2.2 Behaviour

The SCU is a slave device running under full supervision of the DPU software. Once initialised, it responds to DPU-initiated commands issued on the *Cmd Interface*. These commands first install the required configuration, and then start SCU operation.

2.2.1 Data frame sequence

When in operation, the SCU *Acquisition Sequencer* regularly prepares a well-defined *Data Frame* and autonomously transfers it to the DPU over the *Data Interface*. The frequency and duration of this *Data Frame* sequence are adjustable by configuration. The *Data Frames* are individually time stamped with a local clock value, which is also under control of the DPU software.

2.2.2 Subsystem parameter access

Asynchronous commands can be issued by the DPU at any time on the *Cmd* interface, to update or request a SCU parameter value.

2.2.2.1 Parameter update

SCU write-able parameters are updated immediately when the corresponding DPU write command is received and accepted, independent of the activity of the *Acquisition Sequencer*.

2.2.2.2 Parameter request

SCU readable parameters are provided when the corresponding DPU read command is received and accepted. However, the response time depends on the current activity of the *Acquisition Sequencer* when the request is issued. The SCU subsystem logic interleaves the atomic parameter sampling operations corresponding to either cyclic acquisition or asynchronous requests.

3 Digital functions

This section describes the functions handled by the FPGA circuit.

3.1 Generic DPU Interface

The DPU interface uses an instance of a generic design considered for all three DRCU subsystems (DCU, MCU and SCU). The detailed description of the generic part is given elsewhere (AD 5). Only the main features of this generic block are recalled here, to introduce the description of the SCU-specific control modules.

The generic interface handles the low level serial port protocol of the DPU *Cmd* and *Data* transactions, and presents 2 simple word-oriented interfaces to the subsystem logic :

- On the Cmd side, the subsystem parameter interface provides controlled read/write access to the subsystem parameters, seen as 16-bit words located at specific locations in a 12-bit address space.
- On the Data side, the subsystem data interface is a 16-bit parallel word register on which the subsystem places the individual 16-bit data words of the Data Frame payload in sequence. The encapsulation and transmission of the Data Frame is handled by the generic interface. For each Data Frame, the subsystem logic has the responsibility to signal completion of the payload with a “Last Word” indication. The SCU implementation does not use the optional FIFO mechanism of the generic interface.

3.2 SCU Subsystem Logic

Once activated, the *SCU Subsystem Logic* manages several concurrent threads of control :

1. *Acquisition Sequencer* : Automatic periodic parameter measurement, and associated word-per-word Data Frame payload construction ;
2. *Get Parameter* : On-demand analogue parameter measurement, in response to an individual DPU read command.
3. *Get CSR* : On-demand read access to a Control and Status Register (CSR), in response to an individual DPU read command.
4. *Set Parameter/CSR* : On-demand update of an analogue parameter or CSR register, in response to an individual DPU write command.

Operations 1. and 2. require a fresh value of the corresponding parameters, and compete for access to the involved analogue channels. A hardware time scheduling mechanism ensures forward progress for both operations. Operations 3. and 4. do not interfere with 1. and are handled independently.

3.2.1.1 Acquisition Sequencer

When the SCU is started, the *Acquisition Sequencer* schedules a sequence of cyclic acquisitions, and triggers the corresponding *Data Frame* transfers to be produced over the DPU *Data Interface*. The interval between acquisitions and the number of acquisitions expected for a particular operational run are both configured by dedicated parameters.

For each acquisition, the *Acquisition Sequencer* loops over the analogue parameters that are expected in the *Data Frame* payload. Each of them is selected in turn, converted to digital form and presented to the *Subsystem Data* Interface for inclusion in the current packet.

4 Analogue functions

This section describes the analogue signal conditioning functions.

4.1 Cooler high power heater (HeaterH)

4.1.1 Specification

The following table recalls the requirement for the cooler high power heater [extracted from AD 1].

Type	Number	Heater Resistance	Lead resistance	Power	Max. Voltage	Interface type
Charcoal pump	1	402	TBD	0 to 500 mW	15V	4-wire

Table 1 HeaterH requirements

4.1.2 General description

The high power heater is a variable current source controlled by a digital to analogue converter. The system must develop a variable power dissipation in the [0 - 500 mW] range across the heater. With a 402 Ω heater resistance, the corresponding current range is [0 - 35.3 mA]. The corresponding [0 - 14.2 V] voltage across the heater is measured and made available to the DPU as part of the housekeeping parameters.

The DAC generates a [0 - 5V] voltage used to drive the current source. The current is equilibrated by the heater voltage feedback loop. This voltage is then used for the HSK measurement.

For proper operation at the required 14.2 V heater voltage, bipolar operation is required. A second feedback loop lets the heater voltage develop between the positive and negative power rails.

Two current limiting blocks protect the SCU power supplies against a potential heater short circuit.

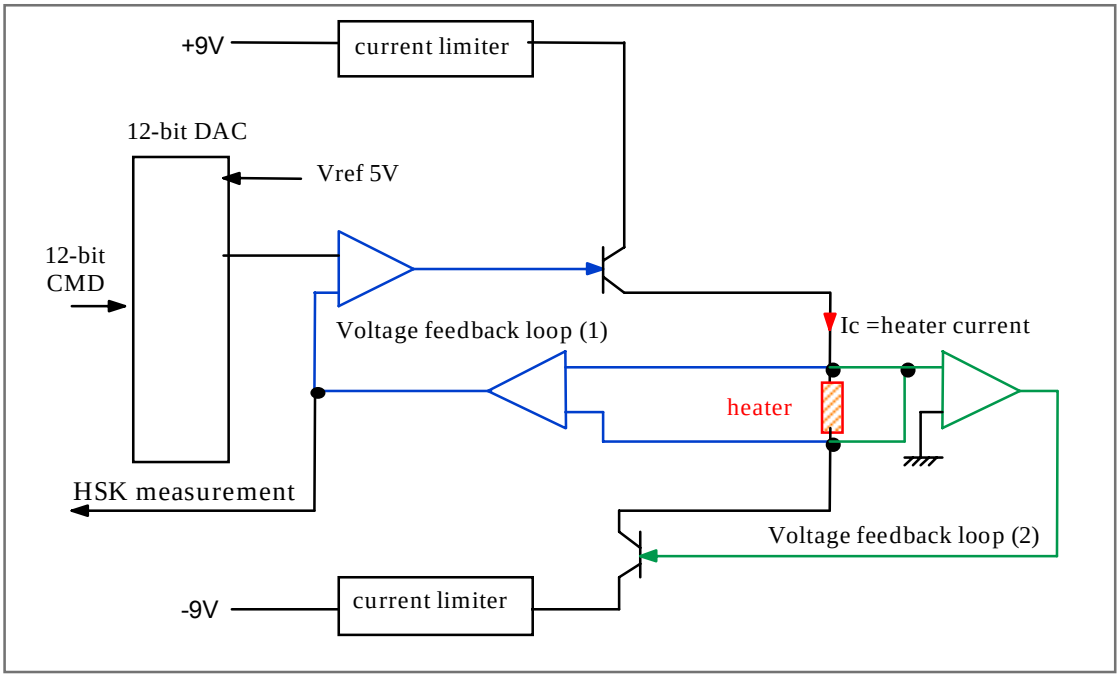


Figure 2 Schematic view of the HeaterH circuit

4.1.3 Simulation

The following simulations only cover the analogue part of the HeaterH circuit (assuming an ideal D/A converter).

4.1.3.1 Pheater = f(Ve)

The maximum heater power (0.5 W) is obtained for a 3.55 V DAC output voltage.

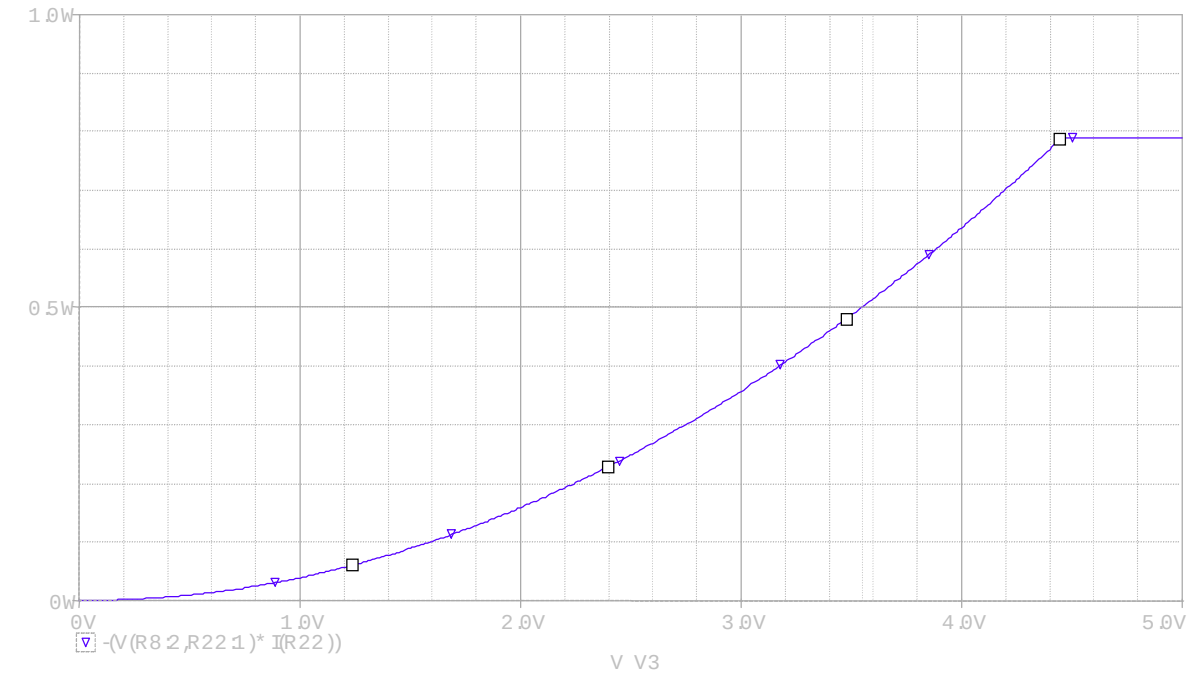


Figure 3 HeaterH simulation : Power variation

4.1.3.2 Ic(heater) = f(Ve)

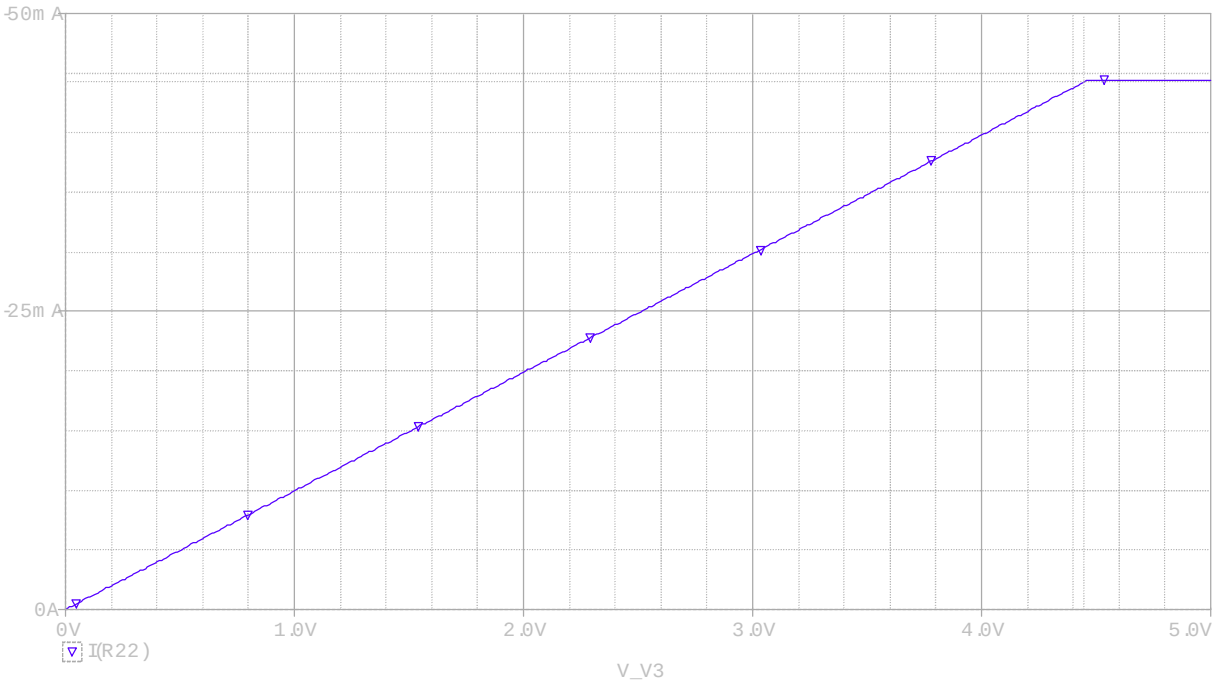


Figure 4 HeaterH simulation : Current variation

The transfer function is Ic(Heater) = 9,94 E^{-3} mA/V * Ve in the linear range.

4.1.3.3 Pheater = f(Vhsk)

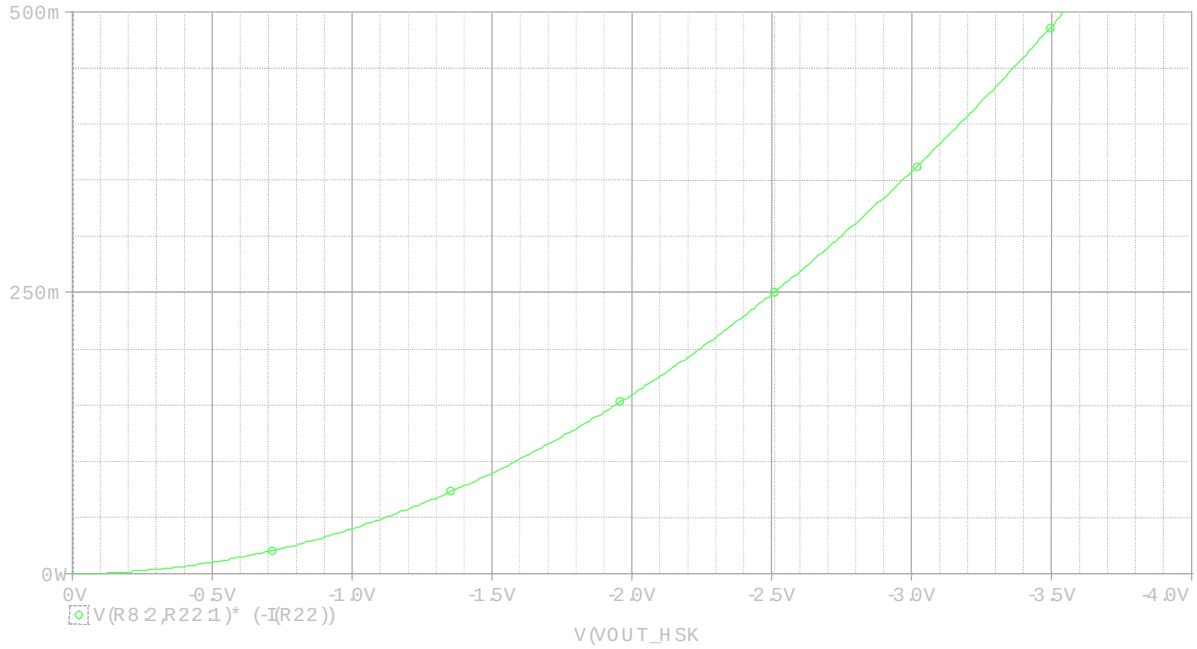


Figure 5 HeaterH simulation : Power dissipation vs HSK voltage

4.1.3.4 Residual current for Ve = 0V

For Ve = 0V, we obtain Ic = 466.4 pA.

4.1.4 Prototype test results

To validate the HeaterH electronic chain, we developed a prototype circuit with both the analogue and digital sections installed. The performance of this prototype was assessed at several temperatures (0°C, 25°C, 50°C). We verified the power supply rejection and the response to a DAC full swing adjustment step. We measured the circuit over a wide range of heater resistor values and checked the effect of a harness disconnect.

The performance of the analogue section at ambient temperature is :

Voltage Reference	DAC output voltage Ve(V)	Vheater (V)	Vhsk (V)	Ic (A)
0	0	20u	-67u	50n
0.5	0.49999	1.99943	0.49804	4.998575m
1	1.00004	4.00702	0.99804	10.01755m
1.5	1.4998	6.01479	1.4981	15.037m
2	1.9998	8.02342	1.9983	20.0585m
2.5	2.4998	10.0316	2.4985	25.079m
3	2.9995	12.03852	2.9983	30.0963m
3.5	3.4996	14.04678	3.4985	35.117m
4	3.9993	16.05384	3.9983	40.1346m
4.5	4.4994	16.57942	4.1293	41.448m
5	4.9996	16.57955	4.1293	41.448m

Table 2 HeaterH prototype : Measurements

As expected by simulation, we obtained the specified 500 mW power dissipation for a 3.5V DAC output voltage, and observed saturation at 690 mW. We measured a 50 nA leakage current, leading to a residual 1 pW dissipation in the heater.

4.1.4.1 Transfer function at 25°C

The transfer function at 25°C is as follows :

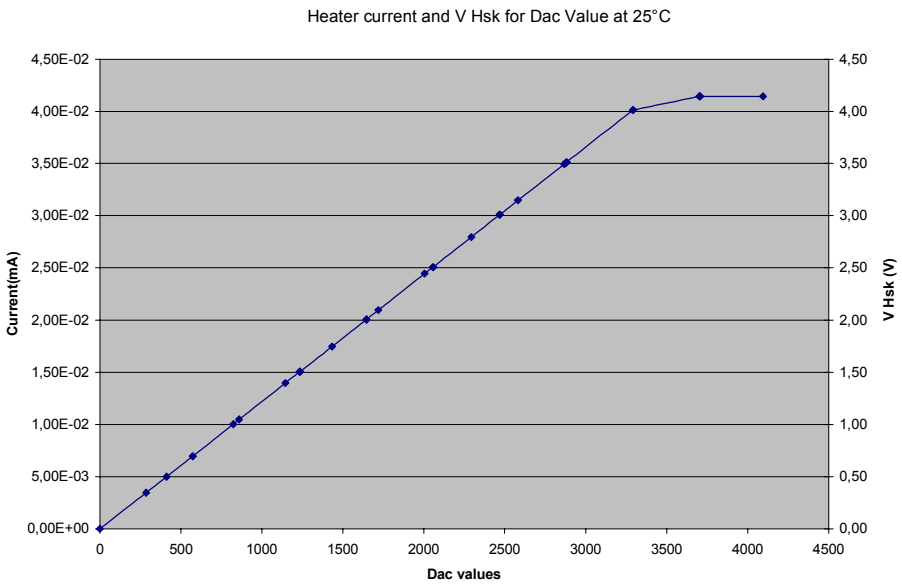


Figure 6 HeaterH prototype :Current variation

4.1.4.2 *Variation with temperature*

To evaluate the effect of temperature, we placed the analogue/digital electronic board in a thermal vacuum chamber and measured the heater current and HSK voltage at 0°C, 25°C and 50°C. The measurements were taken for several DAC settings with a nominal 402 Ω heater resistance.

The DAC output voltage dependence with temperature is as follows :

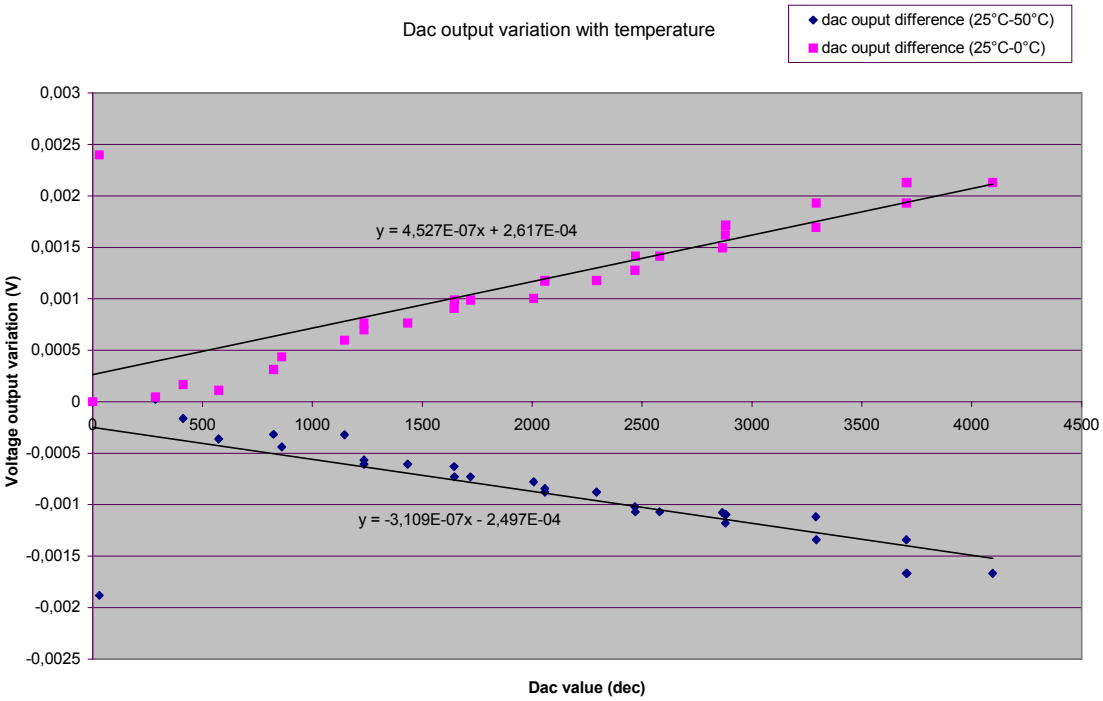


Figure 7 HeaterH prototype : DAC output voltage dependence with temperature

The DAC output voltage variation is linear with temperature. We find a similar variation on the HSK output, as shown below.

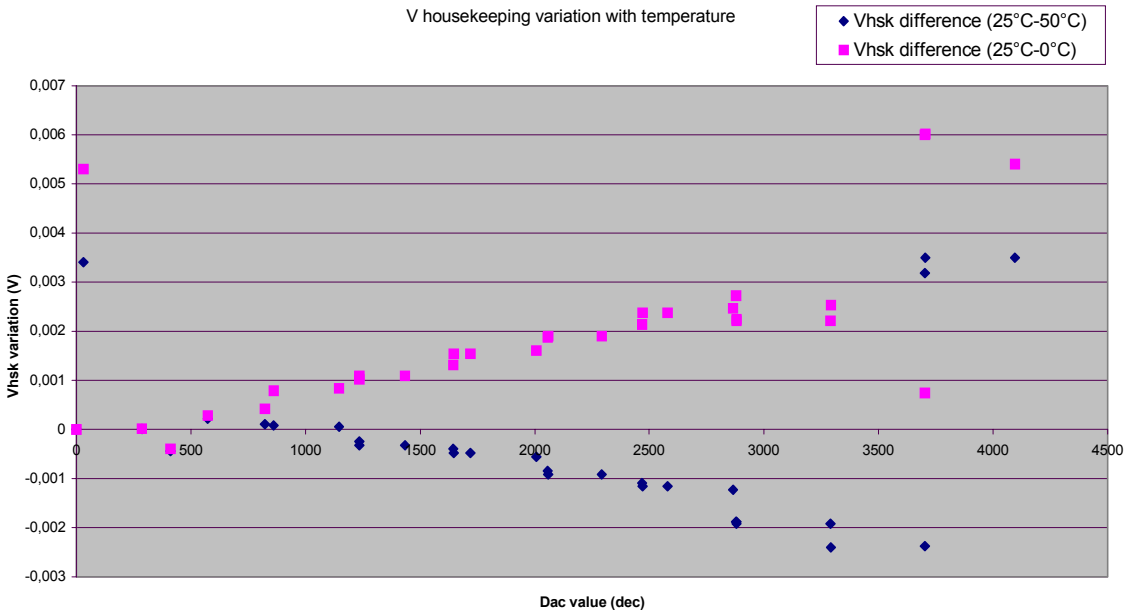


Figure 8 HeaterH prototype : HSK voltage dependence with temperature

The following figure shows the variation of current at 50°C and 0°C, as compared with the reference temperature (25°C).

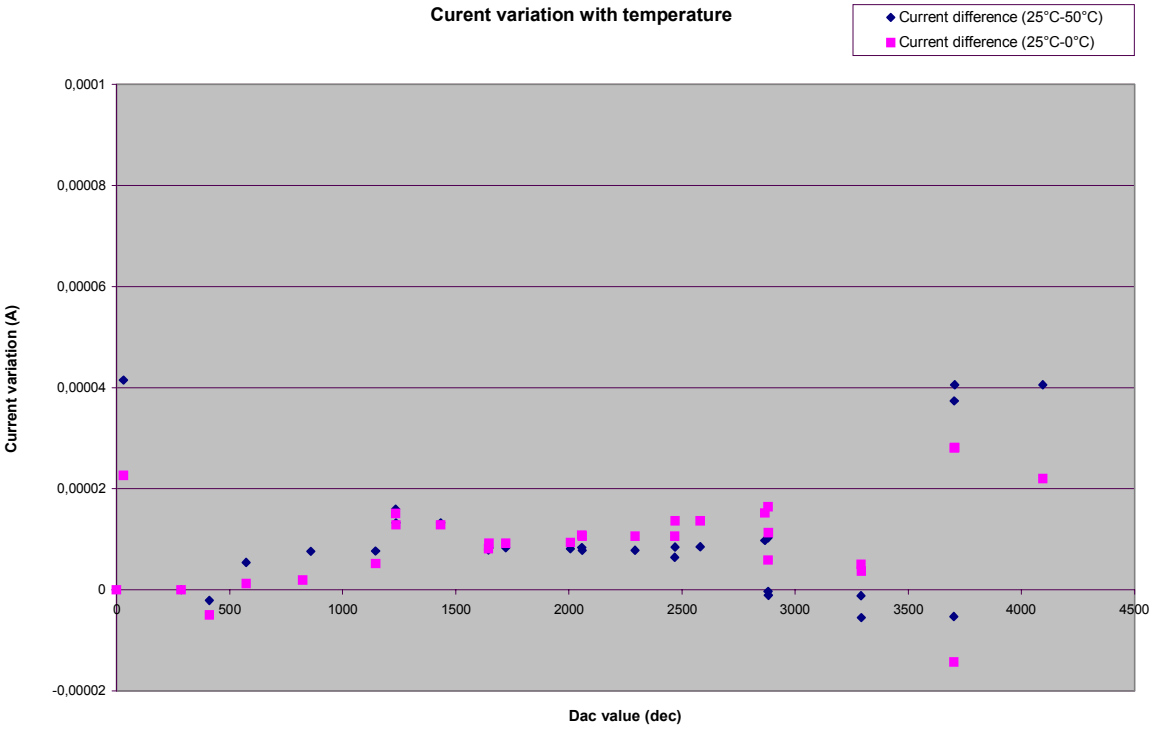


Figure 9 HeaterH prototype : Current dependence with temperature

The current dependence on temperature is not identical, but the total dispersion is less than 100 µA for a 50°C variation. The temperature stability of this design is sufficient for the precision required. If necessary, these systematic effects can be calibrated.

4.1.4.3 Power supply rejection

The power supply rejection is measured at 10% and 90% of the maximum DAC value, with a ±1 V perturbation added to the nominal 9V DC supply. The results are shown in the following tables.

DAC value	Power supply	Is	Relative error (%)	Vhsk	Vch
287 (dec)	Nominal 9V	0.00349925		0.34868	1.3997
	Nominal –1V = 8V	0.003501175	0.055	0.34887	1.40047
	Nominal +1V =10V	0.0034973	-0.055	0.34849	1.39892

Table 3 HeaterH prototype : Power supply rejection @DAC=287

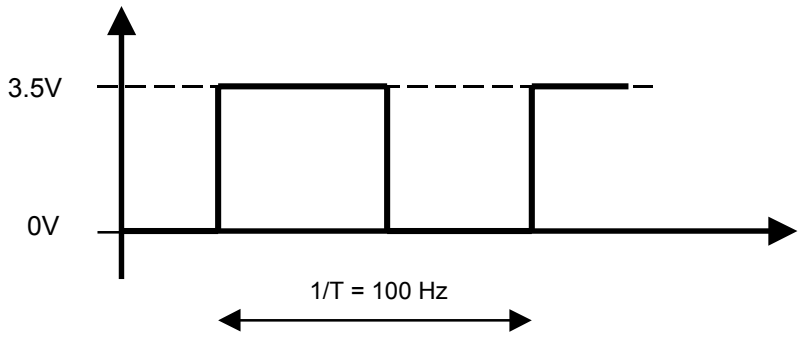
DAC value	Power supply	Is	Relative error (%)	Vhsk	Vch
2570(dec)	Nominal 9V	0.0314975		3.1379	12.599
	Nominal –1V = 8V	0.0314984	0.0028	3.138	12.59936
	Nominal +1V =10V	0.0314963	-0.004	3.1378	12.59852

Table 4 HeaterH prototype : Power supply rejection @DAC=2570

The variation of current in the heater is 0.1% maximum for 2 volts of power supply variation. The power rejection is 0.05%/Volts.

4.1.4.4 Frequency response to a full swing command step

To evaluate the frequency response of the analogue section, we generated a square signal (0 and Imax) at 100 Hz and observed the output voltage with a differential oscilloscope. The frequency response of the electronics is 300 Hz.



4.1.4.5 Variation of the heater resistance

We observed the effect of varying the heater resistance. Keeping the input DAC setting identical, the system parameters were measured for several heater resistance values, including the short and open

circuit conditions. We observed good stability on the actual heater voltage (Vheater) and the housekeeping output (Vhsk), showing the correctness of the voltage control loop and the absence of dependence on the resistance value.

DAC value	Rheater intended : actual	DAC output voltage	Vheater	Vhsk	Is (Vch/Rch)
3367 (dec)	0 Ω	3.4867	0	0.000311	-
	400 Ω : 399.3	3.48695	13.99687	3.4859	35 m
	500 Ω : 497	3.48695	13.9962	3.486	28.16 m
	1000Ω : 1001.3	3.48695	13.9963	3.486	13.97 m
	1500Ω : 1498.3	3.48695	13.99637	3.486	9.34 m
	2000Ω : 2004.4	3.48695	13.9964	3.486	6.98 m
	∞	3.48695	13.99648	3.486	0

Table 5 HeaterH prototype : Temperature variation @DAC=3367

The measured short circuit current limitation (Rheater = 0 Ω) occurs at 70 mA.

4.2 Cooler gas pump heaters (HeaterL)

4.2.1 Specification

The following table recalls the requirement for the cooler gas pump low power heaters [extracted from AD 1].

Type	Number	Heater Resistance	Lead resistance	Power	Max Voltage	Interface type
Gas pump	2	402	TBD	0 to 1mW	15V	4-wire

Table 6 Gas pump heater specification

4.2.2 General description

The gas pump low power heater is a variable current source controlled by a digital to analogue converter. The system must develop a variable power dissipation in the [0 - 1 mW] range across the heater. With a 402 Ω heater resistance, the corresponding current range is [0 – 1.5 mA]. The corresponding [0 - 634 mV] voltage across the heater is measured and made available to the DPU as part of the housekeeping parameters.

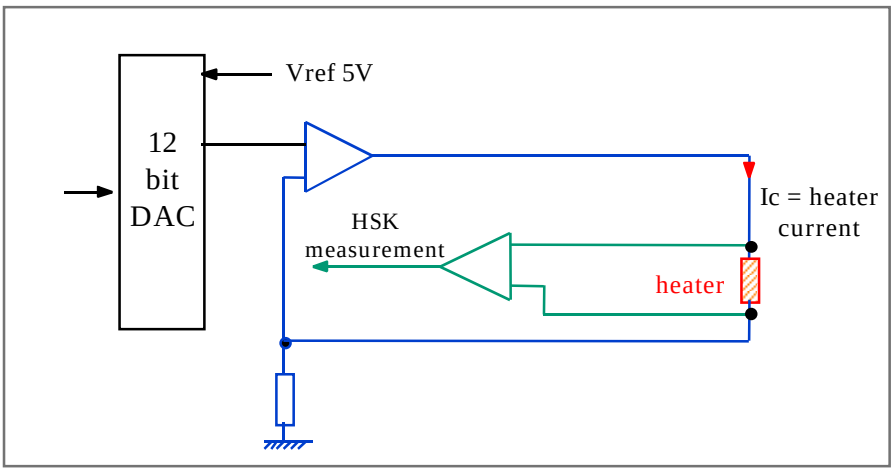


Figure 10 HeaterL circuit : Design principle

The DAC generates a [0 - 5V] voltage used to drive the current source. The current is equilibrated by the heater voltage feedback loop. This voltage is then used for the HSK measurement. The electronic circuit is protected against a potential heater short circuit by a series resistor.

4.2.3 Simulation

The following graphs show simulations for the power and current transfer, as function of the DAC output voltage Ve.

4.2.3.1 Pheater = f(Ve)

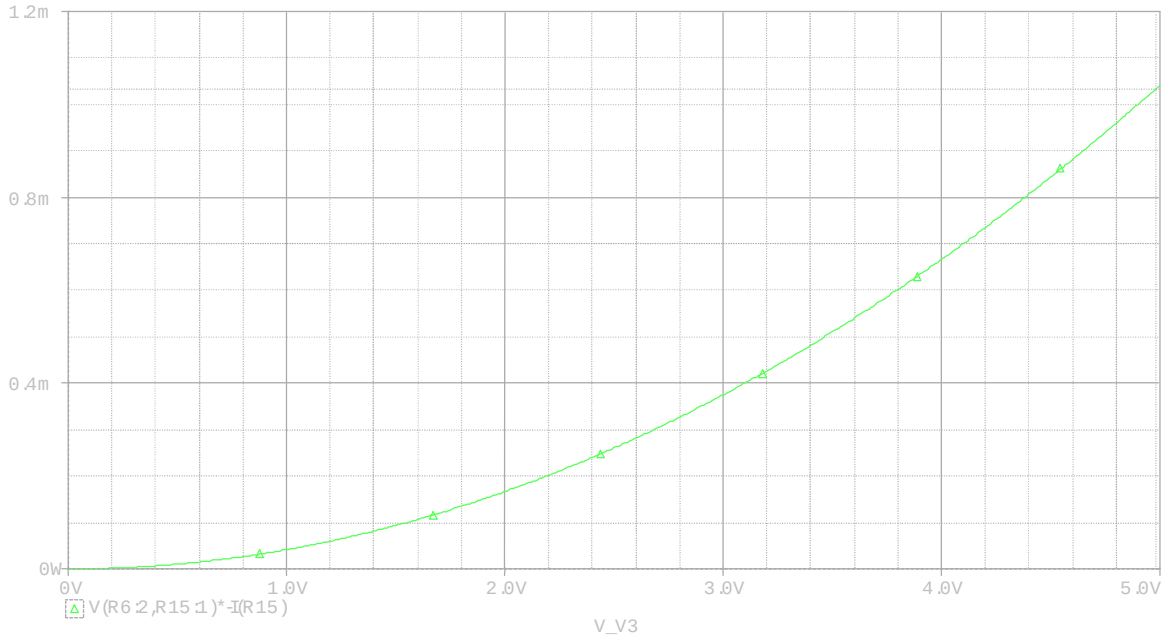


Figure 11 HeaterL simulation : Power variation

4.2.3.2 Iheater = f(Ve)

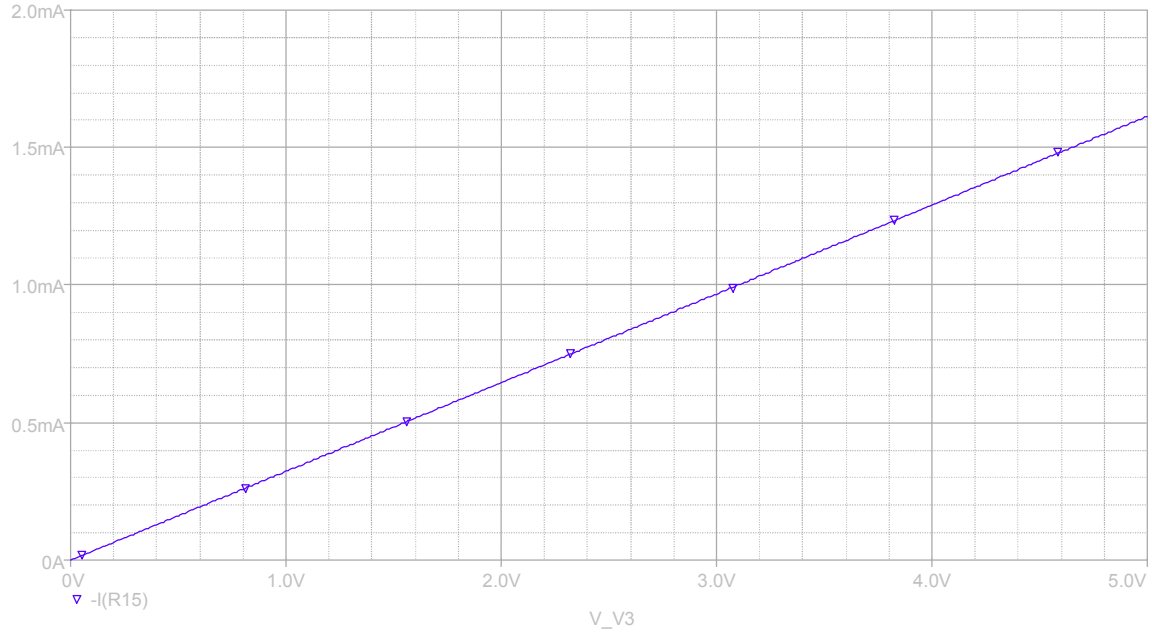


Figure 12 HeaterL simulation : Current variation

The transfer function is Iheater = 323 µA/V * Ve in the linear range. The simulated current limiting saturation occurs at 1.6 mA.

4.2.3.3 Pheater = f(Vhsk)

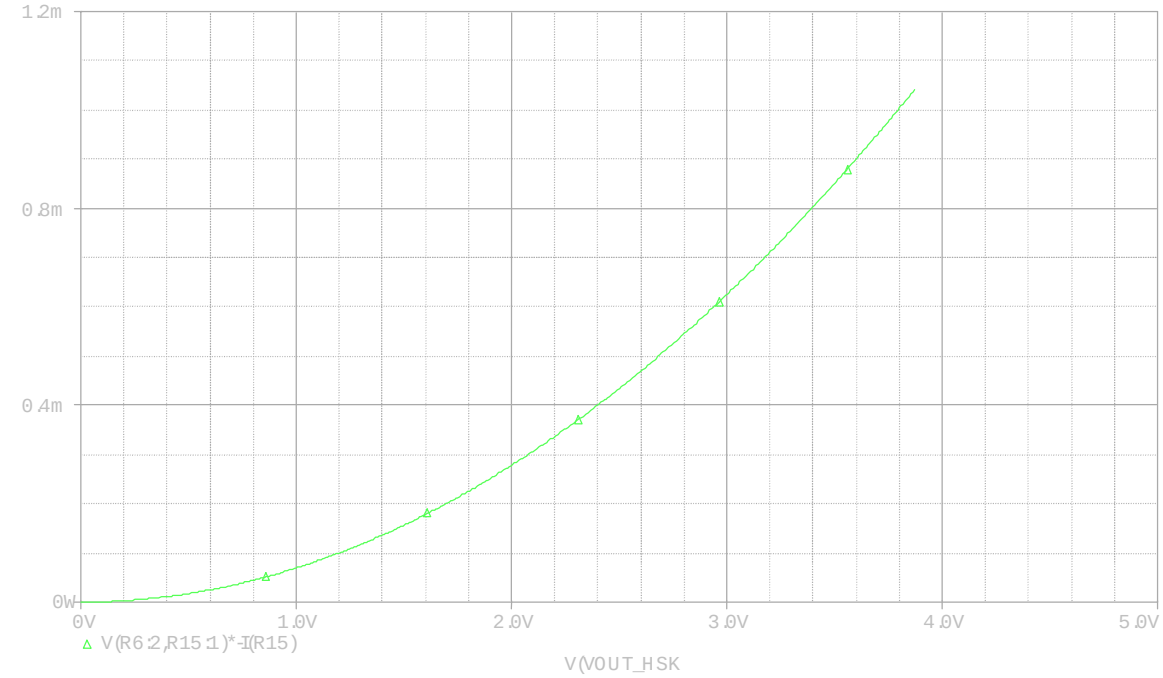


Figure 13 HeaterL simulation : Power dissipation vs HSK voltage

4.2.4 Prototype test result

The performance of the analogue section at ambient temperature is :

Ve	Vch	Vhsk	Is
0	40u	40u	100n
0.5	64.1837m	383.1m	160.459u
1	128.409m	766.19m	321u
1.5	192.634m	1149.27m	481.585u
2	256.89m	1532.5m	642.22u
2.5	321.134m	1915.7m	802.835u
3	385.336m	2298.7m	963.34u
3.5	449.585m	2681.9m	1.124m
4	513.79m	3064.8m	1.284m
4.5	578.04m	3448.1m	1.445m
5	642.293m	3831.3m	1.6m

Table 7 Gas pump heater prototype : Measurements

The prototype performs as expected by simulation.

4.2.4.1 Transfer function at 25°C

The corresponding linear transfer functions are as follows :

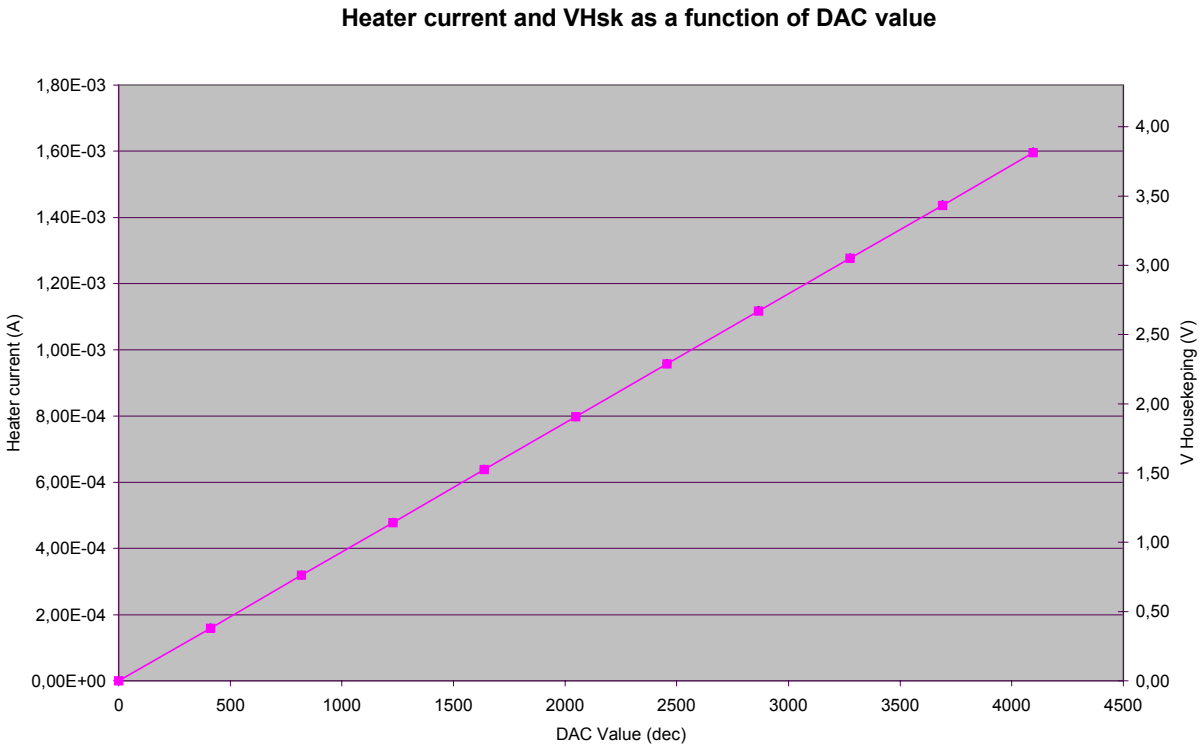


Figure 14 Gas pump heater prototype : Current variation

Current (A) = 3.902 E^{-7} * DAC_value –1.023 E^{-7}

$$Hsk\ (V) = 2386. * Current + 5.01\ E^{-4}$$

$$Hsk\ (V) = 9.311\ E^{-4} * Dac\_value - 2{,}566\ E^{-4}$$

The leakage current is 100 nA, corresponding to a minimum dissipation power of 4 pW in the heater.

4.2.4.2 Variation with temperature

The current drift is linear and reaches 2.5 μA at 50°C for the maximum current 1.6 mA (0.0018%/°C). The variation essentially comes from the DAC temperature drift.

Vhsk drifts in the same proportion. If required, the systematic current drift may be corrected from the HSK measurement.

4.2.4.3 Power supply rejection

The power supply rejection is measured at 10% and 90% of the maximum DAC value, with a ±1 V perturbation added to the nominal 9V DC supply. The results are shown in the following tables.

DAC word	Power Supply (V)	Ve (V)	Vch (V)	Vhsk (V)	Is (A)	Relative error (%)
196h	Nominal 9	0.49817	63.96m	0.38178	159.9u	----------
	8	0.49815	63.96m	0.38178	159.9u	0
	10	0.49818	63.965m	0.38178	159.9125u	0.0078

Table 8 Gas pump heater prototype : Power supply rejection @DAC=$196

DAC word	Power Supply (V)	Ve (V)	Vch (V)	Vhsk (V)	Is (A)	Relative error (%)
E58h	9	4.4839	0.576028	3.4363	1.44007m	----------
	8	4.4838	0.576003	3.4361	1.44m	-0.0048
	10	4.4841	0.57604	3.4364	1.4401m	0.002

Table 9 Gas pump heater prototype : Power supply rejection @DAC=$E58

We observe an excellent rejection, the effect on current being less than 0.01 %.

4.2.4.4 Variation of the heater resistance

DAC word	Heater resistor (R) (intended : actual)	DAC output voltage (V)	V heater (V)	V hsk (V)	Is (A) [Vheater/R]
FFFh	0 Ω	4.9762	40u	5.8m	Limited
	400 Ω : 399.3	4.9762	639.253m	3.8134	1.6009m
	500 Ω : 497	4.9762	795.57m	4.7446	1.6007m
	1000Ω : 1001.3	4.9762	1.60288	6.5846	1.6007m
	1500Ω : 1498.3	4.9762	2.31685	6.5652	1.546m
	2000Ω : 2004.4	4.9762	2.7703	6.5655	1.3821m
	∞	4.9762	5.6543	6.635	0

Table 10 Gas pump heater prototype : Variation of heater resistance @DAC=$FFF

The current is stable for heater resistances lower than 1 kΩ. For upper values, the output operational amplifier reaches saturation at ≈ 6.33 V. The heater current is limited by a 2 kΩ resistor. In case of heater short circuit, the harness current is limited to 3.2 mA (6.33 V/2 kΩ).

4.3 FPU thermal strap heater (HeaterL)

4.3.1 Specification

The following table recalls the requirement for the thermal strap low power heaters [extracted from AD 1].

Type	Number	Heater resistance	Lead resistance	Power	Max. Voltage	Interface type
Thermal strap	1	3K	TBD	300mV/50uA		4-wire

Table 11 Thermal strap heater specification

4.3.2 General description

The FPU thermal strap heater circuit follows the same principle as the gas pump heater circuit. The circuit produces a [0 – 50 μA] current. The maximum power is specified at 7.5 μW.

4.3.3 Simulation

4.3.3.1 Pheater = f(Ve)

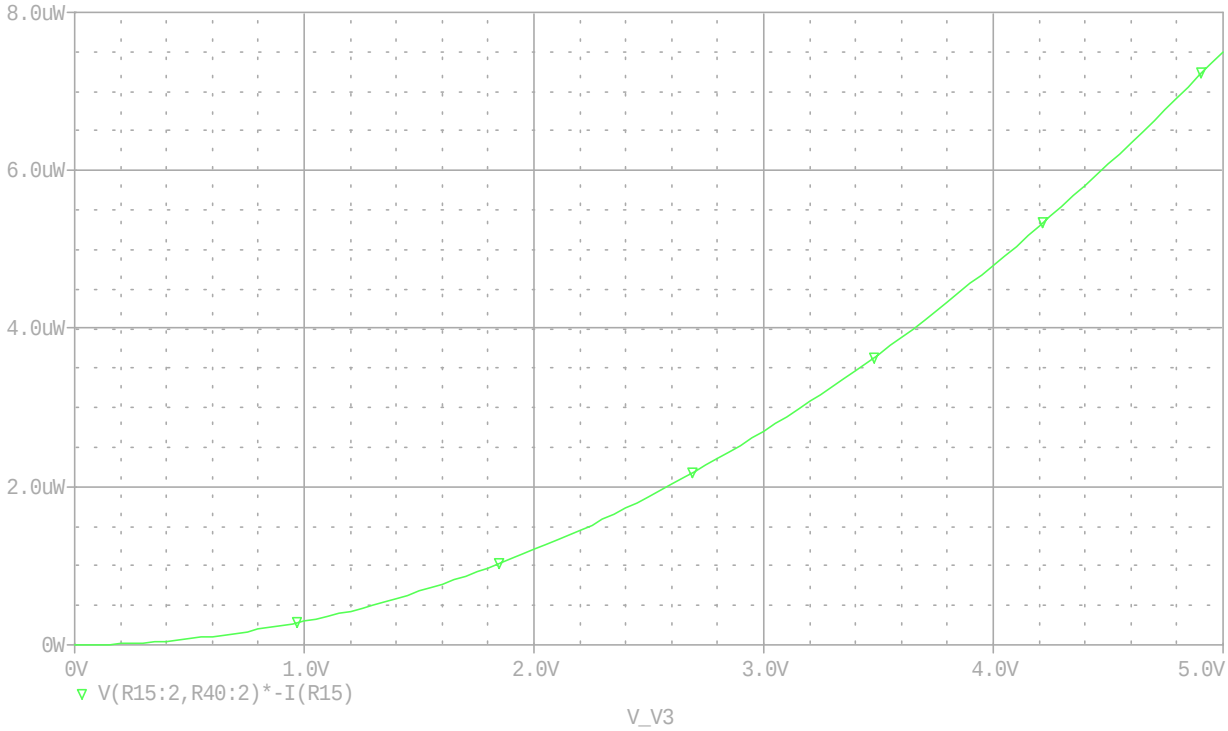


Figure 15 Thermal strap heater simulation : Power variation

The maximum power dissipated in the heater (7.5 μW) is obtained for a 5V DAC output.

4.3.3.2 Ic(heater) = f(Ve)

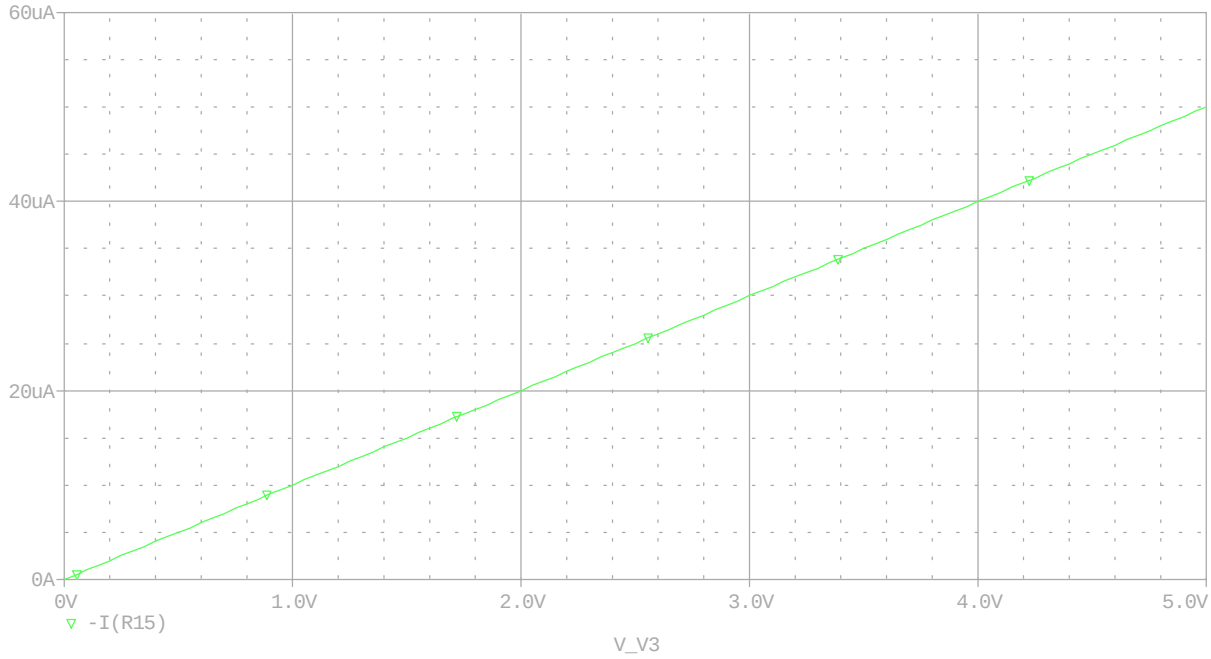


Figure 16 Thermal strap heater simulation : Current variation

4.3.3.3 Pheater = f(Vhsk)

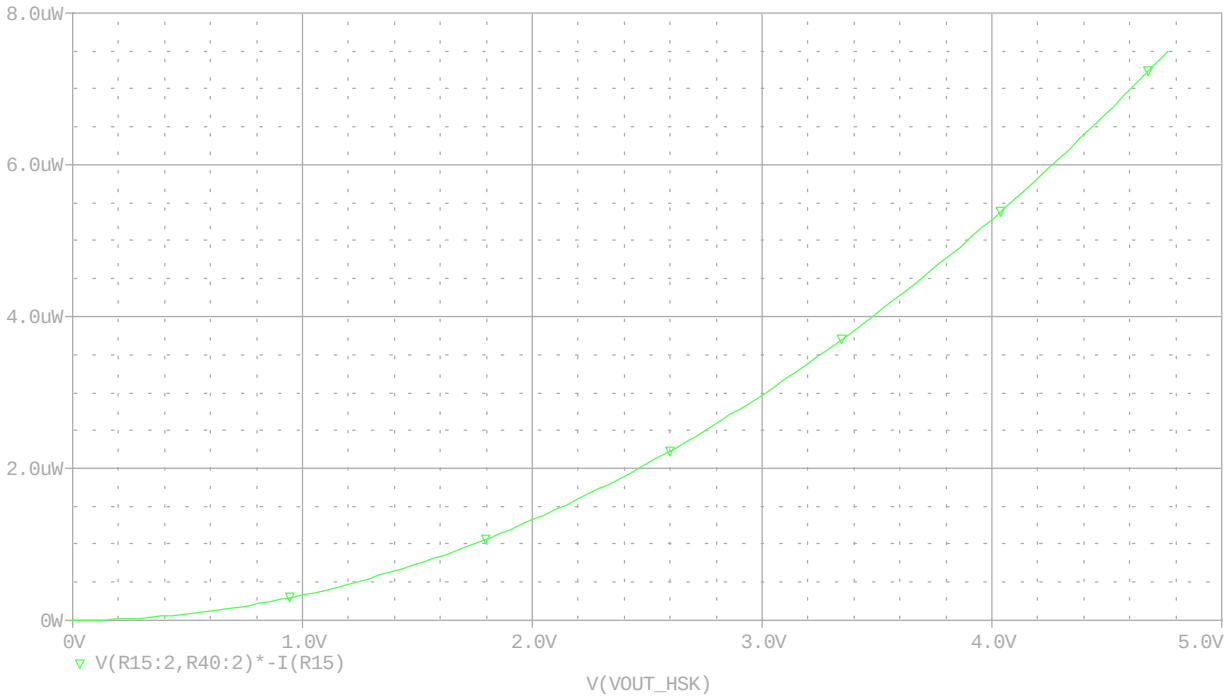


Figure 17 Thermal strap heater simulation : Power dissipation vs HSK voltage

4.3.4 Prototype test result

The results for the FPU thermal strap heater were derived from the low power heater prototype. In this design the leakage current for 0 DAC setting is 100 nA, leading to a residual power dissipation of 30 pW. The heater current is limited by a 50 kΩ resistor. In case of heater short circuit, the harness current is limited to 126 µA.

4.4 IR Calibrators : Pcal, ScalP and ScalF

4.4.1 Specification

The SCU controls three different calibrators : the photometer calibrator source (PCAL), the spectrometer calibrator point source (SCALP) and the spectrometer calibrator flood source (SCALF).

For each of them, the SCU implements a DAC-controlled current source used to bias the heater resistor of the calibrator source and thus generate a reference IR emission level. The actual current applied to the source resistor and the corresponding voltage are measured, converted to digital form and made available to the DPU.

4.4.1.1 The photometer calibrator (PCAL)

The photometer calibrator consists of a heater mounted in an integrating cavity on the BSM structure. The SCU has to bias this heater according to the dynamic DAC programming sequence provided by the DPU on the *Cmd* interface.

The following table recalls the requirements for the PCAL bias current [extracted from AD 1].

Heater Bias Current Range	0 to 7 mA	in 4096 steps
Maximum dissipated power into heater	10 mW	
Heater Resistance Range	200 to 500 Ω	+60 Ω for lead resistance
Stability / Repeatability	0.5 % or 5 µA	Whichever is greater
Maximum drive voltage	4.0 V	Worst case
Bias waveform	square	Spec. for DPU
Waveform frequency	0 to 5 Hz	Spec. for DPU
Waveform resolution	100 ms	Spec. for DPU
Interface Type	4-wire	Supply + sense

Table 12 PCAL calibrator specification

4.4.1.2 The spectrometer calibrator point source (SCALP)

The spectrometer calibrator point source consists of a heater mounted on a blackened plate. The SCU has to bias this heater with a variable amplitude.

The following table recalls the requirements for the SCALP bias current [extracted from AD 1].

Heater Bias Current Range	0 to 7 mA	in 4096 steps
Maximum dissipated power into heater	10 mW	
Heater Resistance Range	200 to 500 Ω	+60 Ω for lead resistance
Stability / Repeatability	0.5 % or 5 µA	Whichever is greater
Maximum drive voltage	4.0 V	Worst case
Bias waveform	DC	
Electrical Interface Type	4-wire + shield	Supply + sense

Table 13 SCALP calibrator specification

4.4.1.3 The spectrometer calibrator flood source (SCALF)

The following table recalls the requirements for the SCALF bias current [extracted from AD 1].

Heater Bias Current Range	0 to 9 mA	in 4096 steps
Maximum dissipated power into heater	15 mW	
Bias waveform	DC	
Stability / Repeatability	0.5 % or 5 µA	Whichever is greater
Heater Resistance Range	200 Ω	+60 Ω for lead resistance
Maximum drive voltage	5.0 V	
Interface type	2-wire (TBC)	None connected to ground

Table 14 SCALF calibrator specification

4.4.2 Circuit description

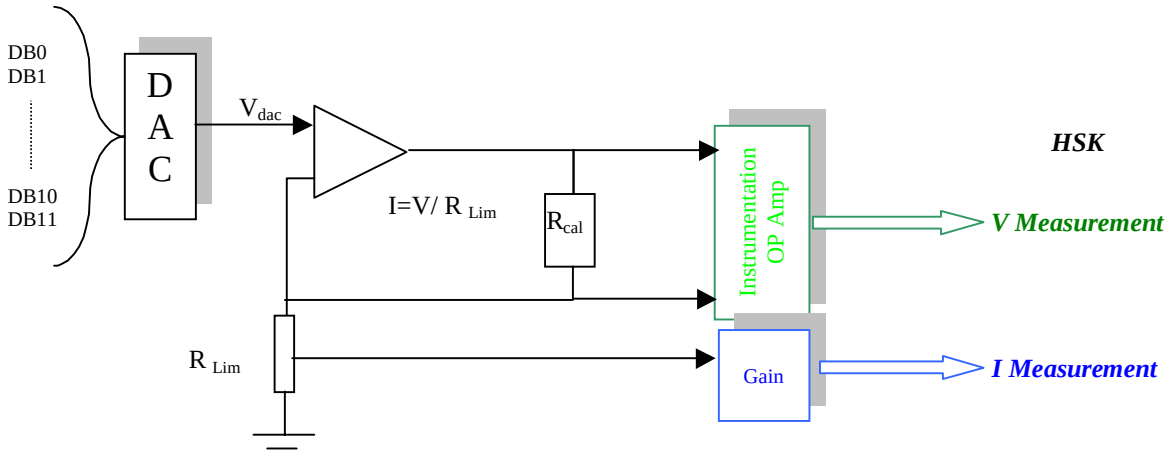


Figure 18 Calibrator current source principle

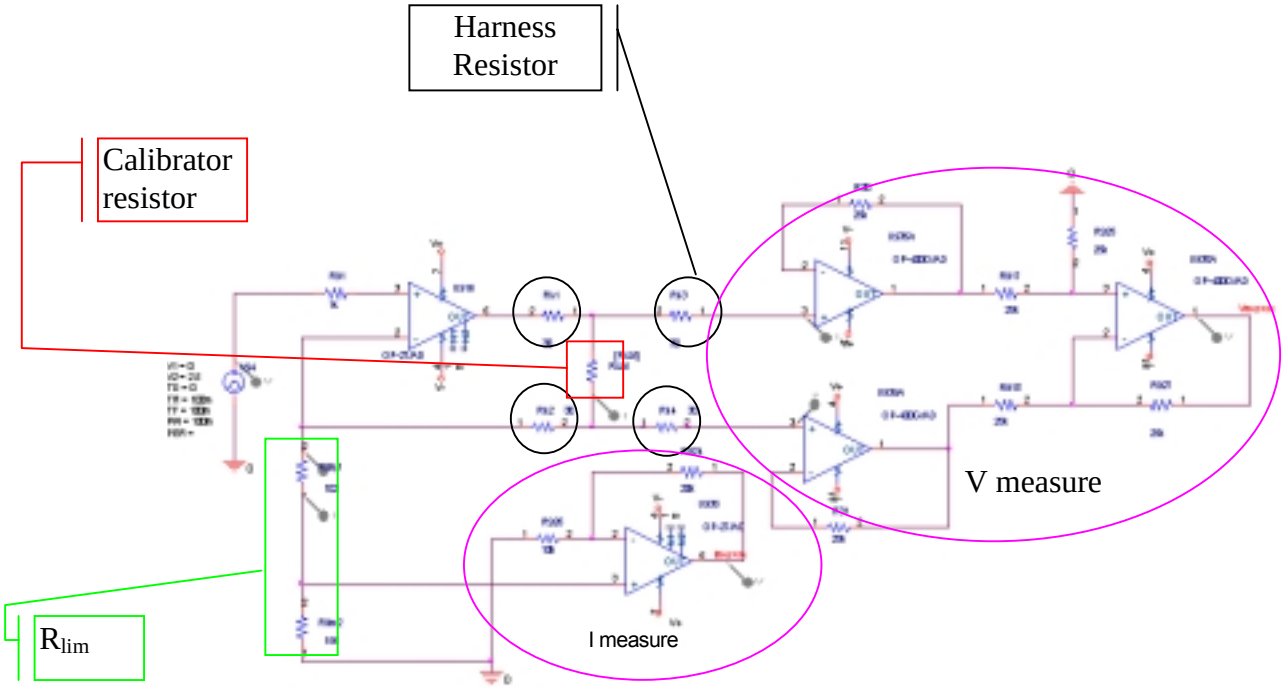


Figure 19 Calibrator current source circuit

4.4.2.1 Current limitation

The calibrator current is limited by the R_{lim} resistance at 0.01% of the maximum specified current value.

The value of R_{lim} is derived in the following expressions.

First, the maximum dissipated power allowed in the calibrator, the calibrator resistor value and the bias current range I_{range} give the maximum current I_{max} expected in the heater.

$$I_{\max} = \sqrt{\frac{P_{\max}}{R_{cal}}} \text{ if } I_{\max} \geq I_{range} \text{ else } I_{\max} = I_{range}$$

Then, I_{max} and the the V_{ref} DAC reference voltage (2.5V) define R_{limit}.

$$R_{\lim} = \frac{V_{ref}}{I_{\max}} \times \frac{4095}{4096}$$

The following table gives R_{lim} for the three different calibrators.

Function	P_{max}	I_{range}	R_{cal} (Ω)	I_{max}	R_{lim} (Ω)
PCAL	11mW	7mA	200	7mA (7.4mA)	357
			500	4.69mA	533
SCALP	11mW	7mA	200	7mA (7.4mA)	357
			500	4.69mA	533
SCALF	16,5mW	9mA	200	9mA (9.08mA)	277.7

Table 15 Current limitation for the PCAL,SCALP and SCALF calibrators

4.4.3 Simulation

A SPICE simulation was used to verify the operation of the analogue part (from DAC output to I and V measurement).

The design was simulated for the more demanding current drive (Ical = 9 mA), with extreme values for the calibrator resistance (200 and 500 Ω). The stimulus applies a voltage ramp from 0 to 2.5 V, then a constant 2.5 V value and finally a decreasing voltage ramp from 2.5 V downto 0 V.

The result is shown on the following graph.

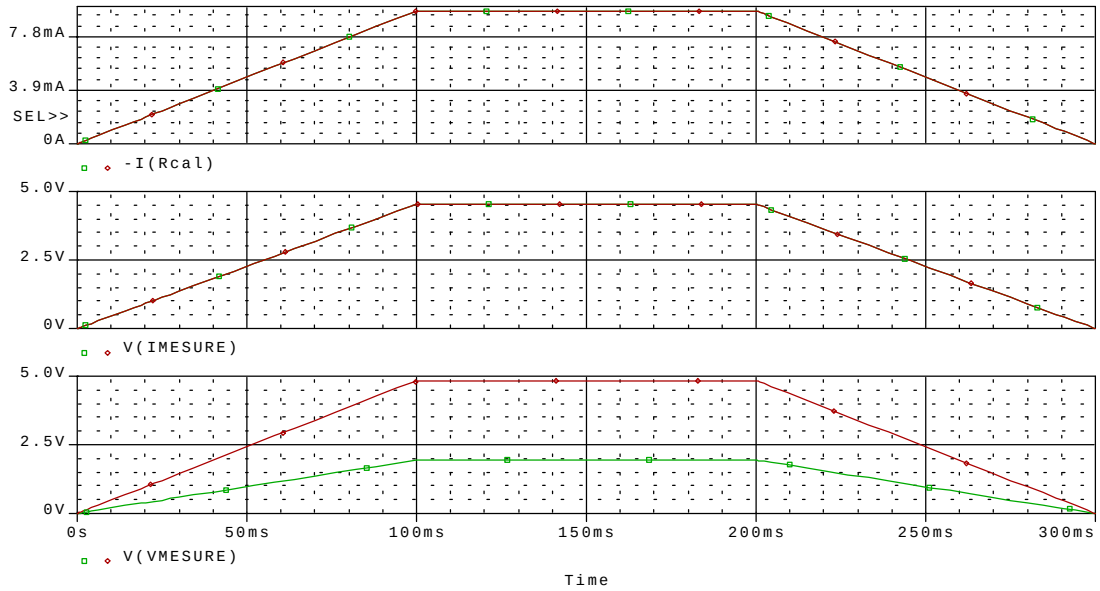


Figure 20 Calibrator current source simulation : Current and Imeas/Vmeas variation

4.4.4 Performance requirements

The specification does not specifically asks for absolute calibration, and does not directly define the expected integral and differential linearity. The main requirement is for stability and repeatability, asking for less than 0.5% relative variation over an hour. The main errors that may affect the stability (or repeatability) are the temperature drift and the power supply variations, which both need to be estimated. The maximum residual current that may be accepted when the source is shut off (DAC setting = 0) must also be controlled.

4.4.4.1 Residual current estimation

To estimate the residual current, we have to consider the sources of voltage offsets for Vdac :

- DAC leakage current : 50 nA ;
- Offset voltage of the OP27 operational amplifier : 100 µV

$$\delta_{dac} = 50 \quad 10^{9-} \times 15 \quad 10^{3} + 3 \times 100 \quad 10^{-6} = 1.05 \quad 10^{-3} \text{ (V)}$$

We have to add the current bias and offsets of the op-amps used in the current and voltage measurements. For the current measurement the OP-27 op-amp adds 155 nA, for the voltage measurement the OP400 adds 21.5 nA. The corresponding leakage currents are negligible.

4.4.4.2 Variation with temperature : calculation

The following calculations give a first estimate of the current and voltage temperature dependence. A more comprehensive error calculation for the current sources will take place in a further version of the present document.

The estimations of the current (ΔI) and voltage (ΔI) errors are done for the SCALF chain, where the highest current leads to the greatest absolute errors when the 5 µA stability / repeatability is expected. For the SCALF chain, the ratio between the current through Rcal and the DAC input code N is :

$$I(Rcal) = 2.228\ e^{-6} \times N$$

Each N step corresponds to a 0.61 mV voltage across the Rlim resistor. In the first approach, the errors that are very small compared to this value may be ignored.

The temperature-dependent parameters for all the components involved in the current source circuits are given in the following table.

Component	Parameter	Drift
OP27	Input offset voltage	1.8 µV/°C
OP27	Input bias current	± 0.8 nA/°C
OP27	Input offset current	0.75 nA/°C
OP400	Input offset voltage	1.2 µV/°C
OP400	Input bias current	0.028 nA/°C
OP400	Input offset current	0.014 nA/°C
DAC AD7545	Gain	± 5 ppm/°C
ADC ADS7809	Gain	± 2 ppm/°C
Voltage reference REF-02	Output voltage	8.5 ppm/°C
Resistors	Resistor value	50 ppm/°C

Table 16 Calibrator circuit: Component temperature dependence

The current value is I = V/Rlim so $\Delta I = I * (\Delta V/V + \Delta Rlim/Rlim) = \Delta V/Rlim + I * \Delta Rlim/Rlim$, where V is the voltage applied on the Rlim resistor.

The error on V is due to the current source, the DAC and three OP27 op-amps, for which the offset values and input bias currents flowing in resistors cause drifts. Taking into account the values listed on Table 16 and on the schematic drawing, the resulting ΔV error is the following :

$$\Delta V \approx (20e^{-6}+V*14e^{-6})\ V/°C$$

Since Rlim = 274Ω and $\Delta Rlim/Rlim = 5e^{-5}$, $\Delta I \approx 73e^{-9} + I * (14e^{-6} + 5e^{-5})$, and we obtain the ΔI expression :

$$\Delta I \approx 73e^{-9} + I * 64e^{-6}\ A/°C$$

As an example, for a full scale current of 9 mA, the temperature drift error is : 0.65 µA/°C.

Because the current measurement is achieved by measuring the I * Rlim2/Rlim voltage, we may assume that the Rlim2/Rlim ratio is not temperature dependent, and thus will not contribute to the error calculation.

Calculating the temperature dependent errors on Imeasured and Vmeasured only needs to add the effects of the OP27 (for Imeasured) and three OP400 input offset voltages and currents, and the gain effects on the output ADC, as listed in Table 16 . We obtain :

$$\Delta(Vmeasured) = (4.6e^{-6} + 2.0\ e^{-6} * Vmeasured)\ V/°C$$

and

$$\Delta(Imeasured) = ((3.35e\text{-}6 + 2.0\ e\text{-}6 * Imeasured*Rlim2\ )/Rlim2)\ A/°C$$

The Rlim2 value is : Rlim2 = 274 Ω.

4.4.4.3 Variation with temperature : simulation

The temperature variation rate is expected to be lower than 3 K/h. The following simulation shows the current variation for T = 0°, 24°, 27°, and 30°C.

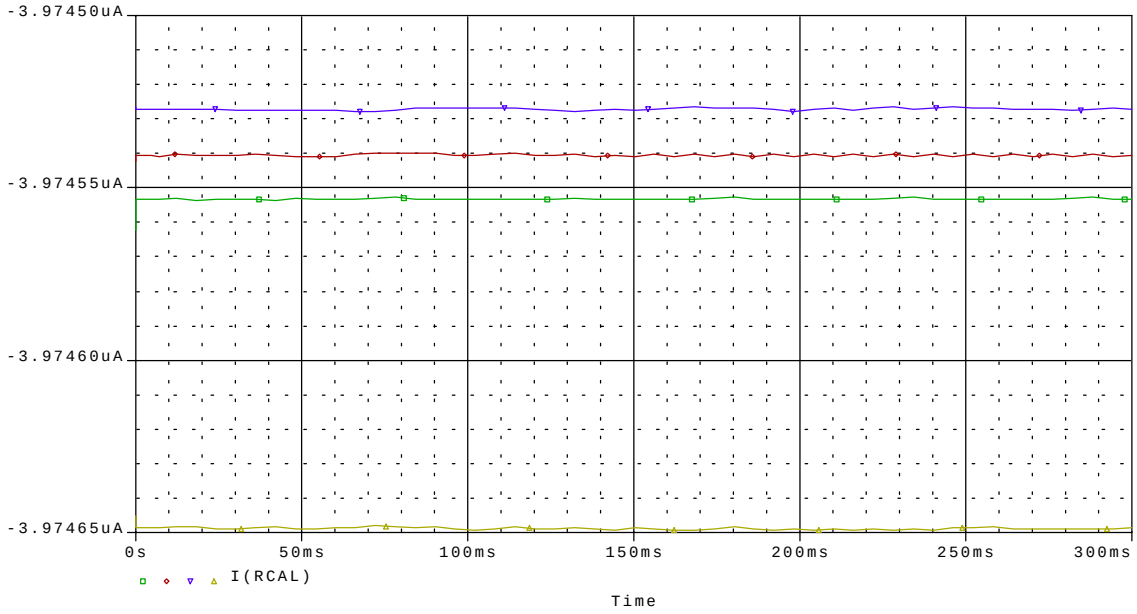


Figure 21 Calibrator current source simulation : Variation with temperature

4.4.5 Prototype test results

A prototype circuit was developed for the calibrator circuit. This circuit includes the DAC, the analogue circuitry, the ADC, and a FPGA for the logic interface with a Personal Computer. The current across the resistive load is measured with an external high precision GPIB-driven instrument.

The following graphs show recent measurements giving the linearity of the current production, and the linearity of the voltage and current housekeeping measurements. These results are very preliminary and require further analysis and discussion.

4.4.5.1 DAC to current linearity

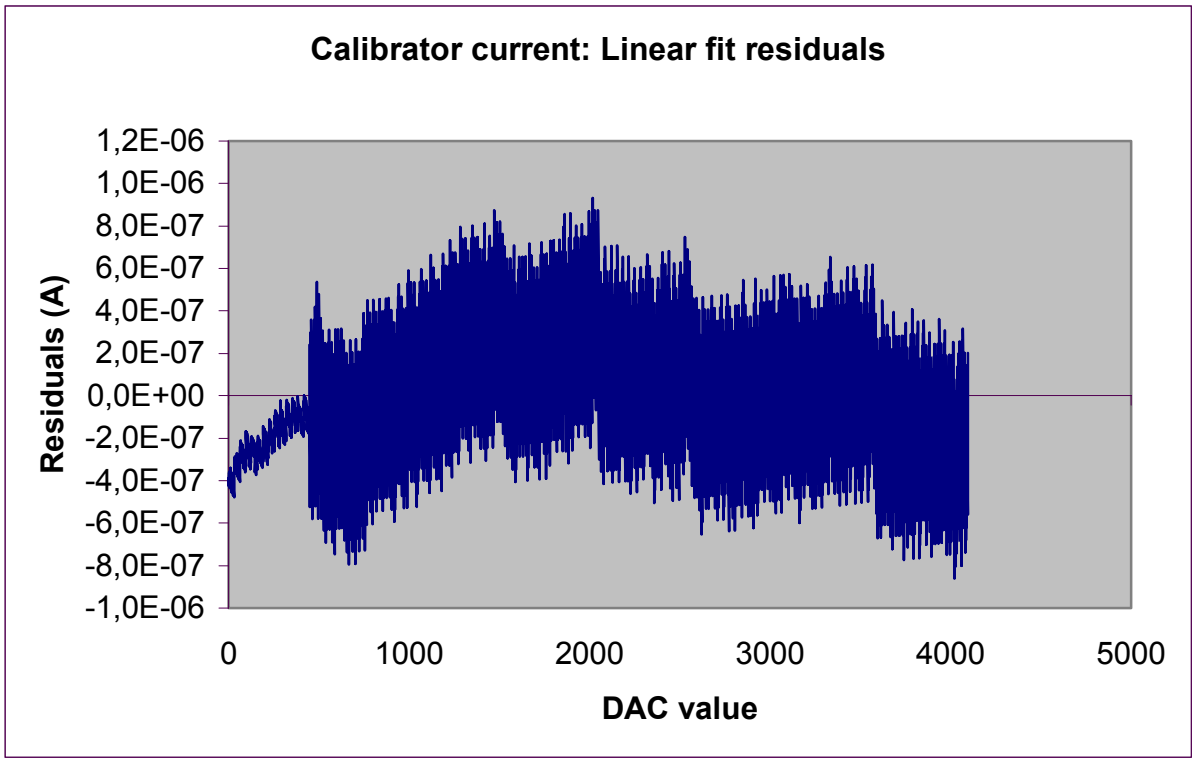


Figure 22 Calibrator prototype : DAC to current linearity

4.4.5.2 Voltage measurement linearity

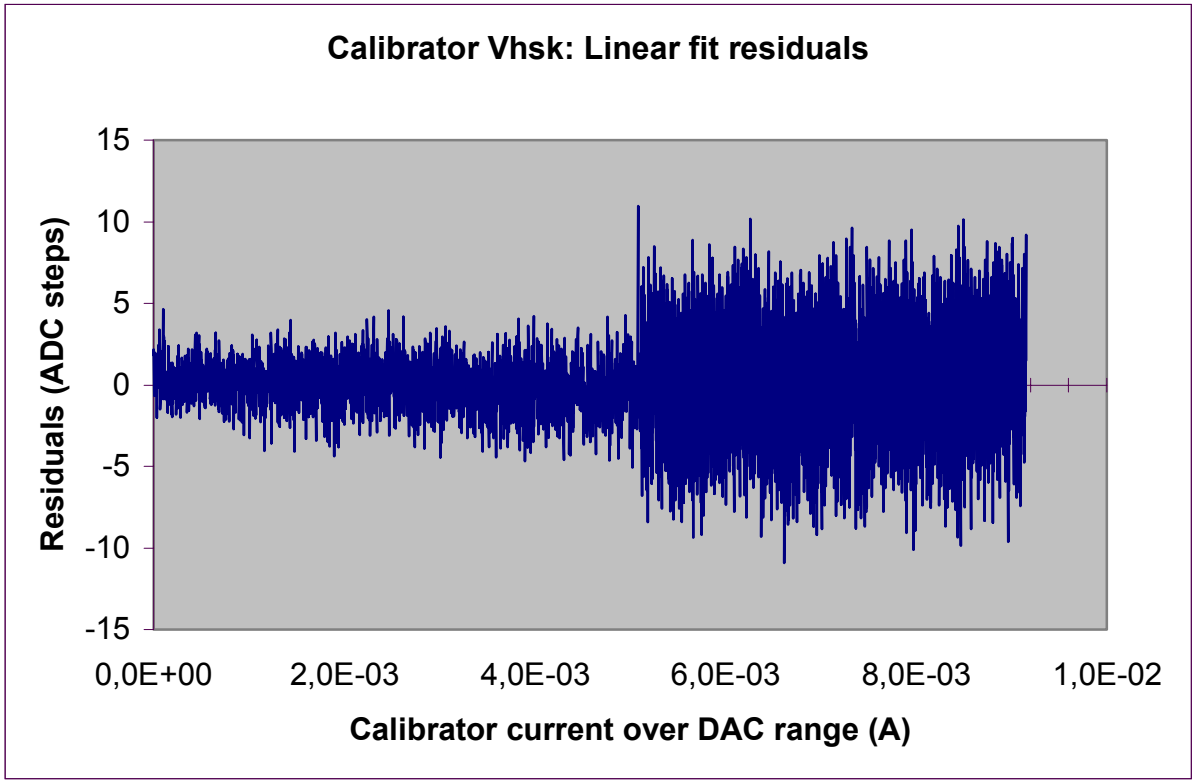


Figure 23 Calibrator prototype : Current to VHSK linearity

4.4.5.3 Current measurement linearity

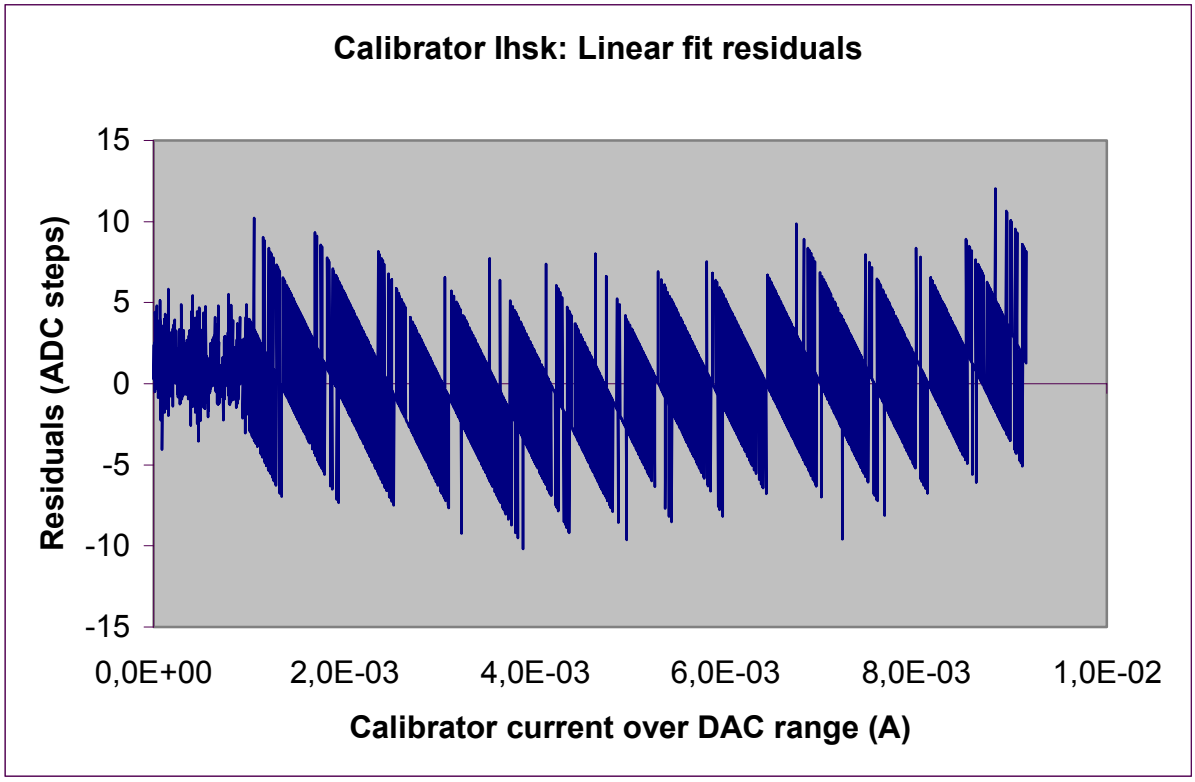


Figure 24 Calibrator prototype : Current to IHSK linearity

4.5 Sub-K thermometry : TempAC

4.5.1 Specification

As extracted from AD 1.

4.5.2 Design principle

The resistance variation [R = f(T)] of the Cernox CX-1030 sensor shows a very strong dR/dT for temperatures lower than 2 K. To obtain the required 0.1 mK resolution at T = 300 mK, a high gain is necessary in the measurement chain. To cancel the low-frequency accumulated offset and temperature drift errors, a differential measurement is implemented. The sensor is AC biased at 20 Hz, and the measurements are synchronous with the AC excitation. Each temperature point results from the differential combination of two measurements taken synchronously with the 2 phases of the AC excitation. This measurement chain was developed in collaboration with the *Service de Basses Températures* (CEA/SBT).

The sensor is current biased, in order to obtain a broad measurement range (up to 10 K) with sufficient resolution while controlling the dissipation at the nominal 300 mK operating point. The selected bias current value is 40 nA. At the operating temperature, the corresponding self-heating error is lower than 1 mK (to be compared with the 5 mK precision of the Cernox R(T) transfer curve).

4.5.3 Block diagram

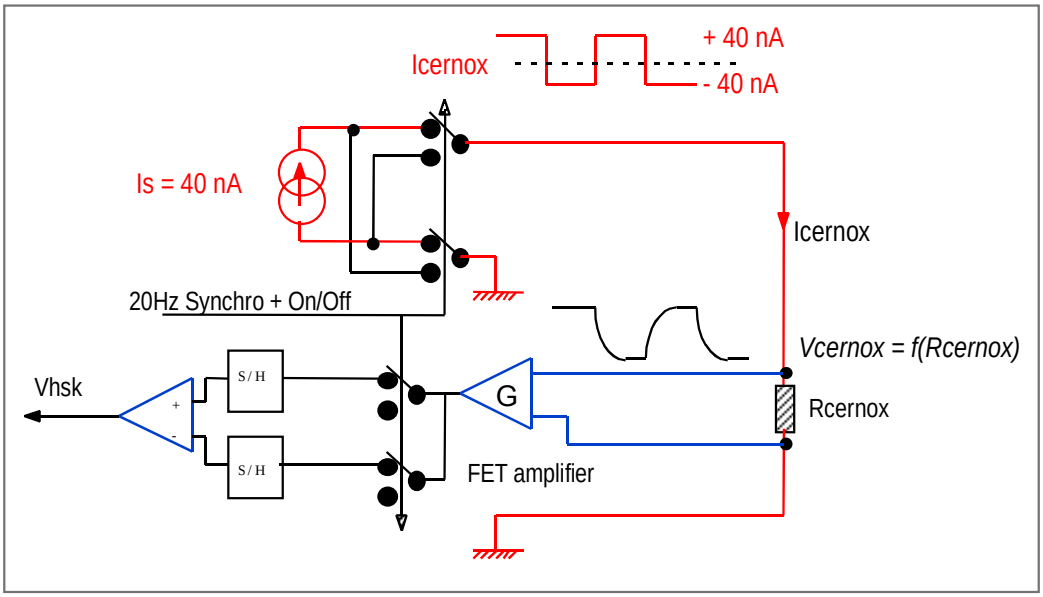


Figure 25 Sub-K bias circuit

The sensor current (Icernox) is a square waveform obtained by current steering from a stable current source (Is). The steering operation is driven by a 20 Hz digital square wave modulation command, alternately injecting +Is and –Is into the Cernox sensor. After amplification, the voltages corresponding to the positive and negative current phases are sampled and held in correlation with the steering command, and then passed to a differential analogue stage to produce the Vhsk measurement. The low frequency error contributions (LFErr) are suppressed by this method, Vhsk being Vcernox*G+LFErr – (-Vcernox*G+LFErr) = 2*G*Vcernox. This alternative measurement technique theoretically cancels the errors caused by bias currents, offset voltages and very low frequency noise sources.

4.5.4 Resolution

The Cooler Evaporator sensor must be sensitive in the [0.25K-10K] temperature range, with 0.1 mK resolution. Taking into account the R(T) response of the Cernox sensor, the expected resolution in the [260mK-1K] range is given in the following graph, computed with G = 800.

4.5.4.1 Expected resolution

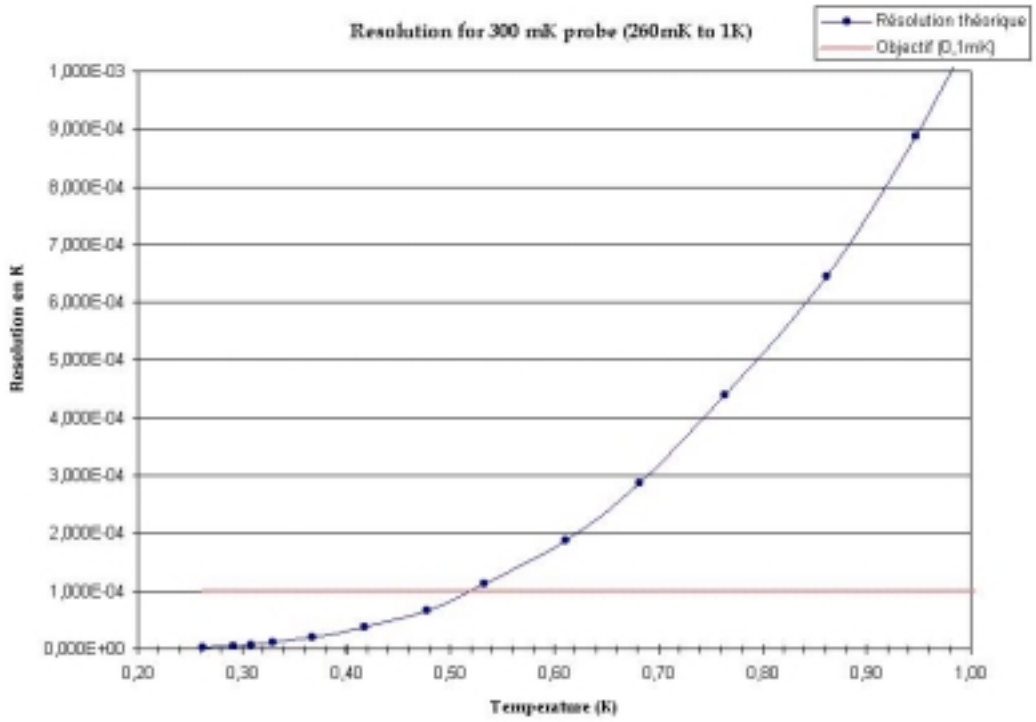


Figure 26 TempAC circuit : Resolution

The requirement for 0.1 mK resolution is easily fulfilled in the operating region (between 250 mK and 550 mK). For higher temperatures, the resolution degrades (1 mK@1K, 0.3K@10K) but is sufficient for gross temperature monitoring.

Due to the current bias technique, the voltage measurement chain may saturate at low temperatures, where the sensor resistance gets very large. The circuit is designed to operate linearly when the sensor resistance does not exceed 150 kΩ. This figure was selected to give sufficient margin from the Lakeshore specification, which gives R<100 kΩ @300mK.

4.5.5 Prototype measurements

To validate the TempAC electronic chain, we developed a prototype circuit with both the analogue and ADC sections installed. The linearity of the voltage measurement was verified over the full variation range of the Cernox resistance value. The performance of the prototype was assessed at several temperatures (0°, 10°, 20°, 30° and 40°C).

4.5.5.1 Vhsk = f(Rcernox)

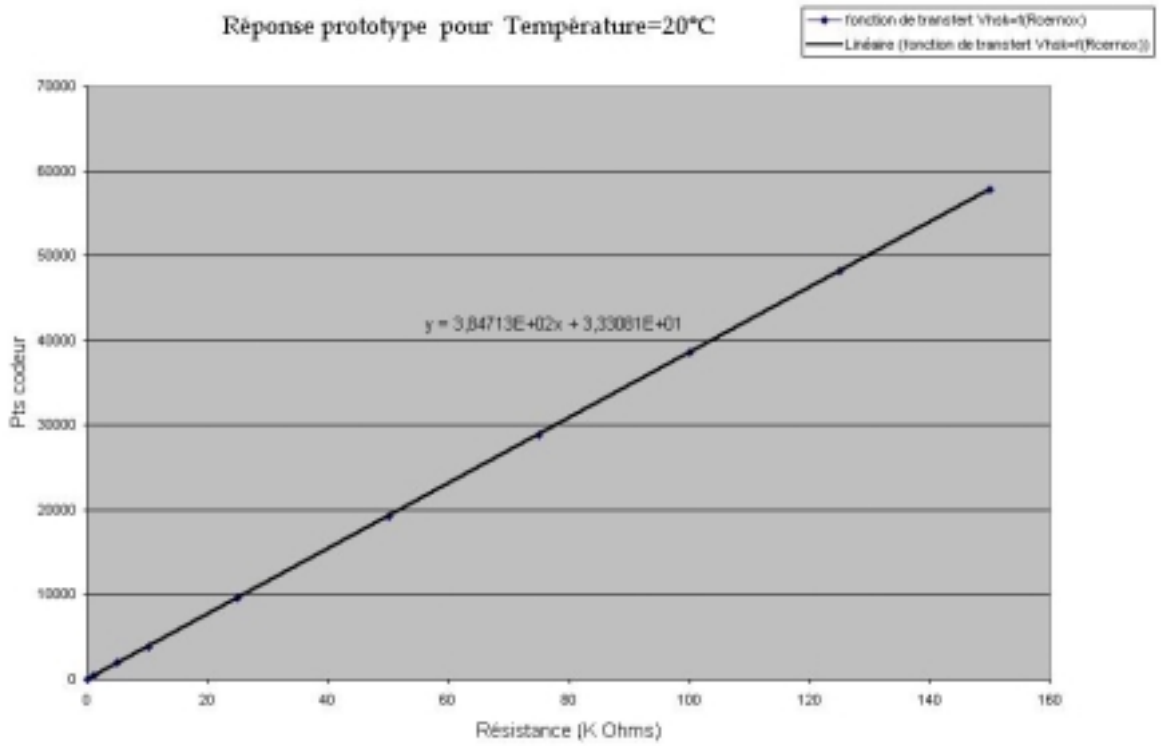


Figure 27 TempAC prototype : Resistance to ADC_step transfer function

The response curve was measured for several reference resistance values, chosen to cover the expected Cernox resistance variation range. The measurement confirms the linearity and the absence of saturation for resistance values as high as 150 kΩ. The measured slope is 384 ADC_steps/kΩ. The corresponding resolution is 3 μK/ADC_step @300 mK (R= 65 kΩ, dR/dT(mK) = 1000).

4.5.5.2 Variation with temperature

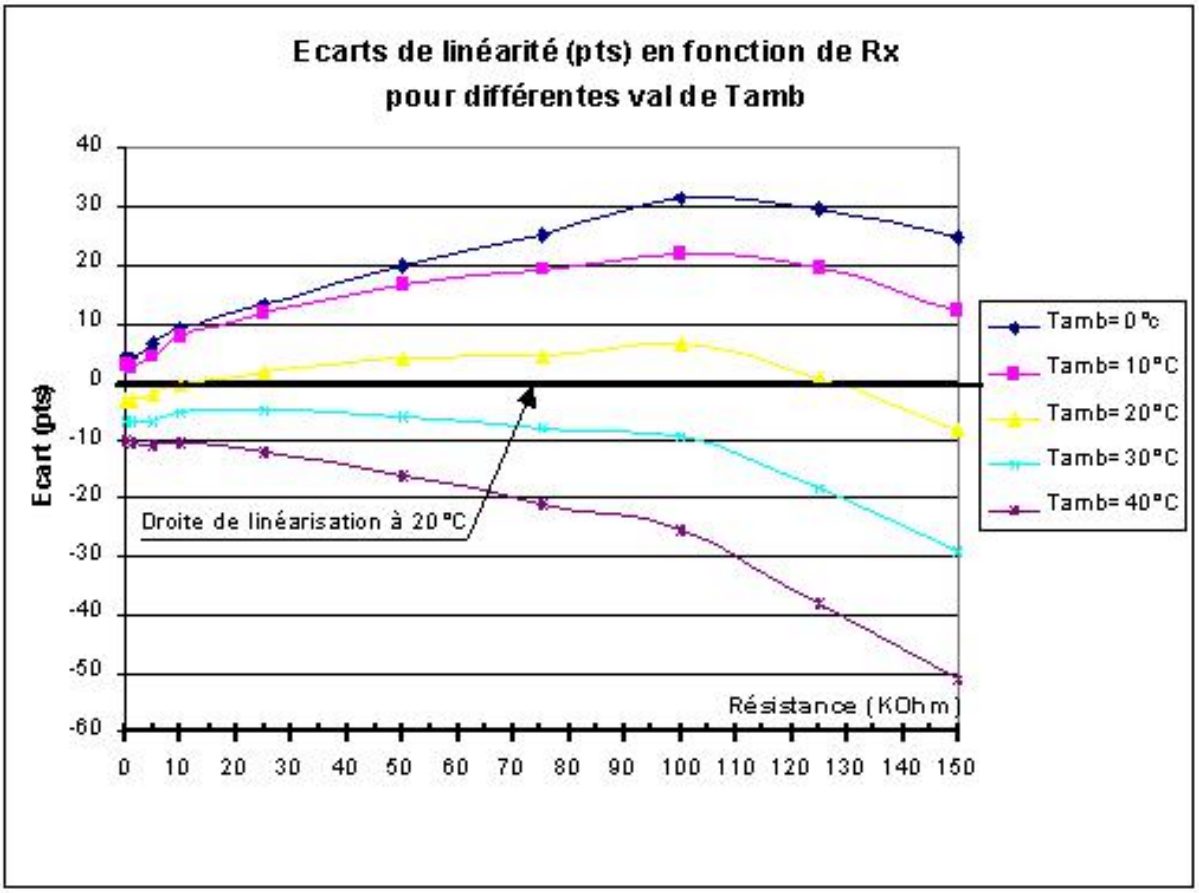


Figure 28 TempAC prototype : Variation with temperature

The above graph shows the variation of the response (expressed in ADC steps) when the circuit is placed at T= 0, 10, 20, 30 and 40°C. At R = 65 kΩ, a 40°C temperature variation displaces the response by 40 ADC steps, which corresponds to a brute error of 0.12 mK. The expected temperature variation of the electronics is much smaller, and compensation will normally be unnecessary ; if required, this systematic error could however be calibrated and compensated.

4.6 Other thermometry channels: TempDC

4.6.1 Specification

As extracted from AD 1.

4.6.2 Design principle

The TempDC circuit produces a fixed voltage bias across the Cernox CX-1030 sensor. The sensor current is measured by a simple current to voltage conversion, and reflects the resistance variation. The calibrated transfer function [R = f(T)] of the Cernox sensor is then used to obtain the temperature.

The rationale for the selection of the voltage bias technique is to obtain a slowly varying resolution over a broad measurement range, the Vhsk = k/R transfer function compensating the strong non-linearity of R(T) at low T values. A more involved discussion can be found in AD 6.

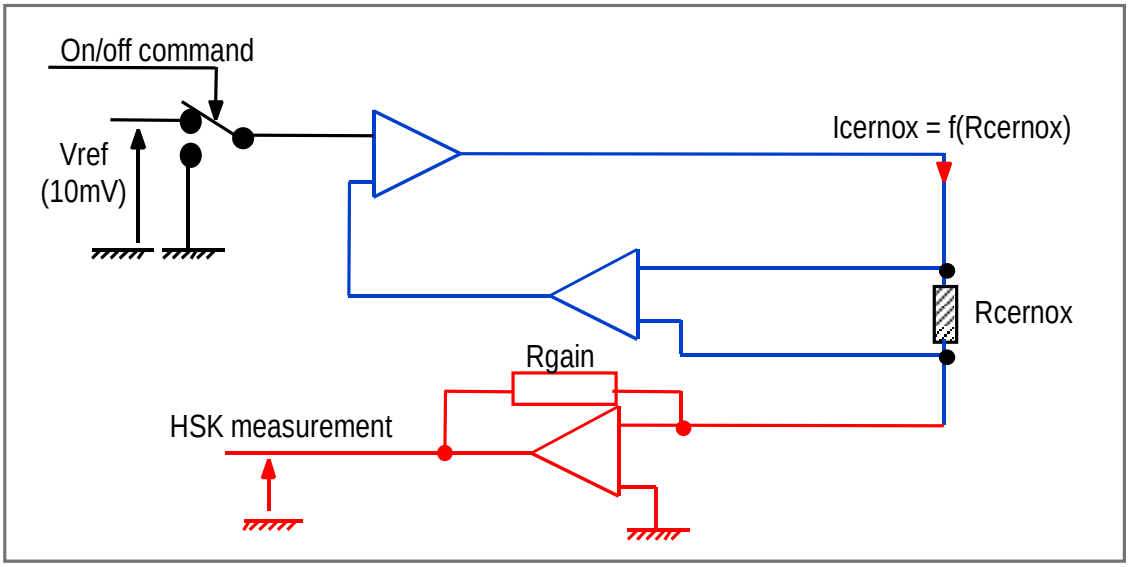


Figure 29 TempDC circuit : Block diagram

The HSK voltage is measured by a 16-bit ADC. The value of the Cernox resistance is derived from the current to voltage conversion formula : Vhsk = - Rgain * (Vref / Rcernox).

4.6.2.1 Bias voltage determination

The power dissipated in the sensor produces self-heating, which in turn disturbs the actual temperature measurement. This perturbation is difficult to estimate because the involved thermal impedance depends on several effects (material used in the sensor, thermalisation of the sensor, etc.). The selected bias voltage was defined after measurements obtained from the CEA/SBT. These measurements are shown in the following graph.

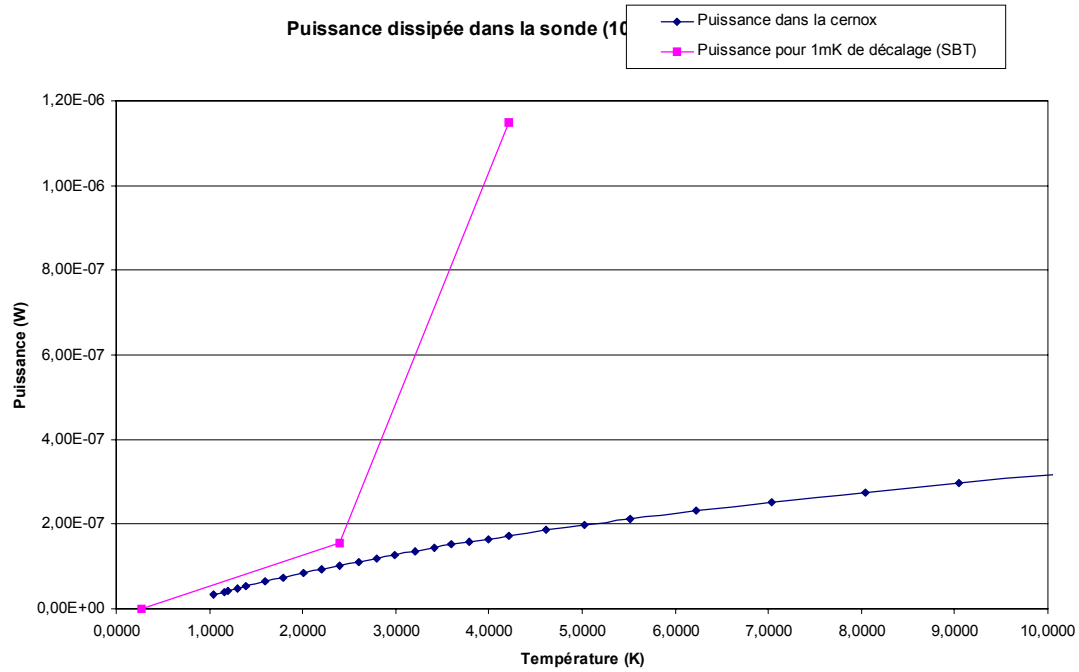


Figure 30 TempDC circuit : Power dissipation

The graph shows the power dissipation level that would create a 1 mK displacement error on the temperature reading (above), and the actual dissipation produced by the circuit when biased at 10 mV (below). Over the full temperature range of the sensor, the dissipation when applying a 10 mV bias is sufficiently small to produce a self-heating error lower than 1 mK (to be compared with the 5 mK precision of the Cernox R(T) transfer curve).

4.6.3 Resolution

The 16 sensors measured by the TempDC circuit pertain to 2 distinct groups : The low temperature group (1 K – 10 K, 2 mK resolution @1 K), and the extended temperature group (3 K – 300 K, 10 mK resolution @3 K).

The Cernox sensor R(T) variation is strongly non-linear with temperature. Knowing the constant Vbias and the R(T) characteristic curve, the gain of the trans-impedance amplifier must be adjusted to obtain the required resolution at the lower end of the corresponding temperature range, and stay in the 5 V full scale of the 16-bit ADC. The following graphs show the obtained resolution for each group.

4.6.3.1 Expected resolution (low temp. group)

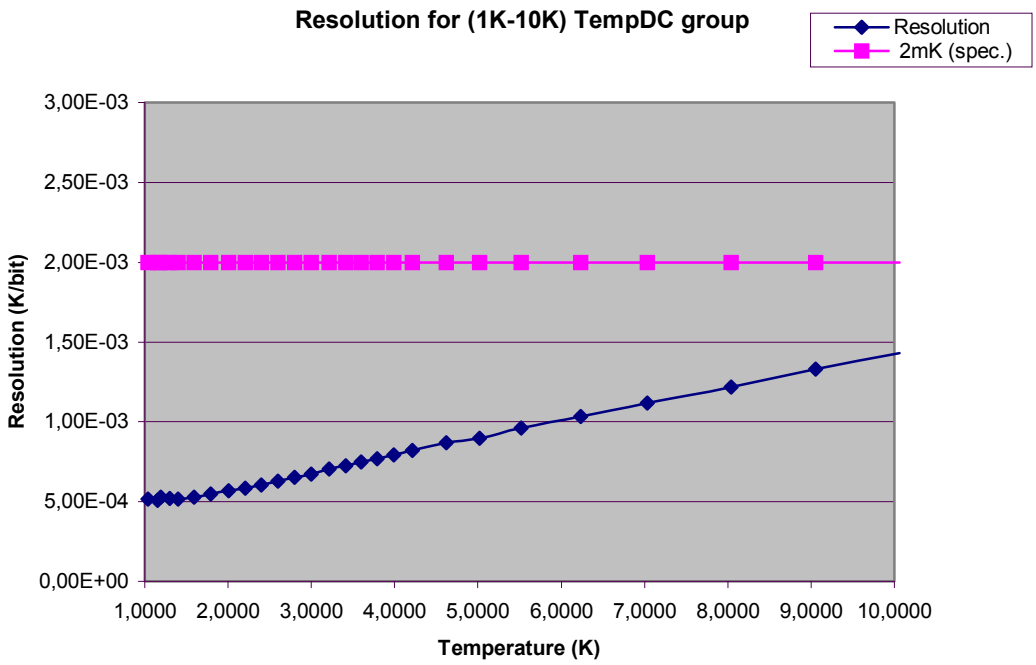


Figure 31 TempDC circuit : Resolution for [1K-10K] group

The above graph shows the evolution of the resolution over the low temperature range (below), as compared with the required resolution (above). The requirement is fulfilled over the full range. The current to voltage gain resistance is 54 kΩ.

4.6.3.2 Expected resolution (extended temp. group)

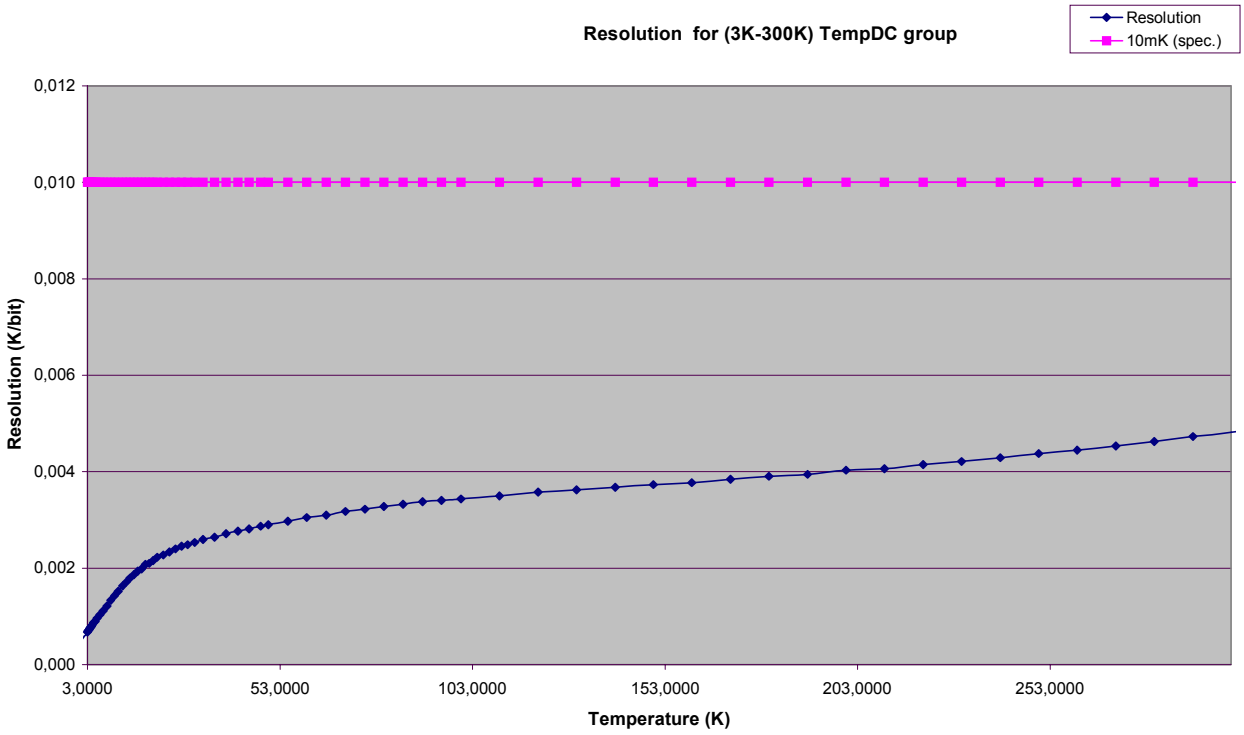


Figure 32 TempDC circuit : Resolution for [3K-300K] group

The above graph shows the evolution of the resolution over the extended temperature range (below), as compared with the required resolution (above). The requirement is fulfilled over the full range. The current to voltage gain resistance is 15 kΩ.

4.6.4 Prototype measurement

A dedicated TempDC prototype circuit was implemented, to validate the circuit principle and study the temperature variation.

4.6.4.1 Vhsk = f(Rcernox)

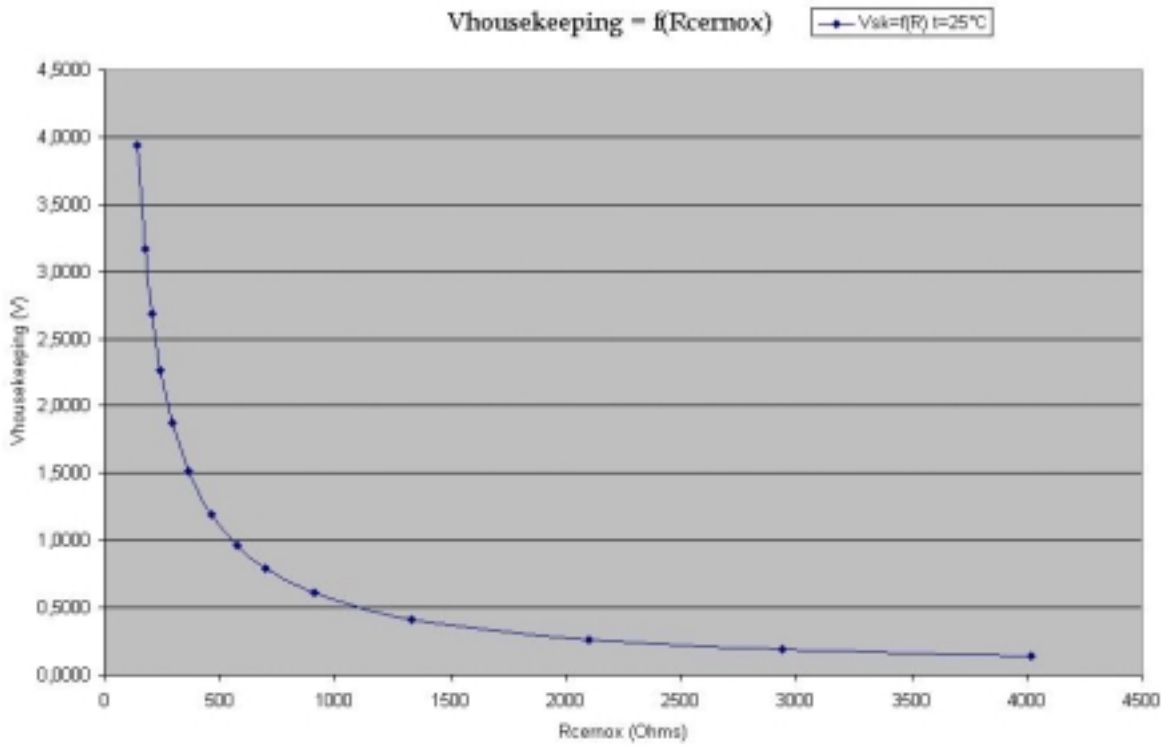


Figure 33 TempDC prototype :Vhsk variation

The above graph shows the evolution of Vhsk when the load resistance varies from 4 KΩ to 100 Ω (corresponding to a temperature variation from 1 K to 65 K on a typical Cernox sensor). The sensitivity is stronger for small resistor values (k/R dependence). This effect somewhat compensates the Cernox non-linearity, which is stronger for high resistor values.

The Vhsk precision directly depends on the precision of the current-to-voltage gain resistance value (Rgain). The precision of Rgain is 0.1% on the prototype, and will be improved to 0.01% on the flight model. The measurement chain will require calibration to maintain this precision.

4.6.4.2 Variation with temperature

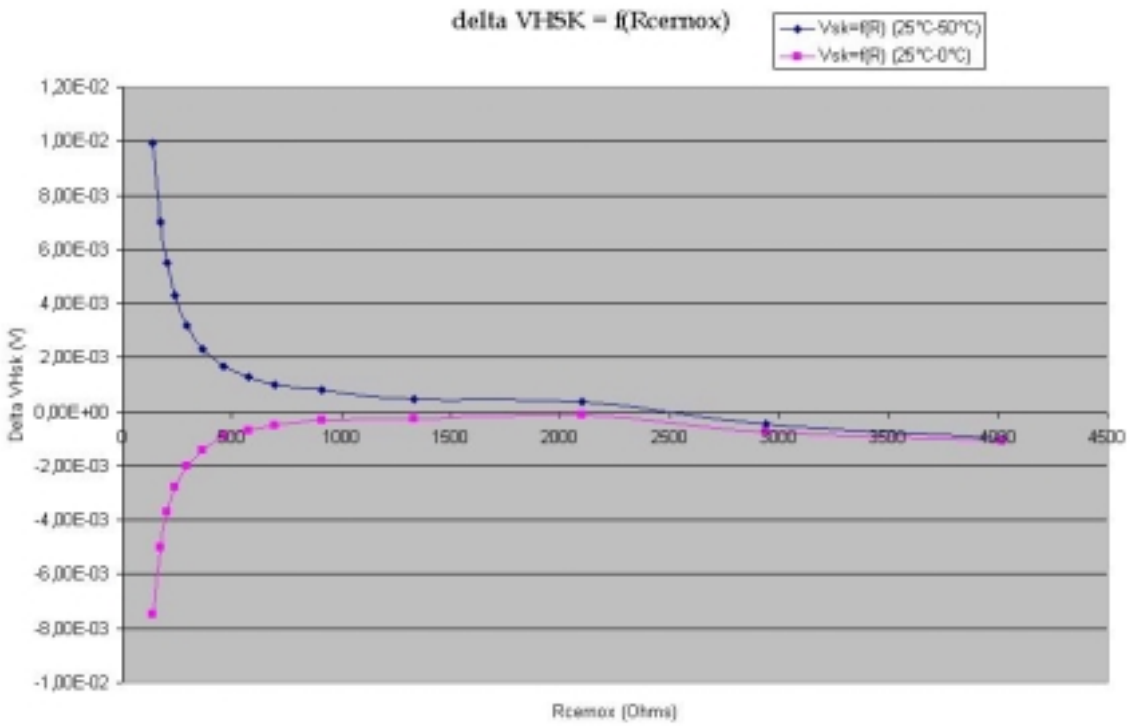


Figure 34 TempDC prototype :Variation with temperature

The above graph shows the variation of Vhsk at 0°C and 50°C as compared with the reference measurement @25°C. The curves show a symmetric spread, proportional to Vhsk. Here again, the temperature behavior could be calibrated and compensated if necessary.

4.7 Electronics Temp. Monitor : TempMon

As specified in AD 1, the electronics temperature monitoring channels use the AD590 sensor, connected to a simple current to voltage converter. They are read out through the common ADC system (ADC2 in Figure 1).

The detailed circuit description and associated performance analysis (vs. DCU-REQ-81) will be added when available.

4.8 Power Supply Monitor : PwrMon

The power supply monitoring channels use simple voltage followers, and are readout through the common ADC system (ADC2 in Figure 1).

The detailed circuit description and associated performance analysis (vs. DCU-REQ-83) will be added when available.

5 Physical implementation

This section covers the actual details of the physical implementation : boards, connectors, pinouts, etc.

5.1 Boards

In conformance with the specified mechanical requirements (AD 2-Section 3.), the SCU module is implemented as a set of 2 active electronic boards (*Temp* and *CcHkIf*), interconnected with a dedicated passive printed circuit backplane (*Bkpln*).

Two identical SCU modules (*Main and Redundant*) are installed in the SCU compartment of the FCU box (see Figure 1).

5.2 Backplane

5.2.1 PSU interconnects

The Bkpln board receives from PSU :

- The secondary power supplies required by the SCU ;
- An analogue temperature sensing level used to monitor the internal temperature of the PSU electronics.

The Bkpln board provides to PSU :

- The On/Off logical power break signals required to control the DCU LIA_P, LIA_S, BIAS_P and BIAS_S secondary power supplies.

These signals are exchanged over the J35(M) / J36(R) side connectors of the SCU.

5.2.2 Board interconnects

Two FRB90 connectors insure electrical and mechanical connection between the Bkpln and Temp / CchkIf boards.

5.2.2.1 Bkpln/Temp connector

The actual connector signal list will be added when available.

5.2.2.2 Bkpln/CchkIf connector

The actual connector signal list will be added when available.

5.3 Temp board

The physical implementation of the Temp board will be added when available.

5.4 CCHkIf board

The physical implementation of the CchkIf board will be added when available.

6 Operation

This section describes the programming model of the SCU, and the phases required to operate it.

6.1 Working cycle

The SCU runs under supervision of the DPU software.

At power on, the SCU takes a definite Reset state for a short time, and then autonomously leaves this state without DPU intervention. The DPU software can later place the SCU in its Reset state, by writing the Subsystem Reset bit in a control register.

In a typical session, the DPU first installs the required configuration for the operational run, and then launches the SCU frame sequence for a limited or infinite time. During operation, the DPU software has unhindered access to all CSR registers and analogue parameters. Once out of Reset, the SCU is stateless and does not apply censorship on DPU transactions. Potential problems may be expected if the DPU changes configuration while a frame sequence is running. The SCU does not include any special mechanism to detect, log or reject incorrect DPU software sequences.

6.2 Parameter list

The following table gives the current state of the SCU parameter list.

Name[1]	Address[2]	Type[3]	Parameter format[4]	Comment	Default[5]
Interface Registers[6]					
CmdIfStat	000 0000 --00	R	R: 0000 0000 00VV VVVV	Return interface status	$0000
CmdIfCtrl	000 0000 --01	BWR	W: ---- ---- ---- -VVV R: 0000 0000 0000 0VVV	Set / return interface controls (active low resets)	$0003
SubSDelay	000 0000 --10	R	R: 0000 000V VVVV VVVV	Return Subsystem response time	$01FF
TStampRst	000 0000 --11	BW	W: ---- ---- ---- ----	Reset time stamp	NA
Unmapped Area					
Unknown1	--- 0001 ----	NA	Not Applicable	Used to test timeout on unknown address	NA
Unknown2	--- 001- ----	NA	Not Applicable	Used to test timeout on unknown address	NA
Unknown3	--- 01-- ----	NA	Not Applicable	Used to test timeout on unknown address	NA
Configuration and Status Registers					
ScuStatus	--- 100- -000	R	R: Not yet defined	Return Subsystem status	$0000
FrRequest	--- 100- -001	W	W: ---- ---- ---- ----	Initiate frame sequence transfer	NA
FrameStop	--- 100- -010	W	W: ---- ---- ---- ----	Stop frame sequence transfer	NA
FrameConf	--- 100- -011	WR	W: V--- ---- VVVV VVVV R: V000 0000 VVVV VVVV	Set / return frame config (type + rate)	$0000
SeqLength	--- 100- -100	WR	W: ---- ---- ---- VVVV R: 0000 0000 0000 VVVV	Set / return number of frames per sequence (0 ≡ infinite)	$0000
TempOnOff	--- 100- -101	WR	W: VVVV VVVV VVVV VVVV R: VVVV VVVV VVVV VVVV	Set / return FPU temperature probe bias On/Off state	$0000
SubKOnOff	--- 100- -110	WR	W: ---- ---- ---- ---V R: 0000 0000 0000 000V	Set / return sub K temperature probe bias On/Off state	$0000
DRelOnOff	--- 100- -111	WR	W: ---- ---- ---- VVVV R: 0000 0000 0000 VVVV	Set / return LIA and BIA power relays On/Off state	$0000
TReserved	--- 101- ----	NA	lp	Reserved for test	NA
CcHkIf analogue resources					
LHeaterIV1	--- 1100 -000	WR	W: ---- IIII IIII IIII R: VVVV VVVV VVVV VVVV	Set current / measure voltage of Low Power Heater 1	Note [7,8]
LHeaterIV2	--- 1100 -001	WR	W: ---- IIII IIII IIII R: VVVV VVVV VVVV VVVV	Set current / measure voltage of Low Power Heater 2	Note [7,8]
LHeaterIV3	--- 1100 -010	WR	W: ---- IIII IIII IIII R: VVVV VVVV VVVV VVVV	Set current / measure voltage of Low Power Heater 3	Note [7,8]
HHeaterIV1	--- 1100 -011	WR	W: ---- IIII IIII IIII R: VVVV VVVV VVVV VVVV	Set current / measure voltage of High Power Heater	Note [7,8]
CsuTempRd	--- 1100 -100	R	R: VVVV VVVV VVVV VVVV	Measure CcHkIf board temperature	NA
TsuTempRd	--- 1100 -101	R	R: VVVV VVVV VVVV VVVV	Measure TEMP board temperature	NA
PsuTempRd	--- 1100 -110	R	R: VVVV VVVV VVVV VVVV	Measure PSU temperature	NA
ScuCHTp05	--- 1100 -111	R	R: VVVV VVVV VVVV VVVV	Measure +05VDC power supply	NA

[1] Parameters are listed in ascending address order.
[2] The "-" character denotes a don't care bit.
[3] B : supports broadcast write access ; W : supports write access; R : supports read access ; F : eligible for inclusion in the Data Frame ; NA : Not Applicable.
[4] The "-" character denotes a don't care bit ; The "v" character denotes a valid bit.
[5] The default value is obtained at Power On or after a Subsystem Reset command ; $hhhh indicates hexadecimal format ; NA : Not Applicable.
[6] Refer to AD 2 for details.
[7] The DAC is automatically placed to its lower possible value ($000) at Power On or Subsystem Reset.
[8] The read operation measures the voltage corresponding to DAC setting = $000.

Name[1]	Address[2]	Type[3]	Parameter format[4]	Comment	Default[5]
ScuCHTn09	--- 1101 -000	R16	R: VVVV VVVV VVVV VVVV	Measure -09VDC power supply	NA
ScuCHTp09	--- 1101 -001	R	R: VVVV VVVV VVVV VVVV	Measure +09VDC power supply	NA
Calibral1	--- 1101 -010	WRF	W: ---- IIII IIII IIII R: VVVV VVVV VVVV VVVV	Set / measure current applied to Calibration source 1	Note [7,9]
CalibraV1	--- 1101 –011	RF	R: VVVV VVVV VVVV VVVV	Measure voltage of Calibration source 1	Note [7,8]
Calibral2	--- 1101 –100	WRF	W: ---- IIII IIII IIII R: VVVV VVVV VVVV VVVV	Set / measure current applied to Calibration source 2	Note [7,9]
CalibraV2	--- 1101 -101	RF	R: VVVV VVVV VVVV VVVV	Measure voltage of Calibration source 2	Note [7,8]
Calibral3	--- 1101 -110	WRF	W: ---- IIII IIII IIII R: VVVV VVVV VVVV VVVV	Set / measure current applied to Calibration source 3	Note [7,9]
CalibraV3	--- 1101 -111	RF	R: VVVV VVVV VVVV VVVV	Measure voltage of Calibration source 3	Note [7,8]
Temp analogue resources					
FpuTemp01	--- 1110 0000	RF	R: VVVV VVVV VVVV VVVV	Measure FPU probe 01 temperature	Note[10,11]
FpuTemp02	--- 1110 0001	RF	R: VVVV VVVV VVVV VVVV	Measure FPU probe 02 temperature	Note[10,11]
FpuTemp03	--- 1110 0010	RF	R: VVVV VVVV VVVV VVVV	Measure FPU probe 03 temperature	Note[10,11]
FpuTemp04	--- 1110 0011	RF	R: VVVV VVVV VVVV VVVV	Measure FPU probe 04 temperature	Note[10,11]
FpuTemp05	--- 1110 0100	RF	R: VVVV VVVV VVVV VVVV	Measure FPU probe 05 temperature	Note[10,11]
FpuTemp06	--- 1110 0101	RF	R: VVVV VVVV VVVV VVVV	Measure FPU probe 06 temperature	Note[10,11]
FpuTemp07	--- 1110 0110	RF	R: VVVV VVVV VVVV VVVV	Measure FPU probe 07 temperature	Note[10,11]
FpuTemp08	--- 1110 0111	RF	R: VVVV VVVV VVVV VVVV	Measure FPU probe 08 temperature	Note[10,11]
FpuTemp09	--- 1110 1000	RF	R: VVVV VVVV VVVV VVVV	Measure FPU probe 09 temperature	Note[10,11]
FpuTemp10	--- 1110 1001	RF	R: VVVV VVVV VVVV VVVV	Measure FPU probe 10 temperature	Note[10,11]
FpuTemp11	--- 1110 1010	RF	R: VVVV VVVV VVVV VVVV	Measure FPU probe 11 temperature	Note[10,11]
FpuTemp12	--- 1110 1011	RF	R: VVVV VVVV VVVV VVVV	Measure FPU probe 12 temperature	Note[10,11]
FpuTemp13	--- 1110 1100	RF	R: VVVV VVVV VVVV VVVV	Measure FPU probe 13 temperature	Note[10,11]
FpuTemp14	--- 1110 1101	RF	R: VVVV VVVV VVVV VVVV	Measure FPU probe 14 temperature	Note[10,11]
FpuTemp15	--- 1110 1110	RF	R: VVVV VVVV VVVV VVVV	Measure FPU probe 15 temperature	Note[10,11]
FpuTemp16	--- 1110 1111	RF	R: VVVV VVVV VVVV VVVV	Measure FPU probe 16 temperature	Note[10,11]
SubKTempP	--- 1111 ----	R	R: VVVV VVVV VVVV VVVV	Measure FPU sub-K probe temperature	Note[12,11]

Table 17 SCU parameter list

The exact channel mapping for FpuTemp01-16 and Calibra1-3 will be added when available.

6.3 Data frame format

The currently proposed format of the SCU *Data Frame* is as follows.

[9] The read operation measures the current corresponding to DAC setting = $000.
[10] The sensor is automatically placed in an unbiased state at Power On or Subsystem Reset (**TempOnOff** = $0000).
[11] The read operation measures the residual voltage corresponding to an unbiased sensor.
[12] The sensor is automatically placed in an unbiased state at Power On or Subsystem Reset (**SubKOnOff** = $0000).

Word #	Name	Comment	Value/Range
0	FrameLength		29
1	FrameHeader	Hsk (normal mode) or Test Pattern	Hsk : $0020 Test : $0021
2 to 17	FpuTemp01 to -16	Frame Payload area	
18	SubKTemp		
19	CalibraI1		
20	CalibraV1		
21	CalibraI2		
22	CalibraV2		
23	CalibraI3		
24	CalibraV3		
25	FrameStatus	ADC latch-up flags	
26	TimeStampH	Higher half of TimeStamp	
27	TimeStampL	Lower half of TimeStamp	
28	LgtdlPrty	Longitudinal Parity	

Table 18 SCU Data Frame format

When the “Test Pattern” frame format is selected [configuration register **FrameConf**(15) = ’1’], the frame payload (Words #2 to #24) is replaced by a series of 16-bit words generated by a fixed seed pseudo-random generator (of the Linear Feedback Shift Register type).

7 Specification coverage

This section checks the SCU design and documentation against the requirements expressed in the specification document.

7.1 Requirement cross reference

The following table takes the requirements expressed in AD 1, and provides links to the sections were they are covered in this documentation.

DRCU-REQ # (from AD 1)	Link(s)	Comment
62	Figure 1 (p7); §5.2.1 (p45);	
63	Figure 1 (p7); §4.5 (p34); §4.6 (p38);	
64	Figure 1 (p7); Figure 1 (p35); Figure 29 (p39);	
65, 66, 67	Figure 1 (p7); §4.4 (p26) ; Figure 18 (p28);	
68	Not a direct SCU requirement	The SCU applies DPU write commands immediately; The DAC stabilisation time after a full swing step will be measured. See related discussion in §4.1.4.4 (p18).
69	Figure 1 (p7); §4.1 (p11); §4.2 (p19);	
70	Figure 2 (p12); Figure 10 (p20);	
71	Figure 10 (p20);	The Thermal Strap Heater is also current-driven by a 12-bit DAC
72	No more applicable	
73	See Req-62	
74	Figure 1 (p7);	
75	Figure 1 (p7); §6.3 (p49); Table 18 (p50);	
76, 77	Table 17 (p49);	
78	Table 18 (p50);	
79, 80, 81	Figure 1 (p7); §4.7 (p44); Table 17 (p49);	The TempMon analogue circuit is not described / analysed in this issue.
82	Table 17 (p49);	
83	Figure 1 (p7); §4.8 (p44); Table 17 (p49);	The PwrMon analogue circuit is not described / analysed in this issue.
84, 85	Figure 1 (p7); §4.5 (p34; Figure 26 (p36); §4.6 (p38); Figure 31 (p41); Figure 32 (p42);	
86	4.5.3(p35); Figure 29 (p39);	
87, 88	Table 15 (p29); Figure 22 (p33); Figure 23 (p33); Figure 24 (p34);	
89	Figure 21 (p32);	Calibrator temperature drift : Discussion and prototype measurements will be added.
90	Table 15 (p29);	
91a	Figure 10 (p20); Figure 11 (p20);	
91b	Figure 2 (p12); Figure 3 (p13);	
91c	Figure 10 (p20); Figure 15 (p25);	
92		See AD 5.
93, 94	Mechanical requirements to be updated.	
95		Power dissipation not yet evaluated.
96, 97	In rush current / power supply filtering specs to be updated.	No special circuit implemented for QM1.

Table 19 Requirement cross reference