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Herschel SPIRE

The Subsystem Control Unit (SCU)

This document describes the SCU, one of the 3 subsystems of the Herschel/SPIRE/DRCU electronic system.

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This section gives an overview of the Herschel/SPIRE/DRCU Subsystem Control Unit.

1.1 Applicable documents

1.1.1 Specification documents

- AD 1 : « DRCU Subsystem Specification », Sap-SPIRE-Cca-0025-00, V1.0.

1.1.2 Interface documents

- AD 2 : « DRCU Interface Control Document », Sap-SPIRE-Cca-0075-02, V1.0 ;
- AD 3 : « DPU Interface Control Document », SPIRE-IFS-PRJ-650, V1.0.

1.1.3 Technical documents

- AD 5 : « A Generic DPU Interface for SPIRE DRCU subsystems », SEDI-DRCU-OG-2002-1, V0.4 ;
- AD 6 : « Note on temperature measurement using CERNOX probe for the SPIRE and PACS instruments », C. CARA - 28/06/01 ;

1.2 Overview

The Subsystem Control Unit (SCU) is an ancillary unit of the DRCU, in charge of various acquisition, control, support and monitoring functions, as specified in AD 1.

1.2.1 Acquisition and control functions

The SCU is in charge of the following low-level acquisition and control functions :

- Control and monitoring of the cryo-cooler heaters (recycling heater [SCU-FUNC-01], gas switch heater [SCU-FUNC-02] and FPU thermal strap heater [SCU-FUNC-03]) ;
- Control and monitoring of the photometer and spectrometer IR calibrators (PCAL, SCAL 2% and SCAL 4%) [SCU-FUNC-04] ;
- Acquisition of the FPU thermal sensors (thermometry subsystem) [SCU-FUNC-05, -06].

1.2.2 Support and monitoring functions

The SCU is in charge of the following low-level support and monitoring functions :

- Logical On/Off control of some PSU secondary power supplies (DCU-LIA P/S, MCU) [SCU-FUNC-13] ;
- SCU power supply monitoring [SCU-FUNC-07, -11] ;
- SCU and PSU electronics temperature monitoring [SCU-FUNC-07, -11] .

1.2.3 DPU interface functions

To support the above functions, the SCU decodes [SCU-FUNC-08] and responds [SCU-FUNC-09] to DPU commands, according to the DPU Cmd protocol. When in operation, it creates and produces a sequence of measurement Data Frames [SCU-FUNC-12], according to the DPU Data protocol. Each Data Frame carries the value of a relative Time Stamp, which is locally maintained in the SCU [SCU-FUNC-10].

1.2.4 Functional block diagram

The following diagram shows the functional organisation of the SCU.

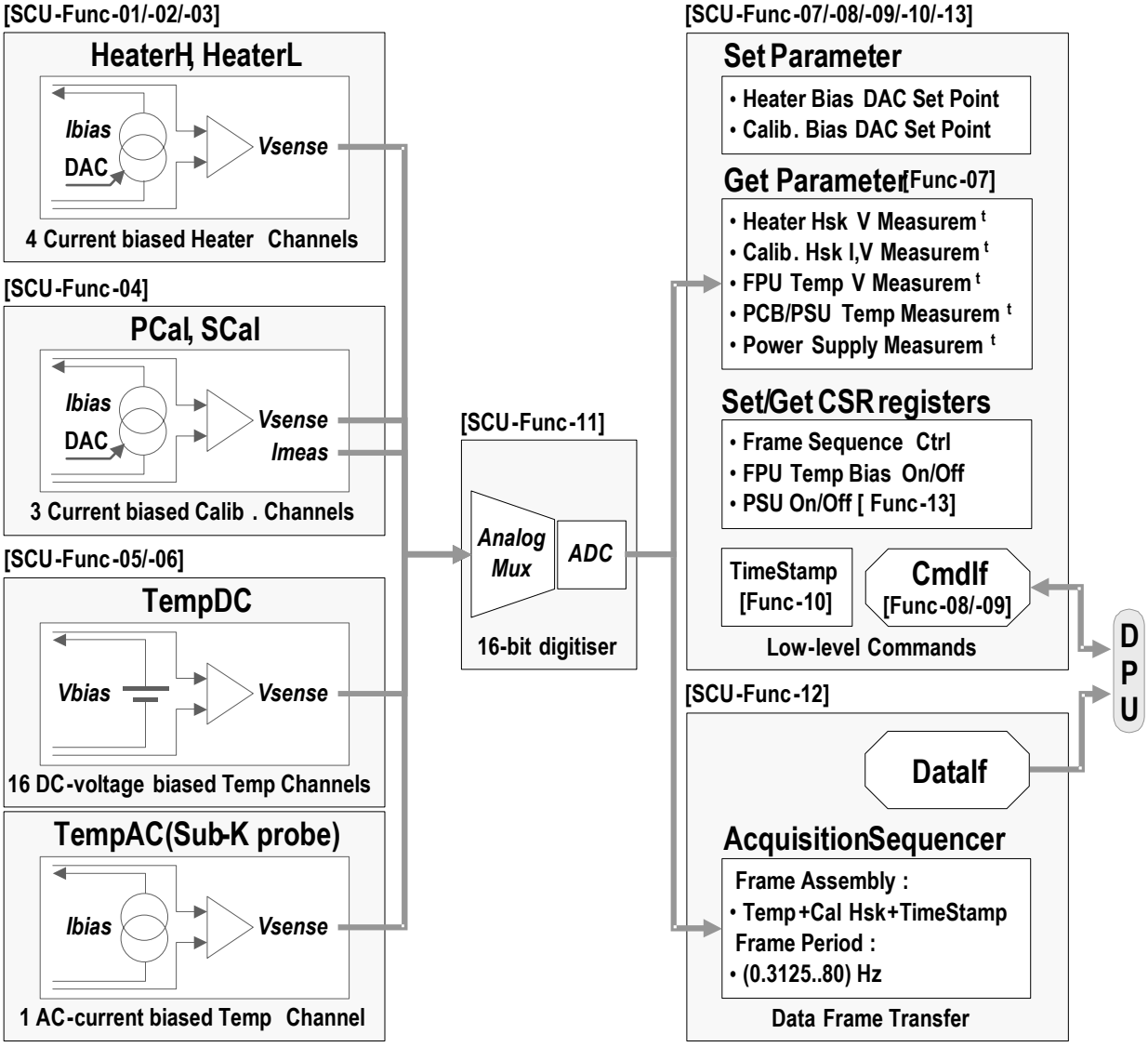


Figure 1 SCU Functional Block Diagram

2 Architecture

This section gives a general view of the SCU architecture and behaviour.

2.1 Structural block diagram

The SCU is implemented as a set of two active electronic boards –Temp and CchkIf– connected to a passive backplane board –Bkpln– as shown in Figure 2 .

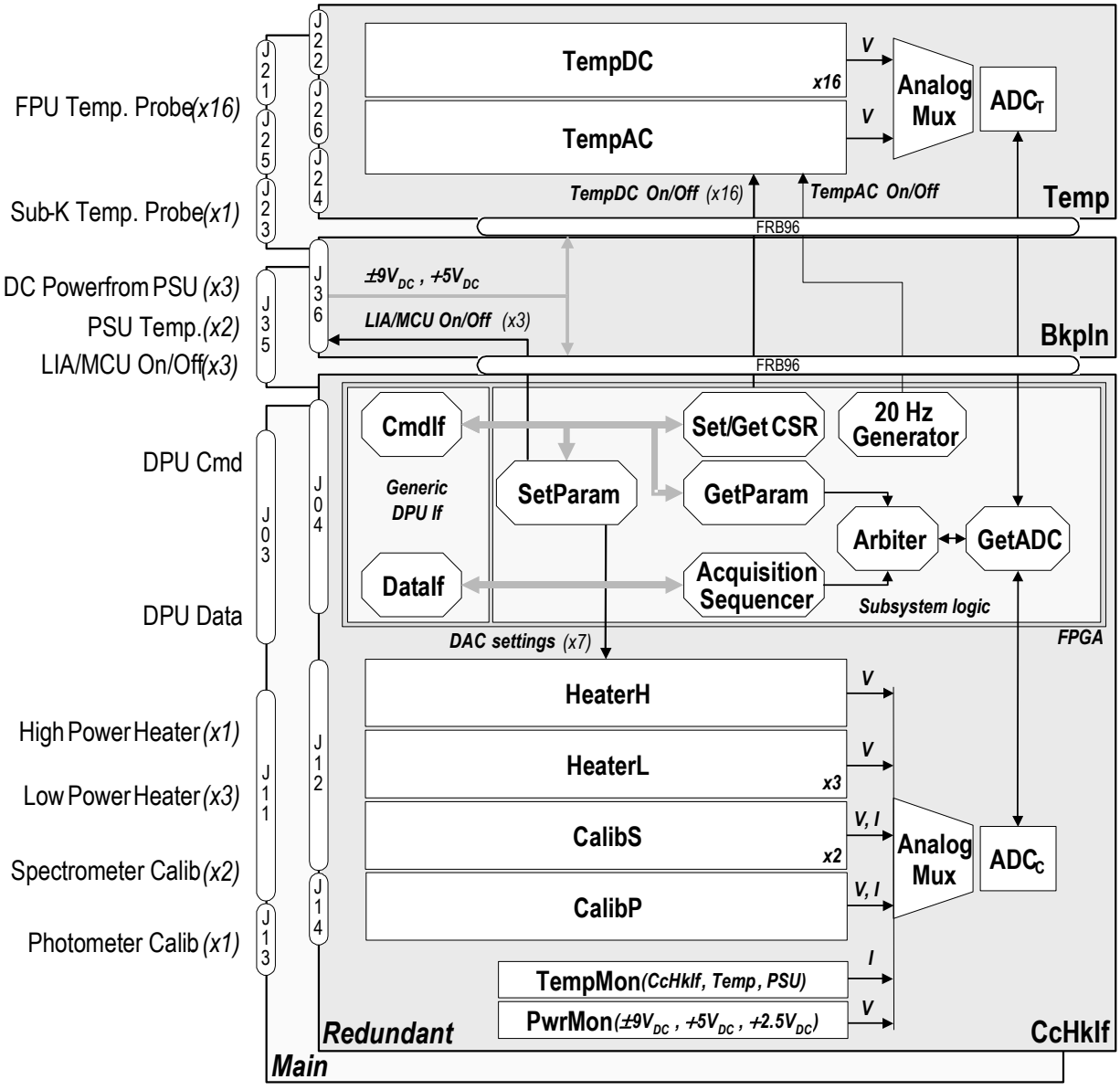


Figure 2 SCU Structural block diagram

The independent single-channel analogue signal conditioning circuits –TempDC, TempAC, HeaterH, HeaterL, CalibS, CalibP, TempMon and PwrMon– are supervised by the SCU Subsystem Logic. This logic is installed in a Field Programmable Gate Array (FPGA) logic cicuit.

2.2 Behaviour

The SCU is a slave device running under full supervision of the DPU software. Once initialised, it responds to DPU-initiated commands issued on the *Cmd Interface*. These commands first install the required configuration, and then start SCU operation.

2.2.1 Data frame sequence

When in operation, the SCU *Acquisition Sequencer* regularly prepares a well-defined *Data Frame* and autonomously transfers it to the DPU over the *Data Interface*. The frequency and duration of this *Data Frame* sequence are adjustable by configuration. The *Data Frames* are individually time stamped with a local clock value, which is also under control of the DPU software.

2.2.2 Subsystem parameter access

Asynchronous commands can be issued by the DPU at any time on the *Cmd* interface, to update or request a SCU parameter value.

2.2.2.1 Parameter update

SCU write-able parameters are updated immediately when the corresponding DPU write command is received and accepted, independent of the activity of the *Acquisition Sequencer*.

2.2.2.2 Parameter request

SCU readable parameters are provided when the corresponding DPU read command is received and accepted. However, the response time depends on the current activity of the *Acquisition Sequencer* when the request is issued. The SCU subsystem logic interleaves the atomic parameter sampling operations corresponding to either cyclic acquisition or asynchronous requests.

3 Digital functions

This section describes the functions handled by the FPGA circuit.

3.1 Generic DPU Interface

The DPU interface uses an instance of a generic design considered for all three DRCU subsystems (DCU, MCU and SCU). The detailed description of the generic part is given elsewhere (AD 5). Only the main features of this generic block are recalled here, to introduce the description of the SCU-specific control modules.

The generic interface handles the low level serial port protocol of the DPU *Cmd* and *Data* transactions, and presents 2 simple word-oriented interfaces to the subsystem logic :

- On the *Cmd* side, the subsystem parameter interface provides controlled read/write access to the subsystem parameters, seen as 16-bit words located at specific locations in a 12-bit address space.
- On the *Data* side, the subsystem data interface is a 16-bit parallel word register on which the subsystem places the individual 16-bit data words of the *Data Frame* payload in sequence. The encapsulation and transmission of the *Data Frame* is handled by the generic interface. For each *Data Frame*, the subsystem logic has the responsibility to signal completion of the payload with a “Last Word” indication. The SCU implementation does not use the optional FIFO mechanism of the generic interface.

3.2 SCU Subsystem Logic

Once activated, the *SCU Subsystem Logic* manages several concurrent threads of control :

1. *Acquisition Sequencer* : Automatic periodic parameter measurement, and associated word-per-word Data Frame payload construction ;
2. *Get Parameter* : On-demand analogue parameter measurement, in response to an individual DPU read command.
3. *Get CSR* : On-demand read access to a Control and Status Register (CSR), in response to an individual DPU read command.
4. *Set Parameter/CSR* : On-demand update of an analogue parameter or CSR register, in response to an individual DPU write command.

Operations 1. and 2. require a fresh value of the corresponding parameters, and compete for access to the involved analogue channels. A hardware time scheduling mechanism ensures forward progress for both operations. Operations 3. and 4. do not interfere with 1. and are handled independently.

3.2.1.1 Acquisition Sequencer

When the SCU is started, the *Acquisition Sequencer* schedules a sequence of cyclic acquisitions, and triggers the corresponding *Data Frame* transfers to be produced over the DPU *Data Interface*. The interval between acquisitions and the number of acquisitions expected for a particular operational run are both configured by dedicated parameters.

For each acquisition, the *Acquisition Sequencer* loops over the analogue parameters that are expected in the *Data Frame* payload. Each of them is selected in turn, converted to digital form and

presented to the *Subsystem Data* Interface for inclusion in the current packet. Each following word of the *Data Frame* payload is transferred piecewise when the *Acquisition Sequencer* has obtained a fresh measurement from the corresponding analogue section. The resulting *Data Frame* transfer seen by the DPU is not contiguous, and can be interleaved with atomic *GetParameter* actions issued on the *Cmd* Interface. The timing analysis of the *Frame* payload construction process shows that the analogue measurements in a *Data Frame* are always taken in a time interval shorter than 6 ms, even in presence of worst case *GetParameter* activity on the *Cmd* side.

4 Analogue functions

This section describes the analogue signal conditioning functions.

4.1 Sorption Pump heater (HeaterH)

4.1.1 Specification

The following table recalls the requirement for the cooler Sorption Pump high power heater [extracted from AD 1].

Type	Number	Heater Resistance	Lead resistance	Power	Max. Voltage	Interface type
Sorption Pump	1	402	≤ 40 Ω	0 to 500 mW	15V	2x2-wire

Table 1 Sorption Pump heater requirements

4.1.2 General description

The Sorption Pump heater control circuit –HeaterH– must develop a variable power dissipation in the [0 - 500 mW] range across the heater. With a 402 Ω heater resistance, the corresponding current range is [0 - 35.3 mA]. The corresponding [0 - 14.2 V] voltage across the heater is measured and made available to the DPU as part of the housekeeping parameters.

The DAC generates a [0 - 5V] voltage used to drive the current source. The current is equilibrated by the heater voltage feedback loop. This voltage is then used for the HSK measurement.

For proper operation at the required 14.2 V heater voltage (taking into account the additional voltage drop in the harness), bipolar operation is required. A second feedback loop lets the heater voltage develop between the positive and negative power rails.

Two current limiting blocks protect the SCU power supplies against a potential heater short circuit.

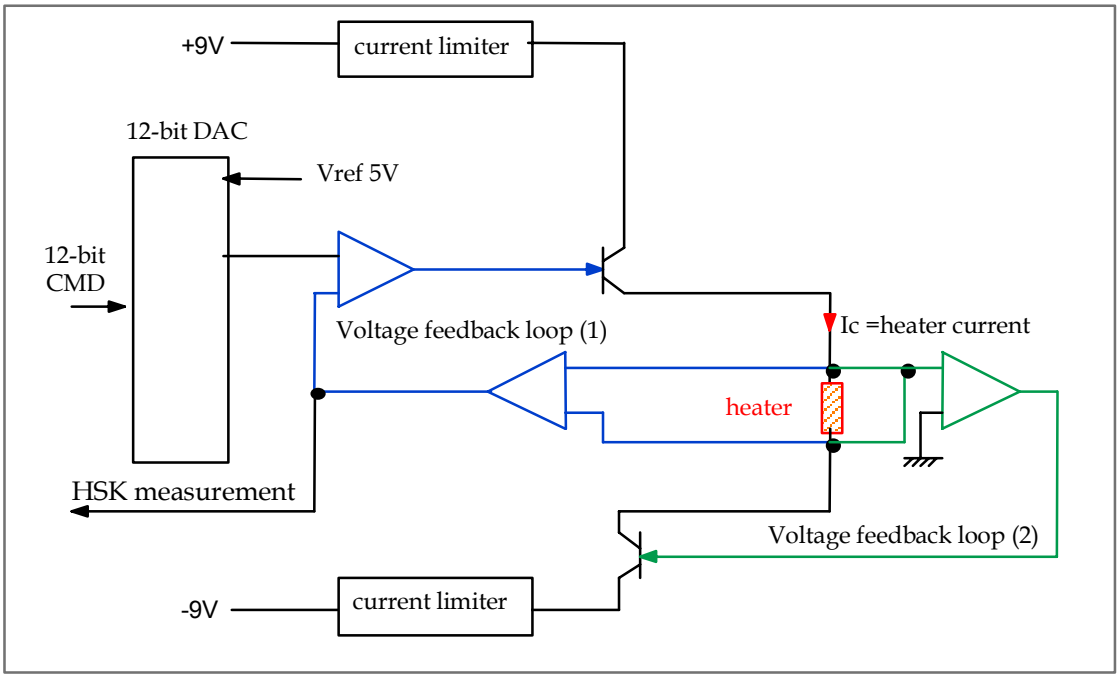


Figure 3 HeaterH circuit: Design principle

4.1.3 Simulation

The following simulations only cover the analogue part of the HeaterH circuit (assuming an ideal D/A converter).

4.1.3.1 Pheater = f(Ve)

The maximum heater power (0.5 W) is obtained for a 3.55 V DAC output voltage.

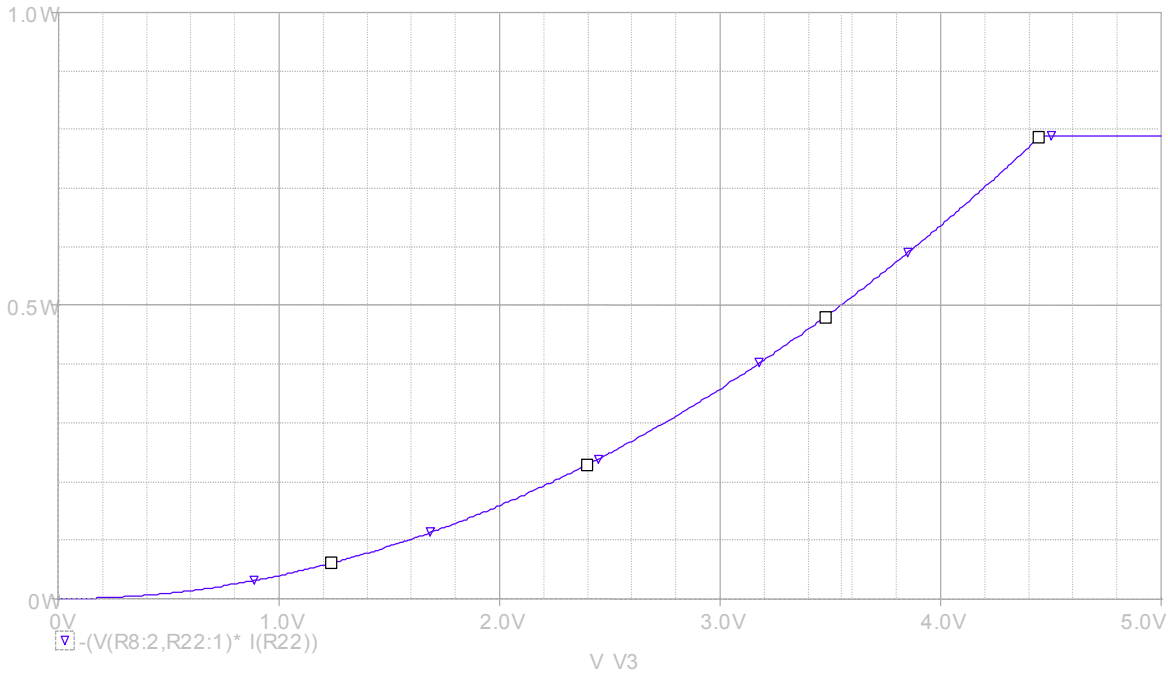


Figure 4 HeaterH simulation : Power variation

4.1.3.2 Ic(heater) = f(Ve)

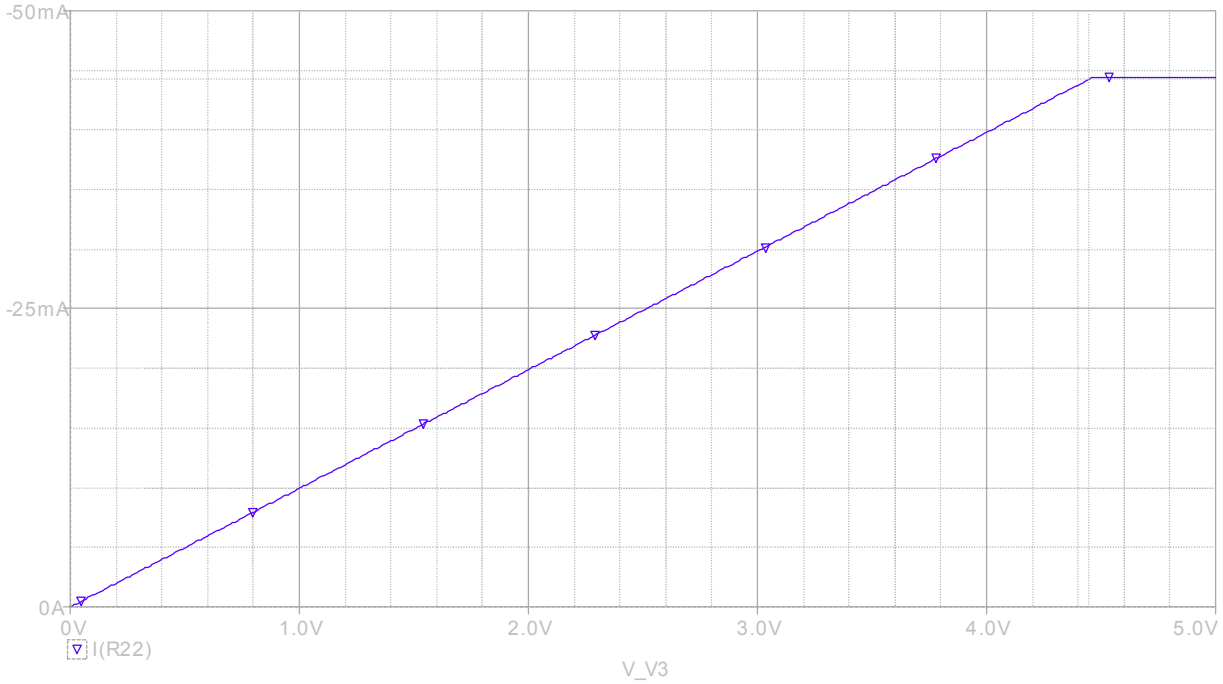


Figure 5 HeaterH simulation : Current variation

The transfer function is Ic(Heater) = 9,94 E^{-3} A/V * Ve in the linear range.

4.1.3.3 Pheater = f(Vhsk)

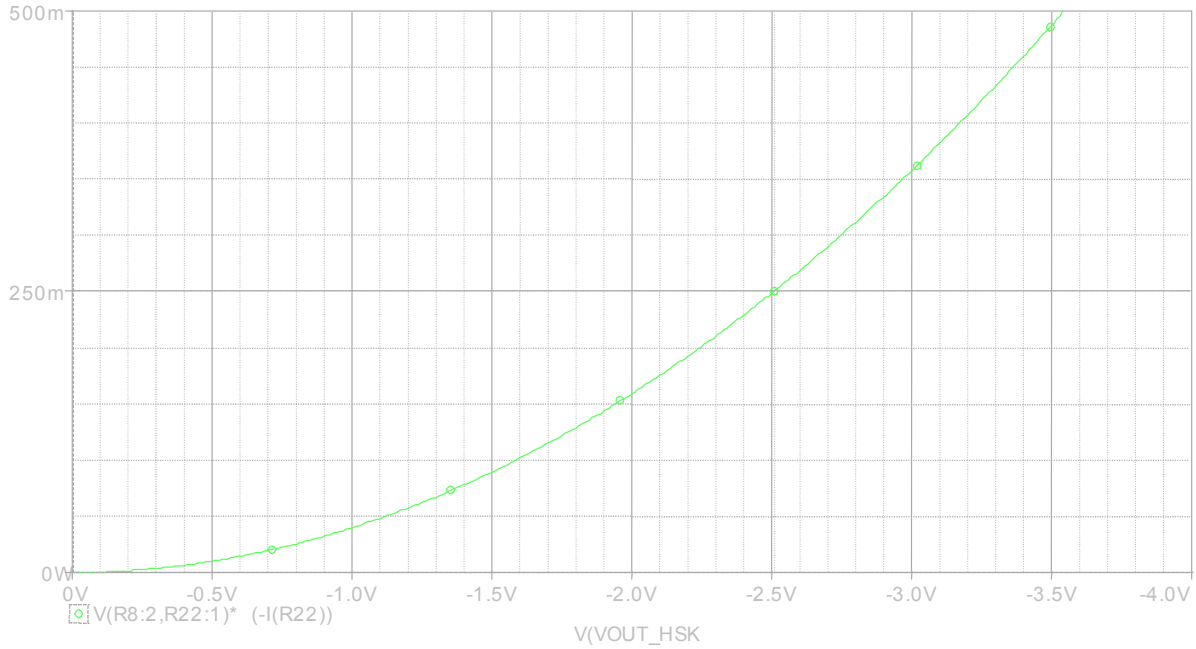


Figure 6 HeaterH simulation : Power dissipation vs HSK voltage

4.1.3.4 Residual current for Ve = 0V

For Ve = 0V, we obtain Ic = 466.4 pA.

4.1.4 Prototype test results

To validate the HeaterH electronic chain, we developed a prototype circuit with both the analogue and digital sections installed. The performance of this prototype was assessed at several temperatures (0°C, 25°C, 50°C). We verified the power supply rejection and the response to a DAC full swing adjustment step. We measured the circuit over a wide range of heater resistor values and checked the effect of a harness disconnect.

The performance of the analogue section at ambient temperature is :

Voltage Reference	DAC output voltage Ve(V)	Vheater (V)	Vhsk (V)	Ic (A)
0	0	20u	-67u	50n
0.5	0.49999	1.99943	0.49804	4.998575m
1	1.00004	4.00702	0.99804	10.01755m
1.5	1.4998	6.01479	1.4981	15.037m
2	1.9998	8.02342	1.9983	20.0585m
2.5	2.4998	10.0316	2.4985	25.079m
3	2.9995	12.03852	2.9983	30.0963m
3.5	3.4996	14.04678	3.4985	35.117m
4	3.9993	16.05384	3.9983	40.1346m
4.5	4.4994	16.57942	4.1293	41.448m
5	4.9996	16.57955	4.1293	41.448m

Table 2 HeaterH prototype : Measurements

As expected by simulation, we obtained the specified 500 mW power dissipation for a 3.5V DAC output voltage, and observed saturation at 690 mW. We measured a 50 nA leakage current, leading to a residual 1 pW dissipation in the heater.

4.1.4.1 Transfer function at 25°C

The transfer function at 25°C is as follows :

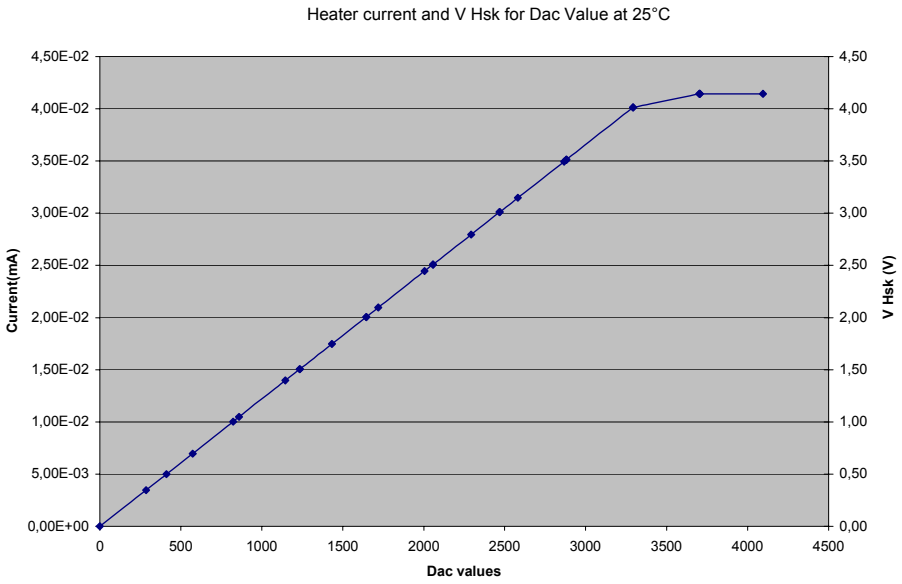


Figure 7 HeaterH prototype :Current variation

4.1.4.2 Variation with temperature

To evaluate the effect of temperature, we placed the analogue/digital electronic board in a thermal vacuum chamber and measured the heater current and HSK voltage at 0°C, 25°C and 50°C. The measurements were taken for several DAC settings with a nominal 402 Ω heater resistance.

The DAC output voltage dependence with temperature is as follows :

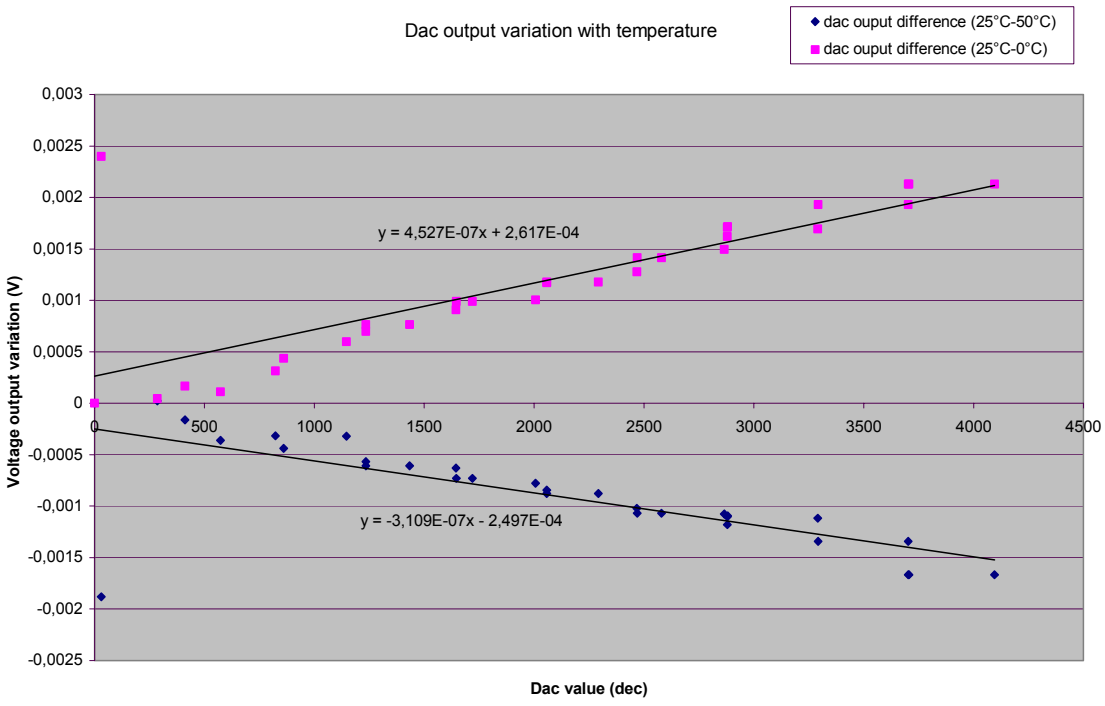


Figure 8 HeaterH prototype : DAC output voltage dependence with temperature

The DAC output voltage variation is linear with temperature. We find a similar variation on the HSK output, as shown below.

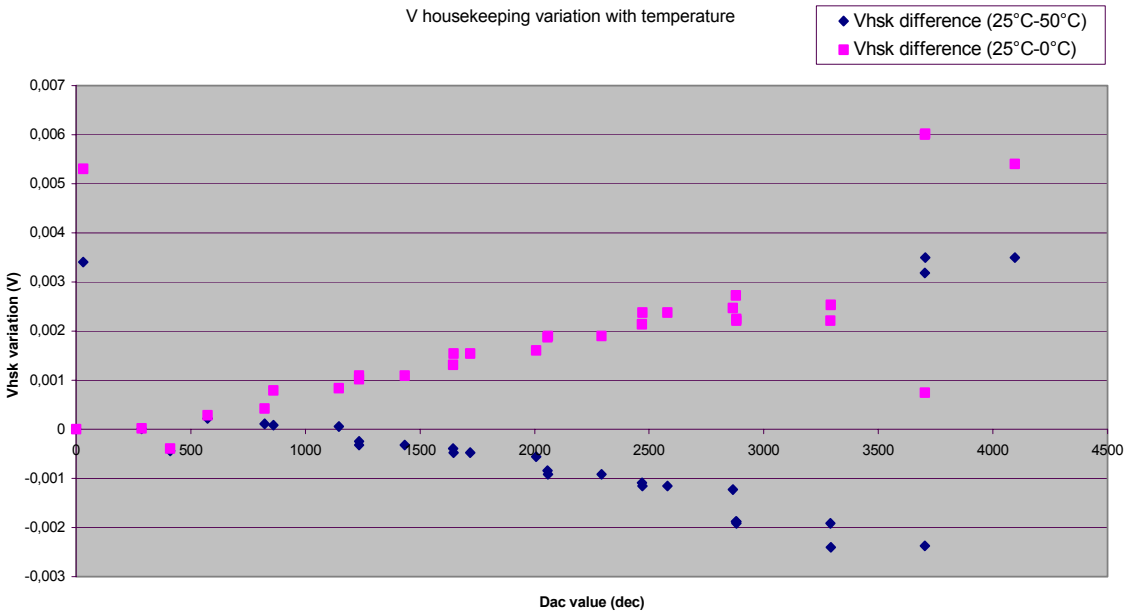


Figure 9 HeaterH prototype : HSK voltage dependence with temperature

The following figure shows the variation of current at 50°C and 0°C, as compared with the reference temperature (25°C).

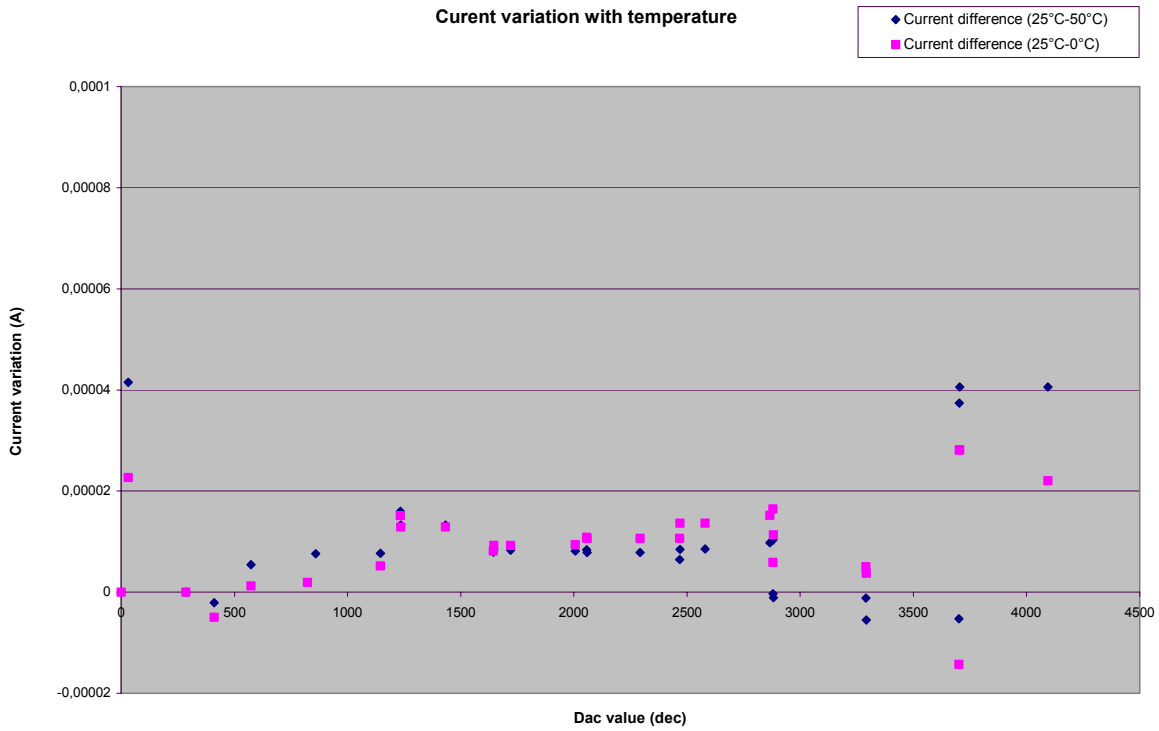


Figure 10 HeaterH prototype : Current dependence with temperature

The current dependence on temperature is not identical, but the total dispersion is less than 100 µA for a 50°C variation. The temperature stability of this design is sufficient for the precision required. If necessary, these systematic effects can be calibrated.

4.1.4.3 Power supply rejection

The power supply rejection is measured at 10% and 90% of the maximum DAC value, with a ±1 V perturbation added to the nominal 9V DC supply. The results are shown in the following tables.

DAC value	Power supply	Is	Relative error (%)	Vhsk	Vch
287 (dec)	Nominal 9V	0.00349925		0.34868	1.3997
	Nominal –1V = 8V	0.003501175	0.055	0.34887	1.40047
	Nominal +1V =10V	0.0034973	-0.055	0.34849	1.39892

Table 3 HeaterH prototype : Power supply rejection @DAC=287

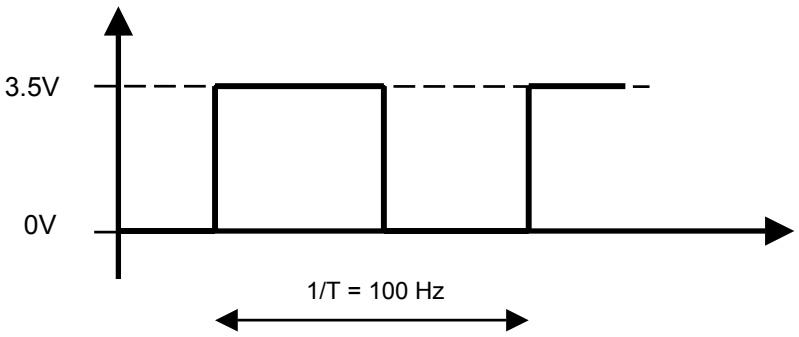
DAC value	Power supply	Is	Relative error (%)	Vhsk	Vch
2570(dec)	Nominal 9V	0.0314975		3.1379	12.599
	Nominal –1V = 8V	0.0314984	0.0028	3.138	12.59936
	Nominal +1V =10V	0.0314963	-0.004	3.1378	12.59852

Table 4 HeaterH prototype : Power supply rejection @DAC=2570

The variation of current in the heater is 0.1% maximum for 2 volts of power supply variation. The power rejection is 0.05%/Volt.

4.1.4.4 Frequency response to a full swing command step

To evaluate the frequency response of the analogue section, we generated a square signal (0 and Imax) at 100 Hz and observed the output voltage with a differential oscilloscope. The frequency response of the electronics is 300 Hz.



4.1.4.5 Variation of the heater resistance

We observed the effect of varying the heater resistance. Keeping the input DAC setting identical, the system parameters were measured for several heater resistance values, including the short and open circuit conditions. We observed good stability on the actual heater voltage (Vheater) and the housekeeping output (Vhsk), showing the correctness of the voltage control loop and the absence of dependence on the resistance value.

DAC value	Rheater intended : actual	DAC output voltage	Vheater	Vhsk	Is (Vch/Rch)
3367 (dec)	0 Ω	3.4867	0	0.000311	-
	400 Ω : 399.3	3.48695	13.99687	3.4859	35 m
	500 Ω : 497	3.48695	13.9962	3.486	28.16 m
	1000Ω : 1001.3	3.48695	13.9963	3.486	13.97 m
	1500Ω : 1498.3	3.48695	13.99637	3.486	9.34 m
	2000Ω : 2004.4	3.48695	13.9964	3.486	6.98 m
	∞	3.48695	13.99648	3.486	0

Table 5 HeaterH prototype : Temperature variation @DAC=3367

The measured short circuit current limitation (Rheater = 0 Ω) occurs at 70 mA.

4.2 Heat Switch heater (HeaterL)

4.2.1 Specification

The following table recalls the requirement for the Heat Switch low power heaters [extracted from AD 1].

Type	Number	Heater Resistance	Lead resistance	Power	Max Voltage	Interface type
Heat Switch	2	402 Ω	≤ 100 Ω	0 to 1mW	15 V	2x2-wire

Table 6 Heat Switch heater specification

4.2.2 General description

The Heat Switch low power heater control circuit (HeaterL) is a variable current source controlled by a digital to analogue converter. The system must develop a variable power dissipation in the [0 - 1 mW] range across the heater. With a 402 Ω heater resistance, the corresponding current range is [0 – 1.5 mA]. The corresponding [0 - 634 mV] voltage across the heater is measured and made available to the DPU as part of the housekeeping parameters.

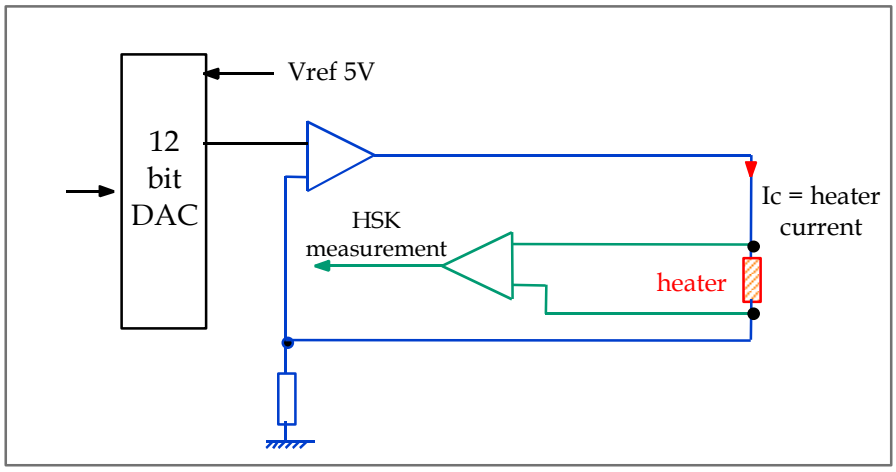


Figure 11 HeaterL circuit : Design principle

The DAC generates a [0 - 5V] voltage used to drive the current source. The current is equilibrated by the heater voltage feedback loop. This voltage is then used for the HSK measurement. The electronic circuit is protected against a potential heater short circuit by a series resistor.

4.2.3 Simulation

The following graphs show simulations for the power and current transfer, as function of the DAC output voltage Ve.

4.2.3.1 Pheater = f(Ve)

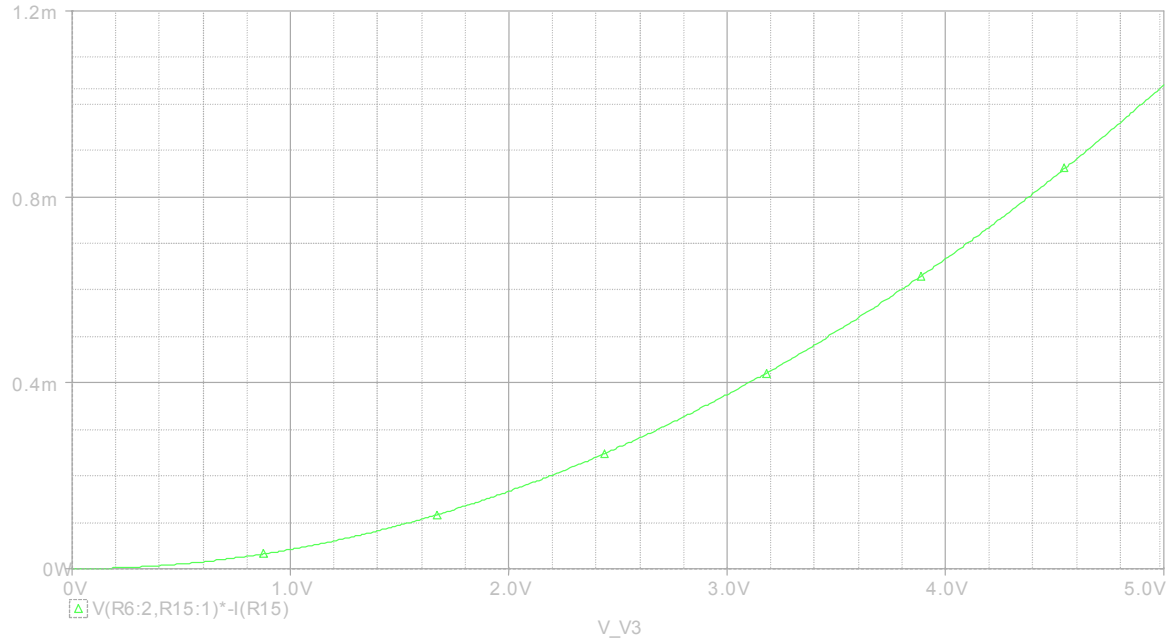


Figure 12 Heat Switch heater simulation : Power variation

4.2.3.2 Iheater = f(Ve)

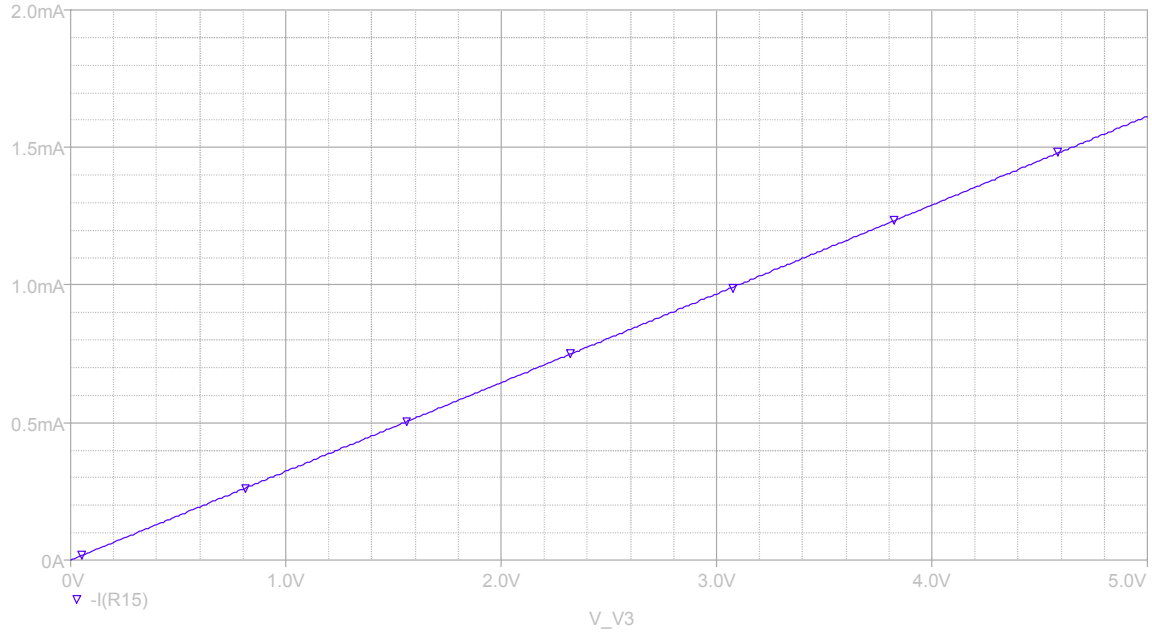


Figure 13 Heat Switch heater simulation : Current variation

The transfer function is Iheater = 323 µA/V * Ve in the linear range. The simulated current limiting saturation occurs at 1.6 mA.

4.2.3.3 Pheater = f(Vhsk)

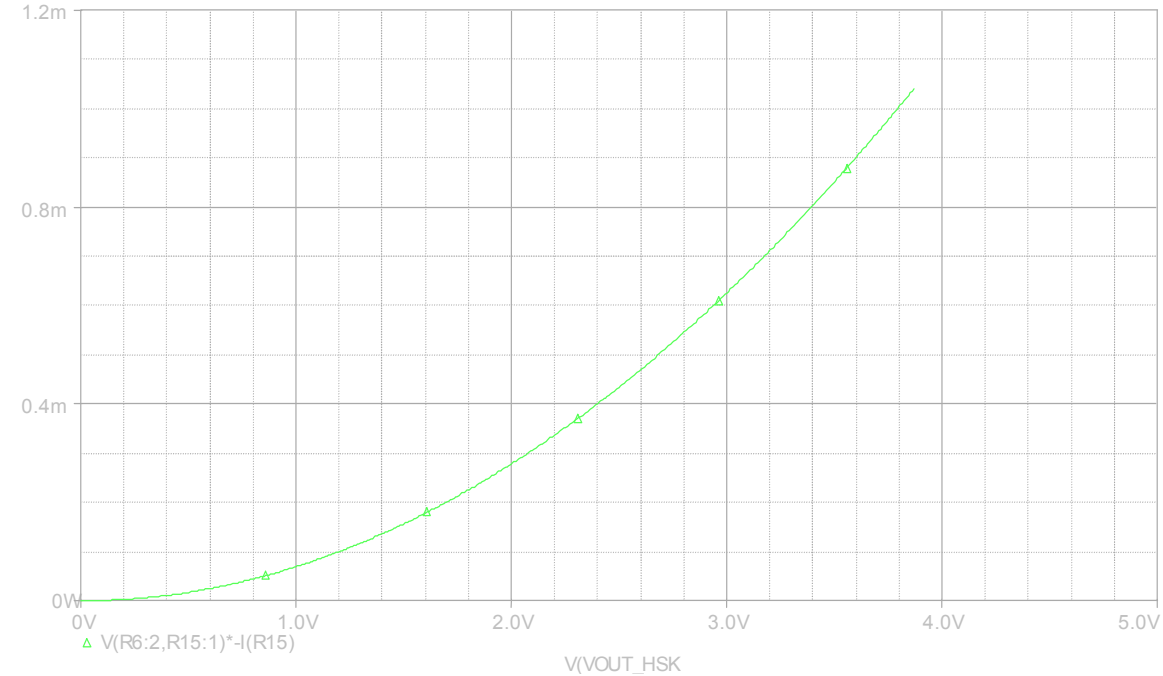


Figure 14 Heat Switch heater simulation : Power dissipation vs HSK voltage

4.2.4 Prototype test result

The performance of the analogue section at ambient temperature is :

Ve	Vch	Vhsk	Is
0	40u	40u	100n
0.5	64.1837m	383.1m	160.459u
1	128.409m	766.19m	321u
1.5	192.634m	1149.27m	481.585u
2	256.89m	1532.5m	642.22u
2.5	321.134m	1915.7m	802.835u
3	385.336m	2298.7m	963.34u
3.5	449.585m	2681.9m	1.124m
4	513.79m	3064.8m	1.284m
4.5	578.04m	3448.1m	1.445m
5	642.293m	3831.3m	1.6m

Table 7 Heat Switch heater prototype : Measurements

The prototype performs as expected by simulation.

4.2.4.1 Transfer function at 25°C

The corresponding linear transfer functions are as follows :

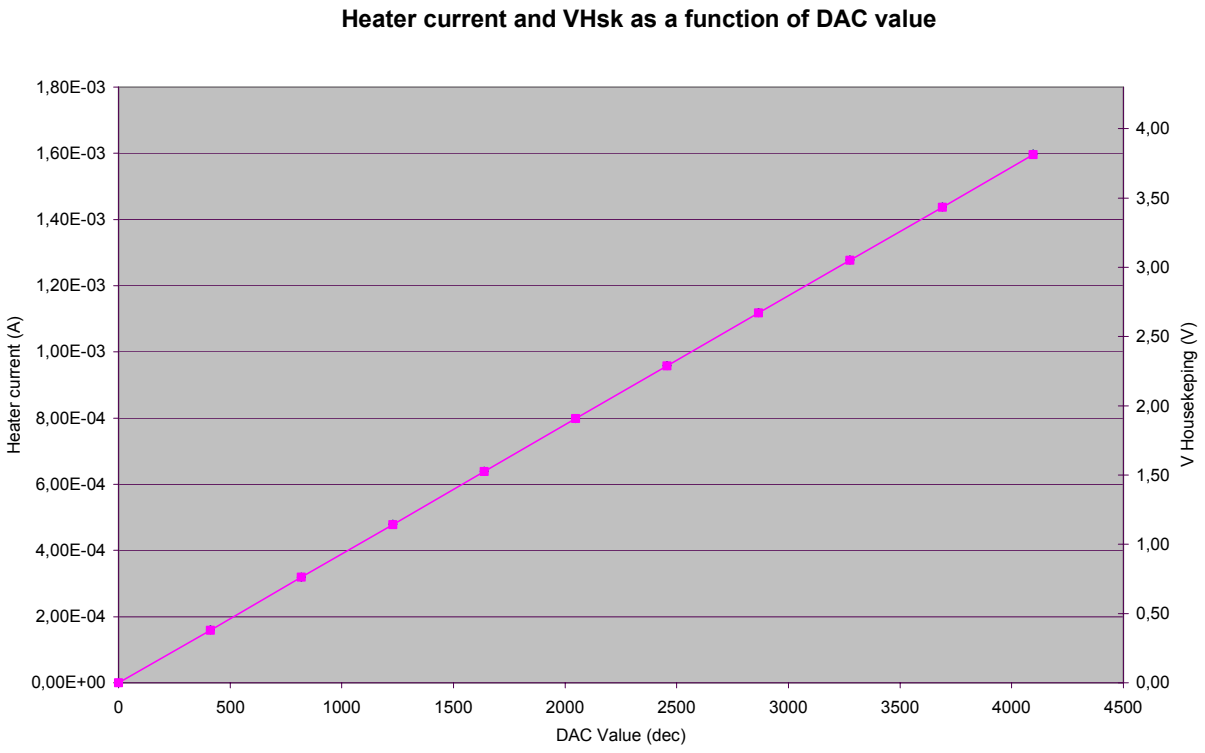


Figure 15 Heat Switch heater prototype : Current variation

Current (A) = 3.902 E^{-7} * DAC_value –1.023 E^{-7}

Hsk (V) = 2386. * Current + 5.01 E^{-4}

$$Hsk\ (V) = 9.311\ E^{-4} * Dac\_value - 2{,}566\ E^{-4}$$

The leakage current is 100 nA, corresponding to a minimum dissipation power of 4 pW in the heater.

4.2.4.2 Variation with temperature

The current drift is linear and reaches 2.5 μA at 50°C for the maximum current 1.6 mA (0.0018%/°C). The variation essentially comes from the DAC temperature drift.

Vhsk drifts in the same proportion. If required, the systematic current drift may be corrected from the HSK measurement.

4.2.4.3 Power supply rejection

The power supply rejection is measured at 10% and 90% of the maximum DAC value, with a ±1 V perturbation added to the nominal 9V DC supply. The results are shown in the following tables.

DAC word	Power Supply (V)	Ve (V)	Vch (V)	Vhsk (V)	Is (A)	Relative error (%)
196h	Nominal 9	0.49817	63.96m	0.38178	159.9u	----------
	8	0.49815	63.96m	0.38178	159.9u	0
	10	0.49818	63.965m	0.38178	159.9125u	0.0078

Table 8 Heat Switch heater prototype : Power supply rejection @DAC=$196

DAC word	Power Supply (V)	Ve (V)	Vch (V)	Vhsk (V)	Is (A)	Relative error (%)
E58h	9	4.4839	0.576028	3.4363	1.44007m	----------
	8	4.4838	0.576003	3.4361	1.44m	-0.0048
	10	4.4841	0.57604	3.4364	1.4401m	0.002

Table 9 Heat Switch heater prototype : Power supply rejection @DAC=$E58

We observe an excellent rejection, the effect on current being less than 0.01 %.

4.2.4.4 Variation of the heater resistance

DAC word	Heater resistor (R) (intended : actual)	DAC output voltage (V)	V heater (V)	V hsk (V)	Is (A) [Vheater/R]
FFFh	0 Ω	4.9762	40u	5.8m	Limited
	400 Ω : 399.3	4.9762	639.253m	3.8134	1.6009m
	500 Ω : 497	4.9762	795.57m	4.7446	1.6007m
	1000Ω : 1001.3	4.9762	1.60288	6.5846	1.6007m
	1500Ω : 1498.3	4.9762	2.31685	6.5652	1.546m
	2000Ω : 2004.4	4.9762	2.7703	6.5655	1.3821m
	∞	4.9762	5.6543	6.635	0

Table 10 Heat Switch heater prototype : Variation of heater resistance @DAC=$FFF

The current is stable for heater resistances lower than 1 kΩ. For upper values, the output operational amplifier reaches saturation at ≈ 6.33 V. The heater current is limited by a 2 kΩ resistor. In case of heater short circuit, the harness current is limited to 3.2 mA (6.33 V/2 kΩ).

4.3 TC heater (HeaterL)

4.3.1 Specification

The following table recalls the requirement for the TC low power heater [extracted from AD 1].

Type	Number	Heater resistance	Lead resistance	Power	Max. Voltage	Interface type
TC Heater	1	6 kΩ	≤ 1 kΩ	300mV/50uA		4-wire

Table 11 TC Heater specification

4.3.2 General description

The TC Heater circuit uses the the same design –HeaterL– as the Heat Switch heater circuits. The circuit produces a [0 – 50 μA] current. The maximum power is specified at 7.5 μW.

4.3.3 Simulation

4.3.3.1 Pheater = f(Ve)

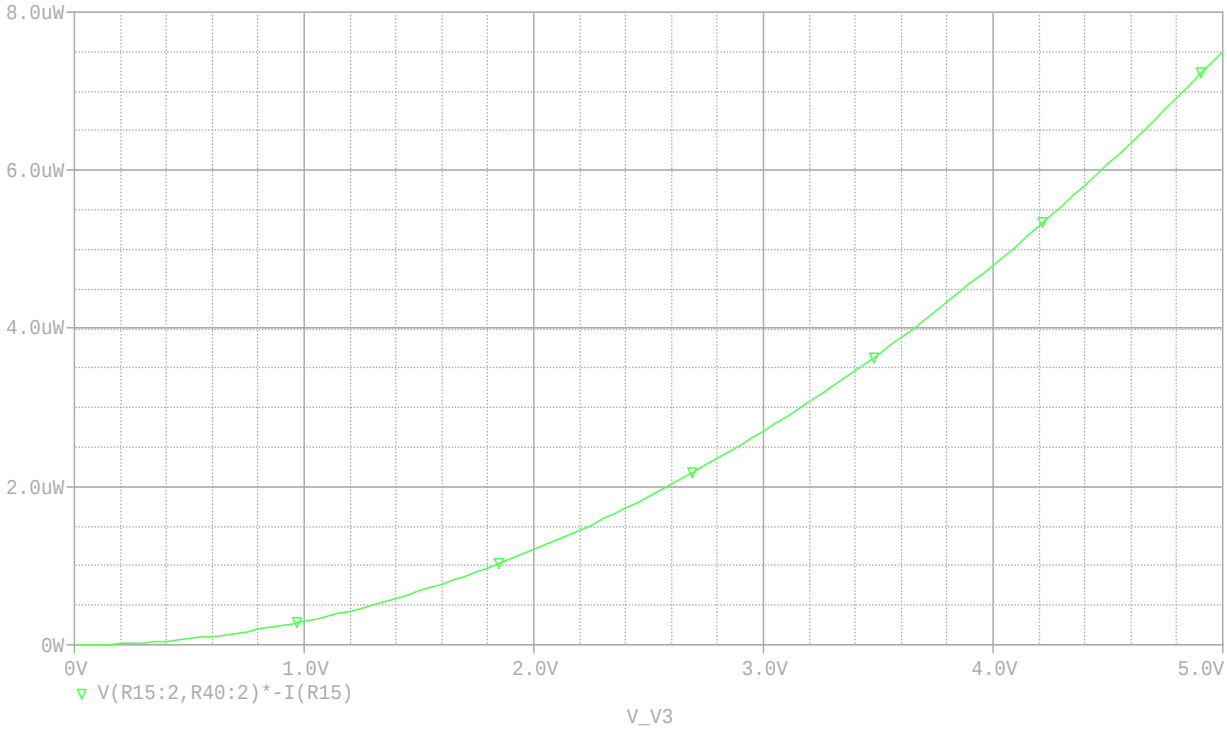


Figure 16 TC Heater simulation : Power variation

The maximum power dissipated in the heater (7.5 µW) is obtained for a 5V DAC output.

4.3.3.2 Ic(heater) = f(Ve)

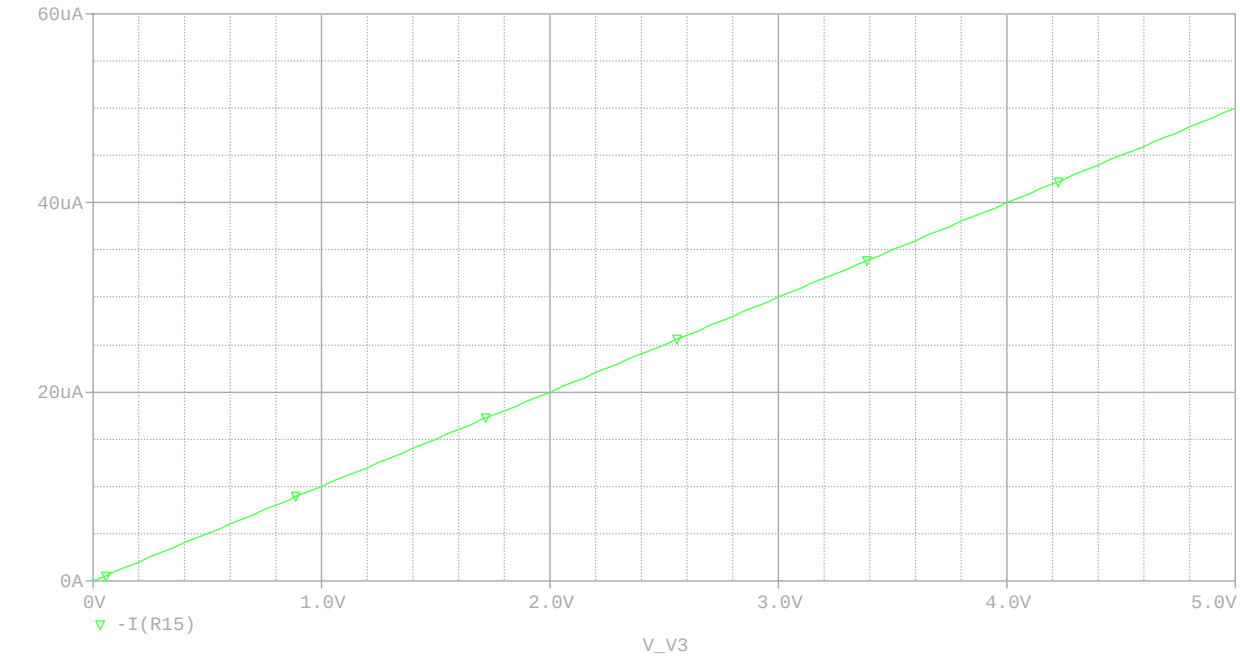


Figure 17 TC Heater simulation : Current variation

4.3.3.3 Pheater = f(Vhsk)

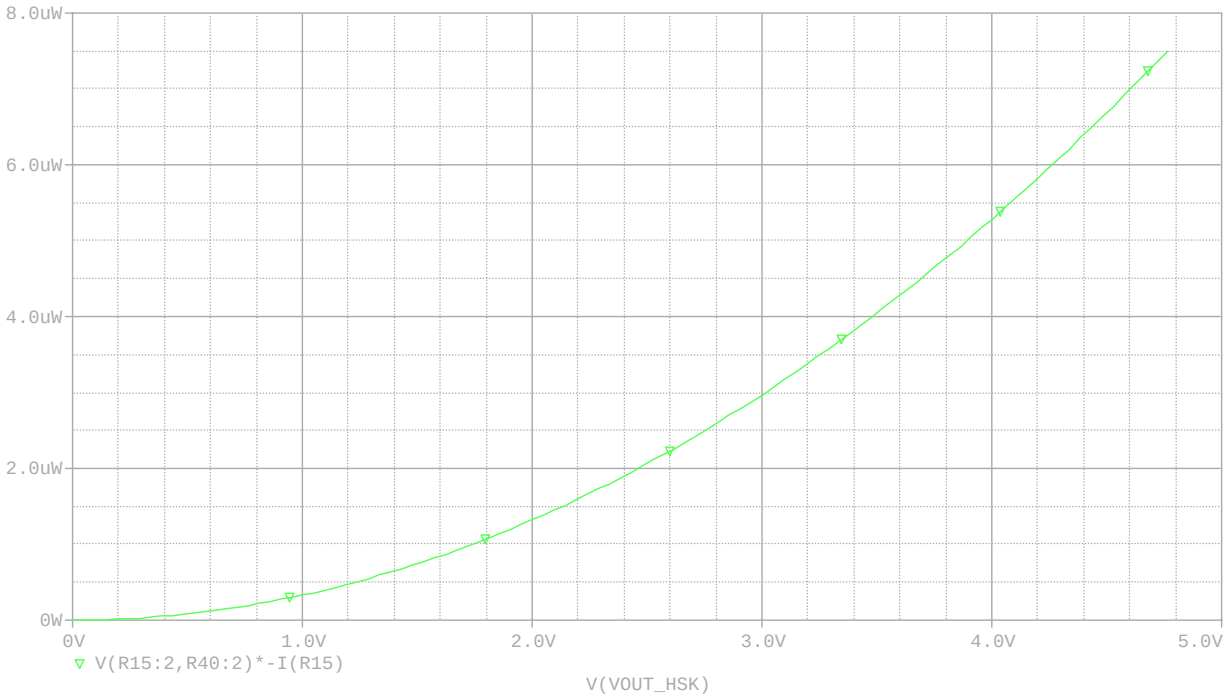


Figure 18 TC Heater simulation : Power dissipation vs HSK voltage

4.3.4 Prototype test result

The results for the TC Heater were derived from the HeaterL circuit prototype. In this design the leakage current for 0 DAC setting is 100 nA, leading to a residual power dissipation of 30 pW. The heater current is limited by a 50 kΩ resistor. In case of heater short circuit, the harness current is limited to 126 μA.

4.4 IR Calibrators : Pcal, Scal

4.4.1 Specification

The SCU controls the photometer calibrator (PCAL) and the 2 spectrometer calibrators (SCAL 2% and 4%).

For each of them, the SCU implements a DAC-controlled current source used to bias the heater resistor of the calibrator source and thus generate a reference IR emission level. The actual current applied to the source resistor and the corresponding voltage are measured, converted to digital form and made available to the DPU.

4.4.1.1 The photometer calibrator (PCAL)

The following table recalls the requirements for the PCAL bias current [extracted from AD 1].

Heater Bias Current Range	0 to 7 mA	in 4096 steps
Maximum dissipated power into heater	10 mW	
Heater Resistance Range	200 to 500 Ω	≤ 100 Ω for lead resistance
Stability / Repeatability	0.5 % or 5 µA	Whichever is greater
Maximum drive voltage	3.9 V	Worst case
Bias waveform	square	Spec. for DPU
Waveform frequency	0 to 5 Hz	Spec. for DPU
Waveform resolution	100 ms	Spec. for DPU
Interface Type	2x2-wire	None connected to ground

Table 12 PCAL calibrator specification

4.4.1.2 The spectrometer calibrators (SCAL)

The following table recalls the requirements for the SCAL bias current [extracted from AD 1].

Heater Bias Current Range	0 to 5.5 mA	in 4096 steps
Maximum dissipated power into heater	15 mW	
Heater Resistance Range	500 Ω	≤ 100 Ω for lead resistance
Stability / Repeatability	0.5 % or 5 µA	Whichever is greater
Maximum drive voltage	3.1 V	Worst case
Bias waveform	DC	
Electrical Interface Type	2x2-wire	None connected to ground

Table 13 SCALP calibrator specification

4.4.2 Circuit description

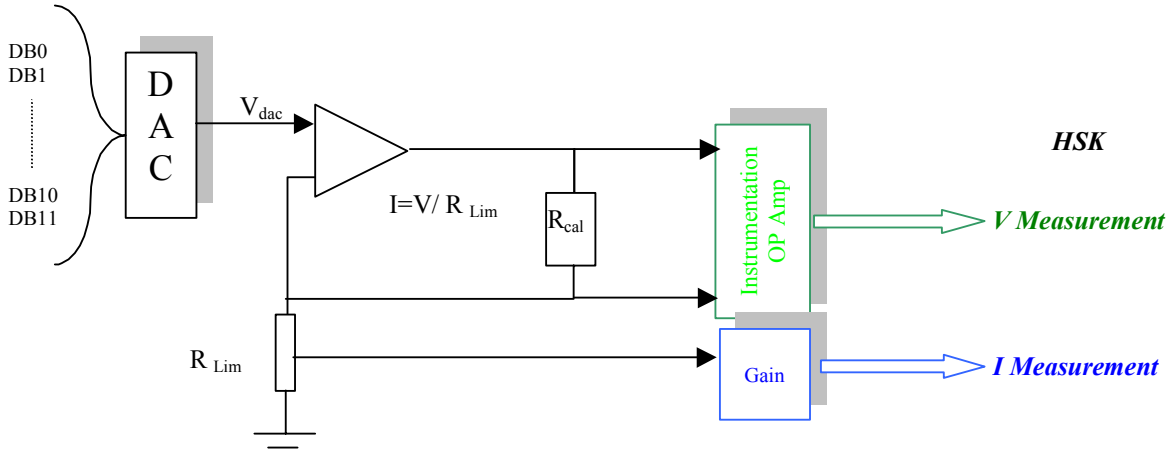


Figure 19 Calibrator current source principle

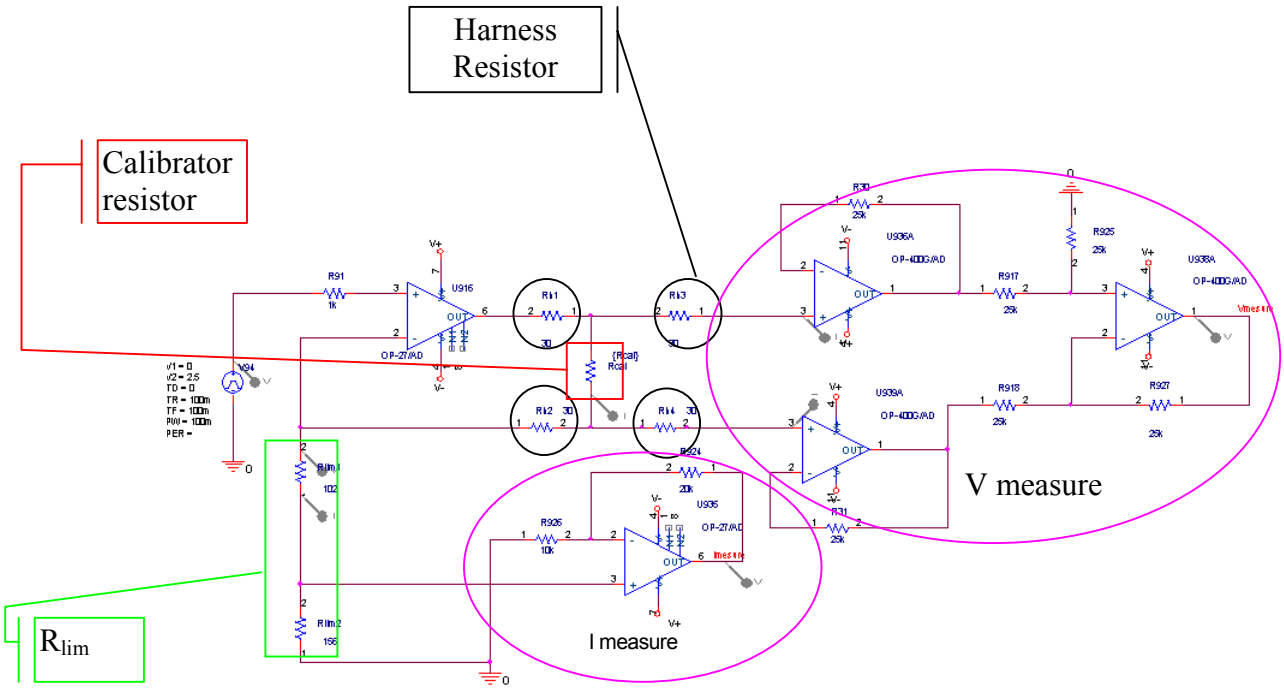


Figure 20 Calibrator current source circuit

4.4.2.1 *Current limitation*

The calibrator current is limited by the R_{lim} resistance at 0.01% of the maximum specified current value.

The value of R_{lim} is derived in the following expressions.

First, the maximum dissipated power allowed in the calibrator and the calibrator resistor value give the maximum current I_{max} expected in the heater.

$$I_{\max} = \sqrt{\frac{P_{\max}}{R_{cal}}}$$

Then, I_{max} and the the V_{ref} DAC reference voltage (2.5V) define R_{limit}.

$$R_{\text{lim}} = \frac{V_{ref}}{I_{\max}} \times \frac{4095}{4096}$$

The following table gives R_{lim} for the two different calibrators, and for the initial 9 mA prototype design.

Function	P_{max}	I_{range}	R_{cal} (Ω)	I_{max}	R_{lim} (Ω)
PCAL	10 mW	7 mA	200	7.16 mA	349
		4.5 mA	500	4.47 mA	560
SCAL	15 mW	5.5 mA	500	5.58 mA	448
Prototype	15 mW	9 mA	500	9.08 mA	274

Table 14 Current limitation for the PCAL and SCAL calibrators

4.4.3 Simulation

A SPICE simulation was used to verify the operation of the analogue part (from DAC output to I and V measurement).

The design was simulated for the more demanding current drive (Ical = 9 mA), with extreme values for the calibrator resistance (200 and 500 Ω). The stimulus applies a voltage ramp from 0 to 2.5 V, then a constant 2.5 V value and finally a decreasing voltage ramp from 2.5 V downto 0 V.

The result is shown on the following graph.

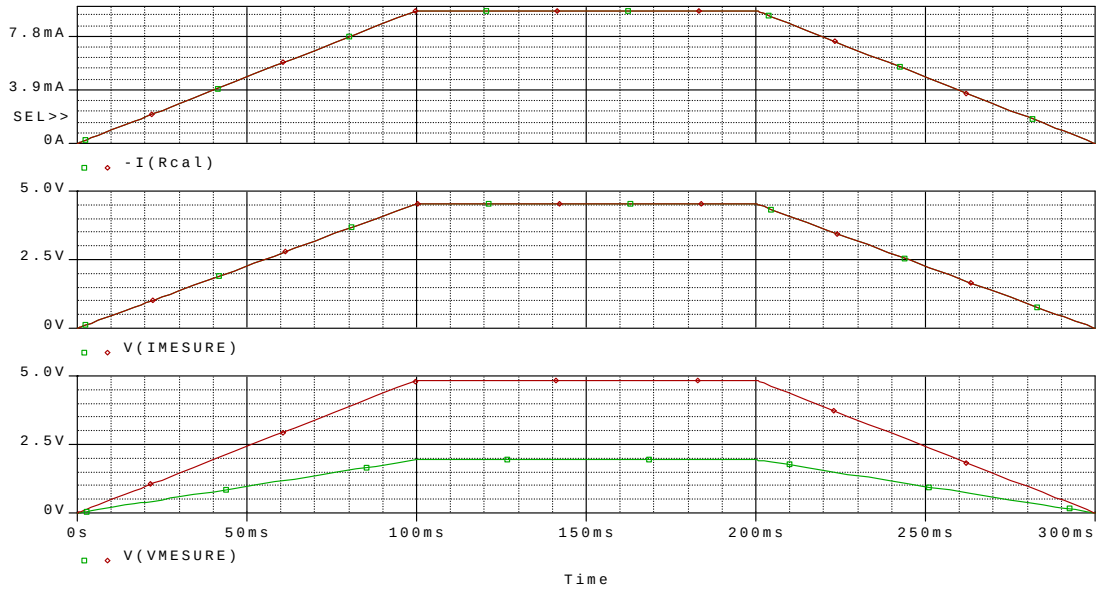


Figure 21 Calibrator current source simulation : Current and Imeas/Vmeas variation

4.4.4 Performance requirements

The specification does not specifically asks for absolute calibration, and does not directly define the expected integral and differential linearity. The main requirement is for stability and repeatability, asking for less than 0.5% relative variation over an hour. The main errors that may affect the stability (or repeatability) are the temperature drift and the power supply variations, which both need to be estimated. The maximum residual current that may be accepted when the source is shut off (DAC setting = 0) must also be controlled.

4.4.4.1 Residual current estimation

To estimate the residual current, we have to consider the sources of voltage offsets for Vdac :

- DAC leakage current : 50 nA ;
- Offset voltage of the OP27 operational amplifier : 100 µV

$$\delta_{dac} = 50 \quad 10^{9-} \times 15 \quad 10^{3} + 3 \times 100 \quad 10^{-6} = 1.05 \quad 10^{-3} \text{ (V)}$$

We have to add the current bias and offsets of the op-amps used in the current and voltage measurements. For the current measurement the OP-27 op-amp adds 155 nA, for the voltage measurement the OP400 adds 21.5 nA. The corresponding leakage currents are negligible.

4.4.4.2 Variation with temperature : calculation

The following calculations give a first estimate of the current and voltage temperature dependence. A more comprehensive error calculation for the current sources will take place in a further version of the present document.

The initial estimations of the current (∆I) and voltage (∆I) errors were done for the 9 mA prototype chain, where the highest current leads to the greatest absolute errors when the 5 µA stability / repeatability is expected. For the SCALF chain, the ratio between the current through Rcal and the DAC input code N is :

$$I(Rcal) = 2.228\ E^{-6} \times N$$

Each N step corresponds to a 0.61 mV voltage across the Rlim resistor. In the first approach, the errors that are very small compared to this value may be ignored.

The temperature-dependent parameters for all the components involved in the current source circuits are given in the following table.

Component	Parameter	Drift
OP27	Input offset voltage	1.8 µV/°C
OP27	Input bias current	± 0.8 nA/°C
OP27	Input offset current	0.75 nA/°C
OP400	Input offset voltage	1.2 µV/°C
OP400	Input bias current	0.028 nA/°C
OP400	Input offset current	0.014 nA/°C
DAC AD7545	Gain	± 5 ppm/°C
ADC ADS7809	Gain	± 2 ppm/°C
Voltage reference REF-02	Output voltage	8.5 ppm/°C
Resistors	Resistor value	50 ppm/°C

Table 15 Calibrator circuit: Component temperature dependence

The current value is I = V/Rlim so $\Delta I = I * (\Delta V/V + \Delta Rlim/Rlim) = \Delta V/Rlim + I * \Delta Rlim/Rlim$, where V is the voltage applied on the Rlim resistor.

The error on V is due to the current source, the DAC and three OP27 op-amps, for which the offset values and input bias currents flowing in resistors cause drifts. Taking into account the values listed on Table 15 and on the schematic drawing, the resulting ∆V error is the following :

$$\boxed{\Delta V \approx (20E^{-6}+V*14E^{-6})\ V/°C}$$

Since Rlim = 274Ω and $\Delta Rlim/Rlim = 5E^{-5}$, $\Delta I \approx 73E^{-9} + I * (14E^{-6} + 5E^{-5})$, and we obtain the ∆I expression :

$$\boxed{\Delta I \approx 73E^{-9} + I * 64E^{-6}\ A/°C}$$

As an example, for a full scale current of 9 mA (prototype study), the temperature drift error is : 0.65 µA/°C.

Because the current measurement is achieved by measuring the I * Rlim2/Rlim voltage, we may assume that the Rlim2/Rlim ratio is not temperature dependent, and thus will not contribute to the error calculation.

Calculating the temperature dependent errors on Imeasured and Vmeasured only needs to add the effects of the OP27 (for Imeasured) and three OP400 input offset voltages and currents, and the gain effects on the output ADC, as listed in Table 15 . We obtain :

$$\Delta(Vmeasured) = (4.6E^{-6} + 2.0\ E^{-6} * Vmeasured)\ V/°C$$

and

$$\Delta(Imeasured) = ((3.35E^{-6} + 2.0\ E^{-6} * Imeasured*Rlim2\ )/Rlim2)\ A/°C$$

The Rlim2 value is : Rlim2 = 274 Ω.

4.4.4.3 Variation with temperature : simulation

The temperature variation rate is expected to be lower than 3 K/h. The following simulation shows the current variation for T = 0°, 24°, 27°, and 30°C.

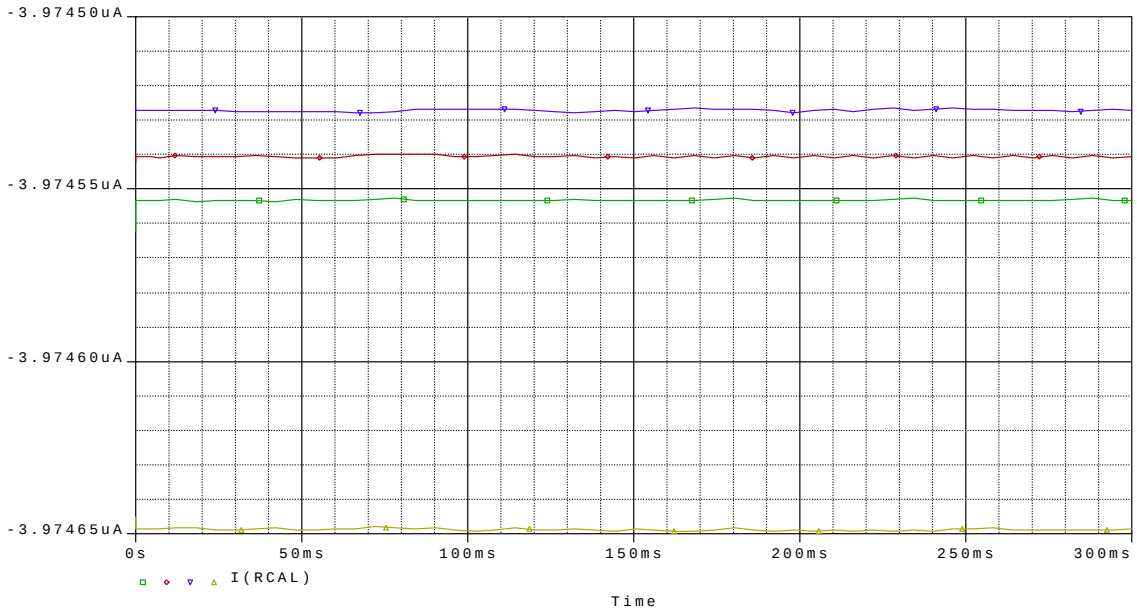


Figure 22 Calibrator current source simulation : Variation with temperature

4.4.5 Prototype test results

A prototype circuit was developed for the calibrator circuit. This circuit includes the DAC, the analogue circuitry (9 mA max drive), the ADC, and a FPGA for the logic interface with a Personal Computer. The current across the resistive load is measured with an external high precision GPIB-driven instrument.

The following graphs show recent measurements giving the linearity of the current production, and the linearity of the voltage and current housekeeping measurements.

4.4.5.1 DAC to current linearity

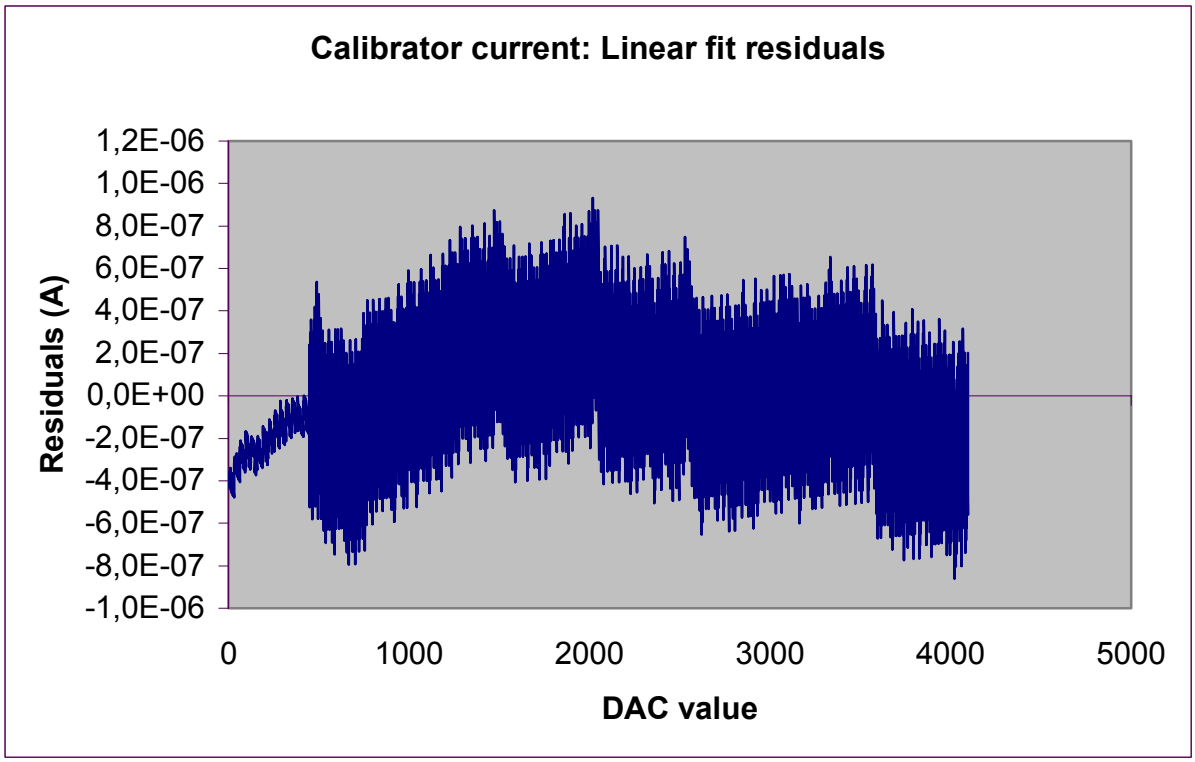


Figure 23 Calibrator prototype : DAC to current linearity

4.4.5.2 Voltage measurement linearity

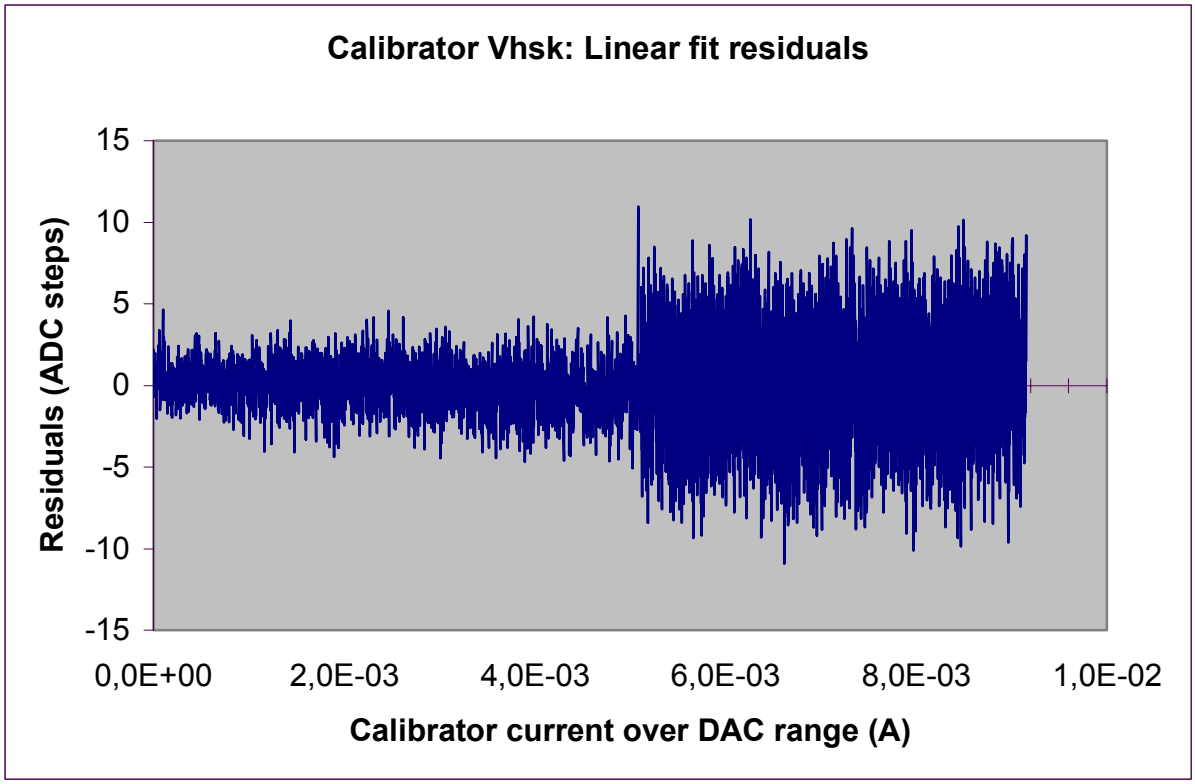


Figure 24 Calibrator prototype : Current to VHSK linearity

4.4.5.3 Current measurement linearity

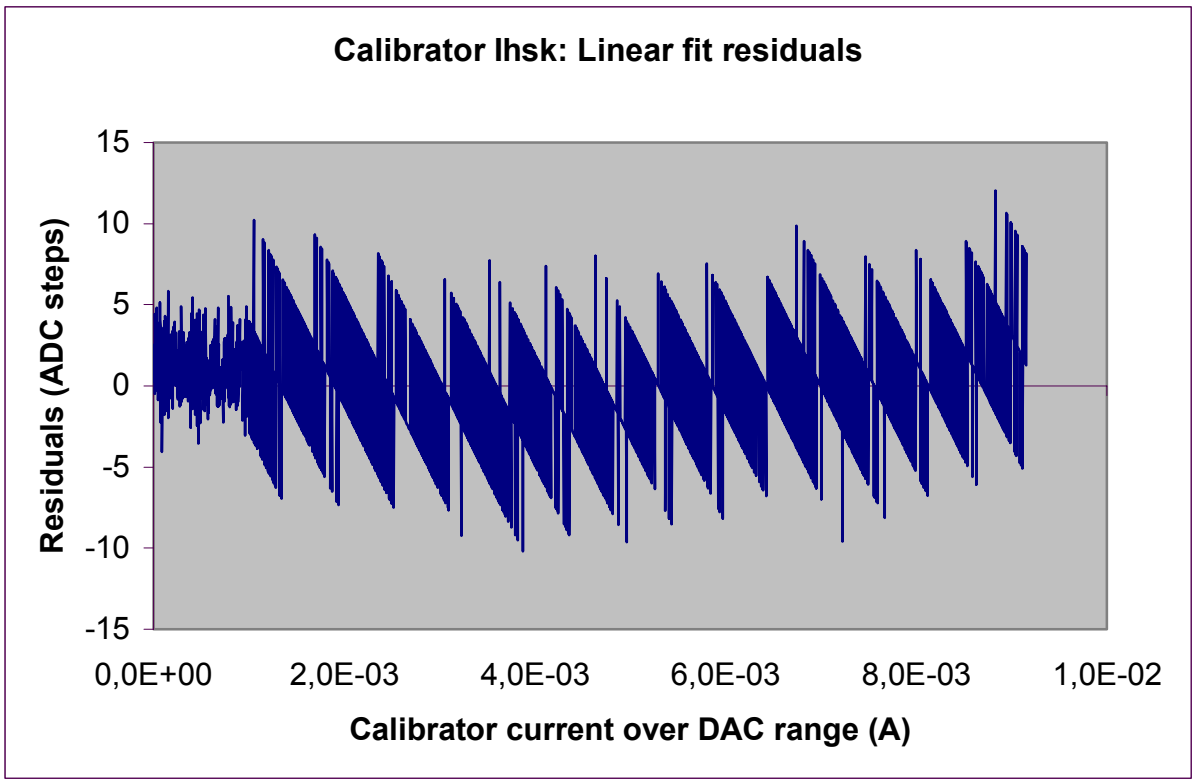


Figure 25 Calibrator prototype : Current to IHSK linearity

4.4.5.4 Variation with temperature

The prototype current variation with temperature was derived from measurements at 0°C, 25°C and 50°C. The measured variation is 25uA/50°C@9mA, corresponding to a relative dependence of less than 60 ppm/°C. The specification for relative stability asks for $5.E^{-3}$/h, with a maximum temperature drift of 3K/h. As a result, and without correction, the temperature variation will account for less than 4% of the total stability budget (180 ppm of the requested 5000 ppm/h).

4.5 Sub-K thermometry : TempAC

4.5.1 Specification

As extracted from AD 1.

4.5.2 Design principle

The resistance variation [R = f(T)] of the Cernox CX-1030 sensor shows a very strong dR/dT for temperatures lower than 2 K. To obtain the required 0.1 mK resolution at T = 300 mK, a high gain is necessary in the measurement chain. To cancel the low-frequency accumulated offset and temperature drift errors, a differential measurement is implemented. The sensor is AC biased at 20 Hz, and the measurements are synchronous with the AC excitation. Each temperature point results from the differential combination of two measurements taken synchronously with the 2 phases of the AC excitation. This measurement chain was developed in collaboration with the *Service de Basses Températures* (CEA/SBT).

The sensor is current biased, in order to obtain a broad measurement range (up to 10 K) with sufficient resolution while controlling the dissipation at the nominal 300 mK operating point. The

selected bias current value is 40 nA. At the operating temperature, the corresponding self-heating error is lower than 1 mK (to be compared with the 5 mK precision of the Cernox R(T) transfer curve).

4.5.3 Block diagram

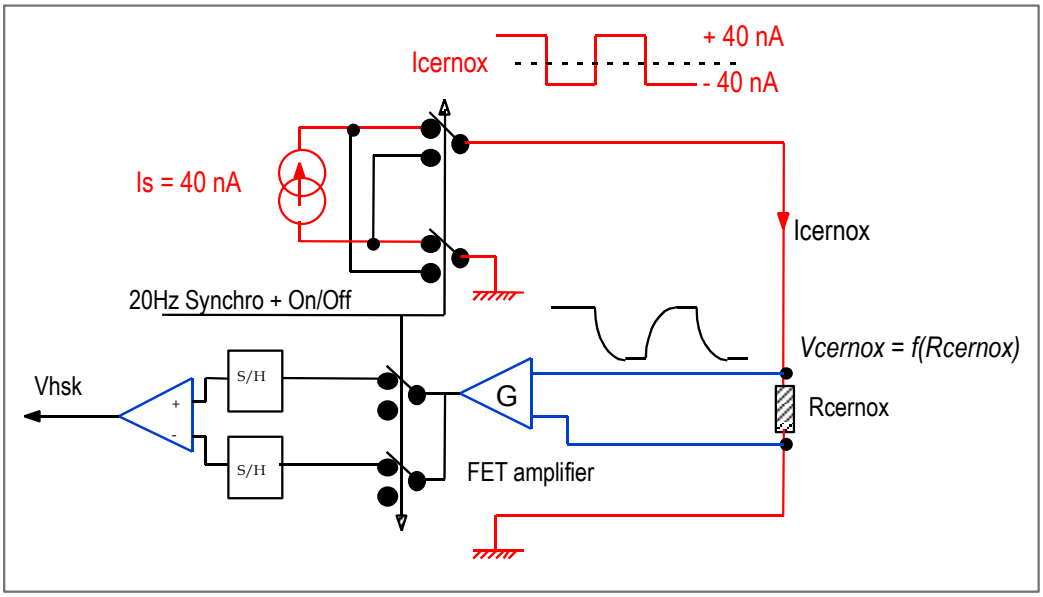


Figure 26 Sub-K bias circuit

The sensor current (Icernox) is a square waveform obtained by current steering from a stable current source (Is). The steering operation is driven by a 20 Hz digital square wave modulation command, alternately injecting +Is and –Is into the Cernox sensor. After amplification, the voltages corresponding to the positive and negative current phases are sampled and held in correlation with the steering command, and then passed to a differential analogue stage to produce the Vhsk measurement. The low frequency error contributions (LFErr) are suppressed by this method, Vhsk being Vcernox*G+LFErr – (-Vcernox*G+LFErr) = 2*G*Vcernox. This alternative measurement technique theoretically cancels the errors caused by bias currents, offset voltages and very low frequency noise sources.

4.5.4 Resolution

The Cooler Evaporator sensor must be sensitive in the [0.25K-10K] temperature range, with 0.1 mK resolution. Taking into account the R(T) response of the Cernox sensor, the expected resolution in the [260mK-1K] range is given in the following graph, computed with G = 800.

4.5.4.1 Expected resolution

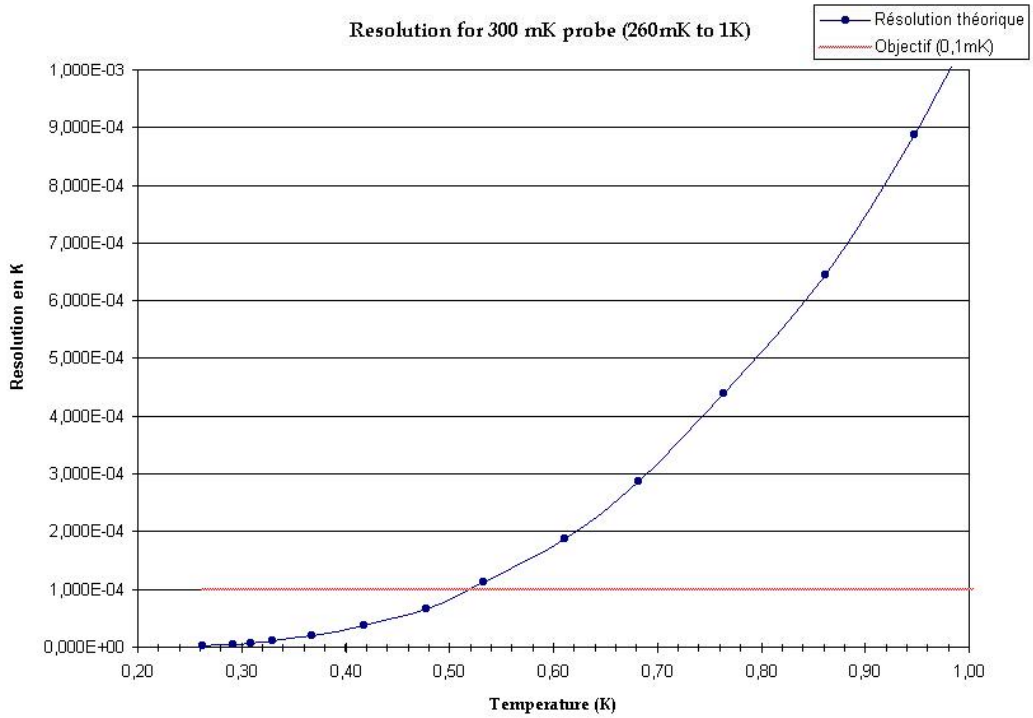


Figure 27 TempAC circuit : Resolution

The requirement for 0.1 mK resolution is easily fulfilled in the operating region (between 250 mK and 550 mK). For higher temperatures, the resolution degrades (1 mK@1K, 0.3K@10K) but is sufficient for gross temperature monitoring.

Due to the current bias technique, the voltage measurement chain may saturate at low temperatures, where the sensor resistance gets very large. The circuit is designed to operate linearly when the sensor resistance does not exceed 150 kΩ. This figure was selected to give sufficient margin from the Lakeshore specification, which gives R<100 kΩ @300mK.

4.5.5 Prototype measurements

To validate the TempAC electronic chain, we developed a prototype circuit with both the analogue and ADC sections installed. The linearity of the voltage measurement was verified over the full variation range of the Cernox resistance value. The performance of the prototype was assessed at several temperatures (0°, 10°, 20°, 30° and 40°C).

4.5.5.1 Vhsk = f(Rcernox)

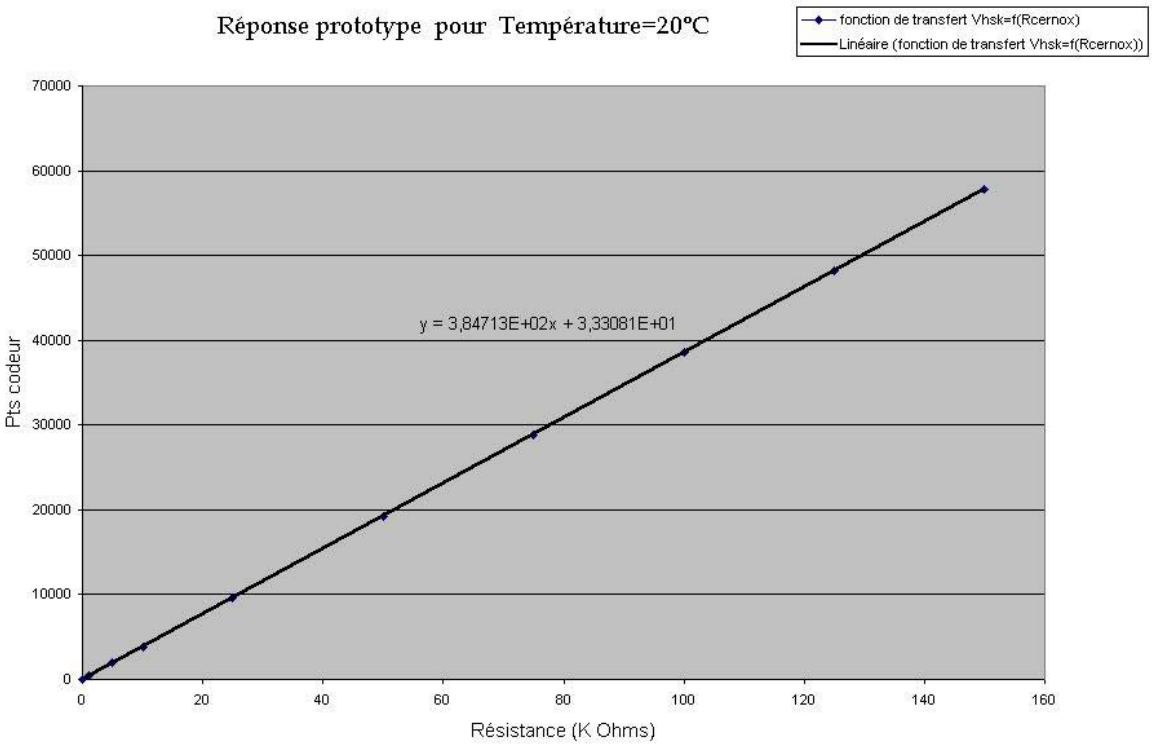


Figure 28 TempAC prototype : Vhsk (ADC-step) vs Resistance (kΩ)

The response curve was measured for several reference resistance values, chosen to cover the expected Cernox resistance variation range. The measurement confirms the linearity and the absence of saturation for resistance values as high as 150 kΩ. The measured slope is 384 ADC_steps/kΩ. The corresponding resolution is 3 μK/ADC_step @300 mK (R= 65 kΩ, dR/dT(mK) = 1000).

4.5.5.2 Variation with temperature

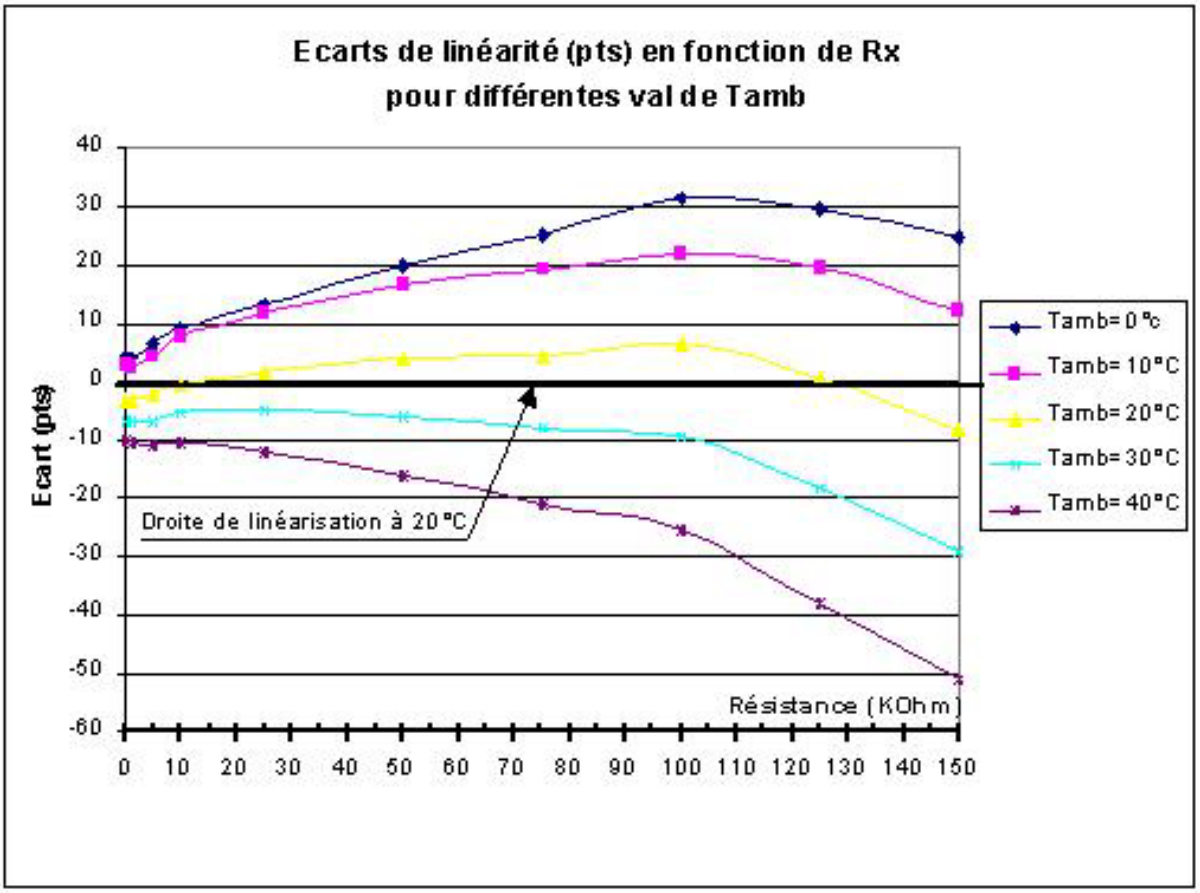


Figure 29 TempAC prototype : Variation with temperature

The above graph shows the variation of the response (expressed in ADC steps) when the circuit is placed at T= 0, 10, 20, 30 and 40°C. At R = 65 kΩ, a 40°C temperature variation displaces the response by 40 ADC steps, which corresponds to a brute error of 0.12 mK. The expected temperature variation of the electronics is much smaller, and compensation will normally be unnecessary ; if required, this systematic error could however be calibrated and compensated.

4.6 Other thermometry channels: TempDC

4.6.1 Specification

As extracted from AD 1.

4.6.2 Design principle

The TempDC circuit produces a fixed voltage bias across the Cernox CX-1030 sensor. The sensor current is measured by a simple current to voltage conversion, and reflects the resistance variation. The calibrated transfer function [R = f(T)] of the Cernox sensor is then used to obtain the temperature.

The rationale for the selection of the voltage bias technique is to obtain a slowly varying resolution over a broad measurement range, the Vhsk = k/R transfer function compensating the strong non-linearity of R(T) at low T values. A more involved discussion can be found in AD 6.

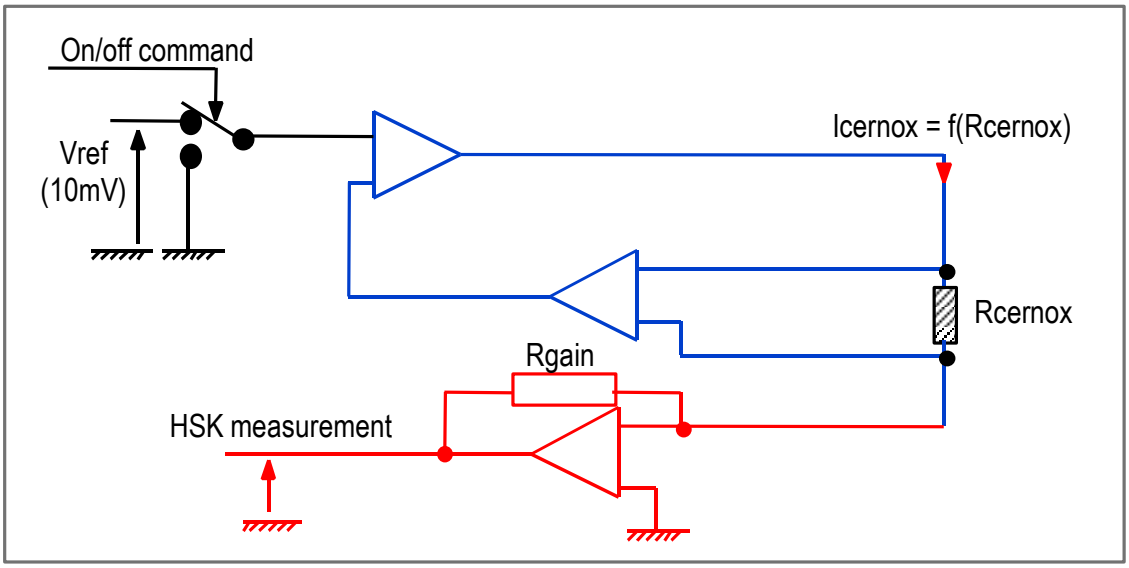


Figure 30 TempDC circuit : Block diagram

The HSK voltage is measured by a 16-bit ADC. The value of the Cernox resistance is derived from the current to voltage conversion formula : Vhsk = - Rgain * (Vref / Rcernox).

4.6.2.1 Bias voltage determination

The power dissipated in the sensor produces self-heating, which in turn disturbs the actual temperature measurement. This perturbation is difficult to estimate because the involved thermal impedance depends on several effects (material used in the sensor, thermalisation of the sensor, etc.). The selected bias voltage was defined after measurements obtained from the CEA/SBT. These measurements are shown in the following graph.

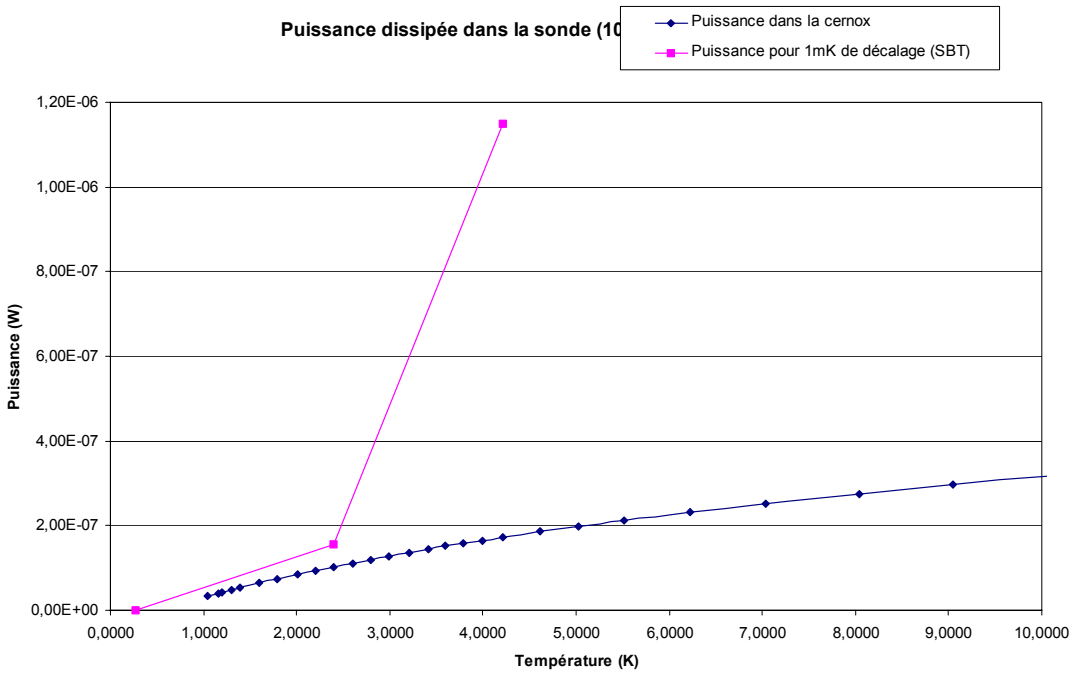


Figure 31 TempDC circuit : Power dissipation

The graph shows the power dissipation level that would create a 1 mK displacement error on the temperature reading (above), and the actual dissipation produced by the circuit when biased at 10 mV (below). Over the full temperature range of the sensor, the dissipation when applying a 10 mV bias is sufficiently small to produce a self-heating error lower than 1 mK (to be compared with the 5 mK precision of the Cernox R(T) transfer curve).

4.6.3 Resolution

The 16 sensors measured by the TempDC circuit pertain to 2 distinct groups : The low temperature group (1 K – 10 K, 2 mK resolution @1 K), and the extended temperature group (3 K – 300 K, 10 mK resolution @3 K).

The Cernox sensor R(T) variation is strongly non-linear with temperature. Knowing the constant Vbias and the R(T) characteristic curve, the gain of the trans-impedance amplifier must be adjusted to obtain the required resolution at the lower end of the corresponding temperature range, and stay in the 5 V full scale of the 16-bit ADC. The following graphs show the obtained resolution for each group.

4.6.3.1 Expected resolution (low temp. group)

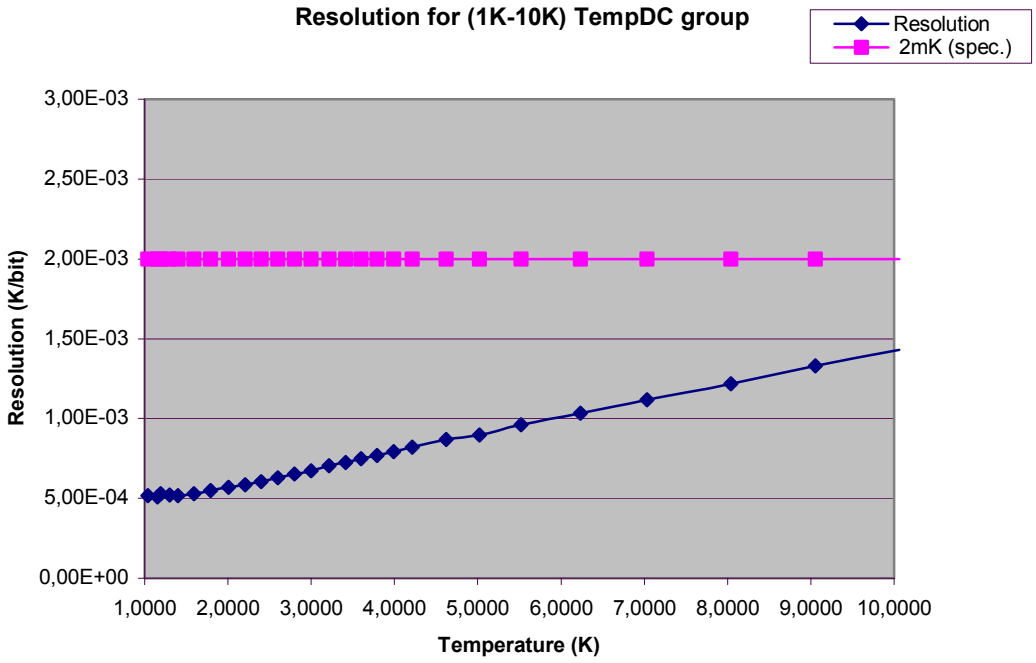


Figure 32 TempDC circuit : Resolution for [1K-10K] group

The above graph shows the evolution of the resolution over the low temperature range (below), as compared with the required resolution (above). The requirement is fulfilled over the full range. The current to voltage gain resistance is 54 kΩ.

4.6.3.2 Expected resolution (extended temp. group)

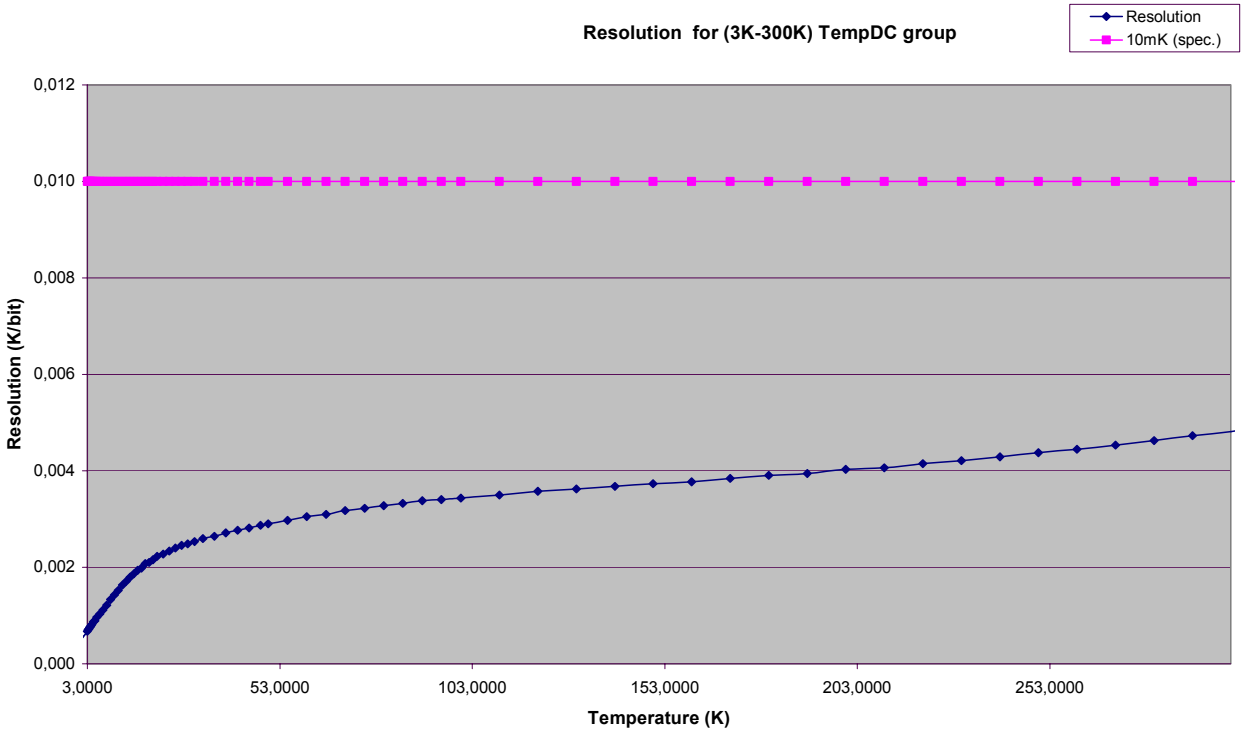


Figure 33 TempDC circuit : Resolution for [3K-300K] group

The above graph shows the evolution of the resolution over the extended temperature range (below), as compared with the required resolution (above). The requirement is fulfilled over the full range. The current to voltage gain resistance is 15 kΩ.

4.6.4 Prototype measurement

A dedicated TempDC prototype circuit was implemented, to validate the circuit principle and study the temperature variation.

4.6.4.1 Vhsk = f(Rcernox)

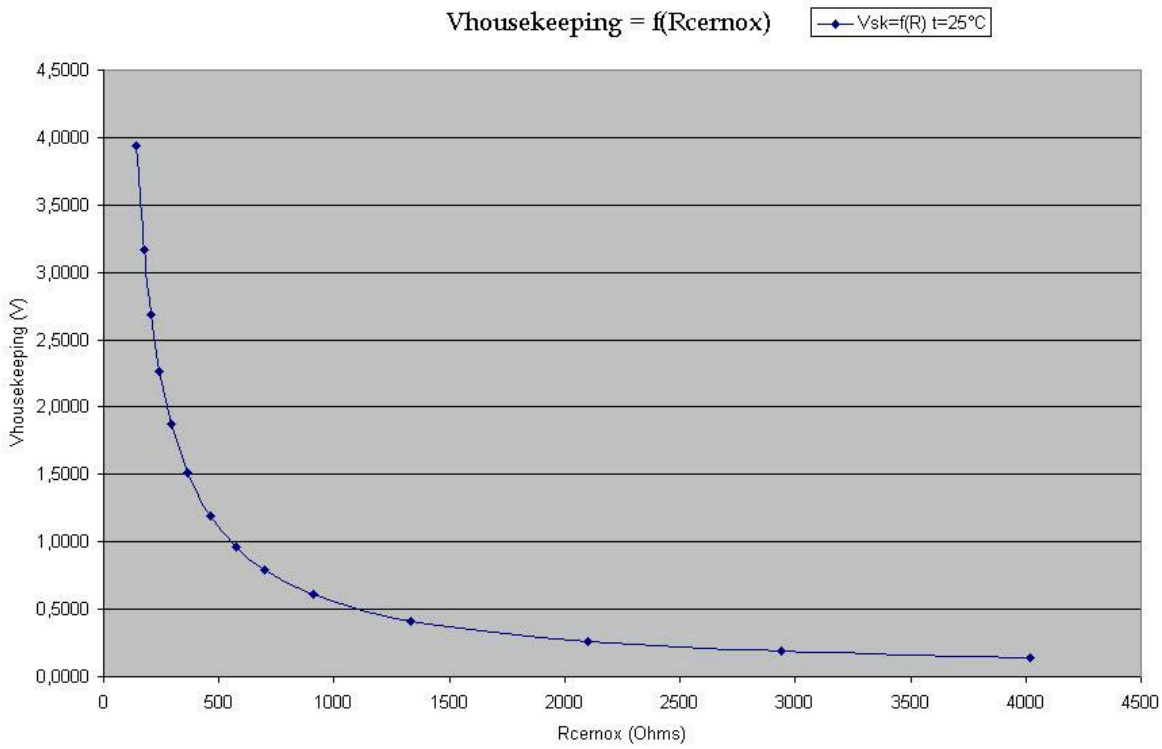


Figure 34 TempDC prototype :Vhsk variation

The above graph shows the evolution of Vhsk when the load resistance varies from 4 KΩ to 100 Ω (corresponding to a temperature varition from 1 K to 65 K on a typical Cernox sensor). The sensitivity is stronger for small resistor values (k/R dependence). This effect somewhat compensates the Cernox non-linearity, which is stronger for high resistor values.

The Vhsk precision directly depends on the precision of the current-to-voltage gain resistance value (Rgain). The precision of Rgain is 0.1% on the prototype, and will be improved to 0.01% on the flight model. The measurement chain will require calibration to maintain this precision.

4.6.4.2 Variation with temperature

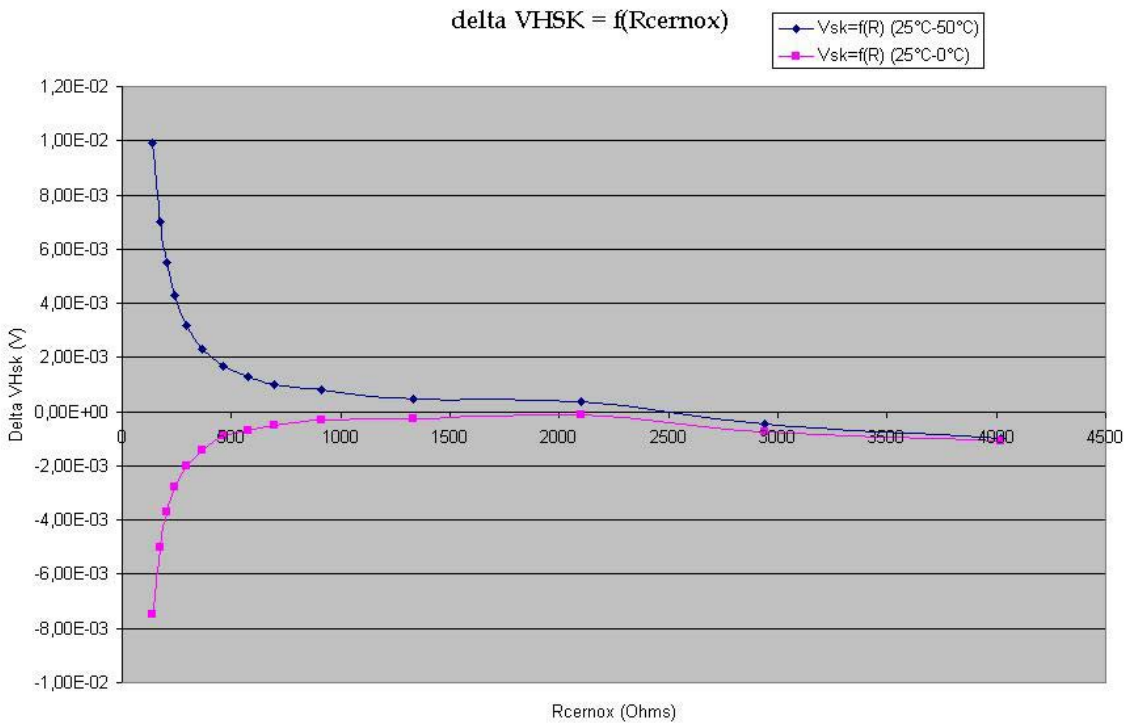


Figure 35 TempDC prototype :Variation with temperature

The above graph shows the variation of Vhsk at 0°C and 50°C as compared with the reference measurement @25°C. The curves show a symmetric spread, proportional to Vhsk. Here again, the temperature behavior could be calibrated and compensated if necessary.

4.7 Electronics Temp. Monitor : TempMon

As specified in AD 1, the electronics temperature monitoring channels use the AD590 sensor, connected to a simple current to voltage converter. They are read out through the common ADC system (Figure 2).

The detailed circuit description and associated performance analysis (vs. DCU-REQ-82) will be added when available.

4.8 Power Supply Monitor : PwrMon

The power supply monitoring channels use simple voltage followers, and are readout through the common ADC system (Figure 2). The +9VDC, -9VDC and +5V PSU supplies are monitored. In addition, the internal +2.5VDC supply (used by the FPGA and various DC voltage reference voltages are also monitored.

The detailed circuit description and associated performance analysis (vs. DCU-REQ-84) will be added when available.

5 Physical implementation

This section covers the actual details of the physical implementation : boards, connectors, pinouts, etc.

5.1 Boards

In conformance with the specified mechanical requirements (AD 2-Section 3.), the SCU module is implemented as a set of 2 active electronic boards (*Temp* and *CcHkIf*), interconnected with a dedicated passive printed circuit backplane (*Bkpln*).

Two identical SCU modules (*Main and Redundant*) are installed in the SCU compartment of the FCU box (see Figure 2).

5.2 CCHkIf board

The following diagram gives the list and nature of the CCHkIf board input an output signals.

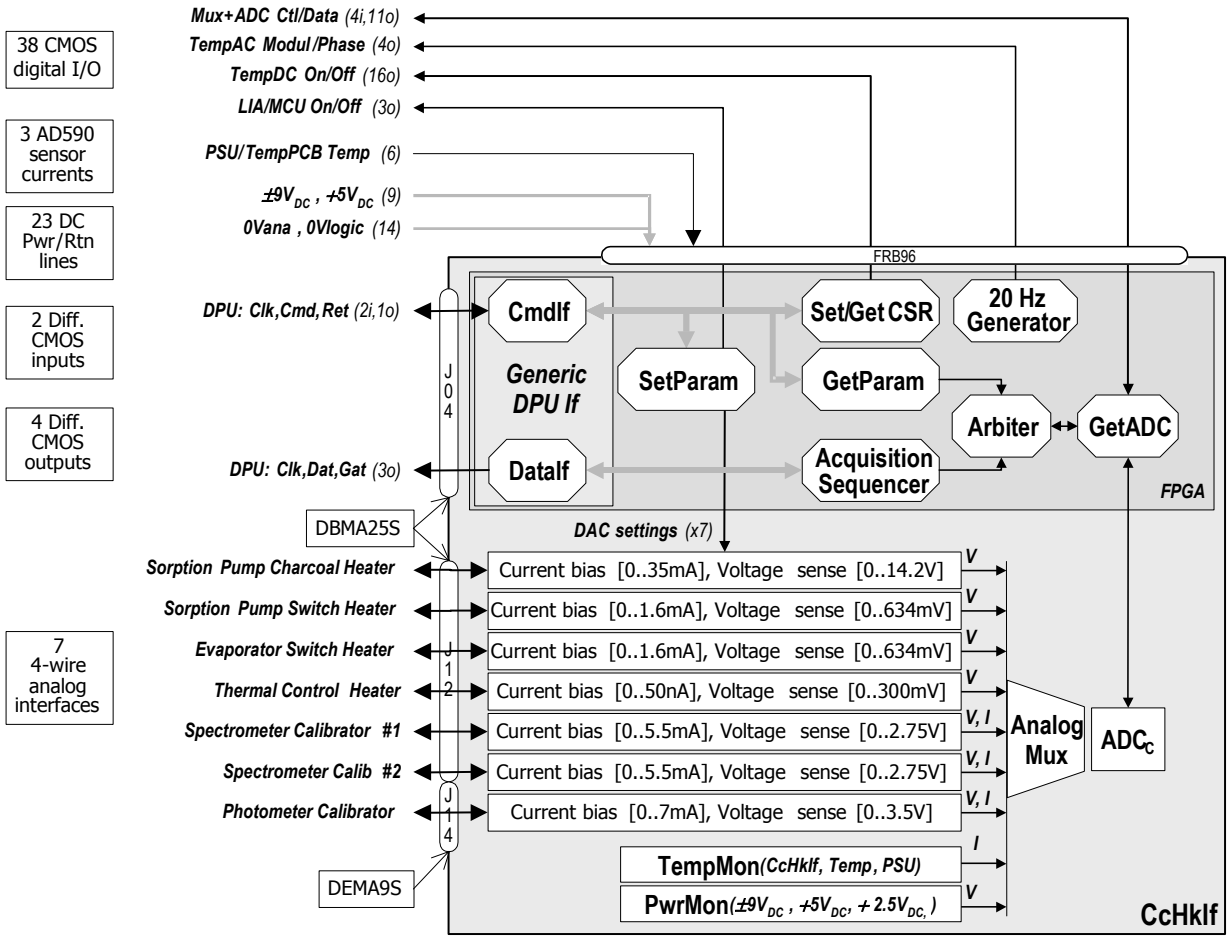


Figure 36 CHkIf board: Input and Outputs

5.3 Temp board

The following diagram gives the list and nature of the Temp board input an output signals.

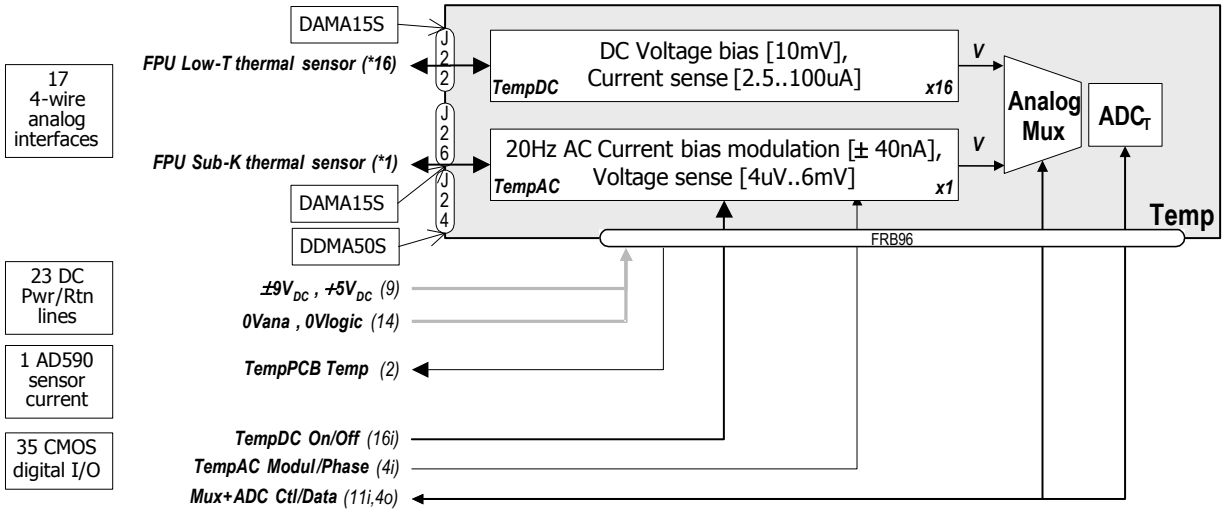


Figure 37 Temp board: Input and Outputs

5.4 Backplane

5.4.1 PSU interconnects

The Bkpln board receives from PSU :

- The secondary power supplies required by the SCU ;
- Two analogue temperature sensing levels used to monitor the internal temperature of the PSU electronics.

The Bkpln board provides to PSU :

- The On/Off logical power break signals required to control the DCU LIA_P, LIA_S, and MCU secondary power supplies.

These signals are exchanged over the J35(M) / J36(R) side connectors of the SCU.

5.4.2 Board interconnects

Two FRB96 connectors insure electrical and mechanical connection between the Bkpln and Temp / CchkIf boards. The following diagram gives the list and nature of the corresponding signals.

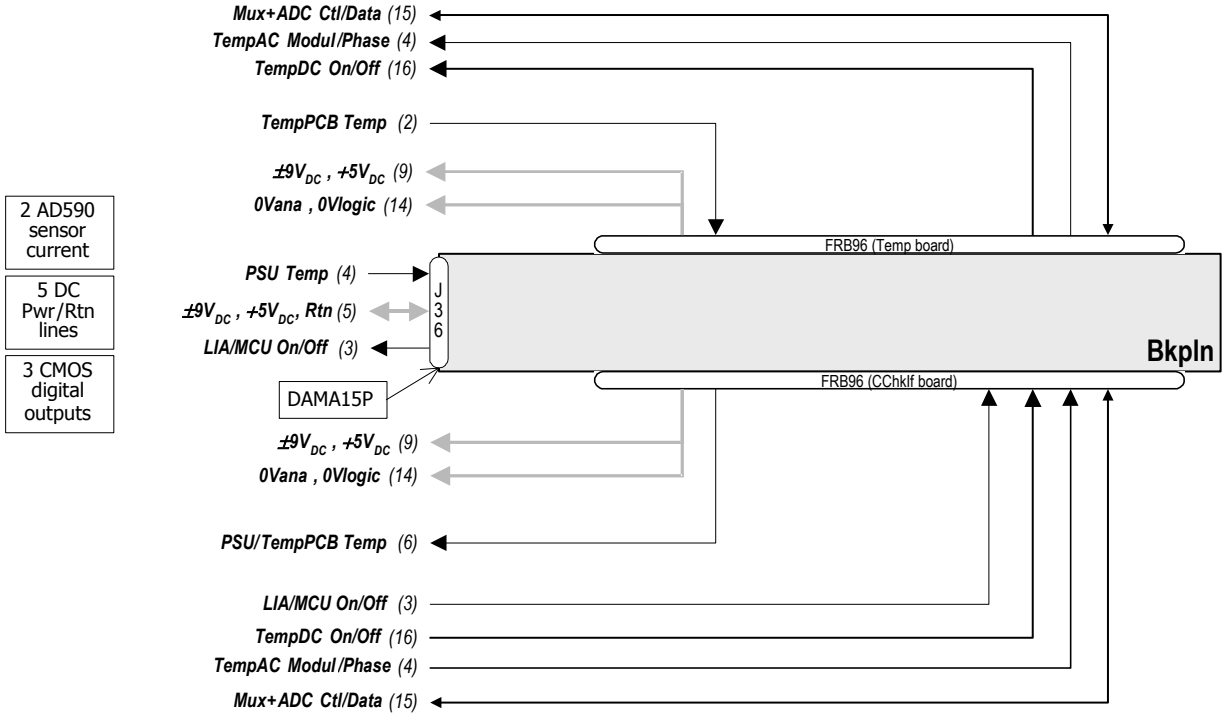


Figure 38 Bkpln board: Input and Outputs

6 Operation

This section describes the programming model of the SCU, and the phases required to operate it.

6.1 Working cycle

The SCU runs under supervision of the DPU software.

At power on, the SCU takes a definite Reset state for a short time, and then autonomously leaves this state without DPU intervention. The DPU software can later place the SCU in its Reset state, by writing the Subsystem Reset bit in a control register.

In a typical session, the DPU first installs the required configuration for the operational run, and then launches the SCU frame sequence for a limited or infinite time. During operation, the DPU software has unhindered access to all CSR registers and analogue parameters. Once out of Reset, the SCU is stateless and does not apply censorship on DPU transactions. Potential problems may be expected if the DPU changes configuration while a frame sequence is running. The SCU does not include any special mechanism to detect, log or reject incorrect DPU software sequences.

6.2 Programming model

The SCU resources are described in the following tables.

6.2.1 Interface Commands and Registers

The following table recalls the function and format of the generic Interface Registers. Refer to AD 2 for a detailed description.

Name[1]	Address[2]	Type[3]	Parameter format[4]	Comment[5]	Default[6]
CmdIfStat	000 0000 --00	R	R: 0000 0000 00VV VVVV	***Return interface status*** Bits (5..4): Response Status [00: Accepted, 01: Unknown[7], 10: Forbidden[8], 11: Timeout[9]] Bit 3: SubSystem Response Timeout (Error) Bit 2: Forbidden Read (Error) Bit 1: Forbidden Broadcast (Error) Bit 0: CommandOverlapped (Error)	$0000
CmdIfCtrl	000 0000 --01	BWR	W: ---- ---- ---- -VVV R: 0000 0000 0000 0VVV	***Set / return interface controls*** Bit 2: Active-low clear of CmdIfStat Status bits Bit 1: Active-low Reset of the SCU Subsystem logic Bit 0: Active-low Reset of DataIf	$0003
SubSDelay	000 0000 --10	R	R: 0000 000V VVVV VVVV	***Return Subsystem response delay*** Bits (8..0): Response delay of last SCU Subsystem command, expressed in DpuClk periods	$01FF
TStampRst	000 0000 --11	BW	W: ---- ---- ---- ----	Reset Time Stamp	NA

Table 16 SCU Interface Registers

[1] Parameters are listed in ascending address order.
[2] The "-" character denotes a don't care bit.
[3] B : supports broadcast write access ; W : supports write access; R : supports read access ; F : eligible for inclusion in the Data Frame ; NA : Not Applicable.
[4] The "-" character denotes a don't care bit ; The "V" character denotes a valid bit ; The "r" character denotes a reserved bit.
[5] Bit numbering convention: Leftmost bit (MSB) is Bit 15; rightmost bit (LSB) is Bit 0.
[6] The default value is obtained at Power On or after a Subsystem Reset command ; $hhhh indicates hexadecimal format ; NA : Not Applicable.
[7] The "Unknown " Response Status is obtained when accessing (R or W) the **Unknown$_i$** areas, when writing a R only resource, and when reading a W only resource.
[8] Since the SCU Subsystem is stateless and never rejects commands; obtaining the "Forbidden" Response Status denotes a hardware failure on the SCU when accessing Subsystem resources.
[9] Since the SCU Subsystem decodes all Subsystem commands; obtaining the "TimeOut" Response Status denotes a hardware failure on the SCU when accessing Subsystem resources.

6.2.2 Subsystem Resources

6.2.2.1 Configuration and Status Registers

Name[1]	Address[2]	Type[3]	Parameter format[4]	Comment[5]	Default[6]
ScuStatus	--- 100- -000	R	R: rrrr rrrr rrrr rVVV	***Return Subsystem Status*** Bit 2: Mirror of FrameOn bit in **FrameCtrl** Bit 1: LatchUpT [ADC_T LatchUp detected on Temp] Bit 0: LatchUpC [ADC_C LatchUp detected on CchkIf]	$0000
ScuContrl	--- 100- -001	WR	W: ---- ---- ---- ---V R: ---- ---- ---- ---V	***SCU Control Register*** Bit 0: LatchUpEn [1:Enables LatchUp Detection/ 0:Resets LatchUp Status bit(s) in **ScuStatus**]	$0001
FrameCtrl	--- 100- -010	WR	W: ---- ---- ---- ---V R: ---- ---- ---- ---V	Start / stop / monitor Frame Sequence Bit 0: FrameOn [1:Starts Frame Sequence/ 0:Stops Frame Sequence]; Automatically cleared at end of Sequence; Mirrored in **ScuStatus**	NA
FrameConf	--- 100- -011	WR	W: V--- ---- VVVV VVVV R: V000 0000 VVVV VVVV	***Set / return Frame Config*** Bit 15: FrameType [1:Test Pattern/ 0:Normal Acquisition] Bits (7..0): FrameRate [Actual rate is 80/(FrameRate+1) Hz]	$0000
SeqLength	--- 100- -100	WR	W: ---- ---- ---V VVVV R: 0000 0000 000V VVVV	***Set / return number of Frames per Sequence*** Bits (4..0): FrameNmbr [1 to 31, 0 ≡ infinite]	$0000
TempOnOff	--- 100- -101	WR	W: VVVV VVVV VVVV VVVV R: VVVV VVVV VVVV VVVV	***Set / return FPU temperature probe bias On/Off state*** [1: Bias On / 0: Bias Off] Bits (15..12): (BSMM,FTSM,FTSS,SCST) Bits (11..08): (SCL4,SCL2,BSMS,BAF) Bits (07..04): (SUB,PLO,SLO,SOB) Bits (03..00): (CSHT,CEHS,CPHS,CPHP)	$0000
SubKOnOff	--- 100- -110	WR	W: ---- ---- ---- ---V R: 0000 0000 0000 000V	***Set / return SubK temperature probe bias On/Off state*** [1: Bias On / 0: Bias Off] Bit 0: Cryo-Cooler Evaporator probe	$0000
DrelOnOff	--- 100- -111	WR	W: ---- ---- ---- -VVV R: 0000 0000 0000 –VVV	***Set / return LIA and MCU power relays On/Off state*** [1: Relay On / 0: Relay Off] Bit 2: MCU Bit 1: LIA_S Bit 0: LIA_P	$0000

Table 17 Subsystem Configuration and Status Registers

6.2.2.2 Subsystem Analogue resources

Name[1]	Address[2]	Type[3]	Parameter format[4]	Comment	Default[6]
CsuTempRd	--- 1100 -000	R	R: VVVV VVVV VVVV VVVV	***Measure CcHklf board temperature***	NA
TsuTempRd	--- 1100 -001	R	R: VVVV VVVV VVVV VVVV	***Measure Temp board temperature***	NA
PsuTmp1Rd	--- 1100 -010	R	R: VVVV VVVV VVVV VVVV	***Measure PSU temperature 1***	NA
PsuTmp2Rd	--- 1100 -011	R	R: VVVV VVVV VVVV VVVV	***Measure PSU temperature 2***	NA
ScuCHTn09	--- 1100 1110	R	R: VVVV VVVV VVVV VVVV	***Measure -09VDC power supply***	NA
ScuCHTp09	--- 1100 1111	R	R: VVVV VVVV VVVV VVVV	***Measure +09VDC power supply***	NA
ScuCHTp05	--- 1101 -000	R	R: VVVV VVVV VVVV VVVV	***Measure +05VDC power supply***	NA
ScuCHTp25	--- 1101 -001	R	R: VVVV VVVV VVVV VVVV	***Measure +2.5VDC internal power supply***	NA
ScuCHTref	--- 1101 -010	R	R: VVVV VVVV VVVV VVVV	***Measure internal Voltage Reference on CChklf***	NA
ScuCHTgnd	--- 1101 -011	R	R: VVVV VVVV VVVV VVVV	***Measure internal Gnd level on CChklf***	NA
ScuTHTref	--- 1111 -001	R	R: VVVV VVVV VVVV VVVV	***Measure internal Voltage Reference on Temp***	NA
ScuTHTgnd	--- 1111 –01-	R	R: VVVV VVVV VVVV VVVV	***Measure internal Gnd level on Temp***	NA

Table 18 Subsystem Analogue resources

6.2.2.3 Subsystem Heater and Calibrator resources

Name[1]	Address[2] (Alias[10])	Type[3]	Parameter format[4]	Comment	Default[6]
EVHSHeatCur	--- 1100 –100 (LHeaterIV1)	W	W: ---- IIII IIII IIII	***Set current of Evaporator Heat Switch heater***	Note[11]
EVHSHeatVolt		R	R: VVVV VVVV VVVV VVVV	***Measure voltage of Evaporator Heat Switch heater***	Note[12]
SPHSHeatCur	--- 1100 –101 (LHeaterIV2)	W	W: ---- IIII IIII IIII	***Set current of Sorption Pump Heat Switch heater***	Note[11]
SPHSHeatVolt		R	R: VVVV VVVV VVVV VVVV	***Measure voltage of Sorption Pump Heat Switch heater***	Note[12]
TCheaterCur	--- 1100 –110 (LHeaterIV3)	W	W: ---- IIII IIII IIII	***Set current of Thermal Control Heater***	Note[11]
TCheaterVolt		R	R: VVVV VVVV VVVV VVVV	***Measure voltage of Thermal Control Heater***	Note[12]
SPheaterCur	--- 1100 –111 (HHeaterIV1)	W	W: ---- IIII IIII IIII	***Set current of Sorption Pump Heater***	Note[11]
SPheaterVolt		R	W: ---- IIII IIII IIII	***Measure voltage of Sorption Pump Heater***	Note[12]
PhCalCurSP	--- 1100 1000 (CalibraI1)	W	W: ---- IIII IIII IIII	***Set current applied to Photometer Calibrator***	Note[11]
PhCalCur		RF	R: VVVV VVVV VVVV VVVV	***Measure current applied to Photometer Calibrator***	Note[13]
PhCalVolt	--- 1100 1001 (CalibraV1)	RF	R: VVVV VVVV VVVV VVVV	***Measure voltage of Photometer Calibrator***	Note[12]
SCal2CurSP	--- 1100 1010 (CalibraI2)	W	W: ---- IIII IIII IIII	***Set current applied to Spectrometer Calibrator 2%***	Note[11]
SCal2Cur		RF	R: VVVV VVVV VVVV VVVV	***Measure current applied to Spectrometer Calibrator 2%***	Note[13]
Scal2Volt	--- 1100 1011 (CalibraV2)	RF	R: VVVV VVVV VVVV VVVV	***Measure voltage of Spectrometer Calibrator 2%***	Note[12]
Scal4CurSP	--- 1100 1100 (CalibraI3)	W	W: ---- IIII IIII IIII	***Set current applied to Spectrometer Calibrator 4%***	Note[11]
Scal4Cur		RF	R: VVVV VVVV VVVV VVVV	***Measure current applied to Spectrometer Calibrator 2%***	Note[13]
Scal4Volt	--- 1100 1101 (CalibraV3)	RF	R: VVVV VVVV VVVV VVVV	***Measure voltage of Spectrometer Calibrator 4%***	Note[12]

Table 19 Subsystem Heater and Calibrator resources

[10] The Address Alias refers to the internal naming convention, when it is different from the actual parameter name.
[11] The DAC is automatically placed to its lower possible value ($000) at Power On or Subsystem Reset.
[12] The read operation measures the voltage corresponding to DAC setting = $000.
[13] The read operation measures the current corresponding to DAC setting = $000.

6.2.2.4 Subsystem Temperature Probe resources

Name[1]	Address[2] (Alias[10])	Type[3]	Parameter format[4]	Comment	Default[6]
T_CPHP	--- 1110 0000 (FpuTemp01)	RF	R: vvvv vvvv vvvv vvvv	Measure Cryo-cooler Sorption Pump temperature	Note[14,15]
T_CPHS	--- 1110 0001 (FpuTemp02)	RF	R: vvvv vvvv vvvv vvvv	Measure Cryo-cooler Sorption Pump Heat Switch temperature	Note[14,15]
T_CEHS	--- 1110 0010 (FpuTemp03)	RF	R: vvvv vvvv vvvv vvvv	Measure Cryo-cooler Evaporator Heat Switch temperature	Note[14,15]
T_CSHT	--- 1110 0011 (FpuTemp04)	RF	R: vvvv vvvv vvvv vvvv	Measure Cryo-cooler Thermal Shunt temperature	Note[14,15]
T_SOB	--- 1110 0100 (FpuTemp05)	RF	R: vvvv vvvv vvvv vvvv	Measure SPIRE Optical Bench temperature	Note[14,15]
T_SLO	--- 1110 0101 (FpuTemp06)	RF	R: vvvv vvvv vvvv vvvv	Measure Spectrometer Detector Box temperature	Note[14,15]
T_PLO	--- 1110 0110 (FpuTemp07)	RF	R: vvvv vvvv vvvv vvvv	Measure Photometer Detector Box temperature	Note[14,15]
T_SUB	--- 1110 0111 (FpuTemp08)	RF	R: vvvv vvvv vvvv vvvv	Measure Optical Sub Bench temperature	Note[14,15]
T_BAF	--- 1110 1000 (FpuTemp09)	RF	R: vvvv vvvv vvvv vvvv	Measure FPU Input Baffle temperature	Note[14,15]
T_BSMS	--- 1110 1001 (FpuTemp10)	RF	R: vvvv vvvv vvvv vvvv	Measure BSM/SOB I/F temperature	Note[14,15]
T_SCL2	--- 1110 1010 (FpuTemp11)	RF	R: vvvv vvvv vvvv vvvv	Measure Spectrometer Calibrator 2% temperature	Note[14,15]
T_SCL4	--- 1110 1011 (FpuTemp12)	RF	R: vvvv vvvv vvvv vvvv	Measure Spectrometer Calibrator 4% temperature	Note[14,15]
T_SCST	--- 1110 1100 (FpuTemp13)	RF	R: vvvv vvvv vvvv vvvv	Measure Spectrometer Calibrator Flange temperature	Note[14,15]
T_FTSS	--- 1110 1101 (FpuTemp14)	RF	R: vvvv vvvv vvvv vvvv	Measure SMEC/SOB I/F temperature	Note[14,15]
T_FTSM	--- 1110 1110 (FpuTemp15)	RF	R: vvvv vvvv vvvv vvvv	Measure SMEC mechanism temperature	Note[14,15]
T_BSMM	--- 1110 1111 (FpuTemp16)	RF	R: vvvv vvvv vvvv vvvv	Measure BSM mechanism temperature	Note[14,15]
T_CEV	--- 1111 -000 (SubKTempP)	RF	R: vvvv vvvv vvvv vvvv	Measure Cryo-Cooler Evaporator temperature	Note[16,15]

Table 20 Subsystem Temperature Probe resources

[14] The sensor is automatically placed in an unbiased state at Power On or Subsystem Reset (**TempOnOff** = $0000).
[15] The read operation measures the residual voltage corresponding to an unbiased sensor.
[16] The sensor is automatically placed in an unbiased state at Power On or Subsystem Reset (**SubKOnOff** = $0000).

6.2.2.5 Subsystem Miscellaneous resources

Name[1]	Address[2]	Type[3]	Parameter format[4]	Comment	Default[6]
Treserved	`--- 101- ----`	*NA*	`Reserved`	*Reserved for test*	*NA*
Unknown1	`--- 0001 ----`	*NA*	`Not Applicable`	*Empty area*	*Note[17]*
Unknown2	`--- 001- ----`	*NA*	`Not Applicable`	*Empty area*	*Note[17]*
Unknown3	`--- 01-- ----`	*NA*	`Not Applicable`	*Empty area*	*Note[17]*
Unknown4	`--- 1101 -1--`	*NA*	`Not Applicable`	*Empty Area*	*Note[17]*
Unknown5	`--- 1111 -1--`	*NA*	`Not Applicable`	*Empty area*	*Note[17]*

Table 21 Subsystem Miscellaneous resources

6.2.3 Command response time

The following table indicates the maximum response time for the various classes of SCU commands. The response time is expressed in μs, given the following assumptions :

- The DPU Command interface runs at the nominal frequency (312.5 kHz) ;
- The SCU FPGA runs at the expected nominal operating frequency (10 MHz) ;
- The DPU Data interface runs at 2.5 MHz.

The read accesses to analogue resources requiring an ADC measurement compete with a potential concurrent *Frame* operation. Due to that, the corresponding maximum response time is larger when a *Frame Sequence* is running (FrameCtrl.FrameOn=1). For completeness, the maximum response time when the *Frame Sequence* is inactive (FrameOn=0) is also given. When FrameOn=1, the actual response time will vary, depending on whether collision occurs or not.

The analogue read response times take into account the capability to do multiple sampling and averaging (up to 8 following measurements), should this be necessary.

Resource type	Maximum Response time (μs)
Interface Registers	W, R: 140
Subsystem Configuration and Status Registers	W, R: 150
Subsystem Heater and Calibrator resources	W: 150 R: 450 (FrameOn=1) / 300 (FrameOn=0)
Subsystem Temperature Probe resources	R: 450 (FrameOn=1) / 300 (FrameOn=0)
Subsystem Analogue resources	
Subsystem Miscellaneous resources	W, R: 150

Table 22 SCU Command Response Time

6.3 Data frame format

The format of the SCU *Data Frame* is as follows.

[17] Read or Write accesses to any of the **Unknown$_i$** areas will create the "Unknown" Response Status in **CmdIfStat**.

Word #	Name	Comment	Value/Range
0	FrameLength	Total number of words	30
1	FrameHeader	Frame Type: Hsk (normal mode) or Test Pattern	Hsk : $0020 Test : $0021
2	**T_CPHP**	Frame Payload area	$0000..$FFFF
3	**T_CPHS**		
4	**T_CEHS**		
5	**T_CSHT**		
6	**T_SOB**		
7	**T_SLO**		
8	**T_PLO**		
9	**T_SUB**		
10	**T_BAF**		
11	**T_BSMS**		
12	**T_SCL2**		
13	**T_SCL4**		
14	**T_SCST**		
15	**T_FTSS**		
16	**T_FTSM**		
17	**T_BSMM**		
18	**T_CEV**		
19	**PhCalCur**		
20	**PhCalVolt**		
21	**SCal2Cur**		
22	**Scal2Volt**		
23	**Scal4Cur**		
24	**Scal4Volt**		
25	**TCheaterVolt**		
26	FrameStatus	ADC latch-up flags	Bits (15..02): $0000 Bit 1: ADC_T LatchUp Bit 0: ADC_C LatchUp
27	TimeStampH	Higher half of TimeStamp	
28	TimeStampL	Lower half of TimeStamp	
29	LgtdlPrty	Longitudinal Parity	

Table 23 SCU Data Frame format

When the “Test Pattern” frame format is selected [configuration register **FrameConf**.FrameType = ’1’], the frame payload (words #2 to #25) is replaced by a series of 16-bit words generated by a fixed seed pseudo-random generator (of the Linear Feedback Shift Register type). Each following word in the sequence is obtained by the following expressions:

SeedWord(15..0)=$AAAA; Word(15..1)=PrevWord(14..0); Word(0)=XOR(PrevWord(15,14,12,3)).

7 Specification coverage

This section checks the SCU design and documentation against the requirements expressed in the specification document.

7.1 Requirement cross reference

The following table takes the requirements expressed in AD 1, and provides links to the sections were they are covered in this documentation.

DRCU-REQ # (from AD 1)	Link(s)	Comment
64	Figure 2 (p9); §4.5 (p34) ; §4.6 (p38);	
65	Figure 2 (p9); Figure 26 (p35); Figure 30 (p39);	
66, 67, 68	Figure 2 (p9); §4.4 (p27) ; Figure 19 (p28);	
69	Not a direct SCU requirement	The SCU applies DPU write commands immediately; The DAC stabilisation time after a full swing step will be measured. See related discussion in §4.1.4.4 (p19).
70	Figure 2 (p9); §4.1 (p13); §4.2 (p20);	
71	Figure 3 (p14); Figure 11 (p21);	The Thermal Strap Heater is also current-driven by a 12-bit DAC
72 (…≥ 256 Thermal Strap Pwr steps…)		The Thermal Strap Heater current being adjusted by a 12-bit DAC, the theoretical Pwr resolution is Pmax/2048
73 (…3 bi-level commands…)		1 mA min drive capability guaranteed by component data sheet
74	Figure 2 (p9);	
75	Figure 2 (p9); §6.3 (p53); Table 23 (p54);	
76, 79	Table 23 (p54);	
77	Table 17 (p49);	The number of frames per sequence may be (1..31) [Req: (1..16)]
78	Table 17 (p49);	
80, 81, 82	Figure 2 (p9); §4.7 (p43); Table 18 (p50);	The TempMon analogue circuit is not described / analysed in this issue.
83	Table 20 (p52) ; Table 19 (p51); Table 18 (p50);	
84	Figure 2 (p9); §4.8 (p43); Table 18 (p50);	The PwrMon analogue circuit is not described / analysed in this issue.
85, 86	Figure 2 (p9); §4.4.5.4 (p34; Figure 27 (p36); §4.6 (p38); Figure 32 (p40); Figure 33 (p41);	
87	4.5.3(p35); Figure 30 (p39);	
88, 89	Table 14 (p29); Figure 23 (p33); Figure 24 (p33); Figure 25 (p34);	The PCAL load resistance must be defined. Current design is based on R=200 Ω.
90	Figure 22 (p32);	Calibrator temperature drift : Discussion and prototype measurements added.
91	Table 14 (p29);	Req 91 (I_limit <= 112% Imax) is guaranteed by the Rlim selection.
92a	§4.2 (p20); Figure 11 (p21);	
92b	§4.1 (p13); Figure 3 (p14);	
92c	§4.3 (p25); Figure 11 (p21);	
93		See AD 5.
94, 95		Board dimensions are compliant.
96		Power dissipation is compliant.

DRCU-REQ # (from AD 1)	Link(s)	Comment
97, 98	In rush current / power supply filtering specs to be updated.	No special circuit implemented for QM1.

Table 24 Requirement cross reference